FemtoClock® NG Jitter Attenuator and Clock Synthesizer

IDT8V19N486-02I

SHORT FORM DATA SHEET

The short form datasheet is intended to provide an overview only. Additional details are available from IDT. Contact information may be found on the last page.

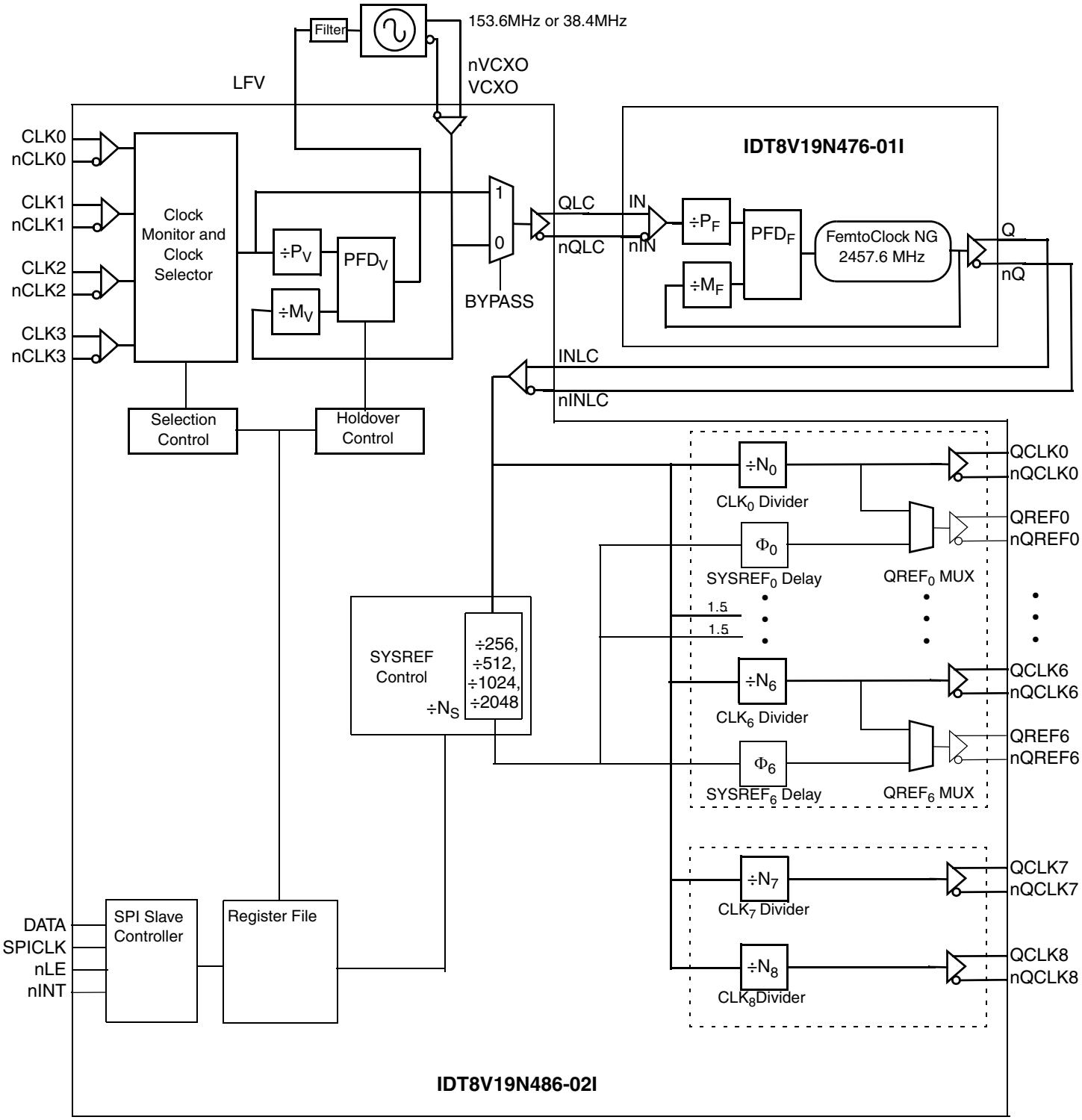
General Description

IDT8V19N486-02I is a FemtoClock® NG Jitter Attenuator and Clock Synthesizer. Together with the IDT8V19N476-01I external synthesizer, the device form a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The two-chip solution is optimized to deliver excellent phase noise performance. The device supports JESD204B subclass 0 and 1 clock implementations. The device is very flexible in programming of the output frequency and phase. A dual-stage PLL architecture (the second stage is implemented in the IDT8V19N476-01I) supports both jitter attenuation and frequency multiplication. The first stage PLL uses an external VCXO for best possible noise characteristics. The device supports the clock generation of high-frequency clocks and low-frequency system reference signals (SYSREF). The system reference signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. Four clock inputs are available for redundancy purpose. All inputs are monitored for activity. Priority-controlled auto-switching, manual switchover and hold-over is provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers and phase adjustment capabilities are added for flexibility. The device is configured through a 3-wire SP serial interface and reports lock and signal loss status in internal registers and optionally via an lock detect (nINT) output. The device is packaged in a lead-free (RoHS 6) 72-lead VFQFN package (IDT8V19N486-02I). The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

Features

- Core timing unit for JESB204B wireless infrastructure clocks
- Fourth generation FemtoClock® NG technology
- Jitter attenuation and frequency multiplication
- Use with the IDT8V19N476-01I synthesizer
- Nine differential configurable LVPECL/LVDS clock outputs with a variable output amplitude
- Seven differential LVDS system reference (SYSREF) signal outputs
- Synchronization between clock and system reference signals
- Phase delay capabilities for alignment/delay of individual system reference signals
- Individual output phase adjustment resolution: 101.7ps
- Individual output phase adjustment range in 128 steps (delay range encompasses one period of a 153.6MHz signal)
- Supports input clocks of 153.6, 76.8, 307.2, 38.4 and 61.44MHz
- Supports a 153.6MHz and 38.4MHz VCXO frequency
- Output clocks frequencies: 1228.8, 614.4, 307.2 and 153.6MHz
- Output clock frequency divider: ÷2, ÷4, ÷8 and ÷16
- Four redundant clock input compatible with LVPECL, LVDS, LVCMOS signals
- Dedicated power-down features for reducing power consumption
- Input clock monitoring, manual and auto-switch over
- Holdover for temporary loss of input signal scenarios
- SPI controlled system reference signal (SYSREF) generation
- First stage PLL uses an external VCXO (153.6MHz)
- Support of output power-down and output disable
- Second stage PLL uses an internal oscillator (2457.6MHz), implemented in the IDT8V19N476-01I synthesizer
- Clock output phase noise at 307.2MHz:
  10Hz offset: -57 dBc/Hz
  100Hz offset: -89 dBc/Hz
  500Hz offset: -114 dBc/Hz
  1kHz offset: -116 dBc/Hz
  10kHz offset: -121 dBc/Hz
  60kHz offset: -121 dBc/Hz
  100kHz offset: -126 dBc/Hz
  200kHz offset: -131 dBc/Hz
  800kHz offset: -148 dBc/Hz
  5MHz offset: - 153 dBc/Hz
  10MHz offset: - 153 dBc/Hz
- Status conditions with programmable functionality for loss-of-lock and loss of reference indication
- Lock detect (nINT) output for status change indication
- LVCMOS/LVTTL compatible SPI serial interface
- 3.3V core and output supply mode
- Supports 1.8V I/O logic levels for all control pins
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) 72-lead VFQFN packaging, (10x10x0.85mm, 0.5mm pitch)

Block Diagram



We've Got Your Timing Solution

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