

SOT223 N-CHANNEL ENHANCEMENT MODE LOW THRESHOLD VERTICAL DMOS FET

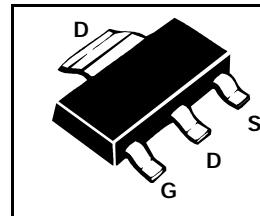
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ZVNL110G

FEATURES

- * LOW $R_{DS(ON)}$ - 3Ω

PARTMARKING DETAIL - ZVNL110



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE		UNIT
Drain-Source Voltage	V_{DS}	100		V
Continuous Drain Current at $T_{amb}=25^\circ C$	I_D	600		mA
Pulsed Drain Current	I_{DM}	6		A
Gate-Source Voltage	V_{GS}	± 20		V
Power Dissipation at $T_{amb}=25^\circ C$	P_{tot}	2		W
Operating and Storage Temperature Range	$T_j \cdot T_{stg}$	-55 to +150		°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^\circ C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100		V	$I_D=1\text{mA}$, $V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.75	1.5	V	$I_D=1\text{mA}$, $V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		100	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		10 100	μA μA	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$ $V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T=125^\circ C$ (2)
On-State Drain Current(1)	$I_{D(on)}$	750		mA	$V_{DS}=25\text{V}$, $V_{GS}=5\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		4.5 3.0	Ω Ω	$V_{GS}=5\text{V}$, $I_D=250\text{mA}$ $V_{GS}=10\text{V}$, $I_D=500\text{mA}$
Forward Transconductance(1)(2)	g_{fs}	225		mS	$V_{DS}=25\text{V}$, $I_D=500\text{mA}$
Input Capacitance (2)	C_{iss}		75	pF	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$
Common Source Output Capacitance (2)	C_{oss}		25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	
Rise Time (2)(3)	t_r		12	ns	$V_{DD}\approx 25\text{V}$, $I_D=1\text{A}$, $V_{GS}=10\text{V}$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15	ns	
Fall Time (2)(3)	t_f		13	ns	

(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤2% (2) Sample test.

(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator