

CIPOS™ Tiny IPM 600V/6A

IM393-S6E

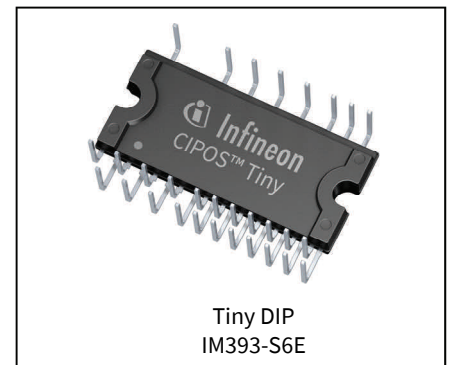
Description

IM393-S6E is a 6A, 600V Integrated Power Hybrid IC with Open Emitter pins for advanced Appliance Motor Drives applications such as energy efficient fan and pumps. Infineon's technology offers an extremely compact, high performance AC motor-driver in a single isolated package to simplify design.

This advanced IPM is a combination of Infineon's newest low VCE(on) Trench IGBT technology optimized for best trade-off between conduction and switching losses and the industry benchmark 3 phase high voltage, high speed driver (3.3V compatible) in a fully isolated thermally enhanced package. A built-in high precision temperature monitor and over-current protection feature, along with the short-circuit rated IGBTs and integrated under-voltage lockout function, deliver high level of protection and fail-safe operation. Using a dual in line package with full transfer mold structure resolves isolation problems to heatsink.

Features

- Integrated gate drivers and bootstrap function
- Temperature monitor
- Protection shutdown pin
- Low VCE (on) Trench IGBT technology
- Under voltage lockout for all channels
- Matched propagation delay for all channels
- 3.3V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Isolation 2000V_{RMS} min and CTI > 600
- Recognized by UL (File Number E314539)



Potential applications

- Washing machines
- Air-conditioners
- Refrigerators
- Fans
- Dishwashers
- Low power motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table1 Part Ordering Table

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|----------------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IM393-S6E | Tiny DIP | 30 Tubes | 450 | IM393-S6E |
| IM393-S6E2 | Tiny DIP, 2.9mm lead | 30 Tubes | 450 | IM393-S6E2 |
| IM393-S6E3 | Tiny DIP, 3.6mm lead | 30 Tubes | 450 | IM393-S6E3 |

Table of Contents

Table of Contents

Description 1

Features 1

Potential Applications 1

Product validation 1

Table of Contents 2

1 Internal Electrical Schematic 3

2 Pin Configuration 4

2.1 Pin Assignment 5

2.2 Pin Descriptions 6

3 Absolute Maximum Rating 8

3.1 Module 8

3.2 Inverter 8

3.3 Control 8

4 Thermal Characteristics 9

5 Recommended Operating Conditions 10

6 Static Parameters 11

6.1 Inverter 11

6.2 Control 11

7 Dynamic Parameters 13

7.1 Inverter 13

7.2 Control 13

8 Thermistor Characteristics 14

9 Mechanical Characteristics and Ratings 15

10 Qualification Information 16

11 Diagrams & Tables 17

11.1 T_c Measurement Point 17

11.2 Input-Output Logic Table 17

11.3 Switching Time Definitions 18

12 Application Notes 19

12.1 Typical Application Schematic 19

12.2 Performance Charts 20

12.3 T_J vs T_{TH} 20

12.4 -V_S Immunity 21

13 Package Outline 22

Revision History 24

1 Internal Electrical Schematic

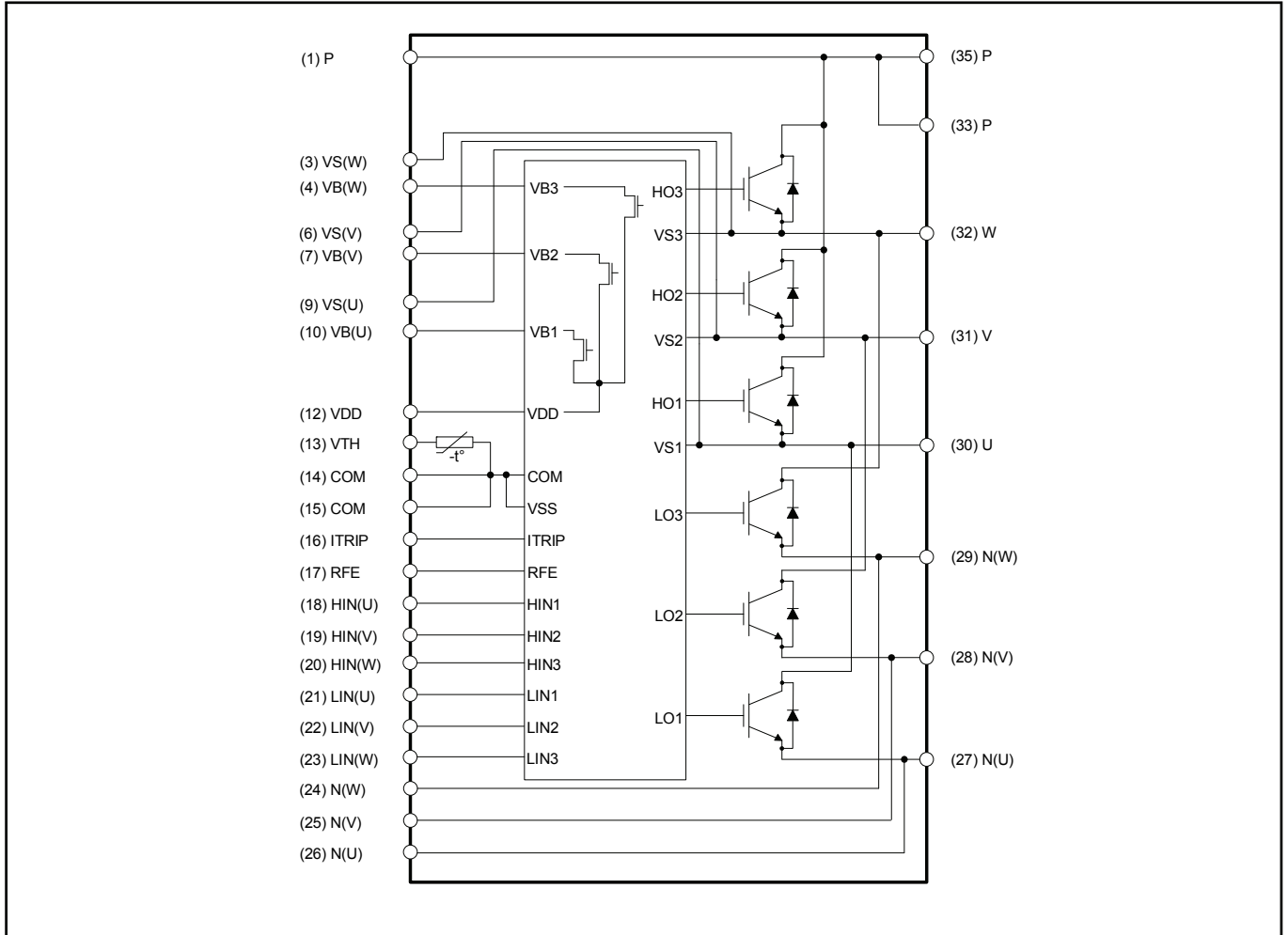


Figure 1 Internal electrical schematic

2 Pin Configuration

2.1 Pin Assignment

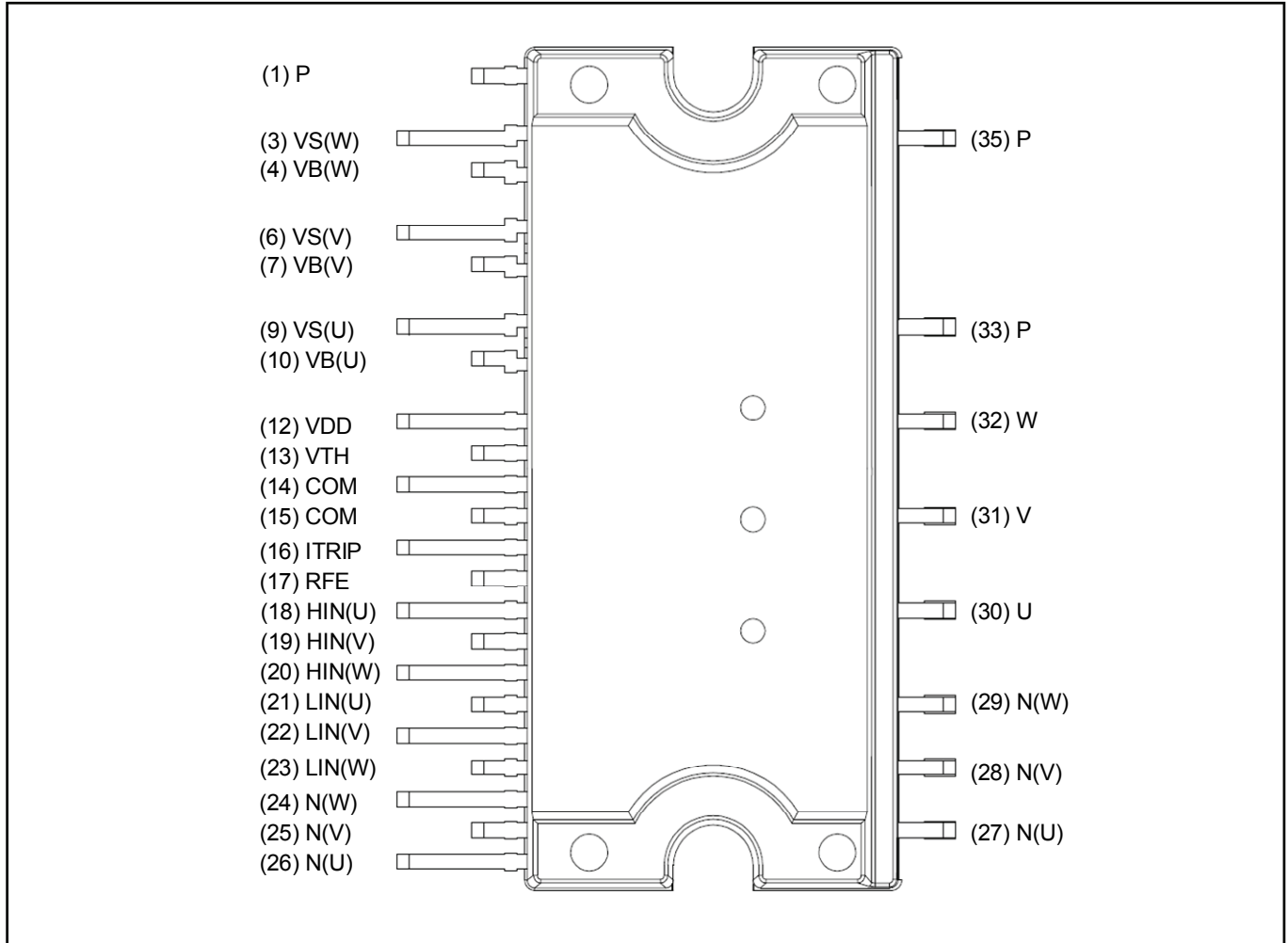


Figure 2 Pin configuration

Pin Configuration
Table 2 Pin Assignment

| Pin | Name | Description |
|-----|--------|--|
| 1 | P | Positive bus input voltage |
| 2 | N/A | None |
| 3 | VS(W) | W-phase high side floating supply offset voltage |
| 4 | VB(W) | W-phase high side floating supply voltage |
| 5 | N/A | None |
| 6 | VS(V) | V - phase high side floating supply offset voltage |
| 7 | VB(V) | V - phase high side floating supply voltage |
| 8 | N/A | None |
| 9 | VS(U) | U- phase high side floating supply offset voltage |
| 10 | VB(U) | U- phase high side floating supply voltage |
| 11 | N/A | None |
| 12 | VDD | Low side control supply |
| 13 | VTH | Temperature monitor |
| 14 | COM | Low side control negative supply |
| 15 | COM | Low side control negative supply |
| 16 | ITRIP | Over current protection input |
| 17 | RFE | RCIN / Fault / Enable |
| 18 | HIN(U) | U-phase high side gate driver input |
| 19 | HIN(V) | V-phase high side gate driver input |
| 20 | HIN(W) | W-phase high side gate driver input |
| 21 | LIN(U) | U-phase low side gate driver input |
| 22 | LIN(V) | V-phase low side gate driver input |
| 23 | LIN(W) | W-phase low side gate driver input |
| 24 | N(W) | W-phase low side emitter |
| 25 | N(V) | V-phase low side emitter |
| 26 | N(U) | U-phase low side emitter |
| 27 | N(U) | U-phase low side emitter |
| 28 | N(V) | V-phase low side emitter |
| 29 | N(W) | W-phase low side emitter |
| 30 | U | U-phase output |
| 31 | V | V-phase output |
| 32 | W | W-phase output |
| 33 | P | Positive bus input voltage |
| 34 | N/A | None |
| 35 | P | Positive bus input voltage |
| 36 | N/A | None |

2.2 Pin Descriptions

HIN(U,V,W) and LIN(U,V,W) (High side and low side control pins)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about $4k\Omega$ is internally provided to pre-bias inputs during supply start-up and an ESD diode is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time T_{FILIN} . The filter acts according to Figure 4.

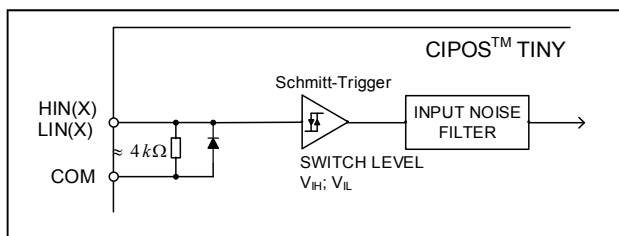


Figure 3 Input pin structure

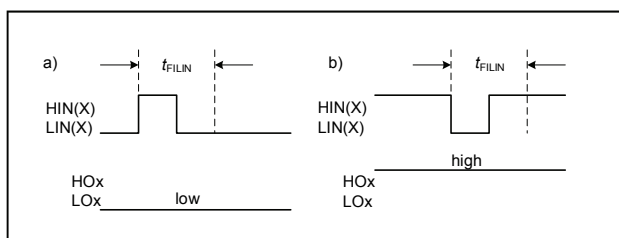


Figure 4 Input filter timing diagram

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A minimum deadtime insertion of typically 275ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

V_{DD}, COM (Low side control supply and reference)

V_{DD} is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to COM ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 10.4V$ is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below $V_{DDUV-} = 9.4V$. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_{B(U,V,W)} and V_{S(U,V,W)} (High side supplies)

V_B to V_S is the high side supply voltage. The high side circuit can float with respect to COM following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 10.41V$ and a falling threshold of $V_{BSUV-} = 9.4V$.

V_{S(U,V,W)} provide a high robustness against negative voltage in respect of COM. This ensures very stable designs even under rough conditions.

N (U, V, W) (Low side emitters)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin COM as short as possible in order to avoid unnecessary inductive voltage drops.

VTH (Thermistor)

A UL certified NTC is integrated in the module with one terminal of the chip connected to COM and the other to VTH. When pulled up to a rail voltage such as V_{DD} or 3.3V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor.

Pin Configuration

RFE (RCIN / Fault / Enable)

The RFE pin combines 3 functions in one pin: RCIN or RC-network based programmable fault clear timer, fault output and enable input.

The RFE pin is normally connected to an RC network on the PCB per the schematic in Figure 5. Under normal operating conditions, R_{RCIN} pulls the RFE pin to 3.3V, thus enabling all the functions in the IPM. The microcontroller can pull this pin low to disable the IPM functionality. This is the Enable function.

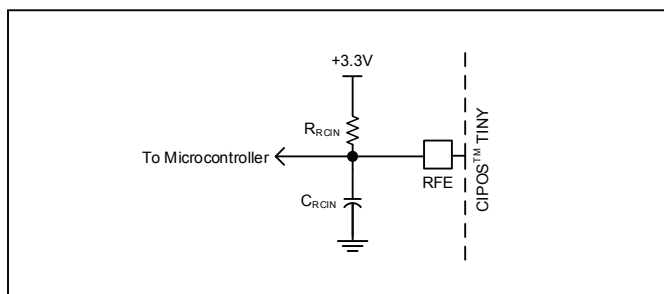


Figure 5 Typical PCB circuit connected to the RFE pin

The Fault function allows the IPM to report a Fault condition to the microcontroller by pulling the RFE pin low in one of two situations. The first is an under-voltage condition on V_{DD} and the second is when the ITRIP pin sees a voltage rising above $V_{IT,TH+}$.

The programmable fault clear timer function provides a means of automatically re-enabling the module operation a preset amount of time ($T_{FLT-CLR}$) after the fault condition has disappeared. Figure 6 shows the RFE-related circuit block diagram inside the IPM.

The length of $T_{FLT-CLR}$ can be determined by using the formula below.

$$V_{RFE}(t) = 3.3V * (1 - e^{-t/RC})$$

$$T_{FLT-CLR} = -R_{RCIN} * C_{RCIN} * \ln(1 - V_{IN,TH+}/3.3V)$$

For example, if R_{RCIN} is 1.2M Ω and C_{RCIN} is 1nF, the $T_{FLT-CLR}$ is about 1.7ms with $V_{IN,TH+}$ of 2.5V. It is also important to note that C_{RCIN} needs to be minimized in order to make sure it is fully discharged in case of over current event.

Since the ITRIP pin has a 350ns input filter, it is appropriate to ensure that C_{RCIN} will be discharged below $V_{IN,TH-}$ by the open-drain MOSFET, after 350ns. Therefore, the max C_{RCIN} can be calculated as:

$$V_{RFE}(t) = 3.3V * e^{-t/RC} < V_{IN,TH-}$$

$$C_{RCIN} < 350ns / (- \ln(V_{IN,TH-} / 3.3V)) * R_{RFE_ON}$$

Consider $V_{IN,TH-}$ of 0.8V and R_{RFE_ON} of 50ohm, C_{RCIN} should be less than 4.9nF. It is also suggested to use a R_{RCIN} of between 0.5M Ω and 2M Ω .

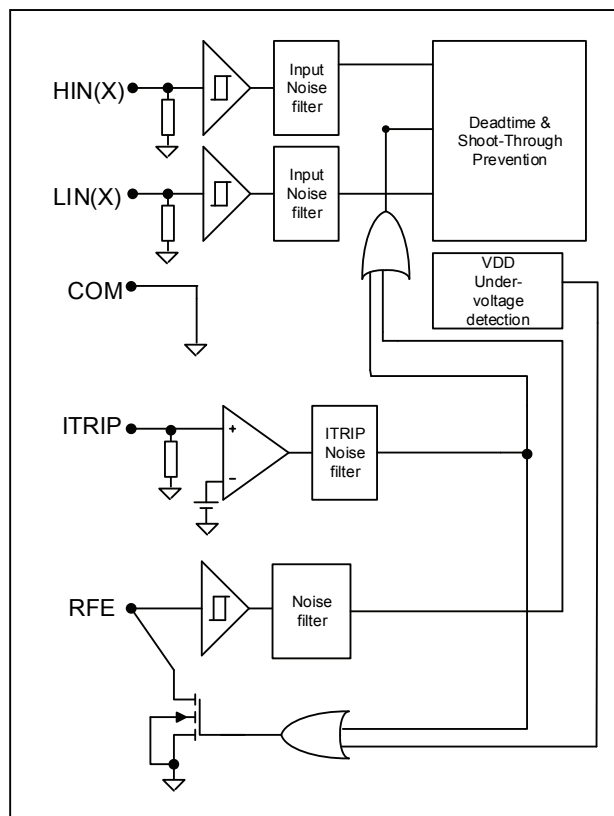


Figure 6 RFE internal circuit structure

U,V,W (High side emitter and low side collector)

These pins are motor U, V, W input pins.

P (Positive bus input voltage)

The high side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450V.

Absolute Maximum Rating

3 Absolute Maximum Rating

3.1 Module

Table 3

| Parameter | Symbol | Conditions | Value | Units |
|--------------------------------|-----------|------------------------|-----------|-------|
| Operating junction temperature | T_J | IGBT, diode, HVIC | -40 ~ 150 | °C |
| Operating case temperature | T_C | | -40 ~ 125 | °C |
| Storage temperature | T_{STG} | | -40 ~ 125 | °C |
| Isolation test voltage | V_{ISO} | AC RMS, 1 minute, 60Hz | 2000 | V |

3.2 Inverter

Table 4

| Parameter | Symbol | Conditions | Value | Units |
|--|-----------------|--|-------|-------|
| Blocking voltage | V_{CES} | IGBT, diode, HVIC | 600 | V |
| DC –link supply voltage of P-N | V_{PN} | Applied between P and N | 450 | V |
| DC –link supply voltage (surge) of P-N | $V_{PN(surge)}$ | Applied between P and N | 500 | V |
| Output current | I_o | $T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$ | ±6 | A |
| Peak output current | $I_{O(peak)}$ | $T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$, less than 1ms | ±9 | A |
| Power dissipation per IGBT | P_{tot} | | 18 | W |
| Short Circuit withstand time | T_{SC} | $T_J < 150^\circ\text{C}$, $V_{DC} = 360\text{V}$, $V_{GE} = 15\text{V}$ | 3 | µs |

3.3 Control

Table 5

| Parameter | Symbol | Conditions | Value | Units |
|-----------------------------------|-----------------|----------------------|-----------|-------|
| Logic supply voltage | V_{DD} | | -0.3 ~ 20 | V |
| Input voltage | V_{IN} | LIN, HIN, ITRIP, RFE | -0.3 ~ 20 | V |
| High side floating supply voltage | $V_{BS(U,V,W)}$ | | -0.3 ~ 20 | V |

4 Thermal Characteristics

Table 6

| Parameter | Symbol | Conditions | Value | | | Units |
|--|----------------|---|-------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Single IGBT thermal resistance, junction-case | $R_{TH(J-C)}$ | Low side W-phase IGBT (See Figure 8 for T_c measurement point) | - | 5.8 | 6.8 | °C/W |
| Single diode thermal resistance, junction-case | $R_{TH(J-C)D}$ | Low side W-phase diode (See Figure 8 for T_c measurement point) | - | 6.6 | 7.7 | °C/W |

5 Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM. The VS offset is tested with all supplies biased at 15V differential.

Table 7

| Parameter | Symbol | Conditions | Value | | | Units |
|---|----------------|----------------------|-------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Positive DC bus input voltage | V_{DC} | | - | - | 450 | V |
| Low side control supply voltage | V_{DD} | | 13.5 | 15 | 16.5 | V |
| High side floating supply voltage | V_{BS} | | 12.5 | 15 | 17.5 | V |
| Input voltage | V_{IN} | LIN, HIN, ITRIP, RFE | 0 | - | 5 | V |
| PWM carrier frequency | F_{PWM} | | - | 20 | - | kHz |
| Voltage between COM and N (including surge) | V_{COM} | | -5 | - | 5 | V |
| External dead time between HIN & LIN | DT | | 1 | - | - | μ s |
| Input pulse width | $PW_{IN(ON)}$ | | 1 | - | - | μ s |
| | $PW_{IN(OFF)}$ | | | | | |

6 Static Parameters

6.1 Inverter

$V_{BIAS}(V_{DD}, V_{BS(U,V,W)})=15V$, $T_J=25^\circ C$ unless otherwise specified

Table 8

| Parameter | Symbol | Conditions | Value | | | Units |
|--------------------------------------|--------------|---|-------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Collector-Emitter saturation voltage | $V_{CE(ON)}$ | $I_C = 3A$ | - | 1.5 | 1.95 | V |
| | | $I_C = 3A, T_J = 150^\circ C$ | - | 1.7 | - | V |
| Collector-Emitter leakage current | I_{CES} | $V_{IN} = 0V, V_{CE} = 600V$ | - | 10 | 80 | μA |
| | | $V_{IN} = 0V, V_{CE} = 600V, T_J=150^\circ C$ | - | 80 | - | μA |
| Diode forward voltage drop | V_F | $I_C = 3A$ | - | 1.5 | 1.95 | V |
| | | $I_C = 3A, T_J = 150^\circ C$ | - | 1.4 | - | V |

6.2 Control

$V_{BIAS}(V_{DD}, V_{BS(U,V,W)})=15V$, $T_J=25^\circ C$, unless otherwise specified. The V_{IN} parameters are referenced to COM and are applicable to all six channels

Table 9

| Parameter | Symbol | Conditions | Value | | | Units |
|---|--------------------------|--------------------|-------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Logic "1" input voltage | $V_{IN,TH+}$ | LIN, HIN, RFE | 2.5 | - | - | V |
| Logic "0" input voltage | $V_{IN,TH-}$ | LIN, HIN, RFE | - | - | 0.8 | V |
| V_{DD}/V_{BS} supply undervoltage, positive going threshold | $V_{DD,UV+}, V_{BS,UV+}$ | | 9.6 | 10.4 | 11.2 | V |
| V_{DD}/V_{BS} supply undervoltage, negative going threshold | $V_{DD,UV-}, V_{BS,UV-}$ | | 8.6 | 9.4 | 10.2 | V |
| V_{DD}/V_{BS} supply undervoltage lock-out hysteresis | V_{DDUVH}, V_{BSUVH} | | - | 1 | - | V |
| Quiescent V_{BS} supply current | I_{QBS} | | - | - | 150 | μA |
| Quiescent V_{DD} supply current | I_{QDD} | | - | - | 3.2 | mA |
| Offset supply leakage current | I_{LK} | $V_S = 600V$ | - | - | 50 | μA |
| Input bias current for LIN, HIN | I_{IN+} | $V_{IN} = 3.3V$ | - | 825 | 1110 | μA |
| Input bias current for RFE | $I_{IN,RFE+}$ | $V_{REF} = 3.3V$ | - | 0 | 1 | μA |
| Input bias current for ITRIP | I_{TRIP+} | $V_{ITRIP} = 3.3V$ | - | 4 | 16 | μA |
| ITRIP threshold voltage | V_{ITRIP} | | 0.44 | 0.49 | 0.54 | V |

Static Parameters

| Parameter | Symbol | Conditions | Value | | | Units |
|------------------------|-----------------|------------|-------|------|------|----------|
| | | | Min. | Typ. | Max. | |
| ITRIP input hysteresis | $V_{ITRIP,HYS}$ | | - | 0.07 | - | V |
| Bootstrap resistance | R_{BS} | | - | 200 | - | Ω |
| RFE low on resistance | R_{RFE} | | - | 50 | 100 | Ω |

7 Dynamic Parameters

7.1 Inverter

$V_{BIAS}(V_{DD}, V_{BS(U,V,W)})=15V$, $T_J=25^\circ C$, unless otherwise specified.

Table 10

| Parameter | Symbol | Conditions | Value | | | Units |
|--|-------------|--|-------------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Input to output turn-on propagation delay | T_{ON} | $I_C = 3A, V_{DC} = 300V$ | - | - | 1.15 | μs |
| Input to output turn-off propagation delay | T_{OFF} | $I_C = 3A, V_{DC} = 300V$ | - | - | 1.15 | μs |
| RFE low to six switch turn-off propagation delay | T_{EN} | $V_{RFE} = 5V \text{ to } 0V$ | - | - | 1.35 | μs |
| ITRIP to six switch turn-off propagation delay | T_{ITRIP} | $I_C = 3A, V_{DC} = 300V$ | - | - | 1.5 | μs |
| IGBT turn-on energy | E_{ON} | $V_{DC} = 300V, I_C = 3A$ $T_J = 25^\circ C$ $150^\circ C$ | - | 90 | - | μJ |
| | | | - | 130 | - | |
| IGBT turn-off energy | E_{OFF} | $V_{DC} = 300V, I_C = 3A$ $T_J = 25^\circ C$ $150^\circ C$ | - | 30 | - | μJ |
| | | | - | 45 | - | |
| Diode reverse recovery energy | E_{REC} | $V_{DC} = 300V, I_C = 3A$ $T_J = 25^\circ C$ $150^\circ C$ | - | 15 | - | μJ |
| | | | - | 35 | - | |
| Reverse Bias Safe Operating Area | RBSOA | $T_J = 150^\circ C, I_C = 12A, V_P = 600V,$ $V_{DC} = 450V, V_{DD} = +15V \text{ to } 0V$ | FULL SQUARE | | | |

7.2 Control

$V_{BIAS}(V_{DD}, V_{BS(U,V,W)})=15V$, $T_J=25^\circ C$, unless otherwise specified.

Table 11

| Parameter | Symbol | Conditions | Value | | | Units |
|---|--------------|--|-------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Input filter time (HIN, LIN, ITRIP) | T_{FILIN} | $V_{IN} = 0 \text{ or } V_{IN} = 5V$ | - | 350 | - | ns |
| Input filter time (RFE) | T_{FILRFE} | $V_{RFE} = 0 \text{ or } V_{RFE} = 5V$ | 100 | 200 | - | ns |
| ITRIP to Fault propagation delay | T_{FLT} | $V_{IN} = 0 \text{ or } V_{IN} = 5V, V_{ITRIP} = 5V$ | 400 | 600 | 800 | ns |
| Internal injected dead time | T_{DT} | $V_{IN} = 0 \text{ or } V_{IN} = 5V$ | 190 | 275 | 420 | ns |
| Matching propagation delay time (On & Off) all channels | M_T | External dead time > 420ns | - | - | 50 | ns |

8 Thermistor Characteristics

Table 12

| Parameter | Symbol | Conditions | Value | | | Units |
|-------------------|-----------|---|-------|------|-------|--------------------|
| | | | Min. | Typ. | Max. | |
| Resistance | R_{25} | $T = 25^{\circ}\text{C}$, $\pm 5\%$ tolerance | 44.65 | 47 | 49.35 | $\text{k}\Omega$ |
| Resistance | R_{125} | $T = 125^{\circ}\text{C}$ | 1.27 | 1.41 | 1.56 | $\text{k}\Omega$ |
| B-constant | B | $25\text{-}50^{\circ}\text{C}$, $R_2 = R_1 e^{[B(1/T_2 - 1/T_1)]}$ | 3989 | 4050 | 4111 | K |
| Temperature Range | | | -40 | - | 125 | $^{\circ}\text{C}$ |

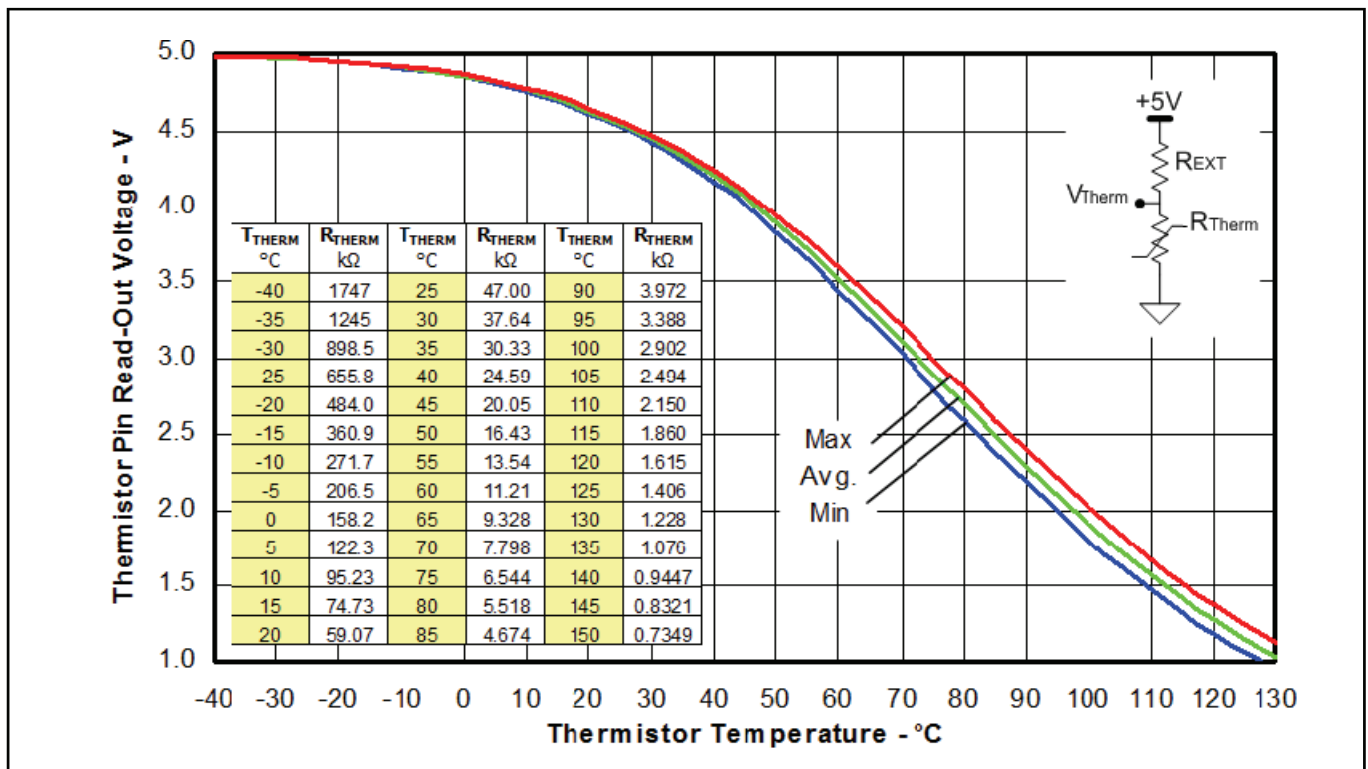


Figure 7 Thermistor readout vs. temperature (with 4.7kohm R_{EXT} pull-down resistor) and typical thermistor resistance values vs. temperature table

9 Mechanical Characteristics and Ratings

Table 13

| Parameter | Symbol | Conditions | Value | | | Units |
|-----------------------------------|---------------|---|-------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Thermal resistance, case-heatsink | $R_{TH(C-S)}$ | Flat, greased surface. Heatsink compound thermal conductivity 1W/mK | - | 0.25 | - | °C/W |
| Comparative Tracking Index | CTI | | 600 | - | - | V |
| Curvature of module backside | BKC | | 0 | - | 150 | μm |
| Mounting torque | T | M3 screw and washer | 0.6 | 0.7 | 0.8 | Nm |

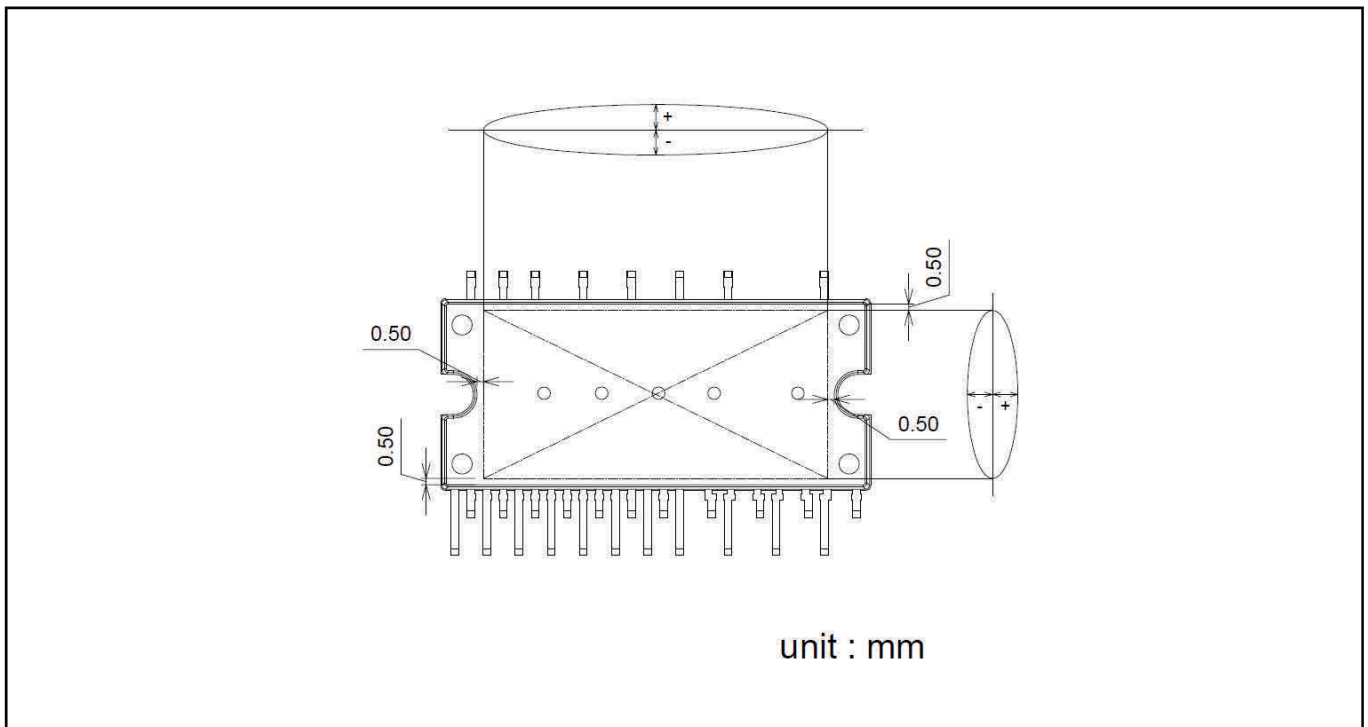


Figure 8 Backside curvature measurement position

10 Qualification Information

Table 14

| | | |
|-----------------------|------------------------|----------|
| UL Certified | File Number E314539 | |
| RoHS Compliant | Yes | |
| ESD | Human body model | Class 3A |
| | Charge discharge model | Class C3 |

11 Diagram & Tables

11.1 Tc Measurement Point

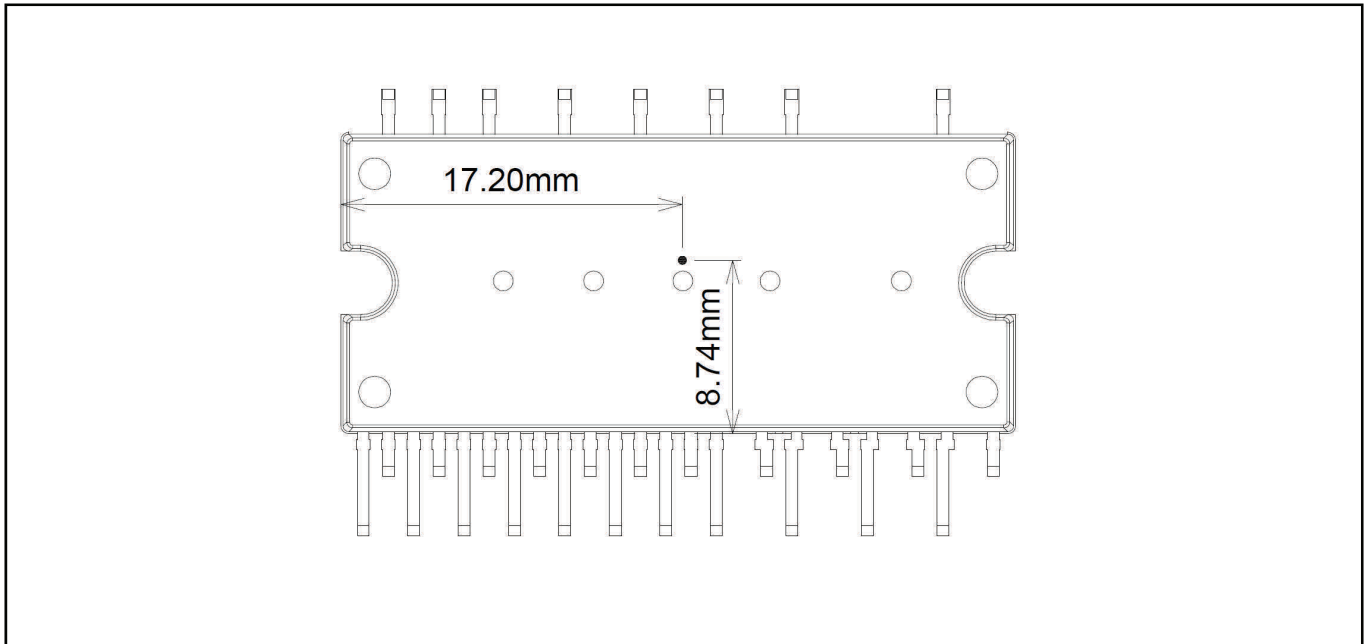


Figure 9 TC measurement point

11.2 Input-Output Logic Table

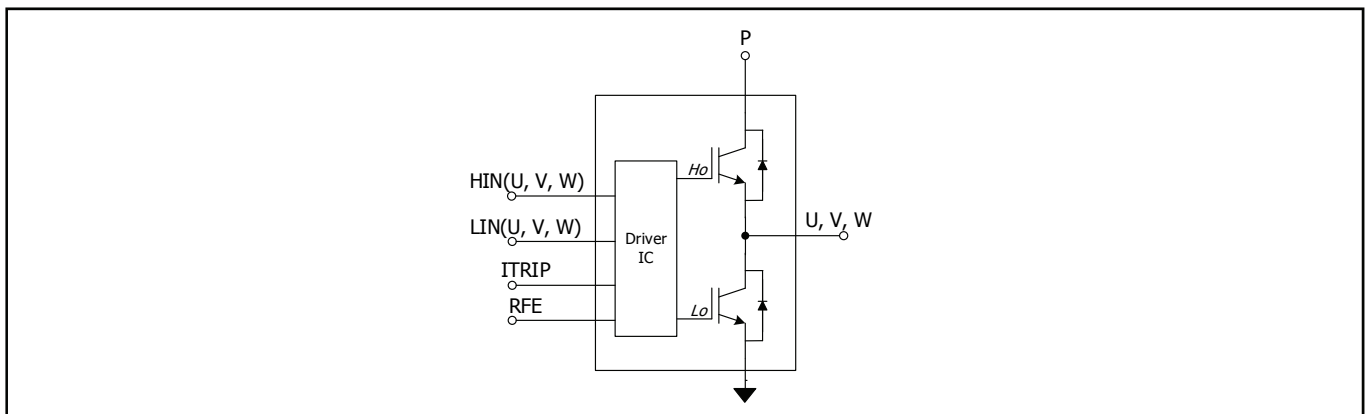


Figure 10 Module block diagram

Table 15 Input-output logic level table

| RFE | ITRIP | HIN(U,V,W) | LIN(U,V,W) | U,V,W |
|-----|-------|------------|------------|----------|
| 1 | 0 | 1 | 0 | V_{DC} |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | Off |
| 1 | 0 | 1 | 1 | Off |
| 1 | 1 | X | X | Off |
| 0 | X | X | X | Off |

11.3 Switching Time Definitions

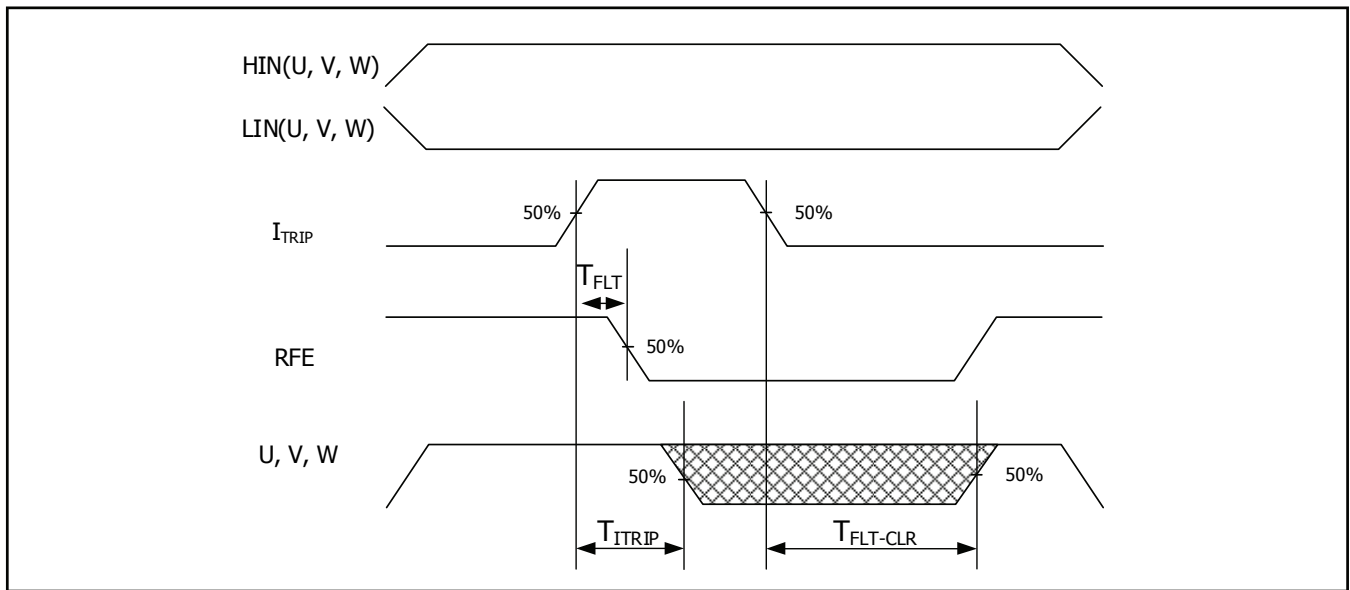


Figure 11 ITRIP time waveform

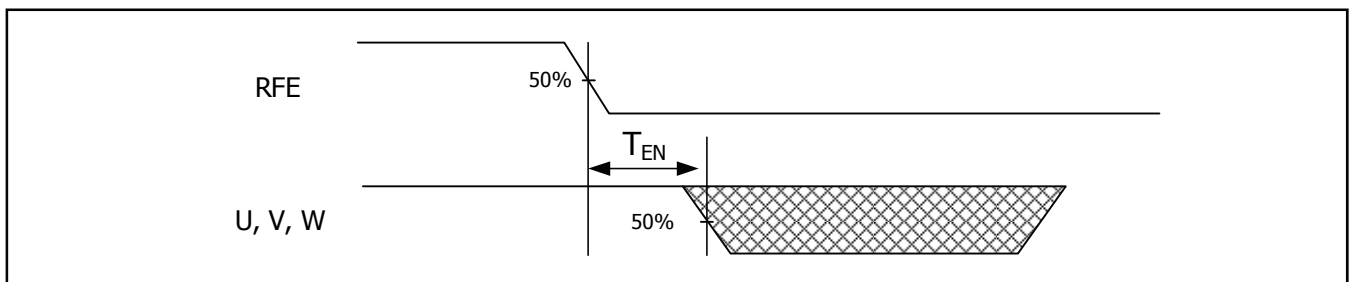


Figure 12 Output disable timing diagram

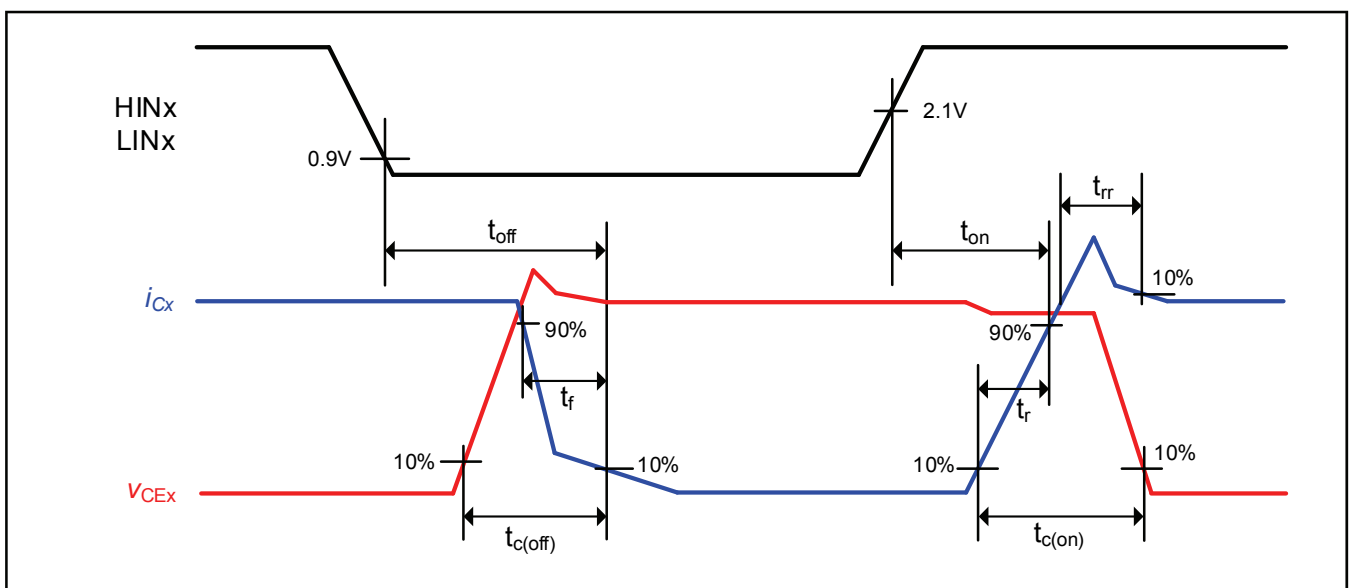


Figure 13 Switching times definition

12 Application Guide

12.1 Typical Application Schematic

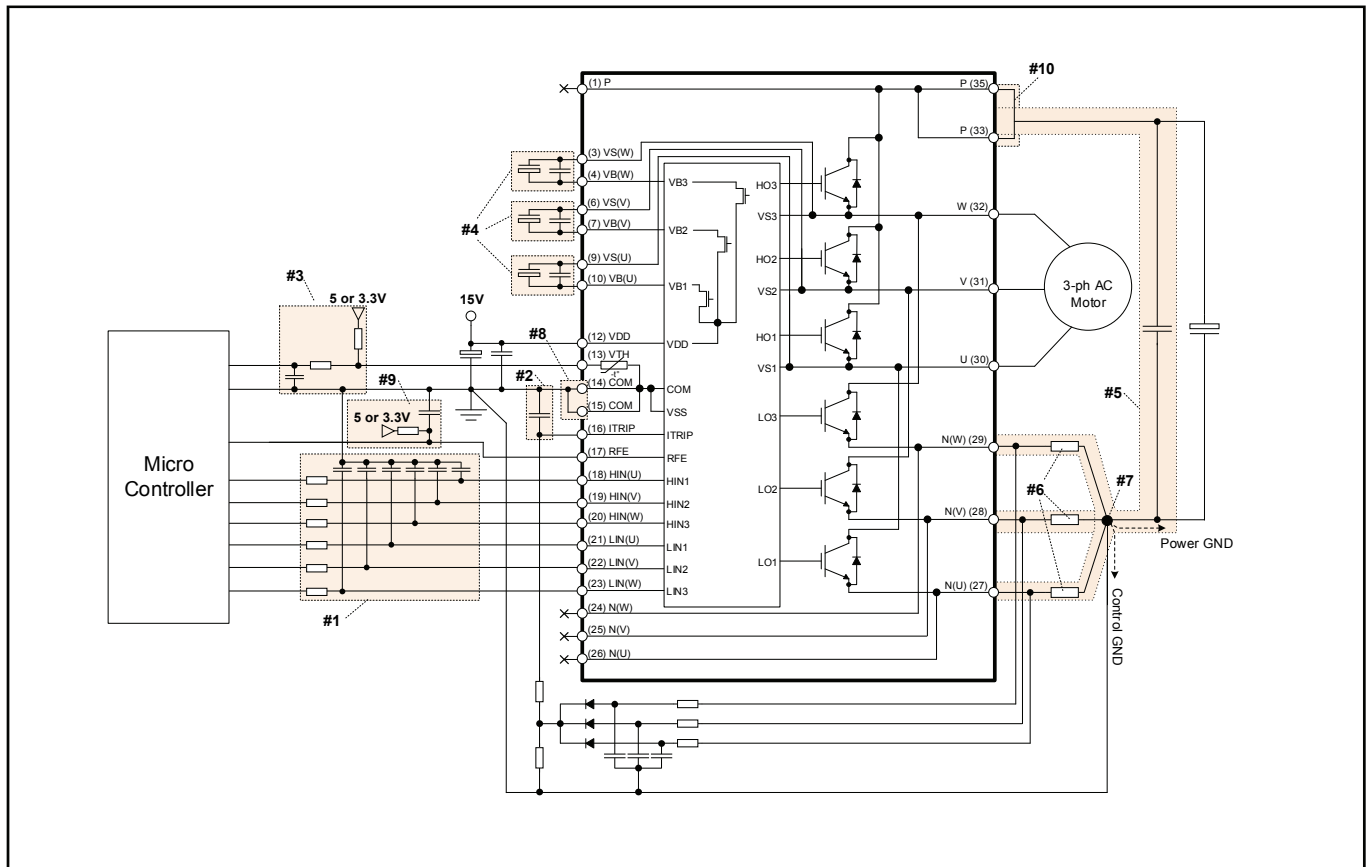


Figure 14 Typical application connection

1. Input circuit
 - RC filter can be used to reduce input signal noise (100Ω, 1nF)
 - The capacitors should be located close to CIPOS™ Tiny (to COM terminal especially).
2. Itrip circuit
 - To prevent a mis operation of protection function, RC filter is recommended
 - The capacitor must be located close to Itrip and COM terminals.
3. VTH circuit
 - This terminal should be pulled up to the bias voltage of 5V/3.3V through a proper resistor to define suitable voltage for temperature monitoring.
 - It is recommended that RC filter is placed close to the controller
4. VB-VS circuit
 - Capacitors for high side floating supply voltage should be placed close to VB and VS terminals.
 - Additional high frequency capacitors, typically 0.1mF, are strongly recommended.
 - Overlap of pattern to motor and pattern to bootstrap capacitors should be minimized.
5. Snubber capacitor
 - The wiring among CIPOS™ Tiny, snubber capacitor and shunt resistors should be short as possible.
6. Shunt resistor
 - SMD type shunt resistors are strongly recommended to minimize its internal stray inductance.
7. Ground pattern
 - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at the common end of shunt resistors only for the same potential.
8. COM pattern
 - Both of the COM terminals should be connected together.
9. RFE circuit
 - To setup R and C parameter for fault clear time, please refer to Figure 5.
 - This R is also mandatory for fault out reporting function because it is open drain structure.
10. P pattern
 - Both of the P terminals should be connected together.

12.2 Performance Charts

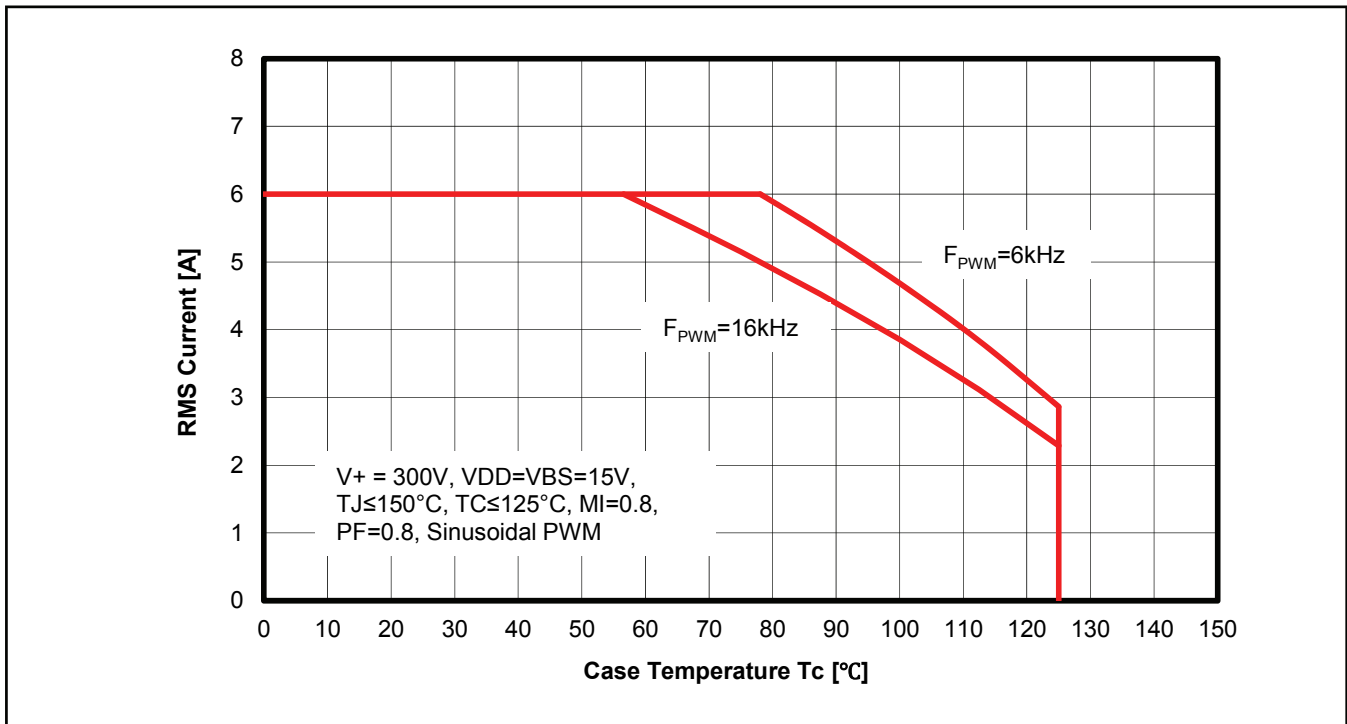


Figure 15 Maximum operating current SOA

1. This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be change by each user's actual operating conditions.

12.3 T_j vs. T_{th}

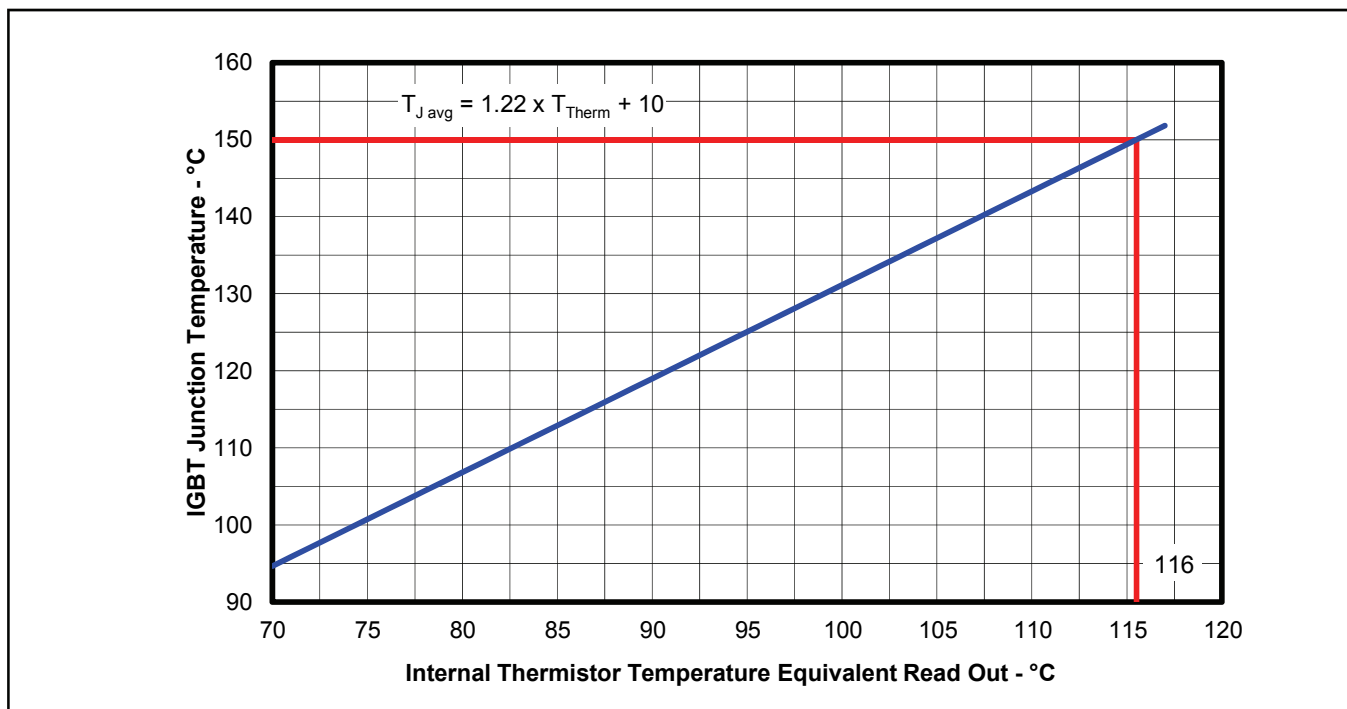


Figure 16 Typical T_j vs T_{th} correlation, sinusoidal modulation, $V_{dc}=300V$, $I_{phase}=5Arms$, $fsw=16kHz$, $fmod=50Hz$, $MI=0.8$, $PF=0.6$

12.4 -V_s Immunity

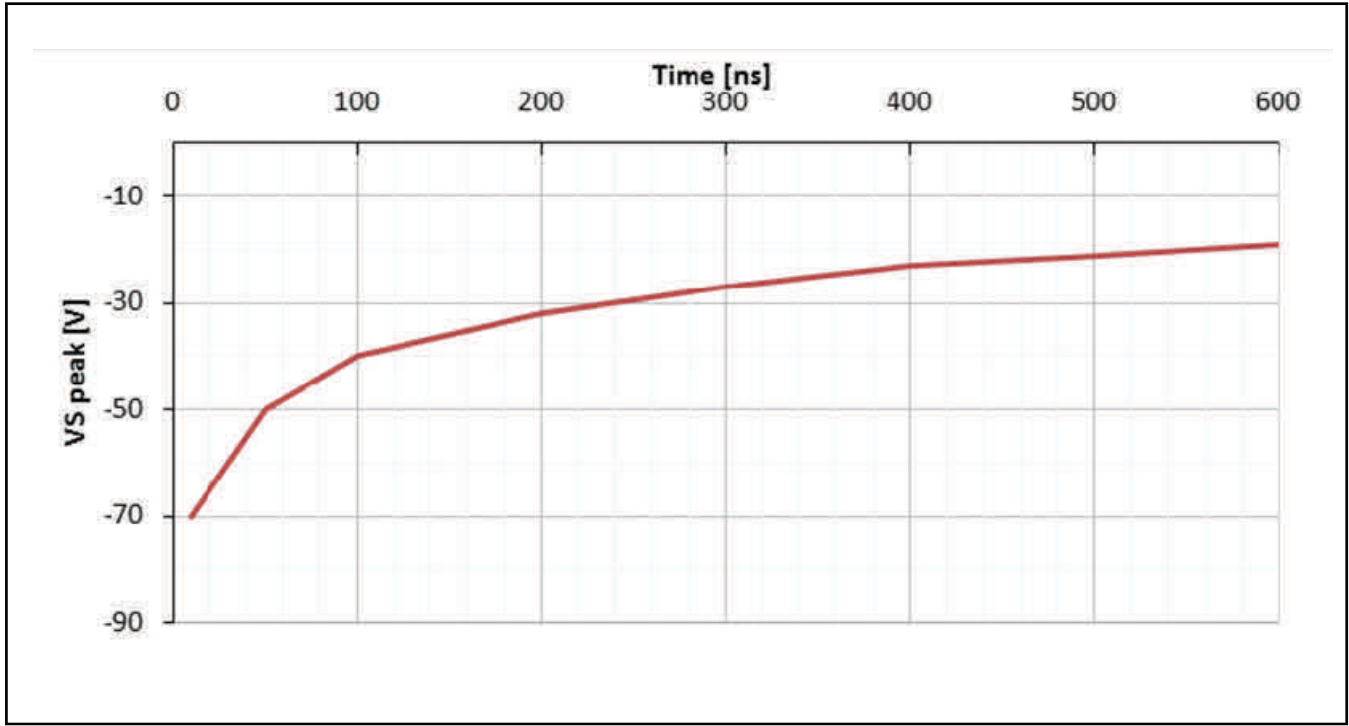


Figure 17 Negative transient Vs SOA for integrated gate driver

13 Package Outline

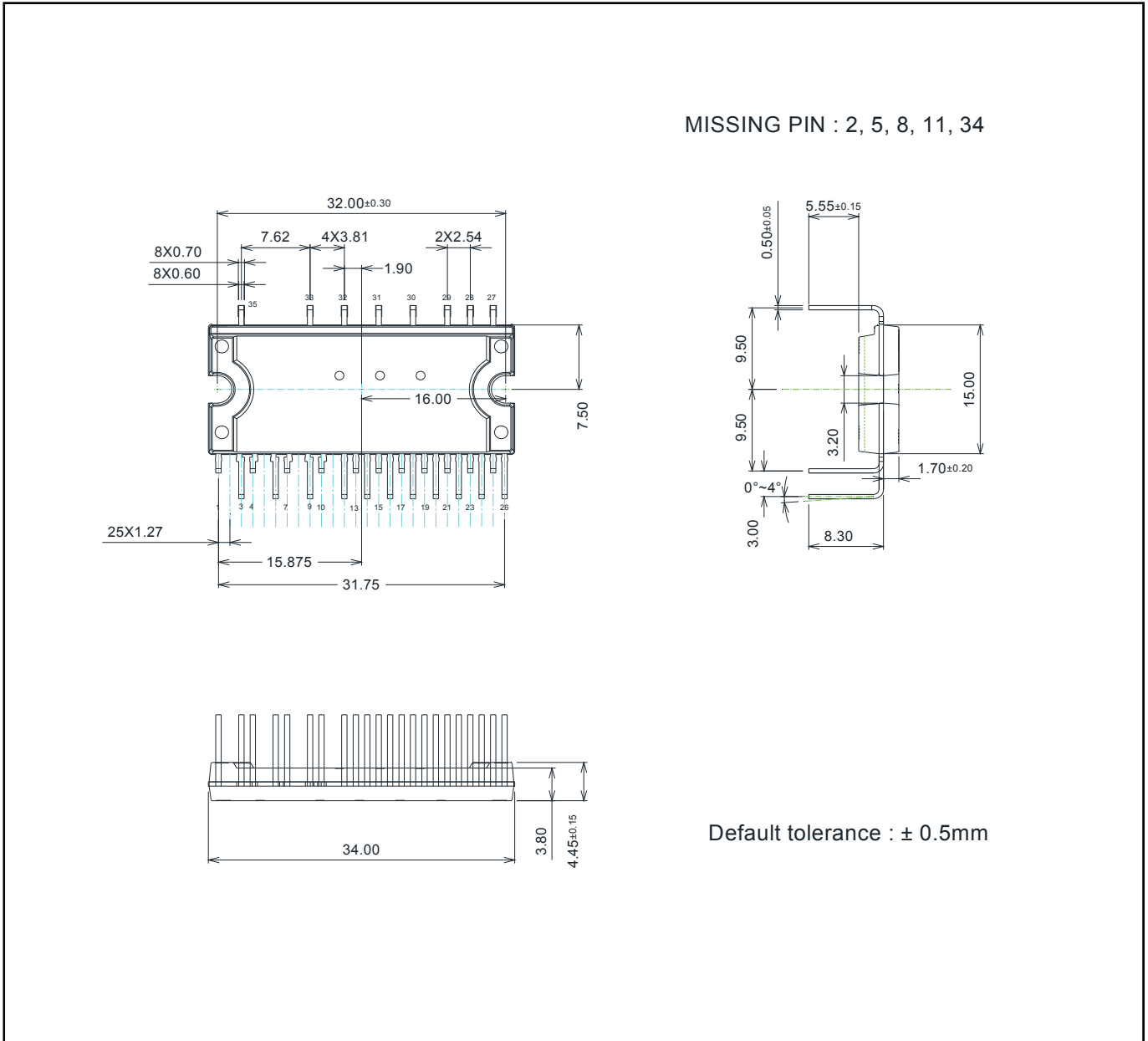


Figure 18 IM393-S6E

Package Information

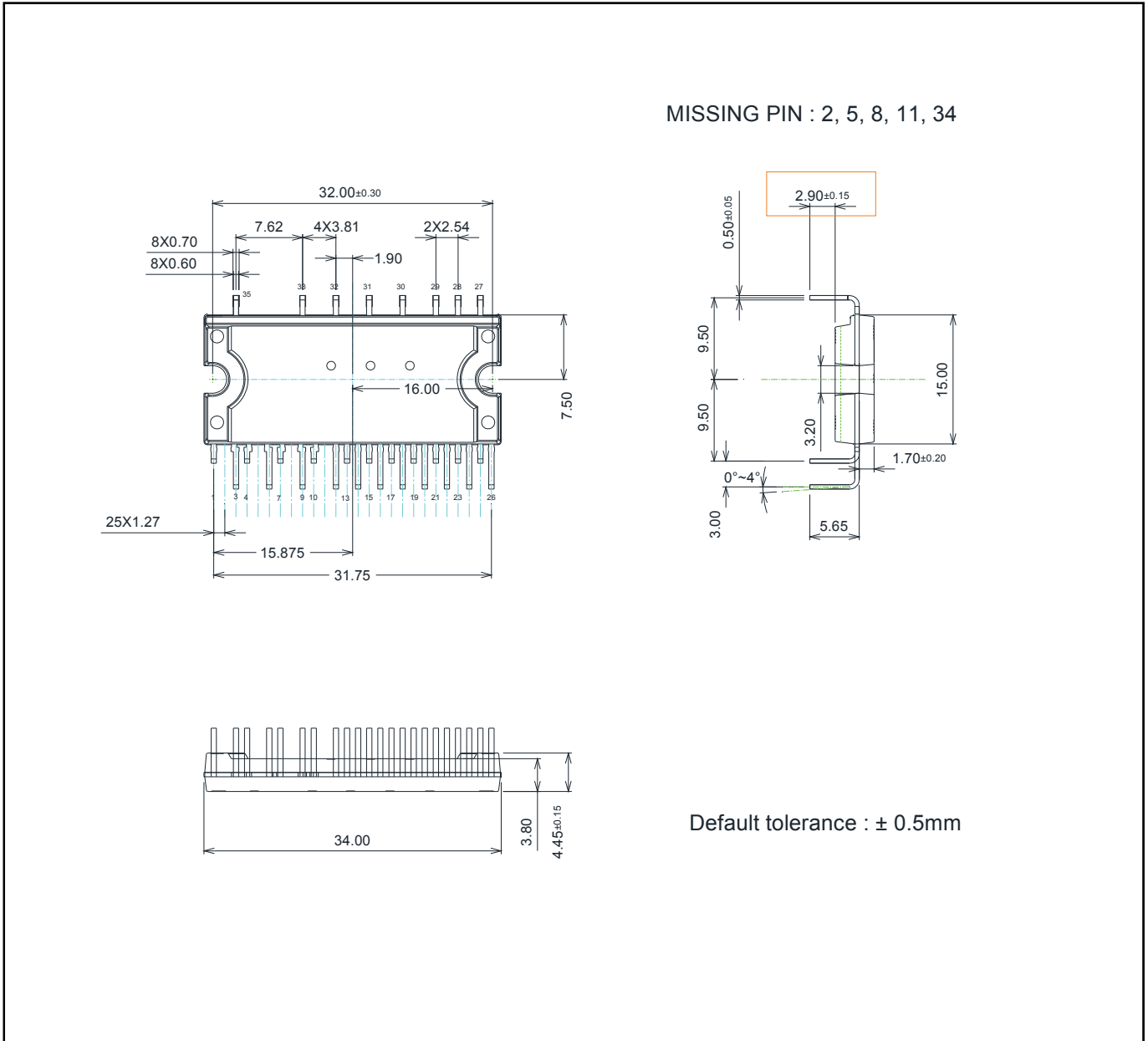


Figure 19 IM393-S6E2

Package Information

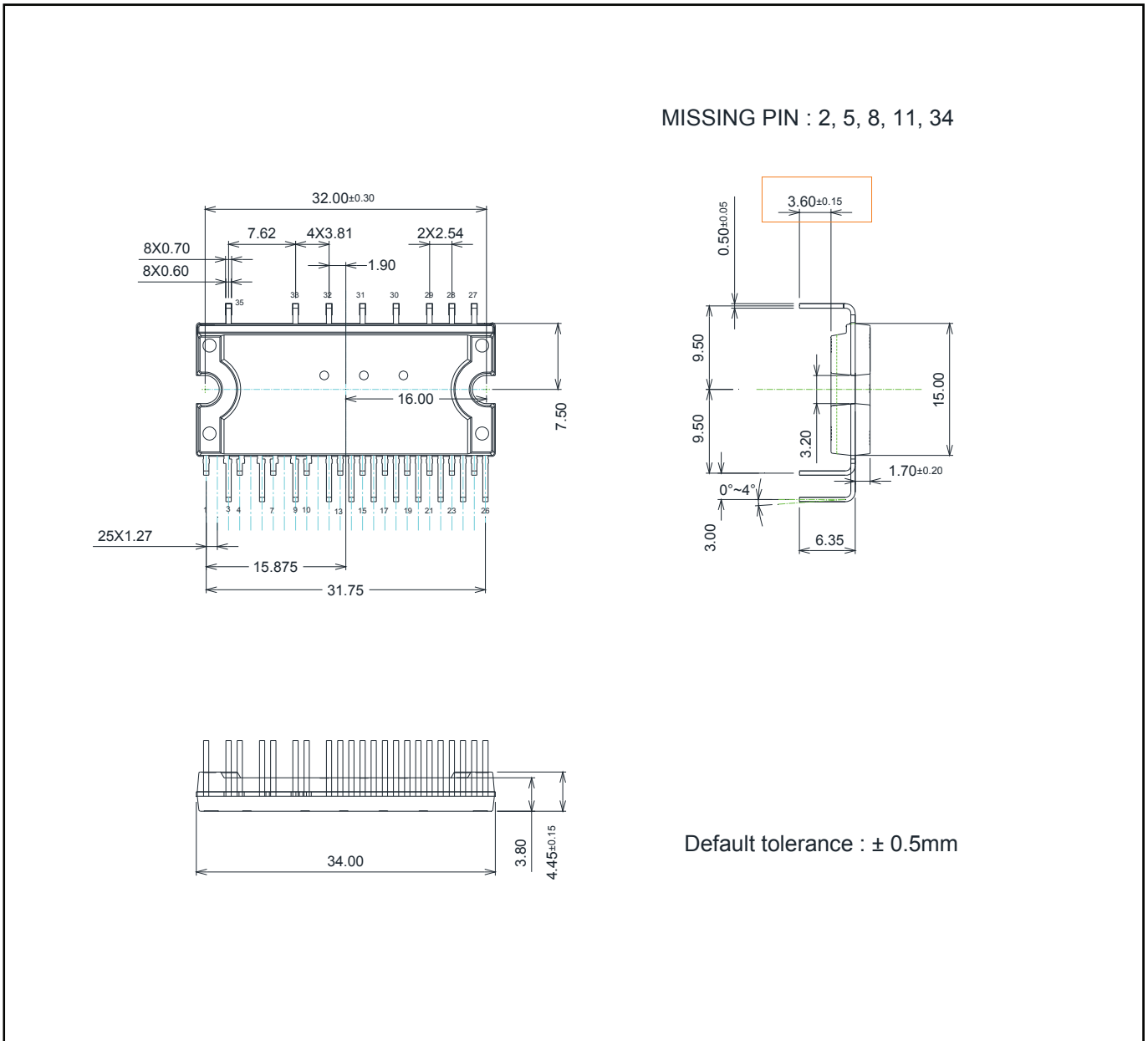


Figure 20 IM393-S6E3

Revision History

Revision History

Major changes since the last revision

| Page or Reference | Revision | Date | Description of changes |
|-------------------|----------|------|------------------------|
| | | | |

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