

# Ultra Series™ Crystal Oscillator

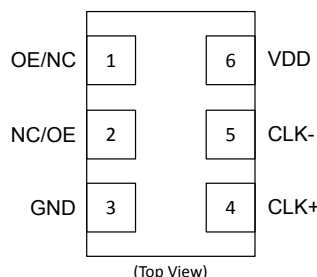
## Si560 Data Sheet

### Ultra Low Jitter Any-Frequency XO (90 fs), 0.2 to 3000 MHz

The Si560 Ultra Series™ oscillator utilizes Silicon Laboratories' advanced 4<sup>th</sup> generation DSPLL® technology to provide an ultra-low jitter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 3000 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. The Si560 offers excellent reliability and frequency stability as well as guaranteed aging performance. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in industry-standard 3.2x5 mm and 5x7 mm footprints, the Si560 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples 1-2 weeks after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si560 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. This process also guarantees 100% electrical testing of every device. The Si560 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.



#### Pin Assignments



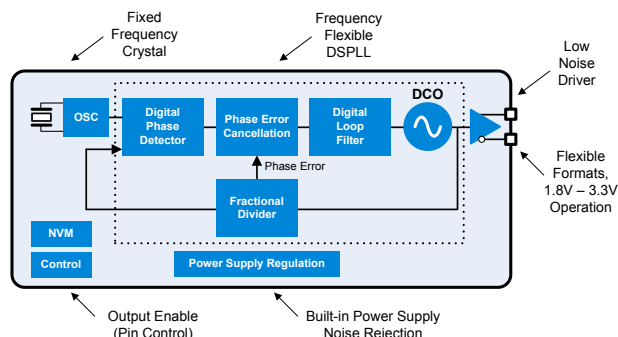
#### KEY FEATURES

- Available with any frequency from 0.2 MHz to 3000 MHz
- Ultra low jitter: 90 fs RMS typical (12 kHz – 20 MHz)
- Excellent PSRR and supply noise immunity: –80 dBc Typ
- 20 ppm temp stability (–40 to 85 °C)
- 3.3 V, 2.5 V and 1.8 V V<sub>DD</sub> supply operation from the same part number
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 3.2x5, 5x7 mm package footprints
- Samples available with 1-2 week lead times

#### APPLICATIONS

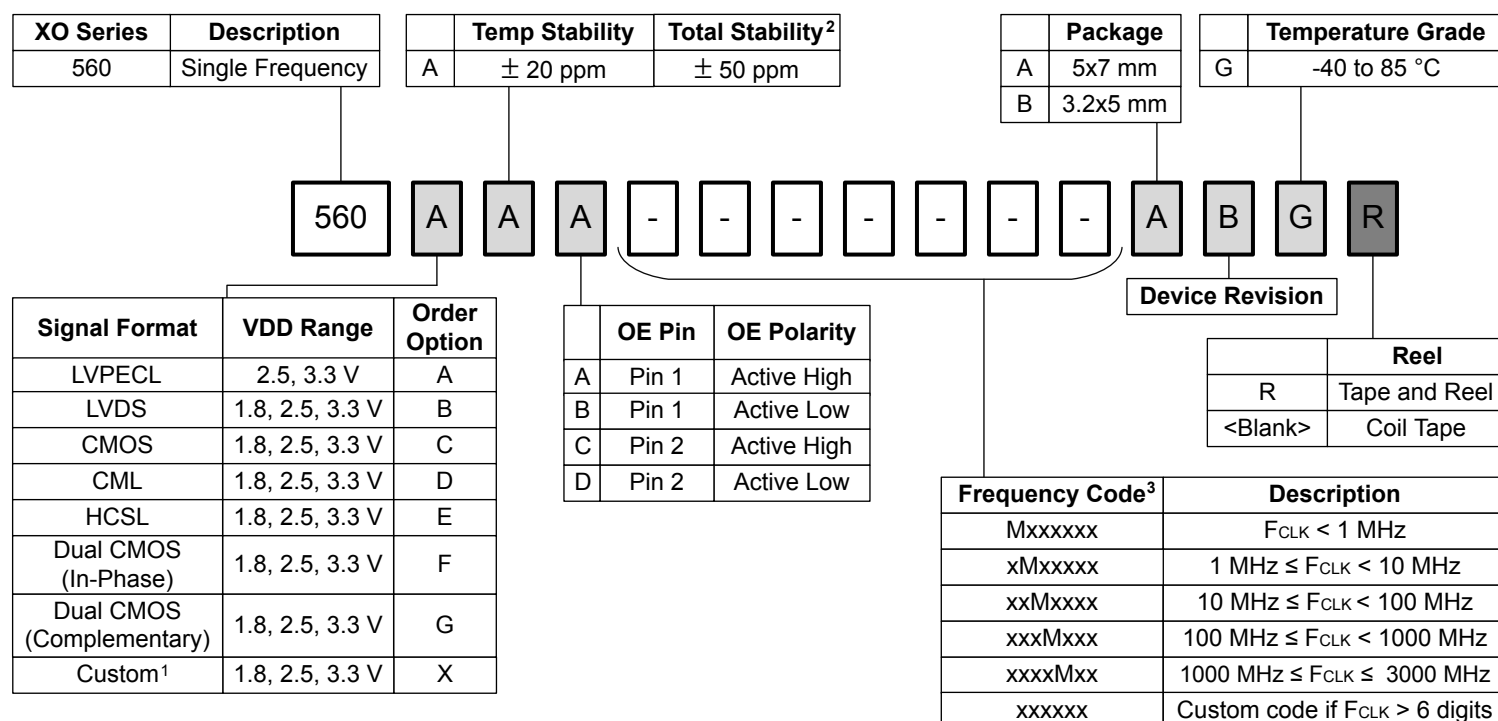
- 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 56G/112G PAM4 clocking
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- Test and measurement
- FPGA/ASIC clocking

Pin #	Descriptions
1, 2	Selectable via ordering option OE = Output enable; NC = No connect
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output. Not used for CMOS.
6	VDD = Power supply



## 1. Ordering Guide

The Si560 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to [www.silabs.com/oscillators](http://www.silabs.com/oscillators) to access this tool and for further ordering instructions.



### Notes:

1. Contact Silicon Labs for non-standard configurations.
2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
3. For example: 156.25 MHz = 156M250; 25 MHz = 25M0000. Create custom part numbers at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).

### 1.1 Technical Support

Frequently Asked Questions (FAQ)	<a href="http://www.silabs.com/Si560-FAQ">www.silabs.com/Si560-FAQ</a>
Oscillator Phase Noise Lookup Utility	<a href="http://www.silabs.com/oscillator-phase-noise-lookup">www.silabs.com/oscillator-phase-noise-lookup</a>
Quality and Reliability	<a href="http://www.silabs.com/quality">www.silabs.com/quality</a>
Development Kits	<a href="http://www.silabs.com/oscillator-tools">www.silabs.com/oscillator-tools</a>

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**

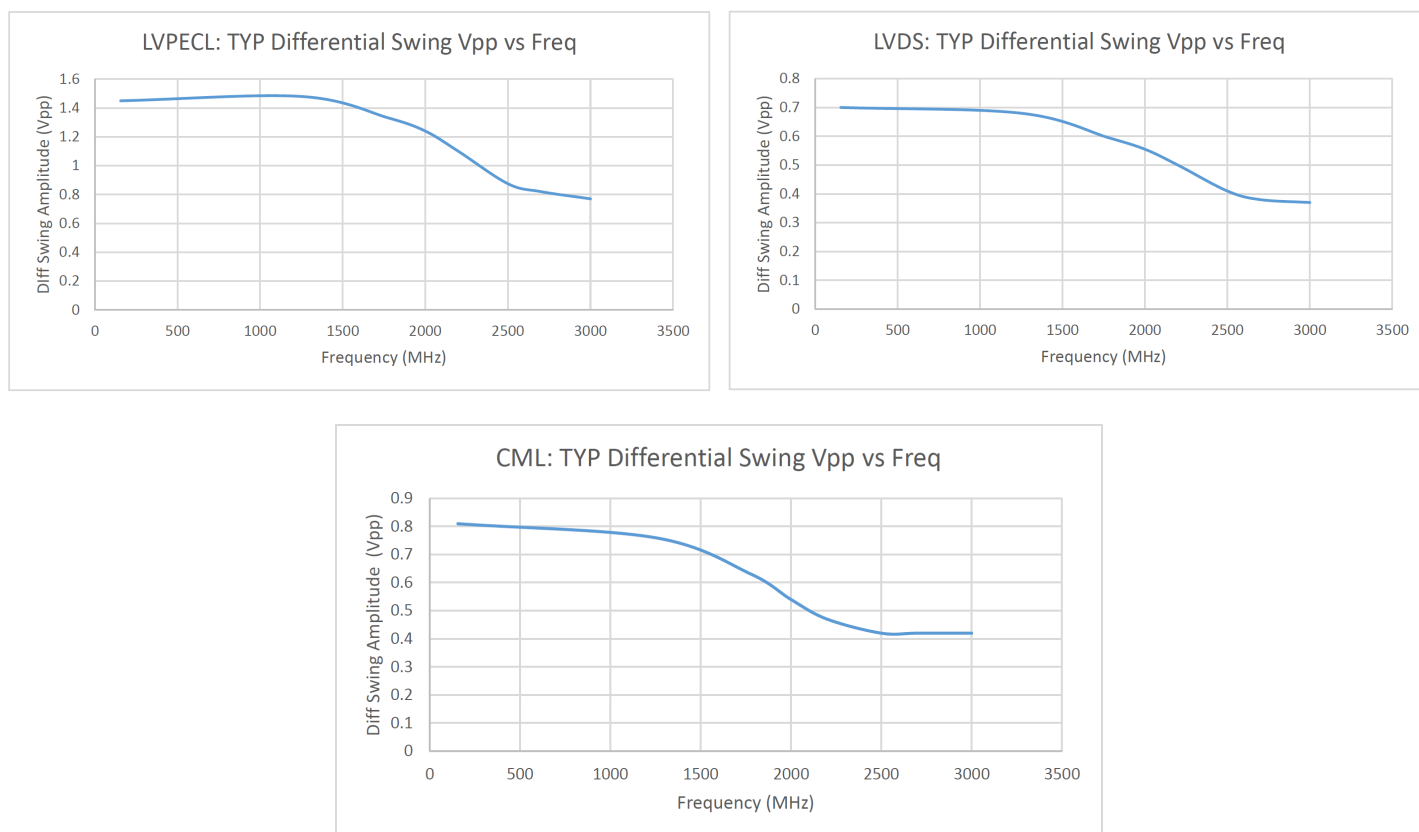
$V_{DD} = 1.8\text{ V}, 2.5\text{ or }3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	$T_A$		-40	—	85	$^\circ\text{C}$
Frequency Range	$F_{CLK}$	LVPECL, LVDS, CML	0.2	—	3000	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	$V_{DD}$	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	$I_{DD}$	LVPECL (output enabled)	—	110	160	mA
		LVDS/CML (output enabled)	—	90	157	mA
		HCSL (output enabled)	—	85	130	mA
		CMOS (output enabled)	—	85	135	mA
		Dual CMOS (output enabled)	—	95	145	mA
		Tristate Hi-Z (output disabled)	—	73	—	mA
Temperature Stability		Frequency stability Grade A	-20	—	20	ppm
Total Stability <sup>1</sup>	$F_{STAB}$	Frequency stability Grade A	-50	—	50	ppm
Rise/Fall Time (20% to 80% $V_{PP}$ )	$T_R/T_F$	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS, ( $C_L = 5\text{ pF}$ )	—	0.5	1.5	ns
		HCSL, $F_{CLK} > 50\text{ MHz}$	—	—	550	ps
Duty Cycle	$D_C$	All formats	45	—	55	%
Output Enable (OE) <sup>2</sup>	$V_{IH}$		$0.7 \times V_{DD}$	—	—	V
	$V_{IL}$		—	—	$0.3 \times V_{DD}$	V
	$T_D$	Output Disable Time, $F_{CLK} > 10\text{ MHz}$	—	—	3	$\mu\text{s}$
	$T_E$	Output Enable Time, $F_{CLK} > 10\text{ MHz}$	—	—	20	$\mu\text{s}$
Powerup Time	$t_{OSC}$	Time from $0.9 \times V_{DD}$ until output frequency ( $F_{CLK}$ ) within spec	—	—	10	ms
LVPECL Output Option <sup>3</sup>	$V_{OC}$	Mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	$V_O$	Swing (diff, $F_{CLK} \leq 1.5\text{ GHz}$ )	1.1	—	1.9	$V_{PP}$
		Swing (diff, $F_{CLK} > 1.5\text{ GHz}$ ) <sup>6</sup>	0.55	—	1.7	$V_{PP}$
LVDS Output Option <sup>4</sup>	$V_{OC}$	Mid-level (2.5 V, 3.3 V VDD)	1.125	1.20	1.275	V
		Mid-level (1.8 V VDD)	0.8	0.9	1.0	V
	$V_O$	Swing (diff, $F_{CLK} \leq 1.5\text{ GHz}$ )	0.5	0.7	0.9	$V_{PP}$
		Swing (diff, $F_{CLK} > 1.5\text{ GHz}$ ) <sup>6</sup>	0.25	0.5	0.8	$V_{PP}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Option <sup>5</sup>	$V_{OH}$	Output voltage high	660	800	850	mV
	$V_{OL}$	Output voltage low	-150	0	150	mV
	$V_C$	Crossing voltage	250	410	550	mV
CML Output Option (AC-Coupled)	$V_O$	Swing (diff, $F_{CLK} \leq 1.5$ GHz)	0.6	0.8	1.0	$V_{PP}$
		Swing (diff, $F_{CLK} > 1.5$ GHz) <sup>6</sup>	0.3	0.55	0.9	$V_{PP}$
CMOS Output Option	$V_{OH}$	$I_{OH} = 8/6/4$ mA for 3.3/2.5/1.8 V VDD	$0.85 \times V_{DD}$	—	—	V
	$V_{OL}$	$I_{OL} = 8/6/4$ mA for 3.3/2.5/1.8 V VDD	—	—	$0.15 \times V_{DD}$	V

**Notes:**

1. Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 °C.
2. OE includes a 50 k $\Omega$  pull-up to VDD for OE active high, or includes a 50 k $\Omega$  pull-down to GND for OE active low.
3.  $R_{term} = 50 \Omega$  to  $V_{DD} - 2.0$  V (see Figure 4.1).
4.  $R_{term} = 100 \Omega$  (differential) (see Figure 4.2).
5.  $R_{term} = 50 \Omega$  to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.

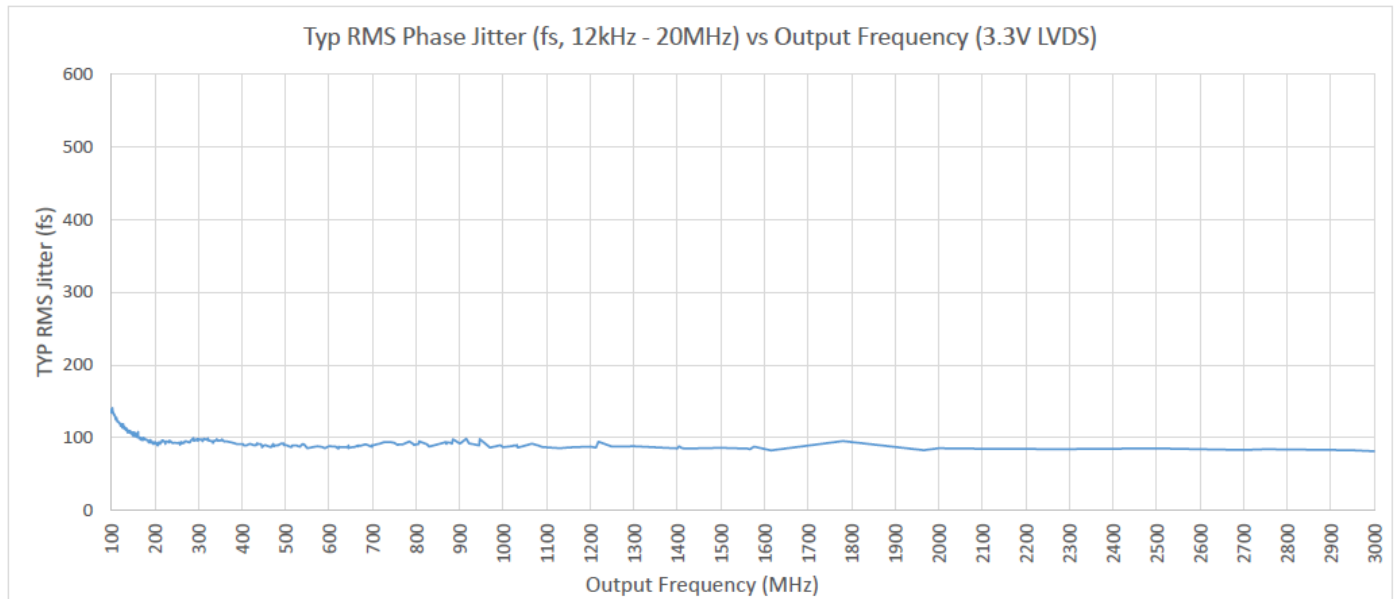
**Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency**

**Table 2.2. Clock Output Phase Jitter and PSRR** $V_{DD} = 1.8\text{ V}, 2.5\text{ or }3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ to }85\text{ }^{\circ}\text{C}$ 

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> All Differential Formats	ϕJ	F <sub>CLK</sub> ≥ 200 MHz	—	90	140	fs
		100 MHz ≤ F <sub>CLK</sub> < 200 MHz	—	105	160	fs
		LVPECL @ 156.25 MHz	—	95	125	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> CMOS / Dual CMOS Formats	ϕJ	10 MHz ≤ F <sub>CLK</sub> < 250 MHz	—	200	—	fs
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output	PSRR	100 kHz sine wave		-83		dBc
		200 kHz sine wave		-83		
		500 kHz sine wave		-82		
		1 MHz sine wave		-85		
<b>Note:</b> 1. Jitter inclusive of any spurs.						

**Table 2.3. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-105	-100	-92	dBc/Hz
1 kHz	-129	-126	-116	
10 kHz	-136	-133	-125	
100 kHz	-142	-140	-131	
1 MHz	-150	-148	-138	
10 MHz	-159	-161	-153	
20 MHz	-160	-162	-154	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	-109	-102	-92	dBc/Hz
1 kHz	-131	-126	-119	
10 kHz	-135	-134	-124	
100 kHz	-143	-141	-130	
1 MHz	-150	-148	-138	
10 MHz	-160	-162	-154	
20 MHz	-161	-163	-155	



**Figure 2.2. Phase Jitter vs. Output Frequency**

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).

**Table 2.4. Environmental Compliance and Package Information**

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL)	1
Contact Pads	Gold over Nickel

**Note:**

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: [www.silabs.com/support/quality/Pages/RoHSInformation.aspx](http://www.silabs.com/support/quality/Pages/RoHSInformation.aspx).

**Table 2.5. Thermal Conditions**

Package	Parameter	Symbol	Test Condition	Value	Unit
3.2 × 5 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	80.3	°C/W
	Thermal Resistance Junction to Board	$\Theta_{JB}$	Still Air, 85 °C	50.8	°C/W
	Max Junction Temperature	$T_J$	Still Air, 85 °C	125	°C
5 × 7 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	68.4	°C/W
	Thermal Resistance Junction to Board	$\Theta_{JB}$	Still Air, 85 °C	52.9	°C/W
	Max Junction Temperature	$T_J$	Still Air, 85 °C	125	°C

**Table 2.6. Absolute Maximum Ratings<sup>1</sup>**

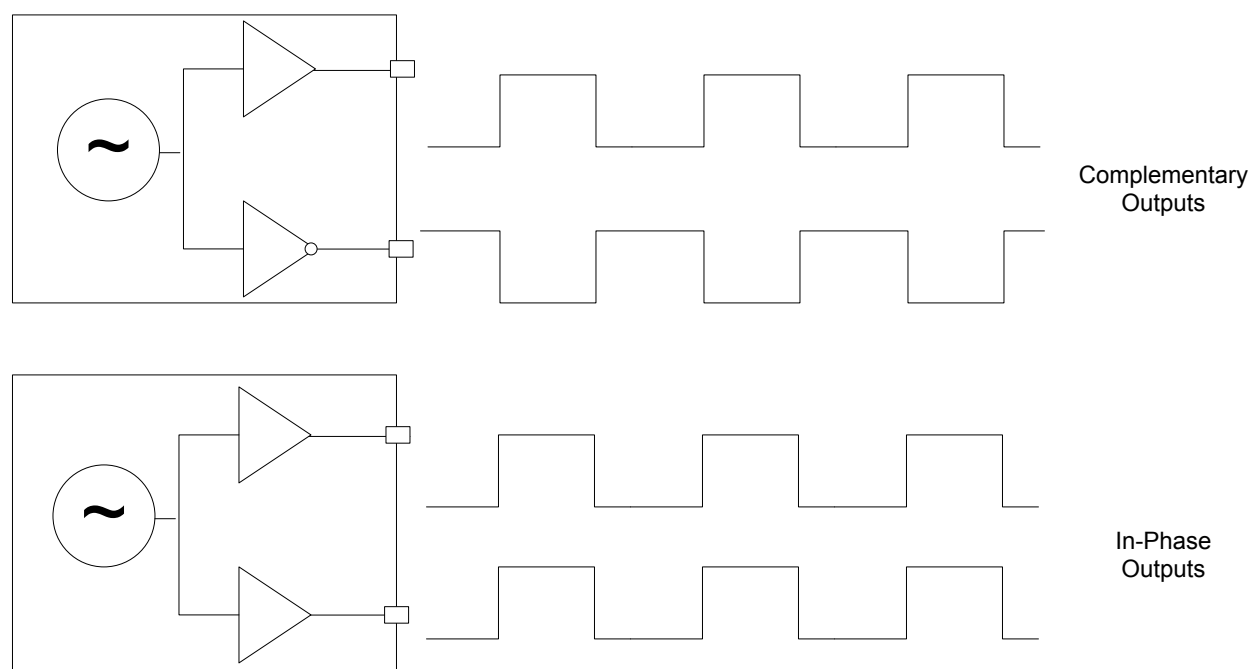
Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	$T_{AMAX}$	95	°C
Storage Temperature	$T_S$	–55 to 125	°C
Supply Voltage	$V_{DD}$	–0.5 to 3.8	°C
Input Voltage	$V_{IN}$	–0.5 to $V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature <sup>2</sup>	$T_{PEAK}$	260	°C
Solder Time at $T_{PEAK}$ <sup>2</sup>	$T_P$	20–40	sec

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

### 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si560 device.

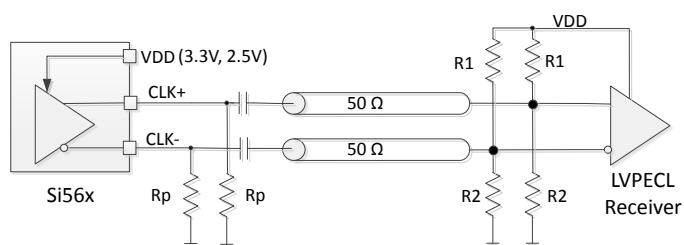


**Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

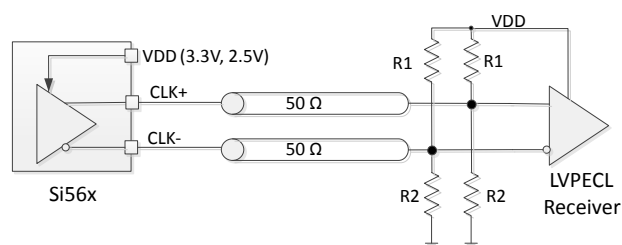


## 4. Recommended Output Terminations

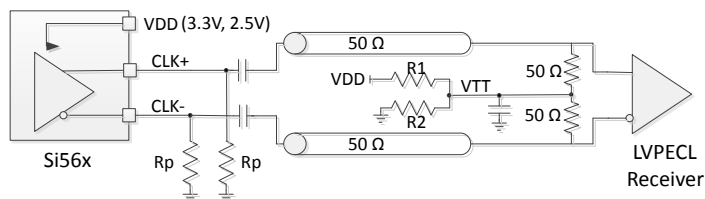
The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.



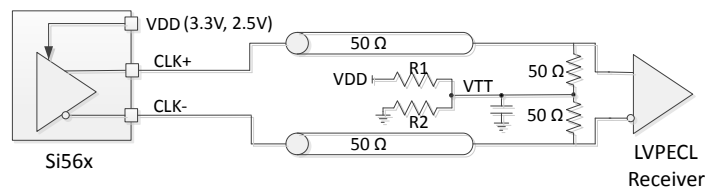
AC-Coupled LVPECL – Thevenin Termination



DC-Coupled LVPECL – Thevenin Termination



AC-Coupled LVPECL - 50 Ω w/VTT Bias



DC-Coupled LVPECL - 50 Ω w/VTT Bias

Figure 4.1. LVPECL Output Terminations

AC-Coupled LVPECL Termination Resistor Values			
VDD	R1	R2	Rp
3.3 V	127 Ω	82.5 Ω	130 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω

DC-Coupled LVPECL Termination Resistor Values		
VDD	R1	R2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

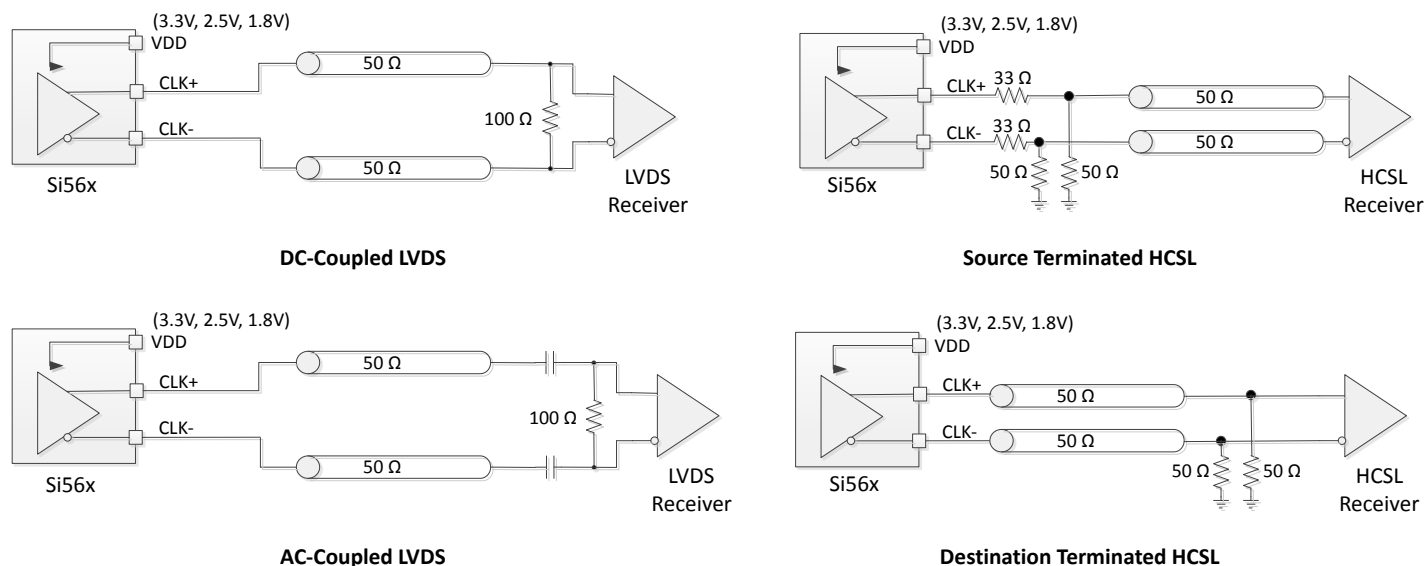


Figure 4.2. LVDS and HCSL Output Terminations

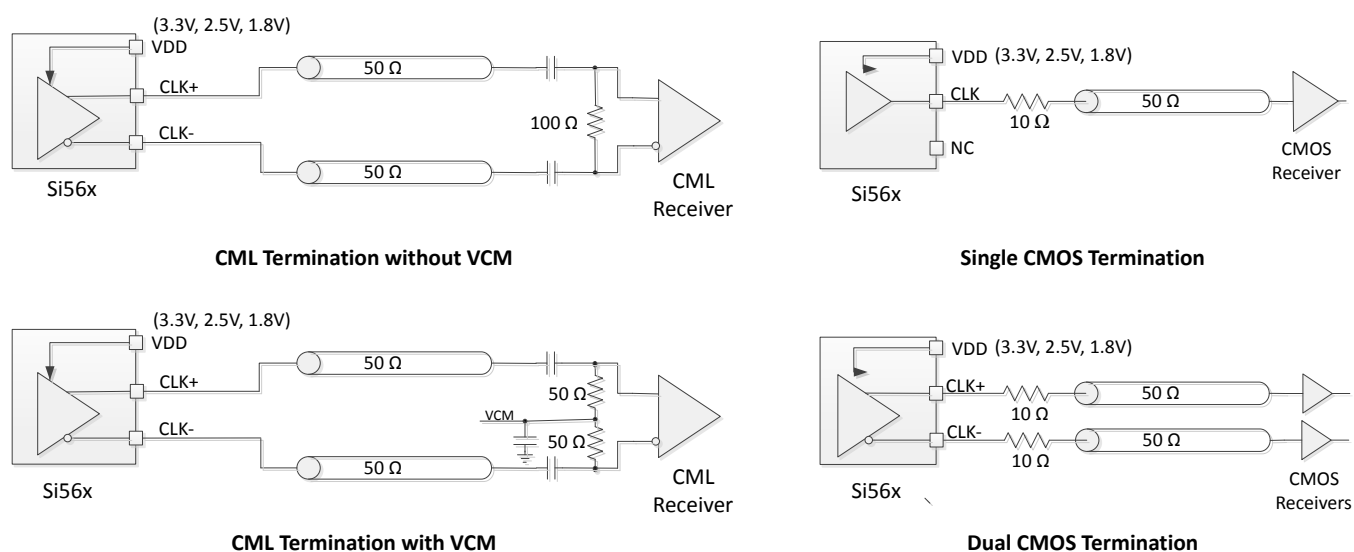


Figure 4.3. CML and CMOS Output Terminations

## 5. Package Outline

### 5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si560. The table below lists the values for the dimensions shown in the illustration.

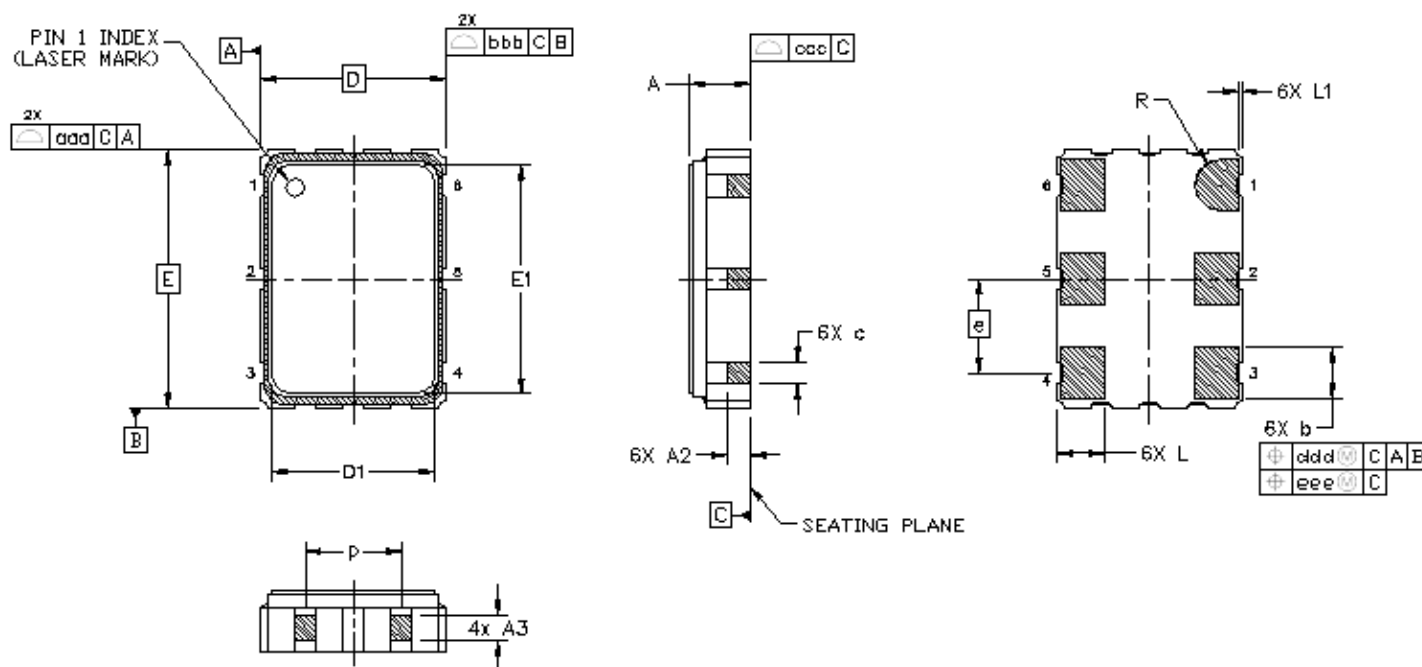


Figure 5.1. Si560 (5×7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

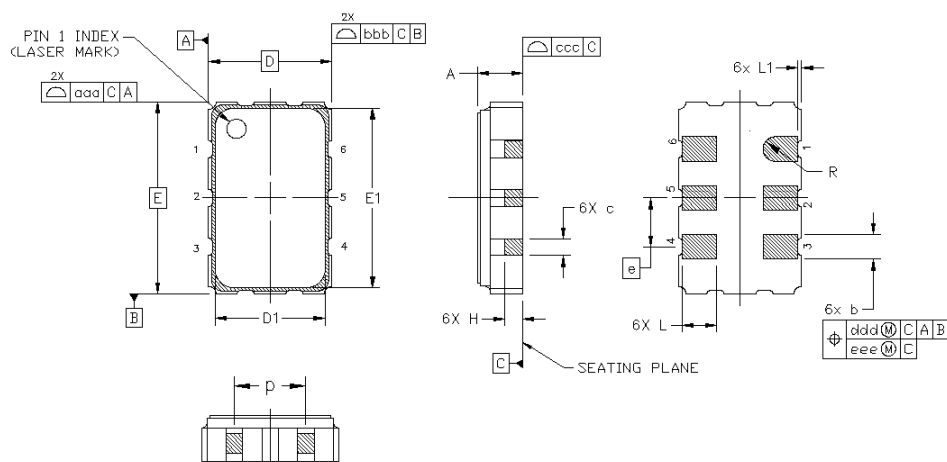
Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.13	1.28	1.43	L	1.17	1.27	1.37
A2	0.50	0.55	0.60	L1	0.05	0.10	0.15
A3	0.50	0.55	0.60	p	1.70	—	1.90
b	1.30	1.40	1.50	R	0.70 REF		
c	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.30	4.40	4.50	ccc	0.08		
e	2.54 BSC			ddd	0.10		
E	7.00 BSC			eee	0.05		
E1	6.10	6.20	6.30				

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si560. The table below lists the values for the dimensions shown in the illustration.



**Figure 5.2. Si560 (3.2×5 mm) Outline Diagram**

**Table 5.2. Package Diagram Dimensions (mm)**

Dimension	Min	Nom	Max
A	1.06	1.17	1.33
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D	3.20 BSC		
D1	2.55	2.60	2.65
e	1.27 BSC		
E	5.00 BSC		
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.80	0.90	1.00
L1	0.05	0.10	0.15
p	1.36	1.46	1.56
R	0.32 REF		
aaa	0.15		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.05		

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 6. PCB Land Pattern

### 6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si560. The table below lists the values for the dimensions shown in the illustration.

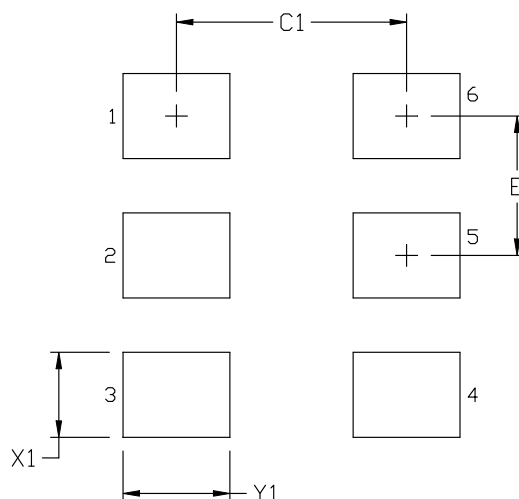


Figure 6.1. Si560 (5×7 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

#### Notes:

##### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

##### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

##### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

##### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si560. The table below lists the values for the dimensions shown in the illustration.

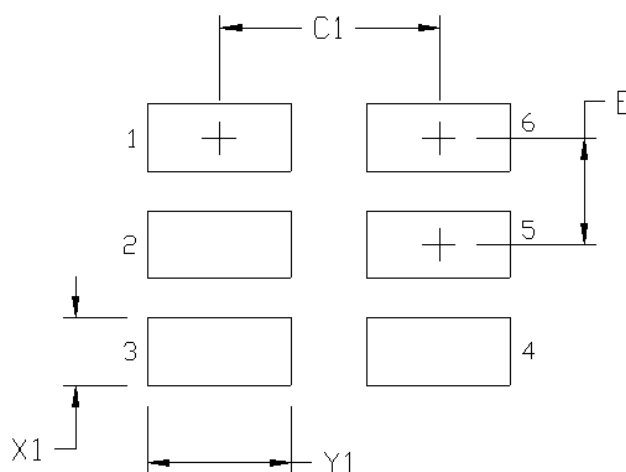


Figure 6.2. Si560 (3.2×5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

### Notes:

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
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3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

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#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 7. Top Marking

The figure below illustrates the mark specification for the Si560. The table below lists the line information.

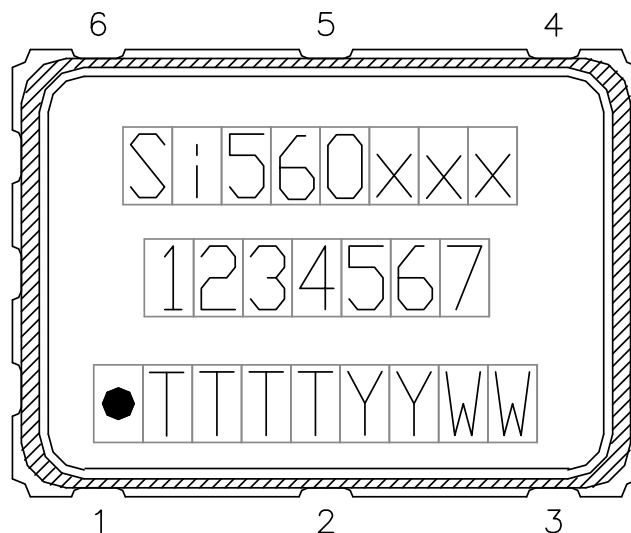


Figure 7.1. Mark Specification

Table 7.1. Si560 Top Mark Description

Line	Position	Description
1	1–8	"Si560", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si560AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

## 8. Revision History

### Revision 1.0

June, 2018

- Initial release.





## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



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[www.silabs.com/timing](http://www.silabs.com/timing)



**SW/HW**  
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**Quality**  
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**Support and Community**  
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Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>