

LTC4225-1/LTC4225-2 Dual Ideal Diode and Hot Swap Controller

DESCRIPTION

Demonstration circuit 1624A contains two independent rail circuits each with Hot Swap™ and ideal diode functionality provided by the LTC4225-1/LTC4225-2 dual ideal diode and Hot Swap controller.

DC1624A facilitates evaluation of LTC4225 performance in different operation modes such as supply ramp-up, power supply switchover, steady state, and overcurrent faults. Power supply switchover mode can be realized as either an ideal diode functionality or as a prioritizer functionality.

Each DC1624A rail circuit is assembled to operate with a 12V supply and 11.5A maximum current load.

The main components of the board are the LTC4225 controller, two MOSFETs operating as ideal diodes, two MOSFETs operating as Hot Swap devices, two power sense resistors, two jumpers for independently enabling each

rail, four LEDs to indicate power good and fault conditions separately for each channel, and input voltage snubbers. There are pads for optional RC circuits for each Hot Swap MOSFET gate in order to adjust output voltage slew rate.

The standard configuration (as DC1624A populated by default) places the ideal diode MOSFET ahead of the Hot Swap MOSFET. The board also has pads for an alternative configuration with the Hot Swap MOSFET located ahead of the ideal diode MOSFET.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN}	Input Supply Range		2.9		18	V
V _{INTVCC(UVL)}	Internal V _{CC} Undervoltage Lockout	INTV _{CC} Rising	2.1	2.2	2.3	V
V _{INTVCC(HYST)}	Internal V _{CC} Undervoltage Lockout Hysteresis		30	60	90	mV

Ideal Diode Control

ΔV _{FWD(REG)}	Forward Regulation Voltage (V _{INN} - V _{OUT})		10	25	40	mV
ΔV _{DGATE}	External N-Channel Gate Drive (V _{DGATEN} - V _{INN})	ΔV _{FWD} = 0.1V IN < 7V IN = 7V to 18V	5 10	7 12	14 14	V V
I _{CPO(UP)}	CPO _N Pull-Up Current	CPO = IN = 2.9V CPO = IN = 18V	-60 -50	-95 -85	-120 -110	μA μA
I _{DGATE(FPU)}	DGATE _N Fast Pull-Up Current	ΔV _{FWD} = 0.2V, ΔV _{DGATE} = 0V, CPO = 17V		-1.5		A
I _{DGATE(FPD)}	DGATE _N Fast Pull-Down Current	ΔV _{FWD} = -0.2V, ΔV _{DGATE} = 5V		1.5		A

Hot Swap Control

ΔV _{SENSE(CB)}	Circuit Breaker Trip Sense Voltage (V _{INN} - V _{ISENSEN})		47.5	50	52.5	mV
ΔV _{SENSE(ACL)}	Active Current Limit Sense Voltage (V _{INN} - V _{ISENSEN})		55	65	75	mV

DEMO MANUAL DC1624A

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{HGATE(UP)}	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	7	10	13	μA
I _{HGATE(DN)}	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	150	300	500	μA
I _{HGATE(FPD)}	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	100	200	300	mA

Input/Output Pin

V _{ON(TH)}	ON _N On Pin Threshold Voltage	ON Rising	1.21	1.235	1.26	V
V _{ON(RESET)}	ON _N Pin Fault Reset Threshold Voltage	ON Falling	0.55	0.6	0.63	V
V _{EN(TH)}	EN _N Pin Threshold Voltage	EN Rising	1.185	1.235	1.284	V
V _{TMR(TH)}	TMR _N Pin Threshold Voltage	TMR Rising TMR Falling	1.198 0.15	1.235 0.2	1.272 0.25	V V
I _{TMR(UP)}	TMR _N Pin Pull-Up Current	TMR = 1V, In Fault Mode	75	100	125	μA
I _{TMR(DN)}	TMR _N Pin Pull-Down Current	TMR = 2V, No Faults	1.4	2	2.6	μA
I _{TMR(RATIO)}	TMR _N Current Ratio I _{TMR(DN)} /I _{TMR(UP)}		1.4	2	2.7	%

QUICK START PROCEDURE

The LTC4225 functions as an ideal diode with inrush current limiting and overcurrent protection by controlling two external back-to-back N-channel MOSFETs in a power path. The LTC4225 has two ideal diode and two Hot Swap controllers. Each ideal diode MOSFET is intended to operate with a defined Hot Swap MOSFET, because they are tied by common on/off control, and ideal diode controller sense voltage includes both MOSFETs and sense resistor voltage drop. Therefore, LTC4225 provides independent control for the two input supplies.

The LTC4225 gate drive amplifiers (DGATE_N) monitor the voltage between the IN_N and OUT_N pins and drive the DGATE_N pins. The amplifier quickly pulls up the DGATE pin, turning on the MOSFET (Q1 or Q3), for ideal diode control when it senses a large forward voltage drop.

Pulling the ON pin high and EN pins low initiates a 100ms debounce timing cycle. After 100ms, a 10μA current source from the charge pump ramps up the HGATE_N pin. When the Hot Swap MOSFET (Q2 or Q4) turns on, the inrush current is limited to a set level set by an external sense resistor placed between IN and SENSE pins.

An active current limit amplifier servos the gate of the MOSFET to 65mV across the current sense resistor. Inrush current can be further reduced, if desired, by adding a capacitor from HGATE to GND. When the MOSFET's gate overdrive (HGATE to OUT voltage) exceeds 4.2V, the PWRGD pin pulls low.

When both MOSFETs (Q1 and Q2 or Q3 and Q4) are turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop (V_{IN} - V_{OUT}) across the sense resistor and the back-to-back MOSFETs to 25mV. If the load current causes more than 25mV of voltage drop, the gate voltage rises to enhance the MOSFET used for ideal diode control. For large output currents the MOSFET's gate is driven fully on and the voltage drop is equal to the sum of the I_{LOAD} • RD_{S(ON)} of the two MOSFETs in series.

In the case of an input supply short circuit when the MOSFETs are conducting, a large reverse current starts flowing from the load towards the input. The gate drive amplifier detects this failure condition as soon as it appears and turns off the ideal diode MOSFET by pulling down the DGATE pin.

QUICK START PROCEDURE

Demonstration circuit DC1624A can be easily to set up to evaluate the performance of the LTC4225-1/LTC4225-2. Refer to the Figure 1 for proper measurement equipment setup and follow the procedure below.

The DC1624A test includes independent tests of the LTC4225 Hot Swap functionality, ideal diode functionality and two power rails prioritizer functionality with the channel 1 highest priority.

HOT SWAP FUNCTIONALITY TEST

This test is identical for each 12V rail and is performed in the three steps by the measuring of the transient's parameters in the different operation modes.

The first step is a power-up without any additional load. The second step is the current limit operation after successful power-up transient. The third step is a power-up with a shorted output.

Initially install the jumper heads in the following positions:

- ON1_SEL and ON2_SEL in position OFF;
- EN1_SEL and EN2_SEL in position LOW.

First Step

Connect a 12V power supply to the board input turrets IN1 (IN2) and GND. Do not load the output. Place current probe on the 12V supply and voltage probes on the OUT1 (OUT2) turret.

Provide ON1 (ON2) signal at the ON1 (ON2) pin by moving the ON1_SEL (ON2_SEL) jumper header from OFF

position to the ON position. Observe the transient. The output voltage rise time should be in the range of 12ms to 29ms. $\overline{\text{PWRGD1}}$ ($\overline{\text{PWRGD2}}$) green LED should be lit. Turn off the rail using the ON1_SEL (ON2_SEL) jumper.

Second Step

Initially adjust an electronic resistive load to 10 Ω to 12 Ω and connect it to the OUT1 (OUT2) turret and GND. Turn on the rail and slowly increase load current up to the circuit breaker threshold level. The current limit range should be from 11.5A to 13.3A. Turn off the rail using the ON1_SEL (ON2_SEL) jumper.

Third Step

Short the output to ground with a wire. Place the current probe on this wire. Turn on the rail and record the current shape. The maximum current should be in the (13.6A to 18.9A) range. The LTC4225-1 latches off after overcurrent condition, but the LTC4225-2 automatically retries after 200ms to 450ms.

IDEAL DIODE FUNCTIONALITY TEST

Use an individual 12V power supply for each rail; connect the two outputs together at a common load. Adjust each input voltage to 12V with maximum possible accuracy.

In this test, both rails are active and small variations in the input voltage will force one channel off and the other channel on.

QUICK START PROCEDURE

Place a voltmeter between IN1 and IN2 turrets to measure the difference between two input voltages. Activate both rails and keep a load around 1A to 3A. Adjust with the input voltage levels and verify that when the difference between input voltages exceeds 40mV only one rail is active.

THE PRIORITIZER FUNCTIONALITY TEST

The DC1624A is assembled with components to implement a two power rails prioritizer with channel 1 having the higher priority.

Install R17 with 470 and R18 with 41.2k.

Place JP5 PPR_SEL (power priority select) jumper in position ON2 and JP4 ON2_SEL (ON2 select) in position OFF. Apply independent supply voltages (12V) to both inputs. Channel 1 will be connected to load. Reduce channel 1 input voltage until it reaches an undervoltage condition and D5 (PWRGD2) lights. At the same time channel 2 power supply will deliver power to the load.

QUICK START PROCEDURE

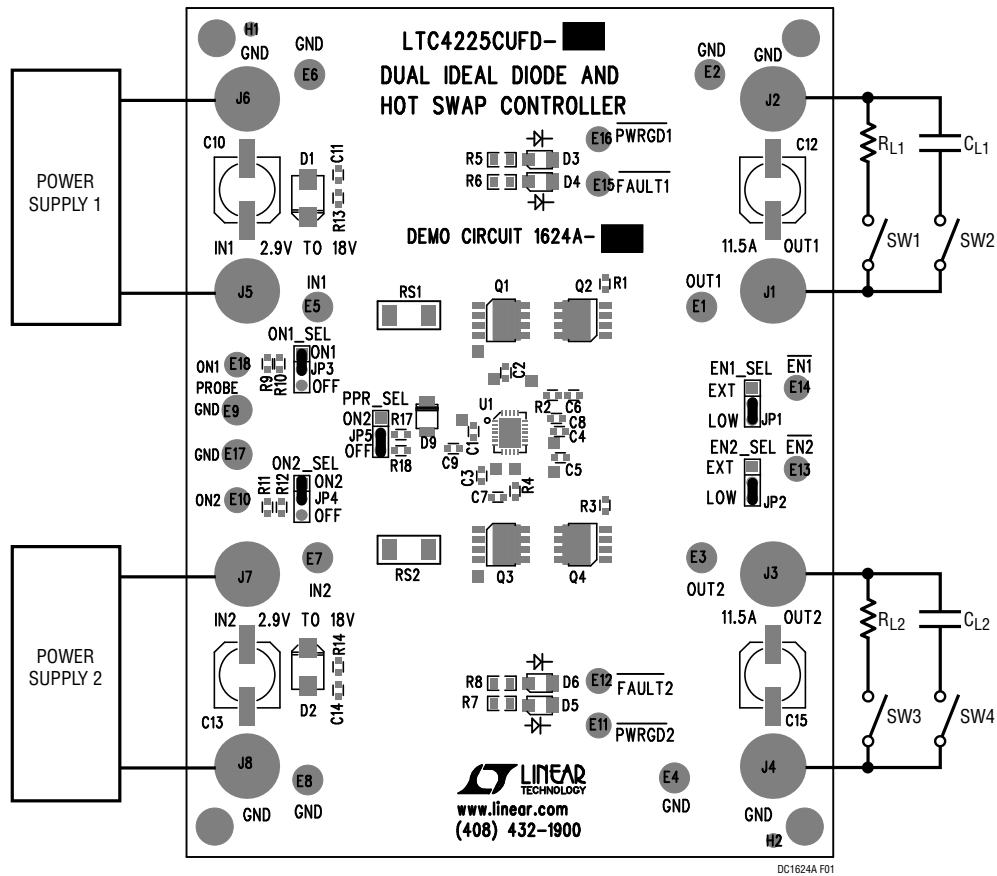


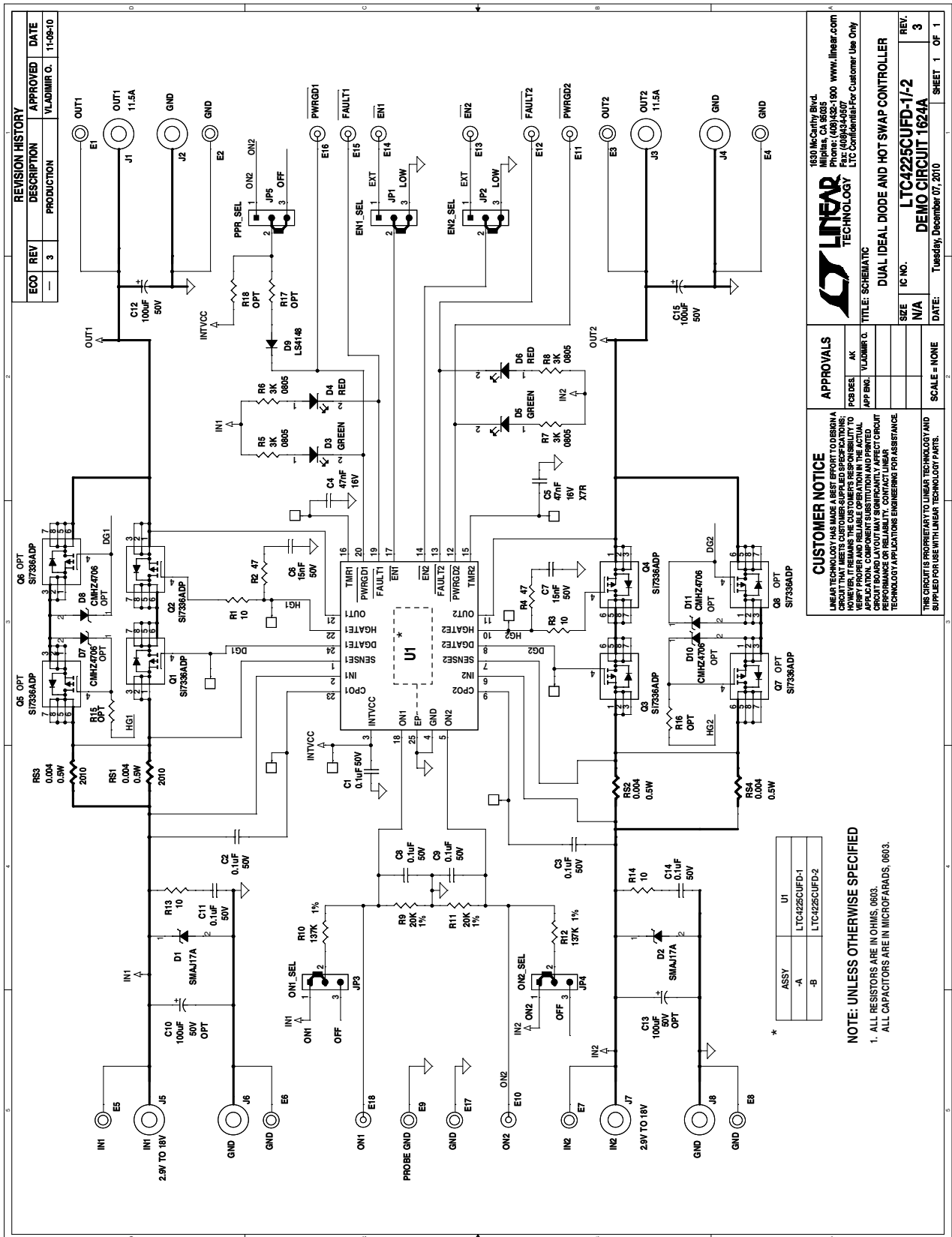
Figure 1. Measurement Equipment Setup for Hot Swap Functionality Test

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PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	7	C1, C2, C3, C8, C9, C11, C14	CAP, X7R, 0.1 μ F, 50V, 0603	AVX, 06035C104KAT
2	2	C4, C5	CAP, X7R, 47nF, 50V, 0603	AVX, 06035C473KAT
3	2	C6, C7	CAP, X7R, 15nF, 50V, 0603	AVX, 06035C153KAT
4	0	C10, C13	OPT	
5	2	C12, C15	CAP, AL, EI, S/M 100 μ F, 50V	SANYO, 50CE100BS
6	2	D1, D2	DIODE, VOLTAGE SUPP 13V 5% SMA	VISHAY, SMAJ17A-E3
7	2	D3, D5	LED, SMT GREEN	PANASONIC, LN1351C
8	2	D4, D6	LED, SMT RED	PANASONIC, LN1251CTR
9	0	D7, D8, D10, D11	OPT	
10	1	D9	DIODE, SWITCHING, SOD80	VISHAY, LS4148
11	8	E10 to E16, E18	TURRET, TESTPOINT, 2308	MILL-MAX, 2308-2-00-80-00-00-07-0
12	10	E1 to E9, E17	TURRET, TESTPOINT, 2501	MILL-MAX, 2501-2-00-80-00-00-07-0
13	8	J1 to J8	JACK BANANA	KEYSTONE, 575-4
14	5	JP1, JP2, JP3, JP4, JP5	HEADERS, 3 PINS 2mm CTRS	SAMTEC TMM-103-02-L-S
15	5	XJP1, XJP2, XJP3, XJP4, XJP5	SHUNT, 2mm CTRS	SAMTEC 2SN-BK-G
16	4	Q1, Q2, Q3, Q4,	N-CHANNEL 30-V MOSFET, PPSO-8	VISHAY, Si7336ADP
17	0	Q5, Q6, Q7, Q8	OPT	
18	2	RS1, RS2	RES, CHIP, 0.004, 1/2W, 1%, 2010	VISHAY, WSL20104L000FEA
19	0	RS3, RS4	OPT	
20	4	R1, R3, R13, R14	RES, CHIP, 10, 1%, 0603	VISHAY, CRCW060310R0FKEA
21	2	R2, R4	RES, CHIP, 47, 1%, 0603	VISHAY, CRCW060347R0FKEA
22	4	R5, R6, R7, R8	RES, CHIP, 3k, 1%, 0805	VISHAY, CRCW08053K00FKEA
23	2	R9, R11	RES, CHIP, 20k, 1%, 0603	VISHAY, CRCW060320K0FKEA
24	2	R10, R12	RES, CHIP, 137k, 1%, 0603	VISHAY, CRCW0603137KFKEA
25	0	R15, R16, R17, R18	OPT	
26	4	MTGS AT 4 CORNERS	STANDOFF, NYLON, 0.25, 1/4"	KEYSTONE, 8832 (SNAP ON)

SCHEMATIC DIAGRAM



REVISION HISTORY			
ECCO	REV	DESCRIPTION	APPROVED DATE
—	3	PRODUCTION	V.LADMIR O. 11-08-10

		1800 McCarty Blvd. Milpitas, CA 95028 Phone: 415.964.1900 www.linear.com Fax: 415.964.1999 LTC Confidential For Customer Use Only	
TITLE: SCHEMATIC		DUAL IDEAL DIODE AND HOT SWAP CONTROLLER	
IC NO.		LTC4225CUIFD-1/2	
SIZE		N/A	
DATE:		Tuesday, December 07, 2010	
SCALE = NONE		SHEET 1 OF 1	

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NOTE: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS, 0603.
 ALL CAPACITORS ARE IN MICROFARADS, 0603.

ASSY	U1
-A	LTC4225CUIFD-1
-B	LTC4225CUIFD-2



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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