# 0.5 dB LSB, 6-Bit, Silicon Digital Attenuator, 9 kHz to 40 GHz

Data Sheet

# ADRF5720

## FEATURES

- Ultrawideband frequency range: 9 kHz to 40 GHz
- Attenuation range: 0.5 dB steps to 31.5 dB
- Low insertion loss with impedance match
  - 2.0 dB up to 18 GHz
  - 2.8 dB up to 26 GHz
  - 4.5 dB up to 40 GHz
- Attenuation accuracy with impedance match
  - ±(0.20 + 1.0% of attenuation state) up to 18 GHz
  - ±(0.20 + 1.5% of attenuation state) up to 26 GHz
  - ±(0.40+ 3.0% of attenuation state) up to 40 GHz
- Typical step error with impedance match
  - ±0.25 dB up to 26 GHz
  - ±0.65 dB up to 40 GHz
- High input linearity
  - P0.1dB insertion loss state: 30 dBm
  - P0.1dB other attenuation states: 27 dBm
  - IP3: 50 dBm typical
- High RF input power handling: 27 dBm average, 30 dBm peak
- Tight distribution in relative phase
- No low frequency spurious signals
- SPI and parallel mode control, CMOS/LVTTL compatible
- RF amplitude settling time (0.1 dB of final RF output): 8 µs
- 24-terminal, 4 mm × 4 mm LGA package
- Pin-compatible with ADRF5730, fast switching version

## APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

## FUNCTIONAL BLOCK DIAGRAM

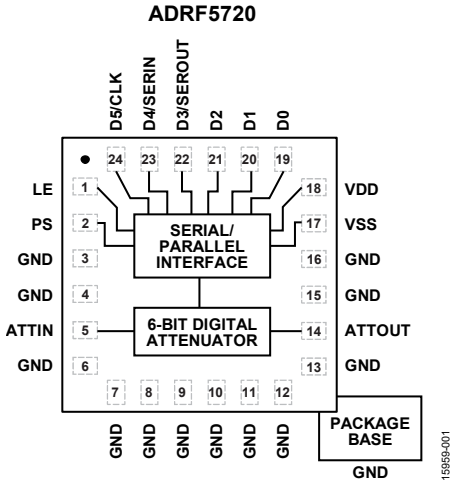


*Figure 1.*

## GENERAL DESCRIPTION

The ADRF5720 is a silicon, 6-bit digital attenuator with 31.5 dB attenuation control range in 0.5 dB steps.

This device operates from 9 kHz to 40 GHz with better than 4.5 dB of insertion loss and excellent attenuation accuracy. The ATTIN port of the ADRF5720 has a radio frequency (RF) input power handling capability of 27 dBm average and 30 dBm peak for all states.

The ADRF5720 requires a dual supply voltage of +3.3 V and −3.3 V. The device features serial peripheral interface (SPI), parallel mode control, and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5720 is pin-compatible with the ADRF5730, the fast switching version, which operates from 100 MHz to 40 GHz.

The ADRF5720 RF ports are designed to match a characteristic impedance of 50 Ω. For wideband applications, impedance matching on the RF transmission lines can further optimize high frequency insertion loss, return loss, and attenuation accuracy characteristics. Refer to the Electrical Specifications section, the Typical Performance Characteristics section, and the Applications Information section for more details.

The ADRF5720 comes in a 24-terminal, 4 mm × 4 mm, RoHS compliant, land grid array (LGA) package and operates from −40°C to +105°C.

Rev. A


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**7/2018—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, digital voltages = 0 V or VDD, case temperature ($T_{CASE}$) = 25°C, and 50 Ω system, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FREQUENCY RANGE | | 0.009 | | 40,000 | MHz |
| INSERTION LOSS (IL) | | | | | |
| With Impedance Match | See Figure 44 | | | | |
| | 9 kHz to 10 GHz | | 1.5 | | dB |
| | 10 GHz to 18 GHz | | 2.0 | | dB |
| | 18 GHz to 26 GHz | | 2.8 | | dB |
| | 26 GHz to 35 GHz | | 3.7 | | dB |
| | 35 GHz to 40 GHz | | 4.5 | | dB |
| Without Impedance Match | See Figure 43 | | | | |
| | 9 kHz to 10 GHz | | 1.6 | | dB |
| | 10 GHz to 18 GHz | | 2.1 | | dB |
| | 18 GHz to 26 GHz | | 2.7 | | dB |
| | 26 GHz to 35 GHz | | 3.6 | | dB |
| | 35 GHz to 40 GHz | | 4.6 | | dB |
| RETURN LOSS | ATTIN and ATTOUT, all attenuation states | | | | |
| With Impedance Match | See Figure 44 | | | | |
| | 9 kHz to 10 GHz | | 18 | | dB |
| | 10 GHz to 18 GHz | | 17 | | dB |
| | 18 GHz to 26 GHz | | 17 | | dB |
| | 26 GHz to 35 GHz | | 15 | | dB |
| | 35 GHz to 40 GHz | | 15 | | dB |
| Without Impedance Match | See Figure 43 | | | | |
| | 9 kHz to 10 GHz | | 18 | | dB |
| | 10 GHz to 18 GHz | | 15 | | dB |
| | 18 GHz to 26 GHz | | 15 | | dB |
| | 26 GHz to 35 GHz | | 14 | | dB |
| | 35 GHz to 40 GHz | | 11 | | dB |
| ATTENUATION | | | | | |
| Range | Between minimum and maximum attenuation states | | 31.5 | | dB |
| Step Size | Between any successive attenuation states | | 0.5 | | dB |
| Accuracy | Referenced to insertion loss | | | | |
| With Impedance Match | See Figure 44 | | | | |
| | 9 kHz to 10 GHz | | ±(0.15 + 1.0% of state) | | dB |
| | 10 GHz to 18 GHz | | ±(0.20 + 1.0% of state) | | dB |
| | 18 GHz to 26 GHz | | ±(0.20 + 1.5% of state) | | dB |
| | 26 GHz to 35 GHz | | ±(0.25 + 2.5% of state) | | dB |
| | 35 GHz to 40 GHz | | ±(0.40 + 3.0% of state) | | dB |
| Without Impedance Match | See Figure 43 | | | | |
| | 9 kHz to 10 GHz | | ±(0.15 + 1.0% of state) | | dB |
| | 10 GHz to 18 GHz | | ±(0.25 + 1.0% of state) | | dB |
| | 18 GHz to 26 GHz | | ±(0.20 + 1.5% of state) | | dB |
| | 26 GHz to 35 GHz | | ±(0.25 + 2.0% of state) | | dB |
| | 35 GHz to 40 GHz | | ±(0.40 + 5.0% of state) | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Step Error | Between any successive state | | | | |
| With Impedance Match | See Figure 44 | | | | |
| | 9 kHz to 10 GHz | | ±0.15 | | dB |
| | 10 GHz to 18 GHz | | ±0.23 | | dB |
| | 18 GHz to 26 GHz | | ±0.25 | | dB |
| | 26 GHz to 35 GHz | | ±0.50 | | dB |
| | 35 GHz to 40 GHz | | ±0.65 | | dB |
| Without Impedance Match | See Figure 43 | | | | |
| | 9 kHz to 10 GHz | | ±0.15 | | dB |
| | 10 GHz to 18 GHz | | ±0.23 | | dB |
| | 18 GHz to 26 GHz | | ±0.25 | | dB |
| | 26 GHz to 35 GHz | | ±0.40 | | dB |
| | 35 GHz to 40 GHz | | ±0.70 | | dB |
| RELATIVE PHASE | Referenced to insertion loss | | | | |
| With Impedance Match | See Figure 44 | | | | |
| | 10 GHz | | 15 | | Degrees |
| | 18 GHz | | 30 | | Degrees |
| | 26 GHz | | 50 | | Degrees |
| | 35 GHz | | 75 | | Degrees |
| | 40 GHz | | 100 | | Degrees |
| Without Impedance Match | See Figure 43 | | | | |
| | 10 GHz | | 15 | | Degrees |
| | 18 GHz | | 30 | | Degrees |
| | 26 GHz | | 50 | | Degrees |
| | 35 GHz | | 80 | | Degrees |
| | 40 GHz | | 105 | | Degrees |
| SWITCHING CHARACTERISTICS | All attenuation states at input power = 10 dBm | | | | |
| Rise and Fall Time ($t_{RISE}$ and $t_{FALL}$) | 10% to 90% of RF output | | 1.3 | | µs |
| On and Off Time ($t_{ON}$ and $t_{OFF}$) | 50% triggered control (CTL) to 90% of RF output | | 3.9 | | µs |
| RF Amplitude Settling Time | | | | | |
| 0.1 dB | 50% triggered CTL to 0.1 dB of final RF output | | 8 | | µs |
| 0.05 dB | 50% triggered CTL to 0.05 dB of final RF output | | 10 | | µs |
| Overshoot | | | 2 | | dB |
| Undershoot | | | −1.5 | | dB |
| RF Phase Settling Time | f = 5 GHz | | | | |
| 5° | 50% triggered CTL to 5° of final RF output | | 3 | | µs |
| 1° | 50% triggered CTL to 1° of final RF output | | 4 | | µs |
| INPUT LINEARITY[1] | 1 MHz to 30 GHz | | | | |
| 0.1 dB Power Compression (P0.1dB) | | | | | |
| Insertion Loss State | | | 30 | | dBm |
| Other Attenuation States | | | 27 | | dBm |
| Third-Order Intercept (IP3) | Two-tone input power = 14 dBm per tone, Δf = 1 MHz, all attenuation states | | 50 | | dBm |
| DIGITAL CONTROL INPUTS | LE, PS, D0, D1, D2, D3/SEROUT[2], D4/SERIN, D5/CLK pins | | | | |
| Voltage | | | | | |
| Low ($V_{INL}$) | | 0 | | 0.8 | V |
| High ($V_{INH}$) | | 1.2 | | 3.3 | V |
| Current | | | | | |
| Low ($I_{INL}$) | | | <1 | | µA |
| High ($I_{INH}$) | D0, D1, D2 | | 33 | | µA |
| | LE, PS, D3/SEROUT[2], D4/SERIN, D5/CLK pins | | <1 | | µA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DIGITAL CONTROL OUTPUT | D3/SEROUT pin[2] | | | | |
| Voltage | | | | | |
| Low ($V_{OUTL}$) | | | 0 ± 0.3 | | V |
| High ($V_{OUTH}$) | | | VDD ± 0.3 | | V |
| Current ($I_{OUTL}$, $I_{OUTH}$) | | | | 0.5 | mA |
| SUPPLY CURRENT | VDD and VSS pins | | | | |
| Positive Supply Current | | | 117 | | µA |
| Negative Supply Current | | | −117 | | µA |
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Supply Voltage | | | | | |
| Positive (VDD) | | 3.15 | | 3.45 | V |
| Negative (VSS) | | −3.45 | | −3.15 | V |
| Digital Control Voltage | | 0 | | VDD | V |
| RF Power[3] | f = 1 MHz to 30 GHz, $T_{CASE}$ = 85°C[4], all attenuation states | | | | |
| Input at ATTIN | Steady state average | | | 27 | dBm |
| | Steady state peak | | | 30 | dBm |
| | Hot switching average | | | 24 | dBm |
| | Hot switching peak | | | 27 | dBm |
| Input at ATTOUT | Steady state average | | | 18 | dBm |
| | Steady state peak | | | 21 | dBm |
| | Hot switching average | | | 15 | dBm |
| | Hot switching peak | | | 18 | dBm |
| Case Temperature ($T_{CASE}$) | | −40 | | +105 | °C |

[1] Input linearity performance degrades over frequency, see Figure 30 and Figure 31.
[2] The D3/SEROUT pin is an input in parallel control mode and an output in serial control mode. See Table 5 for the pin function descriptions.
[3] For power derating over frequency, see Figure 2 to Figure 3. Applicable for all ATTIN and ATTOUT power specifications.
[4] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specifications by 3 dB.

## TIMING SPECIFICATIONS

See Figure 34, Figure 35, and Figure 36 for the timing diagrams.

**Table 2.**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCK}$ | Minimum serial period, see Figure 34 | 70 | | | ns |
| $t_{CS}$ | Control setup time, see Figure 34 | 15 | | | ns |
| $t_{CH}$ | Control hold time, see Figure 34 | | 20 | | ns |
| $t_{LN}$ | LE setup time, see Figure 34 | 15 | | | ns |
| $t_{LEW}$ | Minimum LE pulse width, see Figure 34 and Figure 36 | | 10 | | ns |
| $t_{LES}$ | Minimum LE pulse spacing, see Figure 34 | | 630 | | ns |
| $t_{CKN}$ | Serial clock hold time from LE, see Figure 34 | | 0 | | ns |
| $t_{PH}$ | Hold time, see Figure 36 | | 10 | | ns |
| $t_{PS}$ | Setup time, see Figure 36 | | 2 | | ns |
| $t_{CO}$ | Clock to output (SEROUT) time, see Figure 35 | | 20 | | ns |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Positive Supply Voltage | −0.3 V to +3.6 V |
| Negative Supply Voltage | −3.6 V to +0.3 V |
| Digital Control Inputs | |
| Voltage | −0.3 V to VDD + 0.3 V |
| Current | 3 mA |
| RF Power[1] (f = 1 MHz to 30 GHz, $T_{CASE}$ = 85°C[2]) | |
| Input at ATTIN | |
| Steady State Average | 28 dBm |
| Steady State Peak | 31 dBm |
| Hot Switching Average | 25 dBm |
| Hot Switching Peak | 28 dBm |
| Input at ATTOUT | |
| Steady State Average | 19 dBm |
| Steady State Peak | 22 dBm |
| Hot Switching Average | 16 dBm |
| Hot Switching Peak | 19 dBm |
| RF Power Under Unbiased Condition ($V_{DD}$, $V_{SS}$ = 0 V) | |
| Input at ATTIN | 21 dBm |
| Input at ATTOUT | 15 dBm |
| Temperature | |
| Junction ($T_J$) | 135°C |
| Storage | −65°C to +150°C |
| Reflow | 260°C |
| Continuous Power Dissipation ($P_{DISS}$) | 0.5 W |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | |
| ATTIN and ATTOUT Pins | 1500 V |
| Digital Pins | 2000 V |
| Charged Device Model (CDM) | 1250 V |

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.
[2] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to package bottom) thermal resistance.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JC}$ | Unit |
|---|---|---|
| CC-24-5 | 100 | °C/W |

## POWER DERATING CURVES

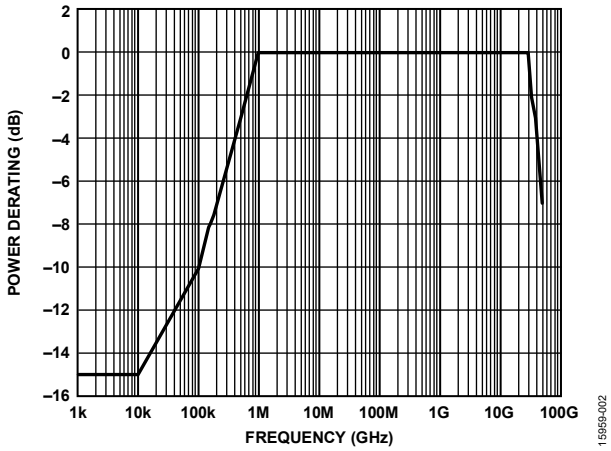


*Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE}$ = 85°C*

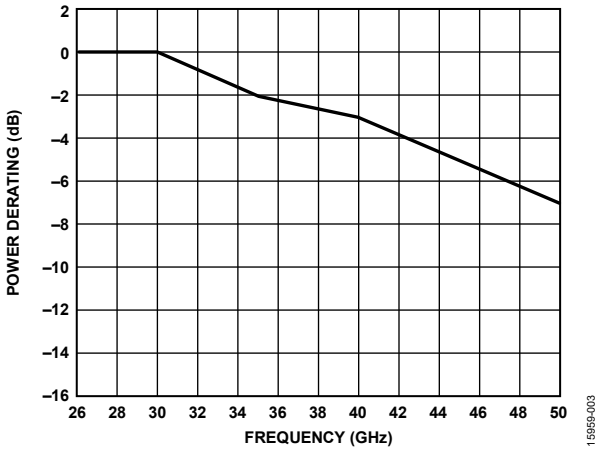


*Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE}$ = 85°C*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

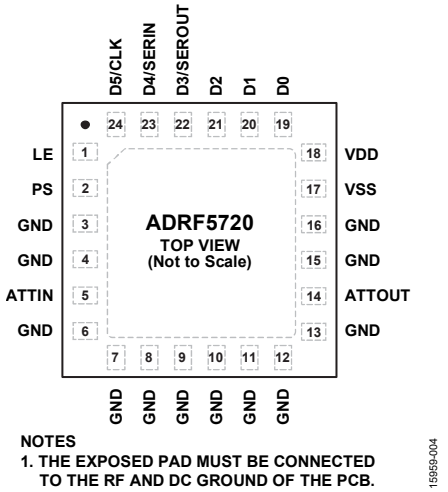


*Figure 4. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | LE | Latch Enable Input. See the Theory of Operation section for more information. |
| 2 | PS | Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. |
| 3, 4, 6 to 13, 15, 16 | GND | Ground. These pins must be connected to the RF and dc ground of the PCB. |
| 5 | ATTIN | Attenuator Input. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. |
| 14 | ATTOUT | Attenuator Output. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. |
| 17 | VSS | Negative Supply Input. |
| 18 | VDD | Positive Supply Input. |
| 19 | D0 | Parallel Control Input for 0.5 dB Attenuator Bit. See the Theory of Operation section for more information. |
| 20 | D1 | Parallel Control Input for 1 dB Attenuator Bit. See the Theory of Operation section for more information. |
| 21 | D2 | Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. |
| 22 | D3/SEROUT | Parallel Control Input for 4 dB Attenuator Bit (D3).<br>Serial Data Output (SEROUT). See the Theory of Operation section for more information. |
| 23 | D4/SERIN | Parallel Control Input for 8 dB Attenuator Bit (D4).<br>Serial Data Input (SERIN). See the Theory of Operation section for more information. |
| 24 | D5/CLK | Parallel Control Input for 16 dB Attenuator Bit (D5).<br>Serial Clock Input (CLK). See the Theory of Operation section for more information. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB. |

## INTERFACE SCHEMATICS

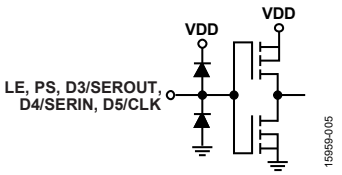


*Figure 5. Digital Input Interface (LE, PS, D3/SEROUT, D4/SERIN, D5/CLK)*

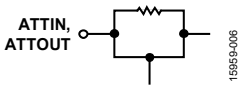


*Figure 6. ATTIN and ATTOUT Interface*

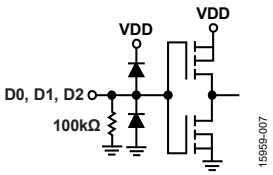


*Figure 7. Digital Input Interface (D0, D1, D2)*

# TYPICAL PERFORMANCE CHARACTERISTICS

## INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = −3.3 V, digital voltages = 0 V or VDD, $T_{CASE}$ = 25°C, and a 50 Ω system, unless otherwise noted. Measured on probe matrix board using ground signal ground (GSG) probes close to the RF pins (ATTIN and ATTOUT). See the Applications Information section for details on evaluation and probe matrix boards.

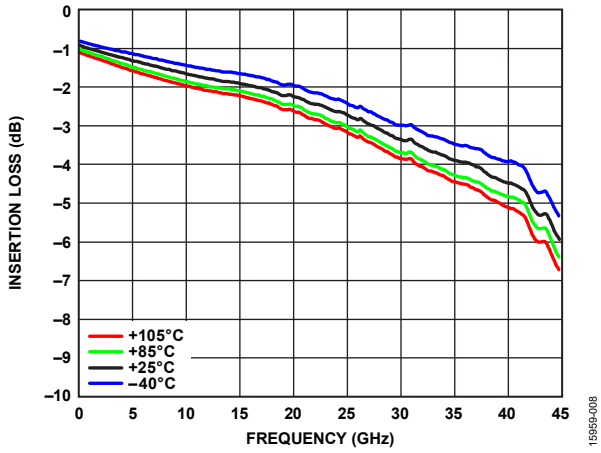


Figure 8. Insertion Loss vs. Frequency over Temperature with Impedance Match

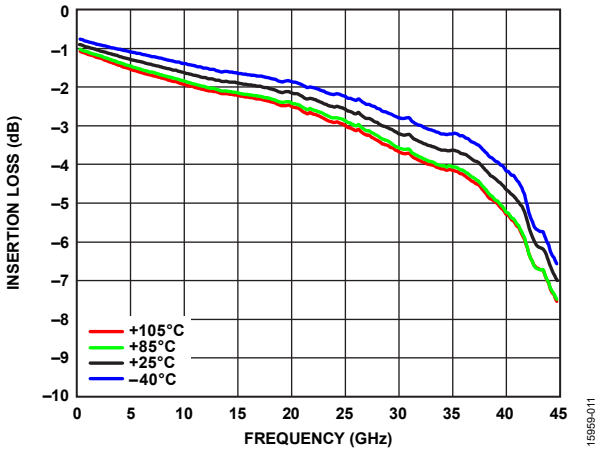


Figure 11. Insertion Loss vs. Frequency over Temperature Without Impedance Match

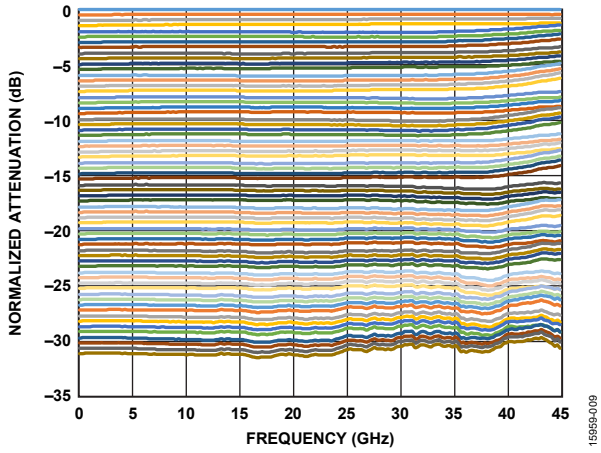


Figure 9. Normalized Attenuation vs. Frequency for All States at Room Temperature with Impedance Match

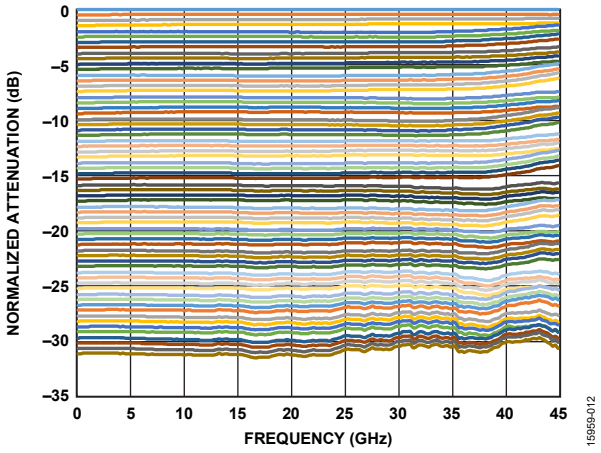


Figure 12. Normalized Attenuation vs. Frequency for All States at Room Temperature Without Impedance Match

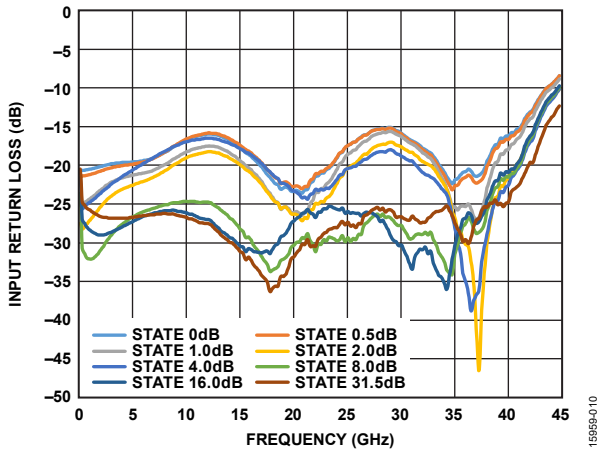


Figure 10. Input Return Loss vs. Frequency (Major States Only) with Impedance Match

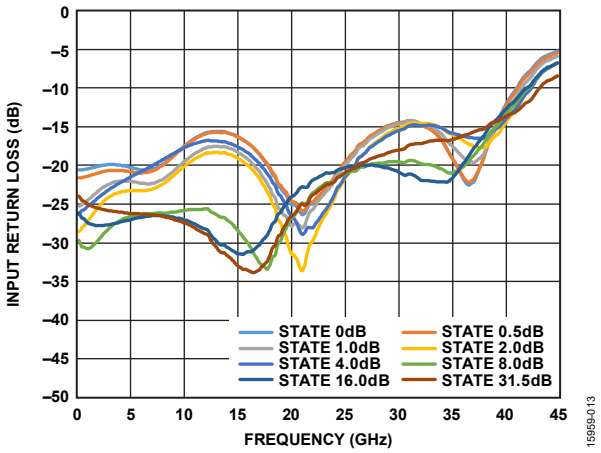


Figure 13. Input Return Loss vs. Frequency (Major States Only) Without Impedance Match

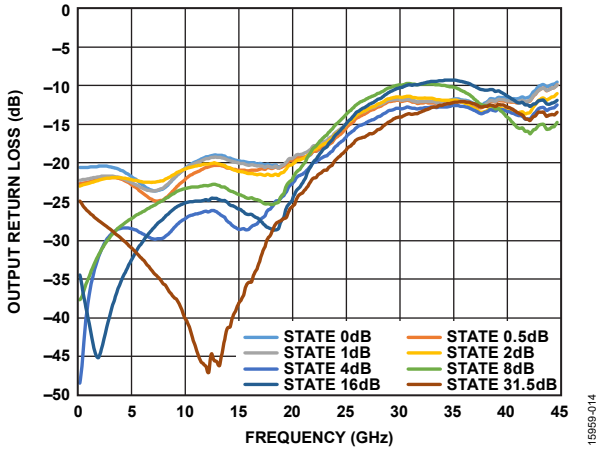


Figure 14. Output Return Loss vs. Frequency (Major States Only) with Impedance Match

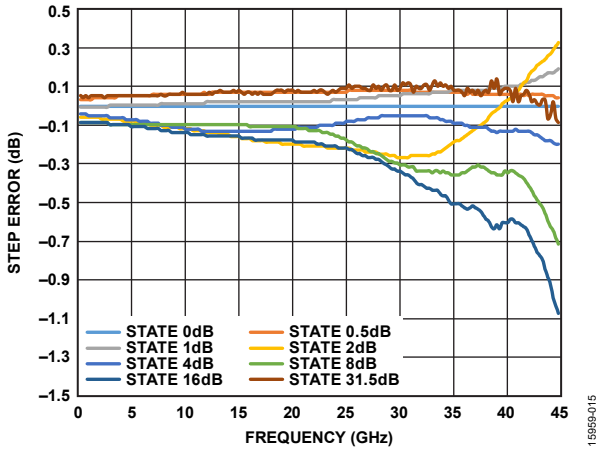


Figure 15. Step Error vs. Frequency (Major States Only) with Impedance Match

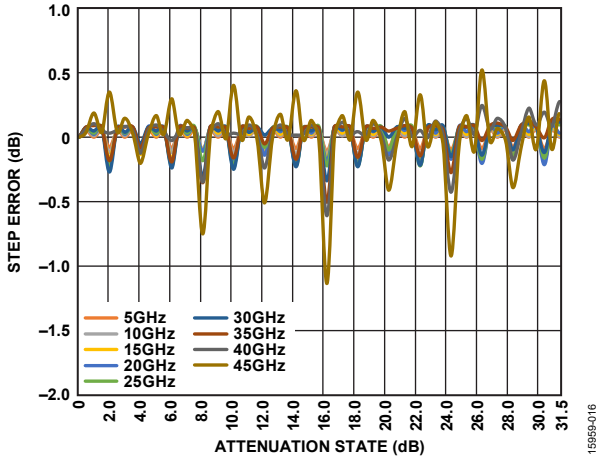


Figure 16. Step Error vs. Attenuation State over Frequency with Impedance Match

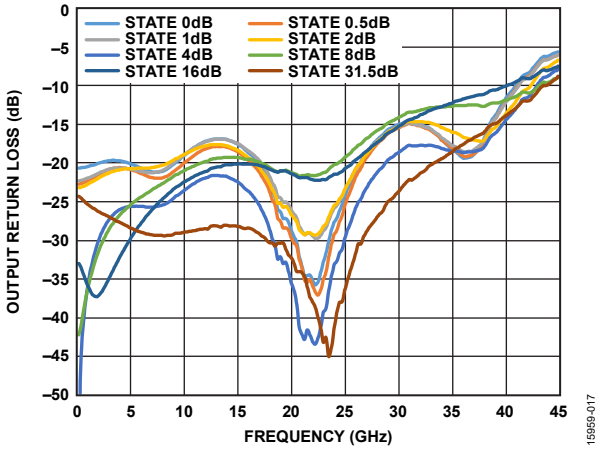


Figure 17. Output Return Loss vs. Frequency (Major States Only) Without Impedance Match

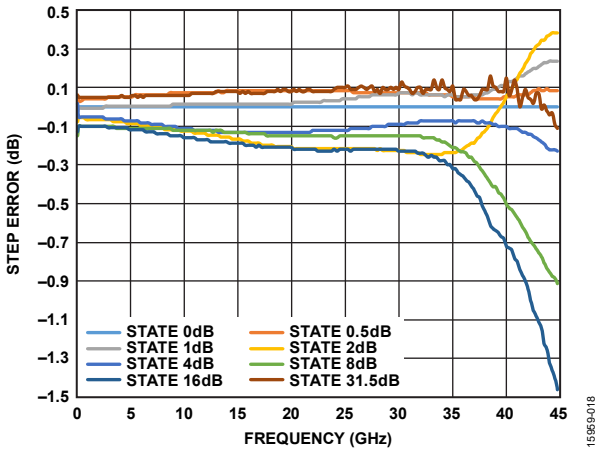


Figure 18. Step Error vs. Frequency (Major States Only) Without Impedance Match

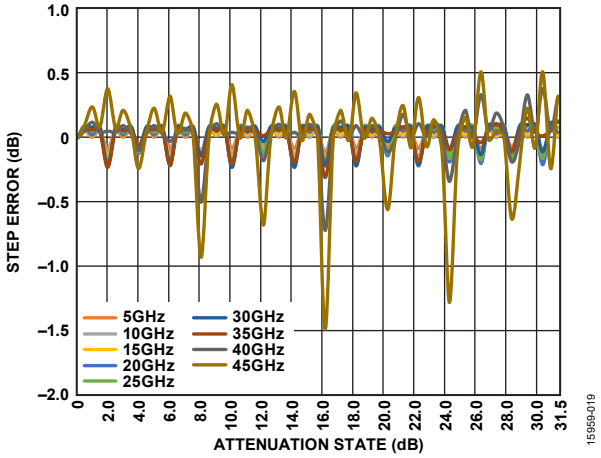


Figure 19. Step Error vs. Attenuation State over Frequency Without Impedance Match

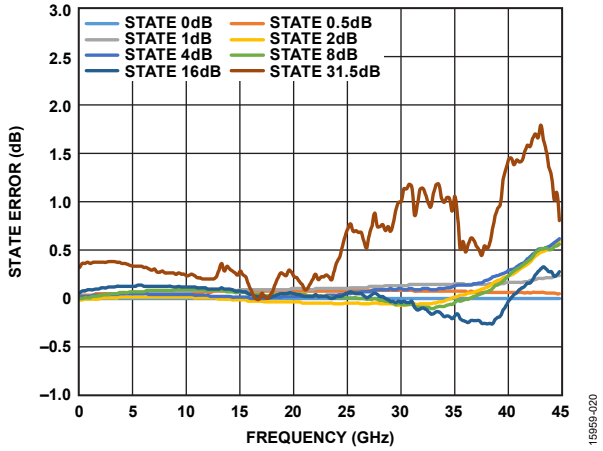


Figure 20. State Error vs. Frequency (Major States Only) with Impedance Match

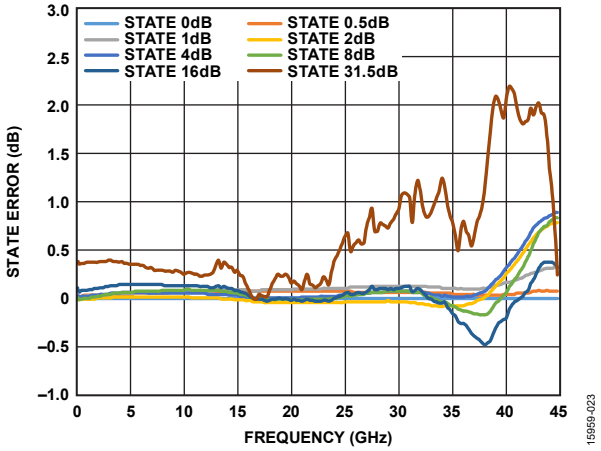


Figure 23. State Error vs. Frequency (Major States Only) Without Impedance Match

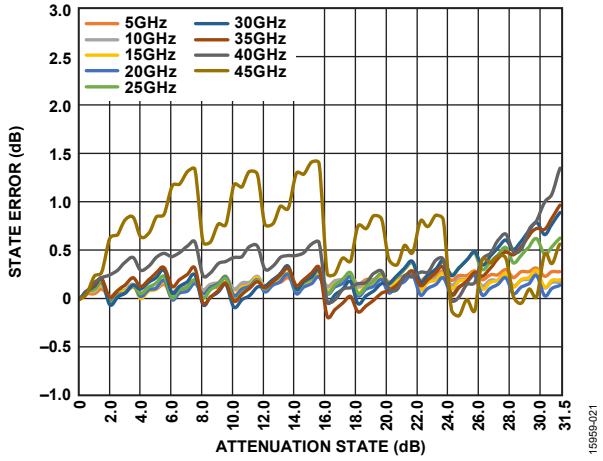


Figure 21. State Error vs. Attenuation State over Frequency with Impedance Match

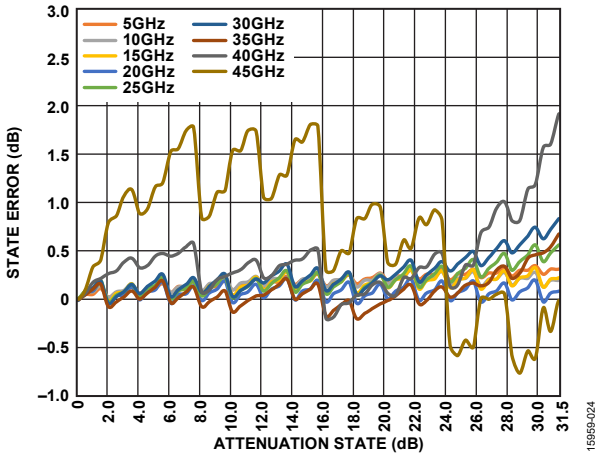


Figure 24. State Error vs. Attenuation State over Frequency Without Impedance Match

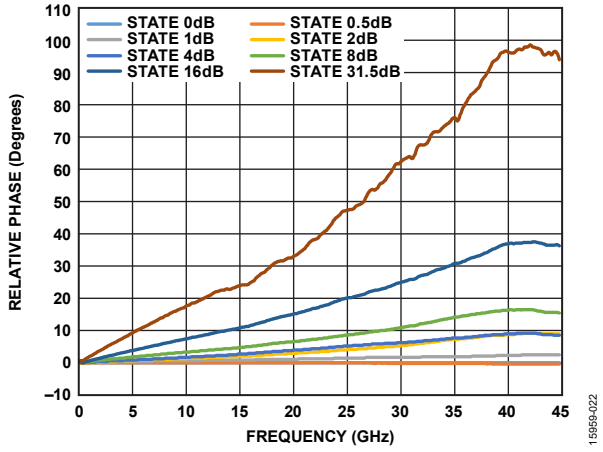


Figure 22. Relative Phase vs. Frequency (Major States Only) with Impedance Match

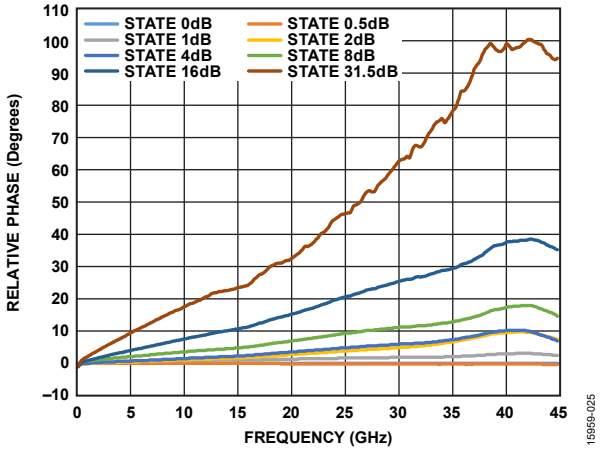


Figure 25. Relative Phase vs. Frequency (Major States Only) Without Impedance Match

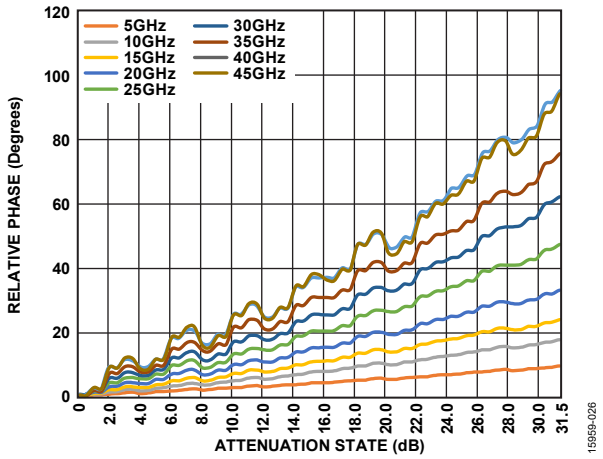


*Figure 26. Relative Phase vs. Attenuation State over Frequency with Impedance Match*

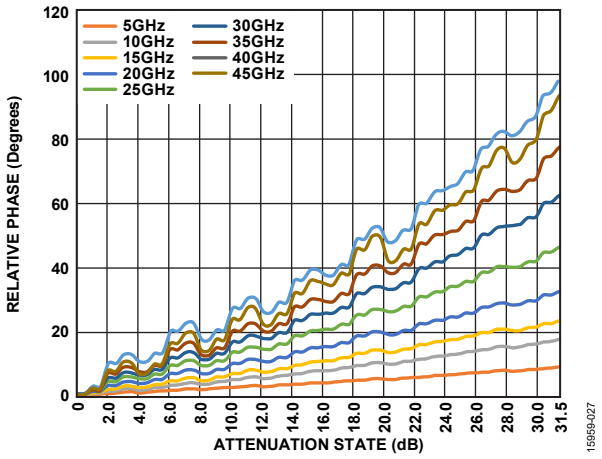


*Figure 27. Relative Phase vs. Attenuation State over Frequency Without Impedance Match*

## INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

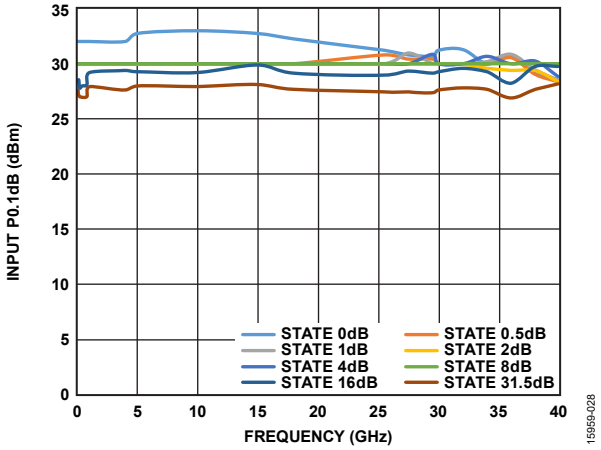


Figure 28. Input P0.1dB vs. Frequency (Major States Only)

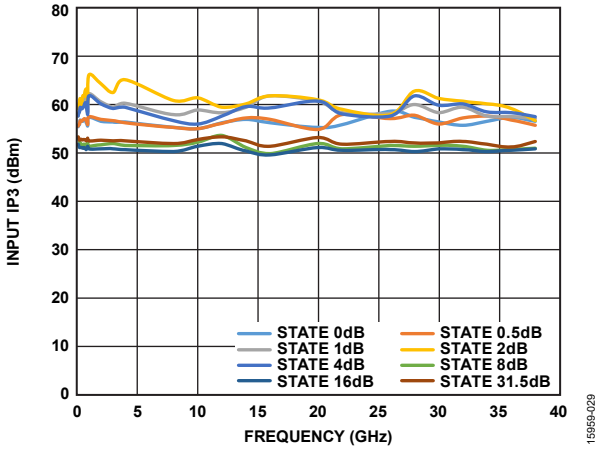


Figure 29. Input IP3 vs. Frequency (Major States Only)

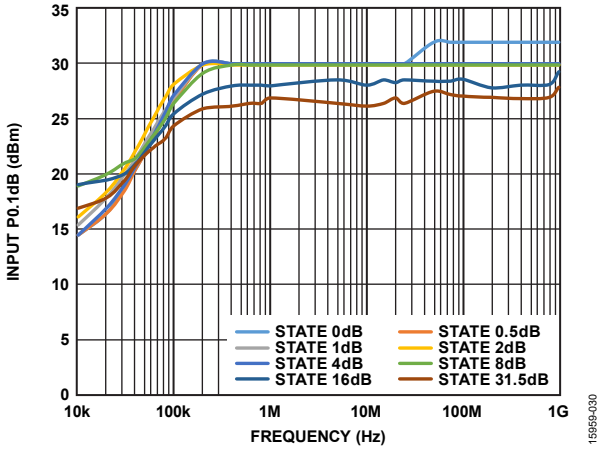


Figure 30. Input P0.1dB vs. Frequency (Major States Only), Low Frequency Detail

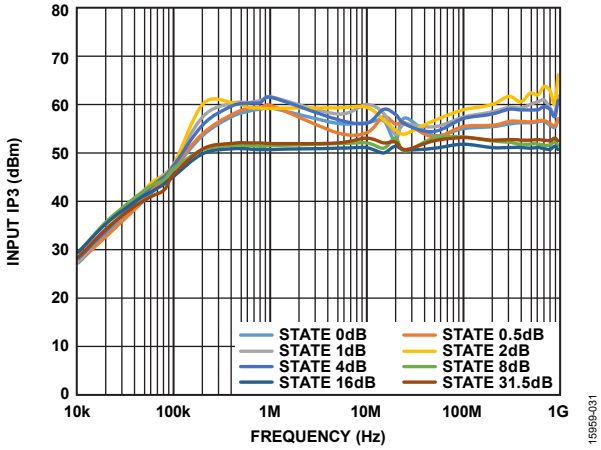


Figure 31. Input IP3 vs. Frequency (Major States Only), Low Frequency Detail

# THEORY OF OPERATION

The ADRF5720 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 32).

Note that when referring to a single function of a multifunction pin in this section, only the portion of the pin name that is relevant is mentioned. For full pin names of the multifunction pins, refer to the Pin Configuration and Function Descriptions section.

## POWER SEQUENCE

Bypassing capacitors are recommended on the positive supply voltage line (VDD) and negative supply line (VSS) to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the VDD and VSS voltages. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the VDD voltage supply may inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing in to the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the VDD voltage is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

### *Power-Up State*

The ADRF5720 has internal power-on reset circuity. This circuity sets the attenuator to the maximum attenuation state (31.5 dB) when the VDD and VSS voltages are applied and LE is set to low.

## RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. No dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required. For wideband applications, use impedance matching to improve insertion loss, return loss, and attenuation accuracy performance at high frequencies. See the Impedance Matching section.

The ADRF5720 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

**Table 6. Truth Table**

| Digital Control Input[1] | | | | | | |
|---|---|---|---|---|---|---|
| **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Attenuation State (dB)** |
| Low | Low | Low | Low | Low | Low | 0 (reference) |
| Low | Low | Low | Low | Low | High | 0.5 |
| Low | Low | Low | Low | High | Low | 1.0 |
| Low | Low | Low | High | Low | Low | 2.0 |
| Low | Low | High | Low | Low | Low | 4.0 |
| Low | High | Low | Low | Low | Low | 8.0 |
| High | Low | Low | Low | Low | Low | 16.0 |
| High | High | High | High | High | High | 31.5 |

[1] Any combination of the control voltage input states shown in Table 6 provides an attenuation equal to the sum of the bits selected.

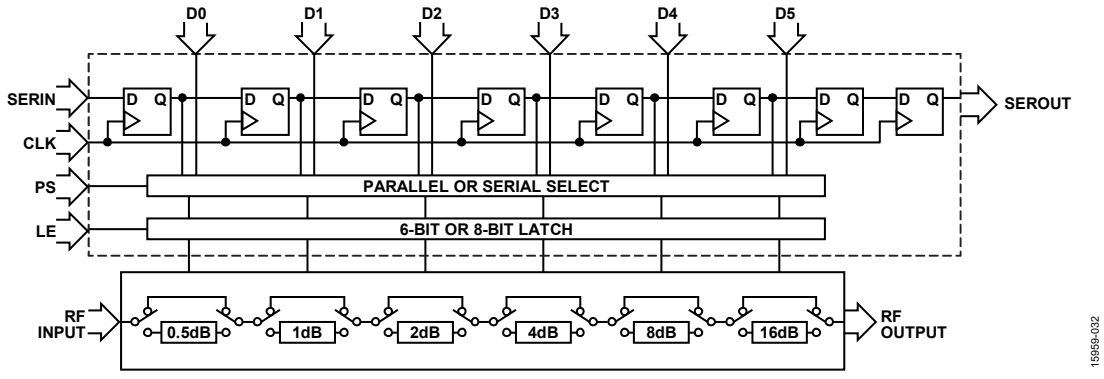


*Figure 32. Simplified Circuit Diagram*

## SERIAL OR PARALLEL MODE SELECTION

The ADRF5720 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 7).

**Table 7. Mode Selection**

| PS | Control Mode |
|---|---|
| Low | Parallel |
| High | Serial |

## SERIAL MODE INTERFACE

The ADRF5720 supports a 3-wire SPI: serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when PS is set to high.

The ADRF5720 attenuation states can be controlled using 6-bit or 8-bit SERIN data. If an 8-bit word is used to control the state of the attenuator, the first two bits, D7 and D6, are don't care bits. It does not matter if these two bits are held low or high, or if they are omitted altogether. Only Bits[D0:D5] set the state of the attenuator.

In serial mode, the SERIN data is clocked most significant bit (MSB) first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 34 in conjunction with Table 2 and Table 6.

### *Using SEROUT*

The ADRF5720 also features a serial data output, SEROUT. SEROUT outputs the serial input data at the 8th clock cycle, and can control a cascaded attenuator using a single SPI bus. Figure 35 shows the serial out timing diagram.

When using the attenuator in a daisy-chain operation, 8-bit SERIN data must be used due to the 8 clock cycle delay between SERIN and SEROUT.

It is optional to use a 1 kΩ resistor between SEROUT on the first attenuator and SERIN of the next attenuator to filter the signal (see Figure 33).

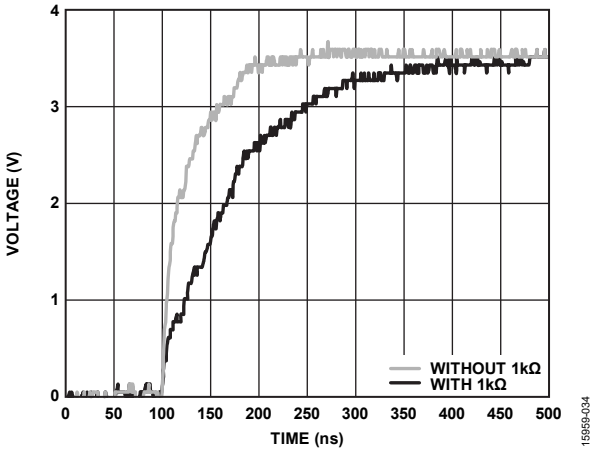


*Figure 33. Using a Resistor on SEROUT*

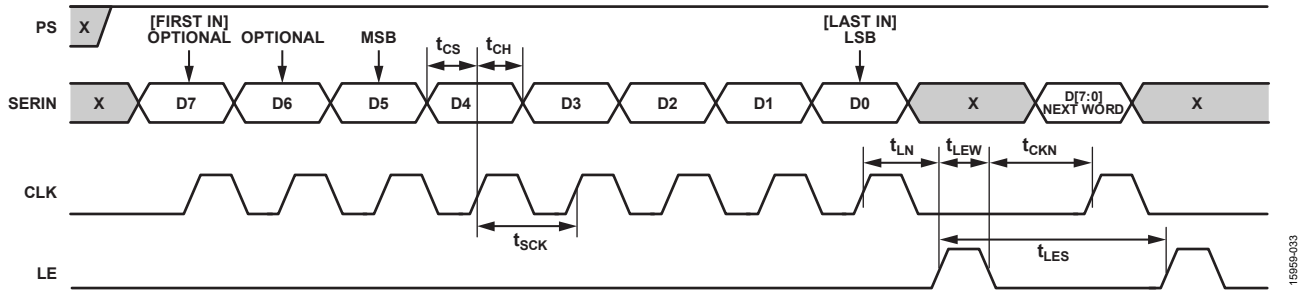


*Figure 34. Serial Control Timing Diagram*

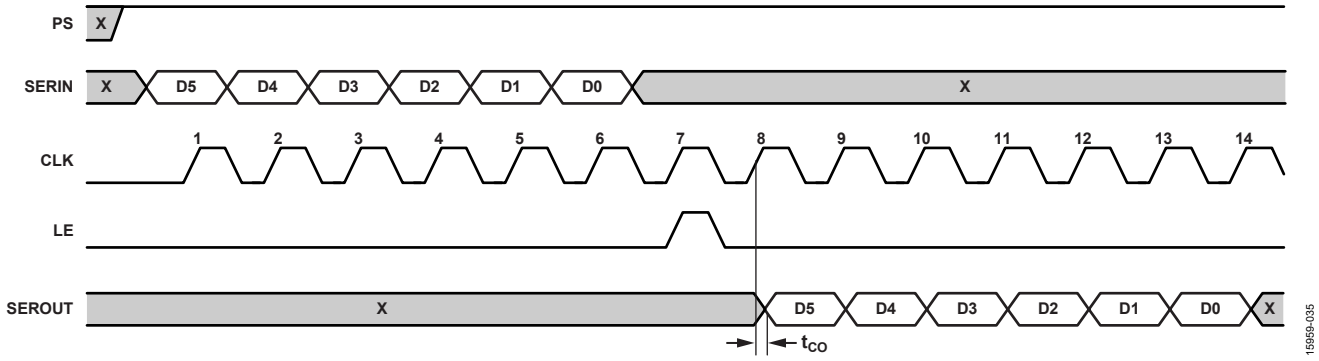


*Figure 35. Serial Output Timing Diagram*

## PARALLEL MODE INTERFACE

The ADRF5720 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 6. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

### *Direct Parallel Mode*

To enable direct parallel mode, the LE pin must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

### *Latched Parallel Mode*

To enable latched parallel mode, the LE pin must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 36 in conjunction with Table 2).

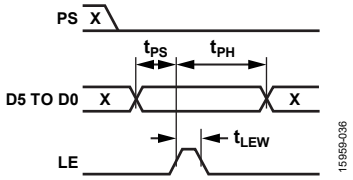


*Figure 36. Latched Parallel Mode Timing Diagram*

# APPLICATIONS INFORMATION

## EVALUATION BOARD

The ADRF5720-EVALZ is a 4-layer evaluation board. The top and bottom copper layer are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. The stackup for this evaluation board is shown in Figure 37.

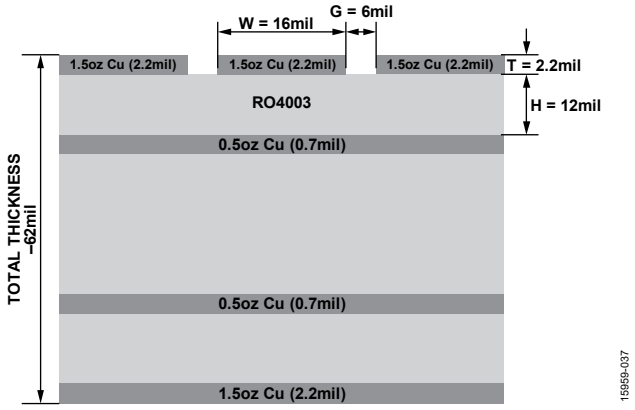


*Figure 37. Evaluation Board Stackup*

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 12 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The ADRF5720-EVALZ does not have high frequency impedance matching implemented on the RF transmission lines. For more details on the impedance matched circuit, refer to the Impedance Matching portion of the Probe Matrix Board section.

Thru calibration can be used to calibrate out the board loss effects from the ADRF5720-EVALZ evaluation board measurements to determine the device performance at the pins of the IC. Figure 38 shows the typical board loss for the ADRF5720-EVALZ evaluation board at room temperature, the embedded insertion loss, and the de-embedded insertion loss for the ADRF5720.

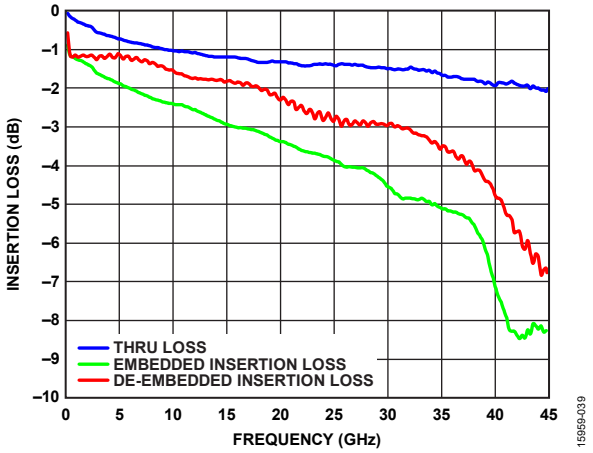


*Figure 38. Insertion Loss vs. Frequency*

Figure 39 shows the actual ADRF5720 evaluation board with component placement.

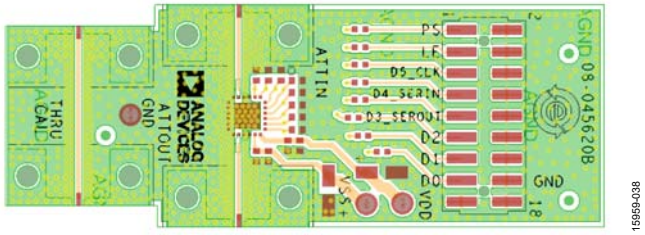


*Figure 39. Evaluation Board, Top View*

Two power supply ports are connected to the VDD and VSS test points, TP1 and TP2, and the ground reference is connected to the GND test point, TP4. On the supply traces, VDD and VSS, a 100 pF bypass capacitor is used to filter high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

All the digital control pins are connected through digital signal traces to the 2 × 9-pin header, P1. There are provisions for a resistor capacitor (RC) filter that helps eliminate dc-coupled noise. The ADRF5720 was evaluated without an external RC filter, the series resistors are 0 Ω, and the shunt capacitors are unpopulated on the evaluation board.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers, J1 and J2, respectively. These high frequency RF launchers are connected by contact and are not soldered onto the board.

A thru calibration line connects the unpopulated J3 and J4 launchers. This transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

The schematic of the ADRF5720-EVALZ evaluation board is shown in Figure 40.

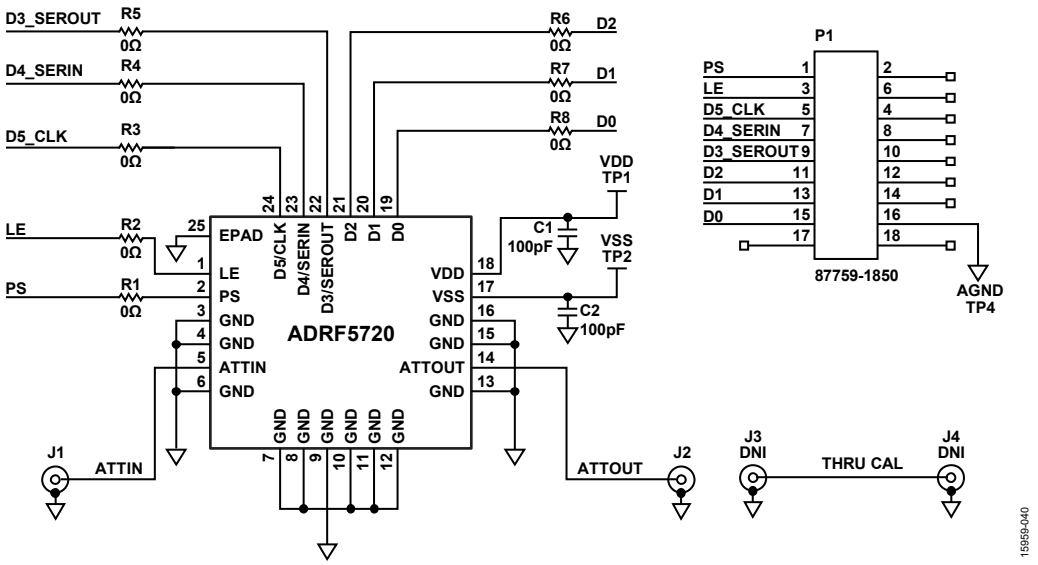


*Figure 40. Evaluation Board Schematic*

**Table 8. Evaluation Board Components**

| Component | Default Value | Description |
|---|---|---|
| C1, C2 | 100 pF | Capacitors, C0402 package |
| J1 to J4 | Not applicable | 2.4 mm end launch connectors (Southwest Microwave: 1492-04A-5) |
| P1 | Not applicable | 2 × 9-pin header |
| R1 to R8 | 0 Ω | Resistors, 0402 package |
| TP1, TP2, TP4 | Not applicable | Through hole mount test points |
| U1 | ADRF5720 | ADRF5720 digital attenuator, Analog Devices, Inc. |

## PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. Similar to the evaluation board, the probe matrix board also uses a 12 mil Rogers RO4003 dielectric. The top and bottom copper layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines are designed using a CPWG model with a width of 16 mil and ground spacing of 6 mil to have a characteristic impedance of 50 Ω.

Figure 41 and Figure 42 show the cross sectional view and the top view of the board, respectively. Measurements are made using GSG probes at close proximity to the RF pins (ATTIN and ATTOUT). Unlike the evaluation board, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the device performance.

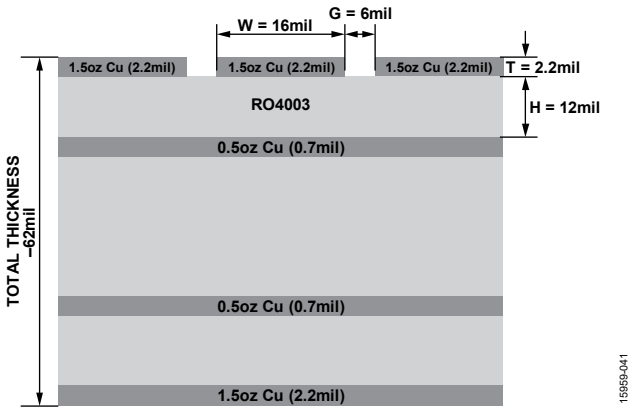


*Figure 41. Probe Matrix Board Stackup, Cross Sectional View*

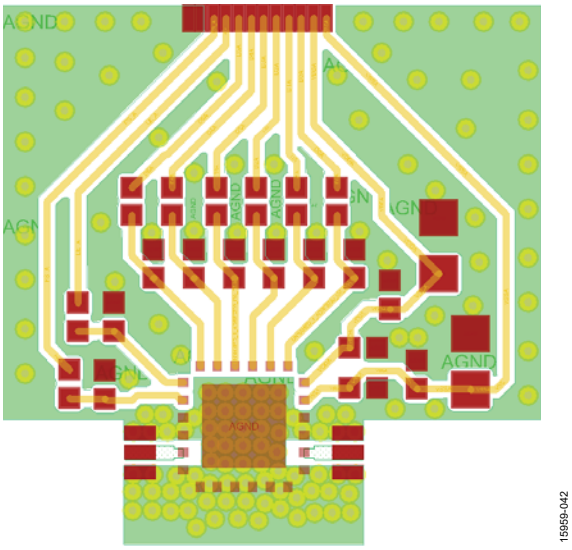


*Figure 42. Probe Matrix Board Top View*

The probe matrix board includes a thru reflect line (TRL) calibration kit, allowing board loss de-embedding. The actual board duplicates the same layout in matrix form to assemble multiple devices at one time. All S-parameters were measured on this board.

### *Impedance Matching*

Impedance matching at the RF pins (ATTIN and ATTOUT) can improve insertion loss, return loss, and attenuation accuracy at high frequencies. Figure 43 and Figure 44 show the difference in the transmission lines at the ATTIN and ATTOUT pins.

The dimensions of the 50 Ω lines are 16 mil trace width and 6 mil gap. To implement this impedance matched circuit, the pad length is extended by 5 mil (from 17 mil to 22 mil). The calibration reference kit does not include the 5 mil matching line and, therefore, the measured insertion loss includes the losses of the matching circuit.

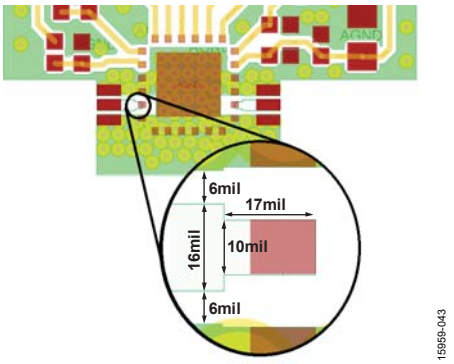


*Figure 43. Without Impedance Match*

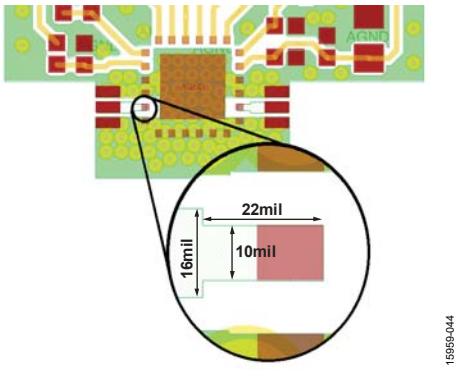


*Figure 44. With Impedance Match*

# OUTLINE DIMENSIONS

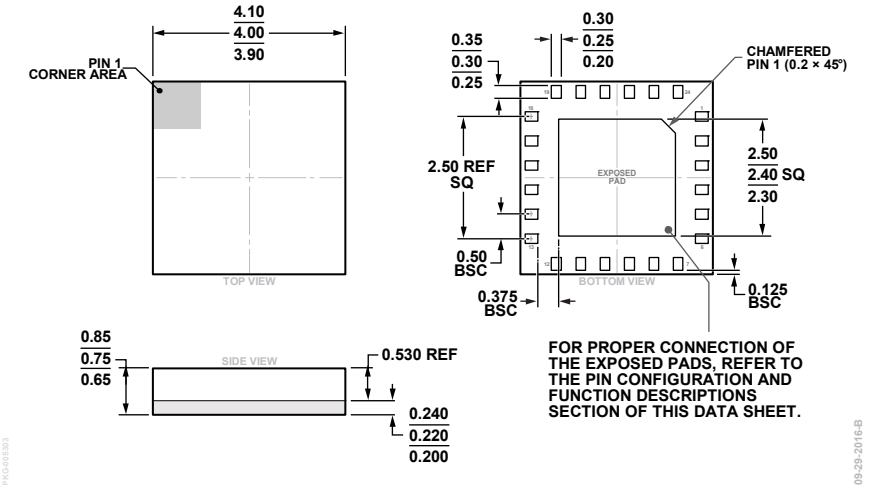


*Figure 45. 24-Terminal Land Grid Array [LGA]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CC-24-5)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADRF5720BCCZN | −40°C to +105°C | 24-Terminal Land Grid Array [LGA] | CC-24-5 |
| ADRF5720BCCZN-R7 | −40°C to +105°C | 24-Terminal Land Grid Array [LGA] | CC-24-5 |
| ADRF5720-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.