# ASL4501SHN

**Four-phase boost converter**

**Rev. 2 — 10 January 2018**                    **Product data sheet**

## 1. Introduction

The ASL4501SHN is a highly integrated and flexible four-phase DC-to-DC boost converter IC. It has a serial peripheral interface (SPI) allowing control and diagnostic communication with an external microcontroller.

It is designed primarily for use in automotive LED lighting applications and provides an optimized supply voltage for ASLx41xSHN multichannel LED buck driver.

## 2. General description

The ASL4501SHN has a fixed frequency peak current mode control with parabolic/non-linear slope compensation. It can operate with input voltages from 5.5 V to 40 V. It can be configured via SPI for output voltages of up to 80 V, to power the LED buck driver IC.

The ASL4501SHN is a four-phase converter which can have two independent outputs. The driver has the flexibility to be configured, via the SPI, as a single output converter, or with multiple combinations of number of outputs and phases.

The ASL4501SHN boost converter can drive up to four external low-side N channel metal-oxide-semiconductor field-effect transistors (MOSFETs) from an internally regulated adjustable supply. It can be used to drive either logic or standard level MOSFETs.

The integrated SPI also allows for programming the supply under/overvoltage range, output voltage range and DC-to-DC switching frequency. It enables the optimization of external components and flexibility for electromagnetic compatibility (EMC) design. This interface can also be used to provide diagnostic information such as the driver temperature.

Additional features include protection against load dump transient voltages of up to 60 V and thermal shutdown when the junction temperature of the ASL4501SHN exceeds +175 °C.

The device is housed in a very small HVQFN32 pin package and is designed to meet the stringent requirements of automotive applications. It is fully AEC-Q100 grade 1 qualified. It operates over the −40 °C to +125 °C ambient automotive temperature range.

## 3. Features and benefits

- The ASL4501SHN is an automotive grade product that is AEC-Q100 grade 1 qualified
- Operating ambient temperature range of −40 °C to +125 °C
- Wide operating input voltage range from 5.5 V to 40 V
- Output voltage programmable via SPI
- Multi-phase operation for higher power
- Up to four phases per output
- Up to two flexible output voltages with 3 % accuracy programmable via SPI
- Both output voltages can be controlled independently
- Fixed frequency operation via built-in oscillator
- Slope compensation tracks the frequency and output voltage
- Programmable control loop compensation
- Fast high efficiency field-effect transistor (FET) switching
- Programmable internal gate driver voltage regulator
- Gate switching is halted when overvoltage on output is detected
- Supports both logic level and standard level FETs
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Output voltage monitoring
- Supply voltage measurement
- Control signal to enable the device
- Read back programmed voltage and frequency range via SPI
- Junction temperature monitoring via SPI
- Small package outline HVQFN32
- Low quiescent current < 5 µA at 25 °C when EN = 0
- Accurate power dissipation in phases assigned to one output

## 4. Applications

- Automotive LED lighting
  - Low beam
  - High beam
  - Daytime running lights
  - Turn indicator
  - Position or park light
  - Front fog light
  - Cornering light
  - Advanced front lighting

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

Rev. 2 — 10 January 2018

2 of 43

## 5. Ordering information

**Table 1.    Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | **Name** | **Description** | **Version** |
| ASL4501SHN | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-12 |

## 6.  Block diagram



**Fig 1.    Block diagram**
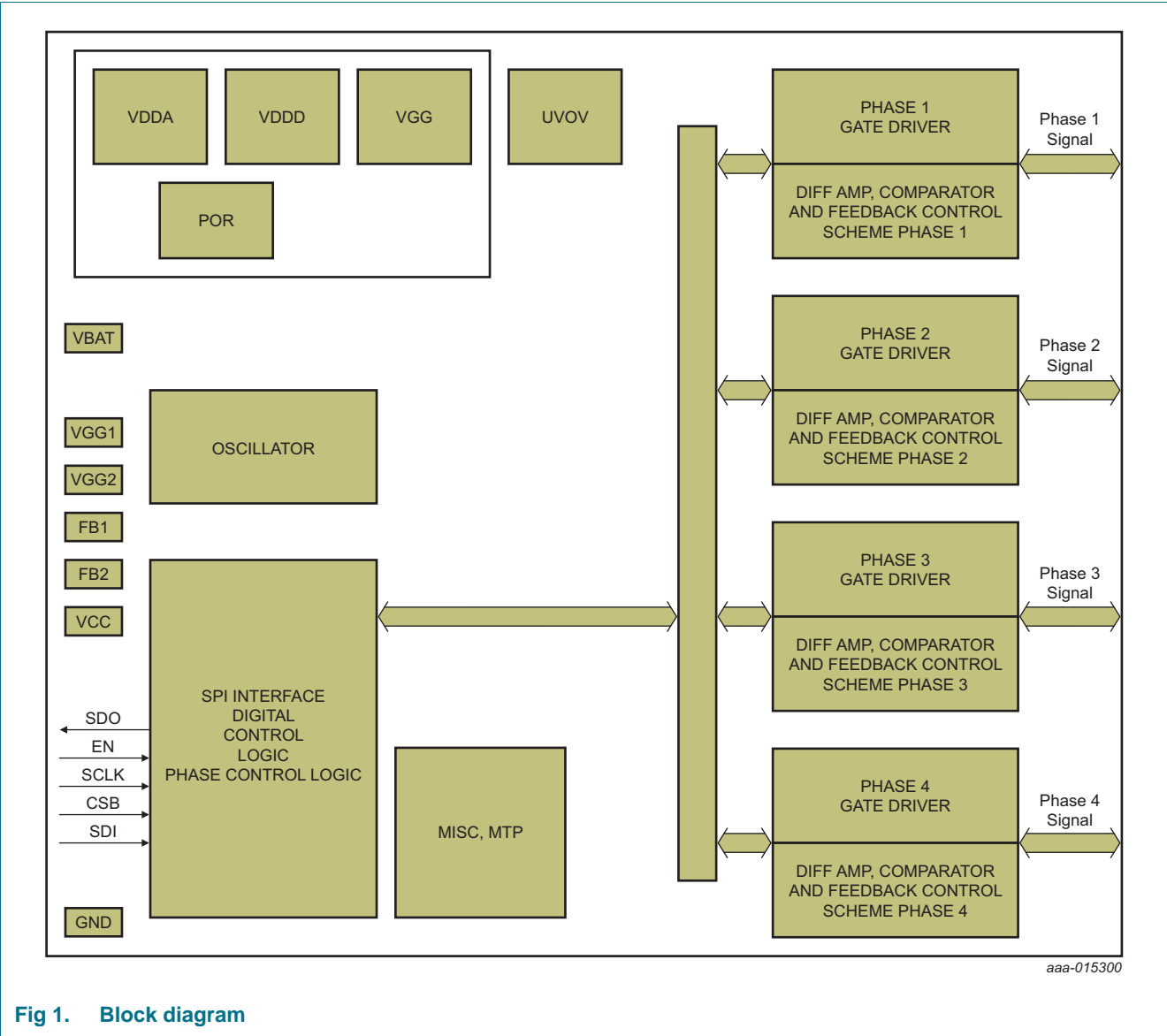
# 7. Pinning information

## 7.1 Pinning



**Fig 2.    Pin configuration**
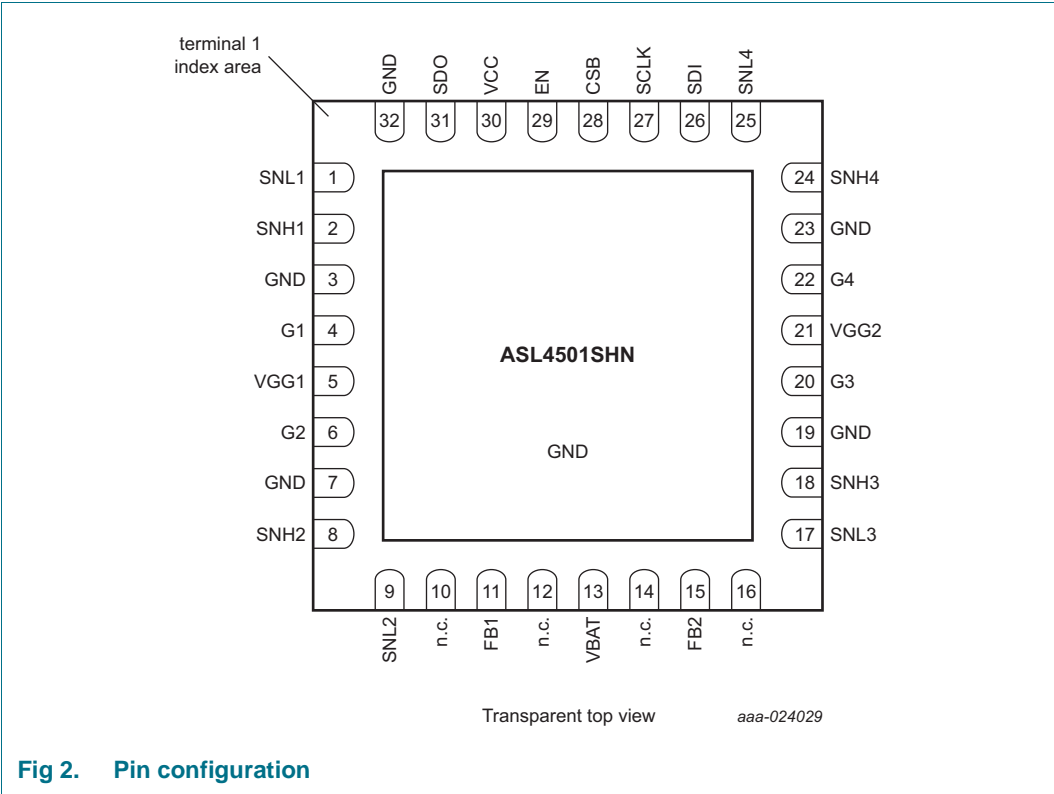
## 7.2 Pin description

**Table 2.    Pin description[1]**

| Symbol | Pin | Description |
|---|---|---|
| SNL1 | 1 | phase 1 sense low |
| SNH1 | 2 | phase 1 sense high |
| GND | 3 | ground |
| G1 | 4 | phase 1 gate driver |
| VGG1 | 5 | gate driver supply 1[2] |
| G2 | 6 | phase 2 gate driver |
| GND | 7 | ground |
| SNH2 | 8 | phase 2 sense high |
| SNL2 | 9 | phase 2 sense low |
| n.c. | 10 | not connected |
| FB1 | 11 | feedback; to be connected to Vout1[3] |
| n.c. | 12 | not connected |
| VBAT | 13 | battery supply |
| n.c. | 14 | not connected |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet** **Rev. 2 — 10 January 2018** 4 of 43

**Table 2.** **Pin description**[1] …*continued*

| Symbol | Pin | Description |
|--------|-----|-------------|
| FB2 | 15 | feedback; to be connected to Vout2[3] |
| n.c. | 16 | not connected |
| SNL3 | 17 | phase 3 sense low |
| SNH3 | 18 | phase 3 sense high |
| GND | 19 | ground |
| G3 | 20 | phase 3 gate driver |
| VGG2 | 21 | gate driver supply 2[2] |
| G4 | 22 | phase 4 gate driver |
| GND | 23 | ground |
| SNH4 | 24 | phase 4 sense high |
| SNL4 | 25 | ph3ase 4 sense low |
| SDI | 26 | SPI data input |
| SCLK | 27 | SPI clock |
| CSB | 28 | SPI chip select |
| EN | 29 | enable signal |
| VCC | 30 | external 5 V supply |
| SDO | 31 | SPI data output |
| GND | 32 | chip ground |

[1] For enhanced thermal and electrical performance, the exposed center pad of the package should be soldered to board ground (and not to any other voltage level).

[2] VGG1 and VGG2 are connected internally.

[3] Refer to Figure 4 and Figure 14 for the recommended connections for pin FB1 and pin FB2.

ASL4501SHN

**Product data sheet** **Rev. 2 — 10 January 2018** **5 of 43**

## 8. Functional description



**Fig 3.    State diagram**

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

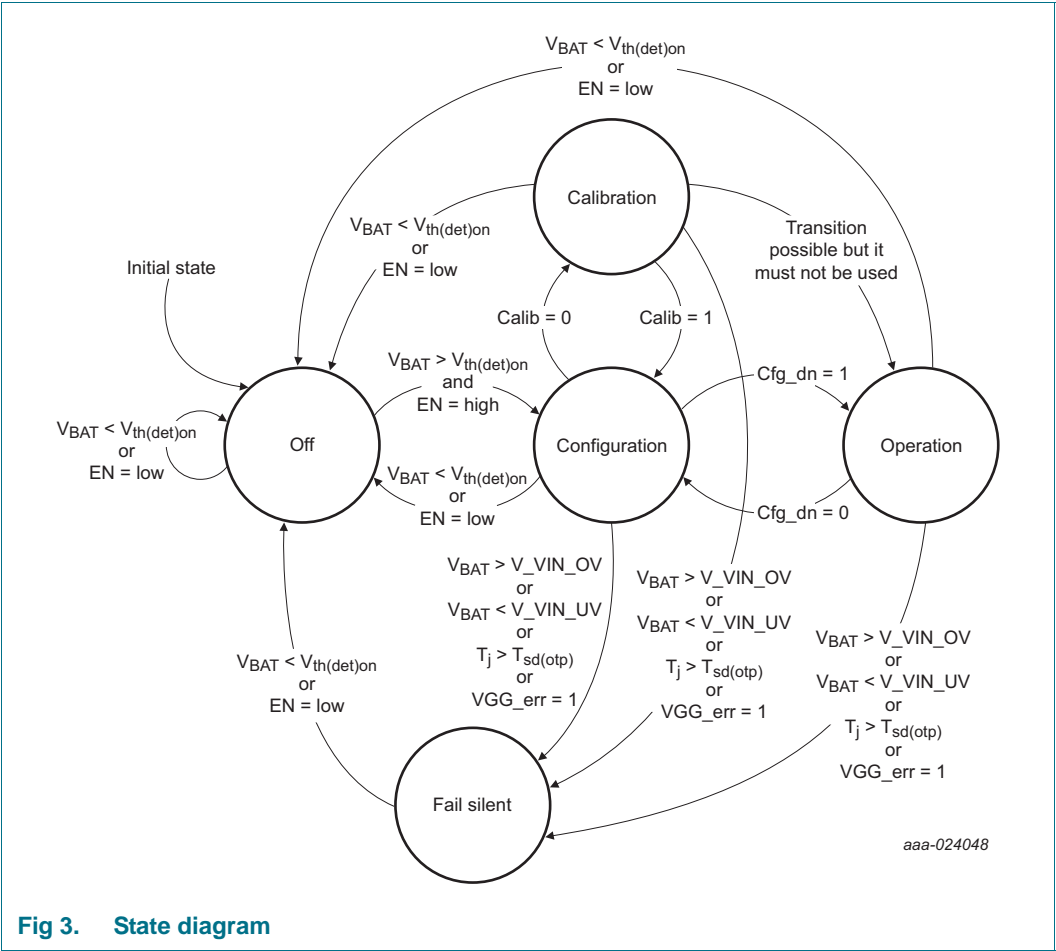**Product data sheet**                 **Rev. 2 — 10 January 2018**                 **6 of 43**

### 8.1 Operating modes

**Table 3.    Operating modes**

| Mode | Control registers | Configuration registers | Diagnostic registers | VGG | Vout1 Vout2 | Remarks |
|------|-------------------|-------------------------|----------------------|-----|-------------|---------|
| Off | n.a. | n.a. | n.a. | off | off | device is off, no communication possible |
| Configuration | read/write | read/write | read | off | off | VGG is off if no outputs were previously enabled |
|  |  |  | read | according to register | off | VGG is on as soon as one of the outputs has been enabled |
| Operation | read/write | read | read | locked | according to register | configuration registers are locked |
| Fail silent | read/write | read | read[1] | off | off | communication possible, but all outputs off; restart via EN possible |
| Calibration | read/write | read/write | read | must be turned on | must be turned off | for successful calibration, the device has to be correctly configured, VGG has to be on and the outputs off; it is achieved by putting cfg_dn HIGH and LOW after the configuration of the device |

[1]    Setting the bit cfg_dn to logic 0 also grants write access to the configuration registers.

#### 8.1.1   Off mode

The ASL4501SHN switches to off mode, if the input voltage drops below the power-on detection threshold voltage ($V_{th(det)pon}$) or the EN pin is LOW.

In off mode, the SPI and all outputs are turned off.

#### 8.1.2   Configuration mode

The ASL4501SHN switches immediately from off mode to configuration mode, when the input voltage rises above the power-on detection threshold voltage ($V_{th(det)pon}$) and pin EN is HIGH.

The configuration registers can be set when the ASL4501SHN is in the configuration mode.

#### 8.1.3   Operation mode

The ASL4501SHN switches from configuration mode to operation mode, as soon as the configuration done bit is set. Once the bit is set, the configuration registers are locked and cannot be changed.

In operation mode, the output is available as configured via the SPI. Setting bits Vout1en or Vout2en, initiates the gate driver. Once the gate driver is in regulation, signaled by bit VGG_ok, the respective programmed target voltages are turned on. When the converters are on, the battery monitoring functionality is available.

### 8.1.4 Fail silent mode

The ASL4501SHN switches from operation mode to fail silent mode, when the junction temperature exceeds the over temperature shutdown threshold or a gate driver error is detected. It also switches modes when the input voltage is below the undervoltage detection threshold or above the overvoltage detection threshold.

In fail silent mode, all outputs are turned off and only the SPI remains operational.

## 8.2 Boost converter configuration

The ASL4501SHN is an automatic boost converter IC delivering constant DC-to-DC voltage to a load. It has a fixed frequency current mode control for an enhanced stable operation.

The ASL4501SHN offers four phases. Each phase consists of a coil, a resistor, a MOSFET and a diode as shown in Figure 4.
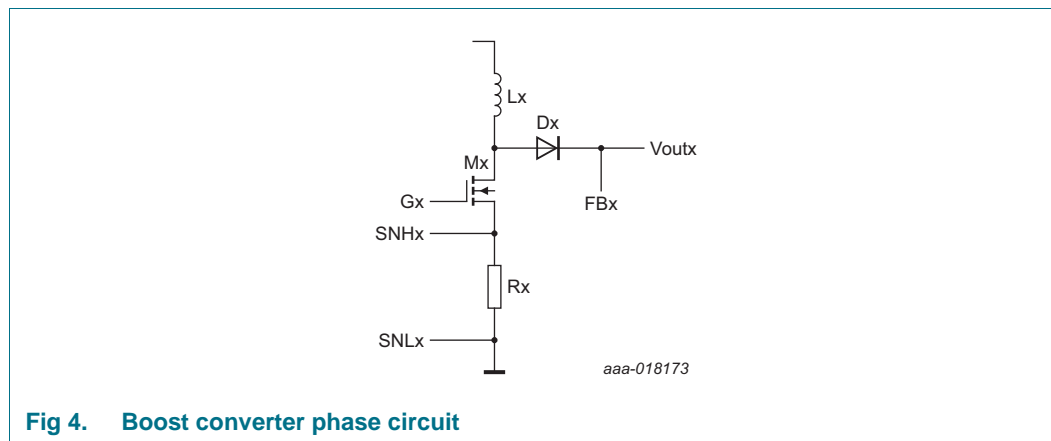


*aaa-018173*

**Fig 4.     Boost converter phase circuit**

To allow flexible use of the ASL4501SHN, the configuration is based on virtual phases. The virtual phases are then mapped to a real physical phase according to the physical connections and conditions of the circuitry around the ASL4501SHN as shown in Figure 5.

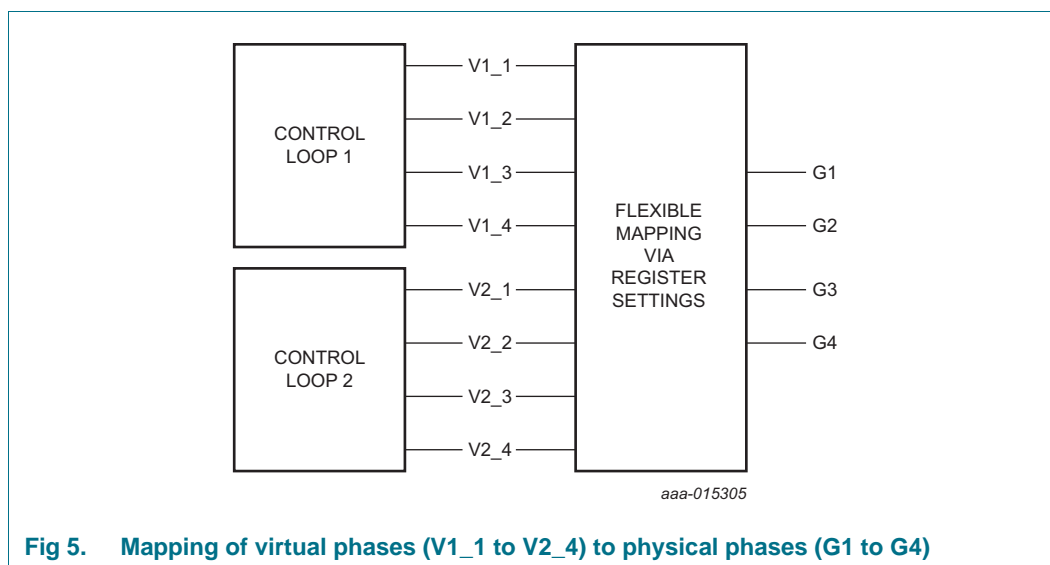ASL4501SHN

**Product data sheet**

Rev. 2 — 10 January 2018

**8 of 43**

*aaa-015305*

**Fig 5.    Mapping of virtual phases (V1_1 to V2_4) to physical phases (G1 to G4)**

### 8.2.1  Virtual phase configuration

The ASL4501SHN can generate up to four internal phases at up to two virtual outputs. With the internal phase control enable registers, it can be selected, how many virtual phases are generated for the individual virtual outputs.

**Table 4.    Internal phase control enable for phase logic 1 (address 0Bh)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | - | reserved | 0000 | reserved for future use: keep clear |
| 3 | EN_P4_1 | phase 4 enabled | 0 | phase 4 is off |
| | | | 1 | phase 4 is enabled |
| 2 | EN_P3_1 | phase 3 enabled | 0 | phase 3 is off |
| | | | 1 | phase 3 is enabled |
| 1 | EN_P2_1 | phase 2 enabled | 0 | phase 2 is off |
| | | | 1 | phase 2 is enabled |
| 0 | EN_P1_1 | phase 1 enabled | 0 | phase 1 is off |
| | | | 1 | phase 1 is enabled |

**Table 5.    Internal phase control enable for phase logic 2 (address 0Ch)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | - | reserved | 0000 | reserved for future use: keep clear |
| 3 | EN_P4_2 | phase 4 enabled | 0 | phase 4 is off |
| | | | 1 | phase 4 is enabled |
| 2 | EN_P3_2 | phase 3 enabled | 0 | phase 3 is off |
| | | | 1 | phase 3 is enabled |
| 1 | EN_P2_2 | phase 2 enabled | 0 | phase 2 is off |
| | | | 1 | phase 2 is enabled |
| 0 | EN_P1_2 | phase 1 enabled | 0 | phase 1 is off |
| | | | 1 | phase 1 is enabled |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**9 of 43**

### 8.2.2 Association of physical phases to the output voltages

The phase that the ASL4501SHN offers, must be associated to the output.

**Table 6.    Gate driver output (address 02h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | - | reserved | 0000 | reserved for future use: keep clear |
| 3 | O_G4 | association phase 4 | 0 | phase 4 is connected to Vout1 |
|  |  |  | 1 | phase 4 is connected to Vout2 |
| 2 | O_G3 | association phase 3 | 0 | phase 3 is connected to Vout1 |
|  |  |  | 1 | phase 3 is connected to Vout2 |
| 1 | O_G2 | association phase 2 | 0 | phase 2 is connected to Vout1 |
|  |  |  | 1 | phase 2 is connected to Vout2 |
| 0 | O_G1 | association phase 1 | 0 | phase 1 is connected to Vout1 |
|  |  |  | 1 | phase 1 is connected to Vout2 |

### 8.2.3 Association of connected phases to the internal phase generation

Each physical phase that the ASL4501SHN offers, must be associated to one of the virtual phases of the output. It is established with the gate driver phase and phase select configuration registers.

**Table 7.    Gate driver phase (address 0Fh)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | - | reserved | 0000 | reserved for future use: keep clear |
| 3 | O_GP4 | association phase 4 | 0 | phase 4 is connected to phase logic 1 |
|  |  |  | 1 | phase 4 is connected to phase logic 2 |
| 2 | O_GP3 | association phase 3 | 0 | phase 3 is connected to phase logic 1 |
|  |  |  | 1 | phase 3 is connected to phase logic 2 |
| 1 | O_GP2 | association phase 2 | 0 | phase 2 is connected to phase logic 1 |
|  |  |  | 1 | phase 2 is connected to phase logic 2 |
| 0 | O_GP1 | association phase 1 | 0 | phase 1 is connected to phase logic 1 |
|  |  |  | 1 | phase 1 is connected to phase logic 2 |

**Table 8.    Phase selection configuration (address 10h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 and 6 | Phsel4[1:0] | phase select gate driver 4 | 0h | routing from phase 1 |
|  |  |  | 1h | routing from phase 2 |
|  |  |  | 2h | routing from phase 3 |
|  |  |  | 3h | routing from phase 4 |
| 5 and 4 | Phsel3[1:0] | phase select gate driver 3 | 0h | routing from phase 1 |
|  |  |  | 1h | routing from phase 2 |
|  |  |  | 2h | routing from phase 3 |
|  |  |  | 3h | routing from phase 4 |

**Table 8.** **Phase selection configuration (address 10h)** *…continued*

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 3 and 2 | Phsel2[1:0] | phase select gate driver 2 | 0h | routing from phase 1 |
| | | | 1h | routing from phase 2 |
| | | | 2h | routing from phase 3 |
| | | | 3h | routing from phase 4 |
| 1 and 0 | Phsel1[1:0] | phase select gate driver 1 | 0h | routing from phase 1 |
| | | | 1h | routing from phase 2 |
| | | | 2h | routing from phase 3 |
| | | | 3h | routing from phase 4 |

ASL4501SHN

**Product data sheet**

**Rev. 2 — 10 January 2018**

11 of 43

### 8.2.4 Enabling of connected phases

The gate driver enable register is used to configure which of the phases is active.

**Table 9.    Gate driver enable (address 01h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | - | reserved | 0000 | reserved for future use: keep clear |
| 3 | EN_G4 | phase 4 enabled | 0 | phase 4 is off |
|  |  |  | 1 | phase 4 is enabled |
| 2 | EN_G3 | phase 3 enabled | 0 | phase 3 is off |
|  |  |  | 1 | phase 3 is enabled |
| 1 | EN_G2 | phase 2 enabled | 0 | phase 2 is off |
|  |  |  | 1 | phase 2 is enabled |
| 0 | EN_G1 | phase 1 enabled | 0 | phase 1 is off |
|  |  |  | 1 | phase 1 is enabled |

### 8.2.5 Boost converter frequencies configuration

The operation frequency of the boost converters can be set with via several SPI registers. To ensure a stable phase delay between the different phases, all timings are derived from the same oscillator. An integer number downscales the internal oscillator frequency for each regulation loop. This slower clock is then used to control the off time of a phase. It also controls the delay from one phase of the regulation loop to the next internal phase. The number of phases determinates finally when the phase is turned on again and defines so the operation frequency of the boost converter.
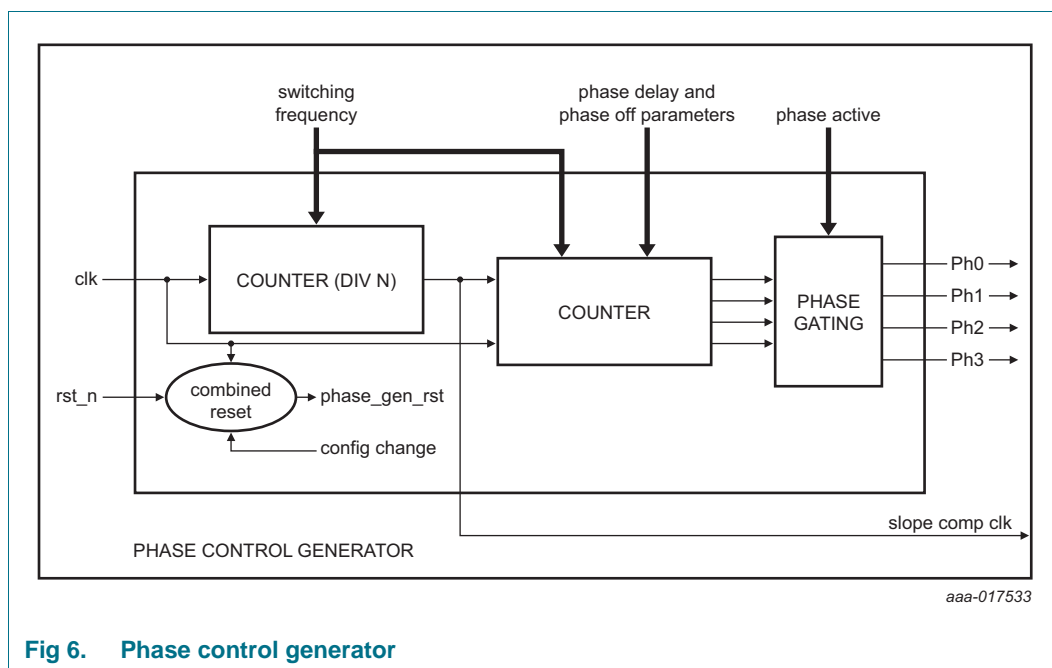


*aaa-017533*

**Fig 6.    Phase control generator**

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

Rev. 2 — 10 January 2018

12 of 43

**Table 10.    Clock divider for Vout1 (address 09h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | Clkdiv1[7:0] | clock divider for phase logic 1 | 00h | clock is not divided |
| | | | ... | clock is divided by Clkdiv1[7:0] + 1 |
| | | | FFh | clock is divided by 256 |

**Table 11.    Clock divider for Vout2 (address 0Ah)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | Clkdiv2[7:0] | clock divider for phase logic 2 | 00h | clock is not divided |
| | | | ... | clock is divided by Clkdiv2[7:0] + 1 |
| | | | FFh | clock is divided by 256 |

**Table 12.    Phase-off time and phase delay of output 1 (address 0Dh)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 3 | Phdel1[4:0] | delay to next phase of phase logic 1 | 0h | phase delay is 1 clock period of the divided clock |
| | | | ... | phase delay is Phdel1[4:0] + 1 clock period of the divided clock |
| | | | 1Fh | phase delay is 32 clock periods of the divided clock |
| 2 to 0 | Phoff1[2:0] | phase-off time of phase logic 1 | 0h | phase-off time is 1 clock period of the divided clock |
| | | | ... | phase-off time is Phoff1[2:0] clock period of the divided clock |
| | | | 7h | phase-off time is 7 clock periods of the divided clock |

**Table 13.    Phase-off time and phase delay of output 2 (address 0Eh)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 3 | Phdel2[4:0] | delay to next phase of phase logic 2 | 0h | phase delay is 1 clock period of the divided clock |
| | | | ... | phase delay is Phdel2[4:0] + 1 clock period of the divided clock |
| | | | 1Fh | phase delay is 32 clock periods of the divided clock |
| 2 to 0 | Phoff2[2:0] | phase-off time of phase logic 2 | 0h | phase-off time is 1 clock period of the divided clock |
| | | | ... | phase-off time is Phoff2[2:0] clock period of the divided clock |
| | | | 7h | phase-off time is 7 clock periods of the divided clock |

**Note:** To obtain the best performance of the internal slope compensation, keep the settings of the delay between the phases as close to 32 as possible.

### 8.2.6  Control loop parameter settings

The ASL4501SHN is able to operate with a wide range of external components and offers a wide range of operating frequencies. To achieve maximum performance for each set of operation conditions, set the control loop parameters in accordance with the external components and operating frequency.

**Table 14.    Loop filter proportional configuration (address 11h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | Prop2[3:0] | proportional factor output 2 | 0h | proportional factor output 2 is 0.05 |
| | | | ... | proportional factor output 2 is Prop2[3:0] $\times$ 0.05 + 0.05 |
| | | | Fh | proportional factor output 2 is 0.8 |
| 3 to 0 | Prop1[3:0] | proportional factor output 1 | 0h | proportional factor output 1 is 0.05 |
| | | | ... | proportional factor output 1 is Prop1[3:0] $\times$ 0.05 + 0.05 |
| | | | Fh | proportional factor output 1 is 0.8 |

**Table 15.    Loop filter integral configuration (address 12h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | Integ2[3:0] | integral factor output 2 | 0h | integral factor output 2 is 0.005 |
| | | | ... | integral factor output 2 is Integ2[3:0] $\times$ 0.005 + 0.005 |
| | | | Fh | integral factor output 2 is 0.08 |
| 3 to 0 | Integ1[3:0] | integral factor output 1 | 0h | integral factor output 1 is 0.005 |
| | | | ... | integral factor output 1 is Integ1[3:0] $\times$ 0.005 + 0.005 |
| | | | Fh | integral factor output 1 is 0.08 |

**Table 16.    Slope compensation configuration (address 13h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 4 | Slpcmp2[3:0] | slope compensation factor output 2 | 0h | slope compensation factor output 2 = 112 k$\Omega$ |
| | | | 1h | slope compensation factor output 2 = 84 k$\Omega$ |
| | | | 2h | slope compensation factor output 2 = 70 k$\Omega$ |
| | | | 4h | slope compensation factor output 2 = 56 k$\Omega$ |
| | | | 8h | slope compensation factor output 2 = 28 k$\Omega$ |
| 3 to 0 | Slpcmp1[3:0] | slope compensation factor output 1 | 0h | slope compensation factor output 1 = 112 k$\Omega$ |
| | | | 1h | slope compensation factor output 1 = 84 k$\Omega$ |
| | | | 2h | slope compensation factor output 1 = 70 k$\Omega$ |
| | | | 4h | slope compensation factor output 1 = 56 k$\Omega$ |
| | | | 8h | slope compensation factor output 1 = 28 k$\Omega$ |

**Table 17. Current sense slope resistor configuration (address 14h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 and 6 | Slpr4[1:0] | slope resistor configuration for gate driver 4 | 0h | 250 Ω |
| | | | 1h | 500 Ω |
| | | | 2h | 1000 Ω |
| | | | 3h | 1500 Ω |
| 5 and 4 | Slpr3[1:0] | slope resistor configuration for gate driver 3 | 0h | 250 Ω |
| | | | 1h | 500 Ω |
| | | | 2h | 1000 Ω |
| | | | 3h | 1500 Ω |
| 3 and 2 | Slpr2[1:0] | slope resistor configuration for gate driver 2 | 00h | 250 Ω |
| | | | 1h | 500 Ω |
| | | | 2h | 1000 Ω |
| | | | 3h | 1500 Ω |
| 1 and 0 | Slpr1[1:0] | slope resistor configuration for gate driver 1 | 0h | 250 Ω |
| | | | 1h | 500 Ω |
| | | | 2h | 1000 Ω |
| | | | 3h | 1500 Ω |

## 8.3 Output voltage programmability

The ASL4501SHN provides the possibility to program the output voltage and output overvoltage protection of the output via the SPI.

### 8.3.1 Output voltage target programmability

The target output voltage can be programmed via the output voltage registers. As the ASL4501SHN is a boost converter, the output voltage cannot be lower than the supply voltage minus the drop of the converter diode (Dx in Figure 4).

**Table 18. Output voltage 1 register (address 03h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | V_Vout_1[7:0] | target voltage output 1 | 00h | output 1 is turned off |
| | | | ... | target voltage output 1 = $0.3555 \times$ V_Vout_1[7:0] $\times (1 + (333 \times 10^{-6}) \times ($T_junction[7:0] $- 38))$ |
| | | | FFh | maximum target output voltage = 90 V |

**Table 19. Output voltage 2 register (address 04h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | V_Vout_2[7:0] | target voltage output 2 | 00h | output 2 is turned off |
| | | | ... | target voltage output 2 = $0.3555 \times$ V_Vout_2[7:0] $\times (1 + (333 \times 10^{-6}) \times ($T_junction[7:0] $- 38))$ |
| | | | FFh | maximum target output voltage = 90 V |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**15 of 43**

### 8.3.2 Output overvoltage protection programming

Due to fast changes in the supply or the output, it is possible that the output voltage is disturbed. To avoid high voltages that may result into damage of attached components, the ASL4501SHN offers a programmable overvoltage protection threshold. Once the output voltage is above this threshold, the gate pin of the output stops toggling. It results in a halt of the energy delivery to the output.

Once the output voltage recovers and is below the threshold again, the gate pin starts toggling again. The regulation loop regulates the output back to the target value.

For stable operation of the device, the limit voltage output register should be programmed around 5 V higher than the output voltage registers.

**Table 20.    Limit voltage output 1 register (address 05h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | Vmax_Vout_1[7:0] | limit output 1 | 00h | output 1 is turned off |
| | | | ... | output overvoltage protection output 1 = $0.3555 \times V\_Vout\_1[7:0] \times (1 + (333 \times 10^{-6}) \times (T\_junction[7:0] - 38))$ |
| | | | FFh | maximum output overvoltage protection output 1 = 90 V |

**Table 21.    Limit voltage output 2 register (address 06h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | Vmax_Vout_2[7:0] | limit output 2 | 00h | output 2 is turned off |
| | | | ... | output overvoltage protection output 2 = $0.3555 \times V\_Vout\_2[7:0] \times (1 + (333 \times 10^{-6}) \times (T\_junction[7:0] - 38))$ |
| | | | FFh | maximum output over voltage protection output 2 = 90 V |

## 8.4 Coil peak current limitation

The ASL4501SHN offers a function to limit peak current inside the coil and therefore to limit the input current for the system. Furthermore, this functionality can be used to avoid magnetic saturation of the coils and allow some soft start feature to be realized.

With the maximum phase current Voutx registers, the maximum peak current for the individual phases assigned to the output can be configured. Once the voltage drop between pins SNLx and SNHx reaches this level, the gate will be turned off until the next switching cycle. To avoid sub harmonic oscillations when the coil peak current limitation is becoming active, the slope compensation is still active. It reduces the coil peak current toward the end of the switching cycle to ensure stable operation of the system.

To avoid that this function interferes with the normal regulation, the limit should be placed well above the maximum expected currents.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**16 of 43**

**Table 22. Maximum phase current Vout1 register (address 07h)**

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 7 to 0 | I_max_per_phase_Vout1[7:0] | coil current limitation for phases assigned to Vout1 | 00h | no current allowed |
| | | | ... | maximum peak current = $(\text{I\_max\_per\_phase\_Vout1}[7:0] \times 1.8\text{ V} / 256 - 0.24\text{ V}) / R_{sense}$ |
| | | | 64h | maximum allowed setting = $(128 / 256 \times 1.8\text{ V} - 0.24\text{ V}) / R_{sense}$ |
| | | | ... | not allowed |
| | | | FFh | not allowed |

**Table 23. Maximum phase current Vout2 register (address 08h)**

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 7 to 0 | I_max_per_phase_Vout2[7:0] | coil current limitation for phases assigned to Vout2 | 00h | no current allowed |
| | | | ... | maximum peak current = $(\text{I\_max\_per\_phase\_Vout2}[7:0] \times 1.8\text{ V} / 256 - 0.24\text{ V}) / R_{sense}$ |
| | | | 64h | maximum allowed setting = $(128 / 256 \times 1.8\text{ V} - 0.24\text{ V}) / R_{sense}$ |
| | | | ... | not allowed |
| | | | FFh | not allowed |

## 8.5 Enabling output voltage

The ASL4501SHN provides two independent output voltages. In operation mode, the output voltages are turned on with the bits Vout1en and Vout2en.

As soon as one of the outputs is turned on, the gate driver voltage regulator is turned on. After the gate driver start-up time, the gate drivers start switching if the bit VGG_ok is set.

**Table 24. Function control register (address 00h)**

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 7 to 4 | - | reserved | 0000 | reserved: keep clear for future use |
| 3 | Cnt_CSB | count chip select time | 0 | chip select LOW count feature is disabled |
| | | | 1 | chip select LOW count feature is enabled |
| 2 | Vout2en | enable output 2 | 0 | output 2 is turned off |
| | | | 1 | output 2 is turned on, when the device is in operation mode |
| 1 | Vout1en | enable output 1 | 0 | output 1 is turned off |
| | | | 1 | output 1 is turned on, when the device is in operation mode |
| 0 | Cfg_dn | configuration done | 0 | device is in configuration mode - no configuration lock |
| | | | 1 | device is in configuration mode - configuration lock is active |

## 8.6 Trimming and calibration

The ASL4501SHN offers an option to trim the oscillator frequency and calibrate the output phases. The trimming allows highly accurate switching frequency. The calibration ensures matching of the power delivered by the individual phases toward an output.

### 8.6.1 Frequency trimming

It is mandatory to adjust the internal oscillator frequency of the device to ensure the ASL4501SHN is operating within the specified oscillator frequency range.

To measure the actual internal frequency, the device measures the time that the CSB pin is LOW during an SPI transfer. This time information is used to adjust the oscillator frequency of the device. The recommended procedure for the time adjustment is shown in Figure 7.
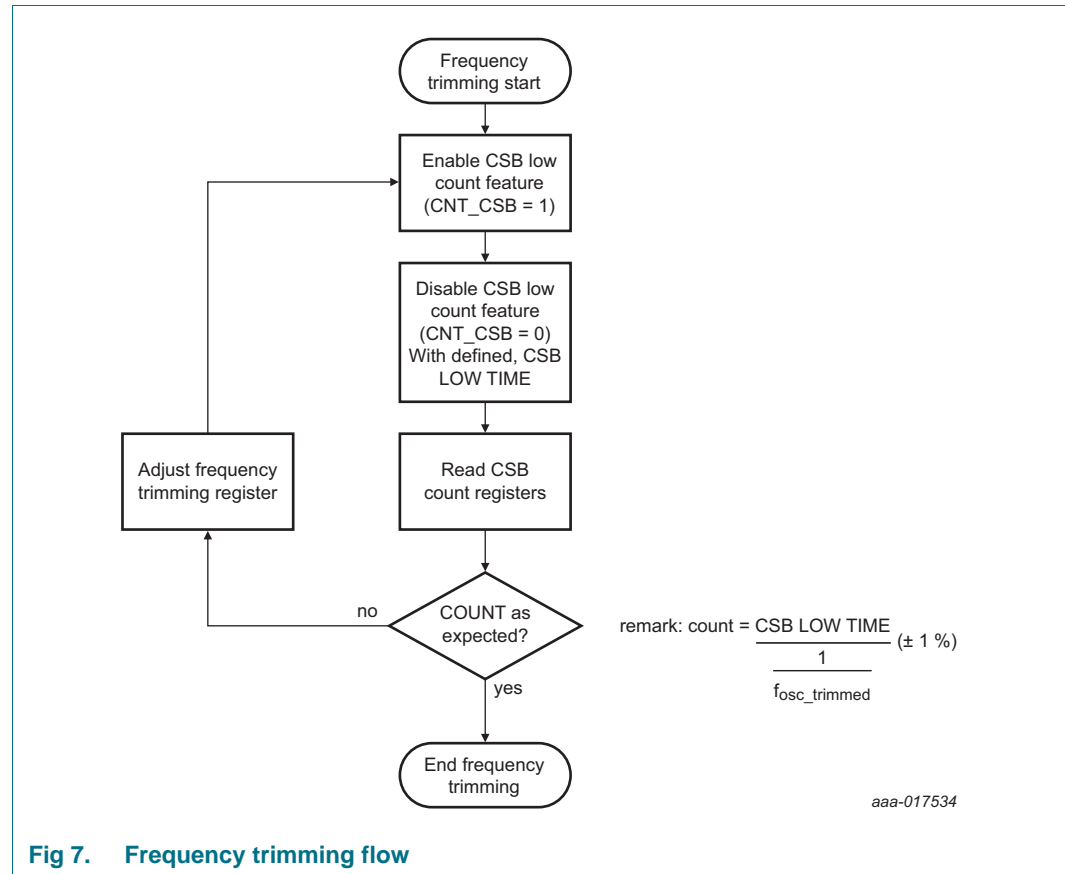


remark: $count = \dfrac{CSB\ LOW\ TIME}{\dfrac{1}{f_{osc\_trimmed}}}$ (± 1 %)

*aaa-017534*

**Fig 7.    Frequency trimming flow**

At the start of the sequence, the CSB LOW count feature is activated. It is done by setting the Cnt_CSB bit HIGH in the frequency trimming control register (bit 3; register 00h). The device now measures the time with its internal time domain each time the CSB pin is LOW. It makes this information available in the CSB count registers. To allow an exact stable reading, set the Cnt_CSB bit LOW again with an accurately known CSB LOW time. Setting the bit LOW freezes the count registers. These registers store the last value, which in this case is the command that sets the Cnt_CSB bit LOW.

The CSB count registers contain the count of the CSB LOW time of the last SPI command the CSB LOW count feature was enabled. CSB count register 1 contains the bits 7 to 0 of the counter, while the CSB count register 2 contains the bits 15 to 8.

**Table 25.    CSB count register 1 (address 41h)**

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 7 to 0 | CSB_cnt[7:0] | CSB count LOW | ... | count value (bits 7 to 0) |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**18 of 43**

**Table 26.  CSB count register 2 (address 42h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 15 to 8 | CSB_cnt[15:8] | CSB count HIGH | ... | count value (bits 15 to 8) |

The count, the CSB count register returns, should correspond to the real time of the CSB LOW time. 1 count should correspond with $1/f_{osc\_trimmed}$ (see Table 46).

When the CSB count register count, deviates from the applied CSB LOW time, adjust the device internal timing by modifying the frequency trimming register.

To ensure that the adjustment had the desired effect, restart the procedure and check the count with the new settings in the frequency trimming register.

When the device internal time matches the applied CSB LOW time, no further adjustment is needed and the trimming procedure is finished.

### 8.6.2  Calibration

A calibration of the IC can be initiated at power-up. The calibration ensures the individual activated phases connected to one output of the ASL4501SHN conduct the same amount of power. The calibration of the device takes care that any spread coming from the IC is minimized. Any effect from external components is not taken care of by the calibration.

As a pre-condition for the calibration, device has to be configured with the target configuration with the integral and proportional factors set to max value. The VGG regulator has to signal VGG_ok. When the Calib bit [bit 0 in frequency trimming register (address 1Ch)] is set LOW, the calibration starts. After t_calib, the calibration is completed and the calibration done bit will be set. The result of the calibration can be read in the calibration result register (address 4Ch).

Note:

While the device is in calibration mode, the device operates with the default oscillator frequency.

To ensure that the device is operating with a valid calibration, it is recommended to execute the calibration multiple times. Valid calibrations give similar calibration values. Invalid calibrations, e.g. because of external disturbances, give outliers.

A restart of the calibration is only allowed once the running calibration is completed or the device was in off mode.

### 8.6.3  Trimming and calibration registers

The frequency trimming register contains the trim bits for the oscillator, but is also used to allow access to the calibration values.

**Table 27.  Calibration/frequency trimming register (address 1Ch)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 and 6 | - | reserved | - | n.a. |
| 5 to 1 | Calib/Ftrim[4:0] | frequency trim bits 4 to 0 | .... | Calib = 1: frequency trim setting |
| | | calibration bits 4 to 0 | .... | Calib = 0: pointer to calibration data |
| 0 | Calib | calibration/frequency trimming | 1 | frequency trimming - normal operation |
| | | | 0 | calibration mode |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**19 of 43**

**Table 28.    Calib/Ftrim settings**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 4 to 0 | Calib/Ftrim[4:0] | frequency trimming bits | 01000 | default frequency − 33.33 % |
| | | | 01001 | default frequency − 30.56 % |
| | | | 01010 | default frequency − 27.78 % |
| | | | 01011 | default frequency − 25.00 % |
| | | | 01100 | default frequency − 22.22 % |
| | | | 01101 | default frequency − 19.44 % |
| | | | 01110 | default frequency − 16.67 % |
| | | | 01111 | default frequency − 13.89 % |
| | | | 00000 | default frequency − 11.11 % |
| | | | 00001 | default frequency − 8.33 % |
| | | | 00010 | default frequency − 5.56 % |
| | | | 00011 | default frequency − 2.78 % |
| | | | 00100 | default frequency |
| | | | 00101 | default frequency + 2.78 % |
| | | | 00110 | default frequency + 5.56 % |
| | | | 00111 | default frequency + 8.33 % |
| | | | 11000 | default frequency + 11.11 % |
| | | | 11001 | default frequency + 13.89 % |
| | | | 11010 | default frequency + 16.67 % |
| | | | 11011 | default frequency + 19.44 % |
| | | | 11100 | default frequency + 22.22 % |
| | | | 11101 | default frequency + 25.00 % |
| | | | 11110 | default frequency + 27.78 % |
| | | | 11111 | default frequency + 30.56 % |
| | | | 10000 | default frequency + 33.33 % |
| | | | 10001 | default frequency + 36.11 % |
| | | | others | not allowed |
| | | content of calibration result register (4Ch); Calib/Ftrim[4:0] select the content available in register 4Ch | bit 0 - calibration complete bit: 1 = calibration complete; 0 = calibration ongoing | |
| | | | 4h | bits 4 to 0 calibration value REF2 |
| | | | 6h | bits 4 to 0 calibration value CAL2 |
| | | | 8h | bits 4 to 0 calibration value REF3 |
| | | | Ah | bits 4 to 0 calibration value CAL3 |
| | | | Ch | bits 4 to 0 calibration value REF4 |
| | | | Eh | bits 4 to 0 calibration value CAL4 |

The calibration result register contains the calibration results based on the selection of the Calib/Ftrim[4:0] setting in Table 27.

**Table 29.    Calibration result register (address 4Ch)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | Calib_value[7:0] | calibration value as selected per Calib/Ftrim[4:0] setting | read only | calibration info per Calib/Ftrim[4:0] setting |

ASL4501SHN

**Product data sheet** **Rev. 2 — 10 January 2018** **20 of 43**

## 8.7 Gate supply voltage

The ASL4501SHN has an integrated linear regulator to generate the supply voltage of the gate drivers. The integrated linear regulator is internally connected to the pins VGG1 and VGG2. The voltage generated by the linear regulator can be set via the VGG control register.

**Table 30. VGG control register (address 15h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | VGG[7:0] | supply voltage for gate drivers | 00h | not allowed |
| | | | ... | not allowed |
| | | | 5Dh | maximum output voltage = 10.3 V |
| | | | ... | $16.25\ \text{V} - 64\ \text{mV} \times \text{VGG[7:0]}$ |
| | | | B7h | minimum output voltage = 4.54 V |
| | | | ... | not allowed |
| | | | FFh | not allowed |

If a setting between 00h and 5Dh is used, a gate driver voltage is targeted that exceeds the limiting values of the IC. Do not program these settings. To ensure that only values in the allowed range are set inside the IC, read back the programmed value immediately after setting it.

If a setting between FFh and B7h is used, the device may not start up VGG. If the device operates, parameters of VGG are not guaranteed.

### 8.7.1 Gate voltage supply diagnostics

The diagnostic options for the gate voltage supply are:

- Gate driver available; details can be found in Section 8.10
- Gate driver protection active; details can be found in Section 8.10

## 8.8 Supply voltage monitoring

When at least one of the outputs is enabled and bit VGG_ok is set, the ASL4501SHN continuously measures the voltage at pin VBAT. It allows the system to monitor the supply voltage without additional external components. It also offers the option to put an automatic undervoltage or overvoltage protection in place.

Note: The VIN_UV and VIN_OV bits in the status register use the battery voltage measurement. As a result, the VIN_UV and VIN_OV bits are only reliable when at least one output is enabled.

### 8.8.1 Battery voltage measurement

The ASL4501SHN continuously measures the voltage at pin VBAT. The measurement result is available in the battery voltage register when at least one output is enabled.

**Table 31. Battery voltage register (address 45h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | V_VBAT[7:0] | battery voltage | 00h | battery voltage = 0 V |
| | | | ... | battery voltage = $0.3555 \times$ V_VBAT[7:0] $\times (1 + (333 \times 10^{-6}) \times$ (T_junction[7:0] $- 38))$ |
| | | | FFh | maximum measurable battery voltage = 90 V |

### 8.8.2 Undervoltage detection

The ASL4501SHN offers a variable undervoltage detection threshold. When the supply voltage drops below this threshold, the undervoltage detect bit is set, and fail silent mode is entered. All gate pins stop toggling and power is no longer delivered to the output.

**Table 32. Undervoltage threshold register (address 1Bh)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | V_VIN_UV[7:0] | undervoltage detection threshold | 00h | undervoltage detection threshold = 0 V |
| | | | ... | undervoltage detection threshold = $0.3555 \times$ V_VIN_UV[7:0] $\times (1 + (333 \times 10^{-6}) \times$ (T_junction[7:0] $- 38))$ |
| | | | FFh | maximum undervoltage detection threshold = 90 V |

### 8.8.3 Overvoltage detection

The ASL4501SHN offers a variable overvoltage detection threshold. When the supply voltage rises above this threshold, the overvoltage detect bit is set, and fail silent mode is entered. All gate pins stop toggling and power is no longer delivered to the output.

**Table 33. Overvoltage threshold register (address 1Ah)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | V_VIN_OV[7:0] | overvoltage detection threshold | 00h | overvoltage detection threshold = 0 V |
| | | | ... | overvoltage detection threshold = $0.3555 \times$ V_VIN_OV[7:0] $\times (1 + (333 \times 10^{-6}) \times$ (T_junction[7:0] $- 38))$ |
| | | | FFh | maximum overvoltage detection threshold = 90 V |

## 8.9 Junction temperature information

The ASL4501SHN provides a measurement of the IC junction temperature. The measurement information is available in the junction temperature register.

**Table 34. Junction temperature register (address 46h)**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 7 to 0 | T_junction[7:0] | junction temperature | 0h to 17h | device junction temperature below $-40$ °C |
| | | | 18h | device junction temperature = $-40$ °C |
| | | | ... | device junction temperature = T_junction[7:0] $\times$ (215 / 106) °C $- 88$ °C |
| | | | 82h | device junction temperature = 175 °C |
| | | | 83h to FFh | device junction temperature above 175 °C |

ASL4501SHN

**Product data sheet**

Rev. 2 — 10 January 2018

22 of 43

## 8.10 Diagnostic information

The diagnostic register contains useful information for diagnostic purposes. Details for each bit can be found in the following subchapters.

**Table 35.    Diagnostic register (address 5Fh)**

| Bit | Symbol | Description | Value | Function |
|-----|--------|-------------|-------|----------|
| 7 | Vout1_ok | Vout1 regulated | 0 | Vout1 is deviating from the target value |
|   |          |                 | 1 | Vout1 is regulated to the target value |
| 6 | Vout2_ok | Vout2 regulated | 0 | Vout2 is deviating from the target value |
|   |          |                 | 1 | Vout2 is regulated to the target value |
| 5 | VGG_ok | gate driver regulation is ok | 0 | gate driver is not available |
|   |        |                              | 1 | gate driver is available |
| 4 | Tj_err | device temperature is too high | 0 | device temperature below 175 °C |
|   |        |                                | 1 | device temperature above 175 °C |
| 3 | VIN_UV | VIN undervoltage | 0 | undervoltage not detected at VIN |
|   |        |                  | 1 | undervoltage detected at VIN |
| 2 | VIN_OV | VIN overvoltage | 0 | overvoltage not detected at VIN |
|   |        |                 | 1 | overvoltage detected at VIN |
| 1 | SPI_err | SPI error | 0 | last SPI command was executed correctly |
|   |         |           | 1 | last SPI command was erroneous and has been discarded |
| 0 | VGG_err | VGG error | 0 | VGG overload protection not active |
|   |         |           | 1 | VGG overload protection has turned on and VGG is deactivated |

### 8.10.1 Bit VIN_OV

The bit VIN_OV depends on the battery monitoring functionality as described in Section 8.8. It indicates that the device has detected an overvoltage condition and entered the fail silent mode. A write access to the diagnostic register, or once the off mode is entered, clears the bit. The device stays in fail silent mode irrespective of the clearing of the bit.

### 8.10.2 Bit VIN_UV

The bit VIN_UV depends on the battery monitoring functionality as described in Section 8.8. It indicates that the device has detected an undervoltage condition and entered the fail silent mode. A write access to the diagnostic register, or once the off mode is entered, clears the bit. The device stays in fail silent mode irrespective of the clearing of the bit.

### 8.10.3 Bit SPI_err

The device evaluates all SPI accesses to the device for the correctness of the commands. When the command is not allowed, the SPI_err bit is set. A write access to the diagnostic register, or once off mode has been entered, clears the bit.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

Rev. 2 — 10 January 2018

23 of 43

### 8.10.4 Bit Tj_err

The bit Tj_err indicates that the junction temperature has exceeded the maximum allowable temperature, and the device has entered fail silent mode. A write access to the diagnostic register, or once off mode has been entered, clears the bit. The device stays in fail silent mode irrespective of the clearing of the bit. After leaving the off mode (at IC start-up), it is possible that bit Tj_err is set. To avoid wrong diagnostics, clear the diagnostic register before it is evaluated.

### 8.10.5 Bit VGG_err

Bit VGG_err is set when the gate driver does not reach the VGG_ok _window (when $V_{VGG}$ is within range) within the regulator voltage start-up error time. Once bit VGG_err is set, it indicates that an error on the gate driver has been detected and the device has entered fail silent mode. A write access to the diagnostic register, or once off mode has been entered, clears the bit. The device stays in fail silent mode irrespective of the clearing of the bit.

### 8.10.6 Bit VGG_ok

The bit VGG_ok indicates that the gate driver is regulated to the target voltage and allows the gate drivers to drive the gate driver pins. If the gate driver is outside the VGG_ok window after $t_{startup}$, and $V_{VGG}$ is within range, the device clears VGG_ok bit and enters fail silent mode.

### 8.10.7 Bits Vout1_ok and Vout2_ok

The bits Vout1_ok and Vout2_ok indicate whether the output voltage is regulated to the target value or deviating from the target value. The bits are set as soon as the corresponding output is within the Vout_ok window (when $V_O$ is within the range) for more than $t_{fltr(ov)}$. The bits are cleared when the corresponding output is outside the Vout_ok window for more than $t_{fltr(ov)}$.

## 8.11 SPI

The ASL4501SHN uses an SPI to communicate with an external microcontroller. The SPI can be used for setting the LEDs current, reading and writing the control register.

### 8.11.1 SPI introduction

The SPI provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back the registers without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- CSB - SPI chip select; active LOW
- SCLK - SPI clock - default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output - floating when pin CSB is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge as illustrated in Figure 8.
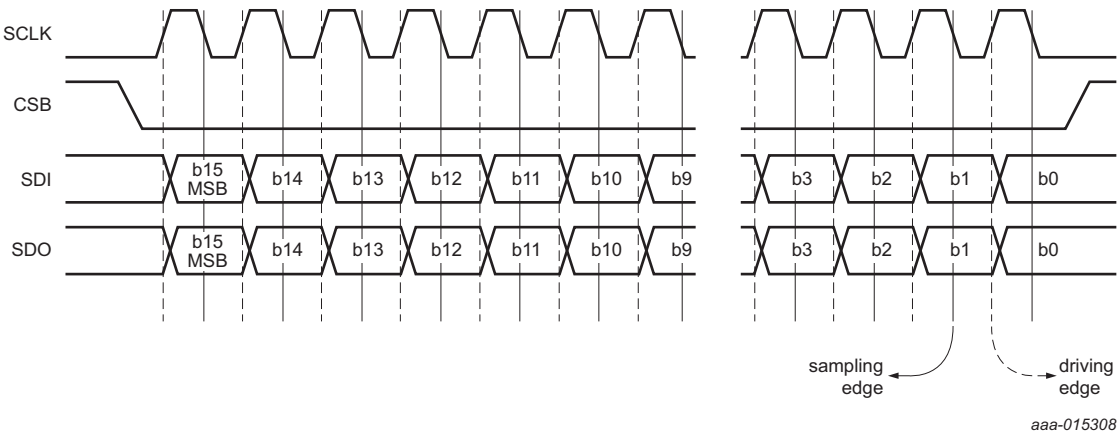
Format:

Steady state SCLK = 0

Data driving edge = positive edge

Data sampling edge = negative edge

**Fig 8.    SPI timing protocol**

The data bits of the ASL4501SHN are arranged in registers of one-byte length. Each register is assigned to a 7-bit address. For writing into a register, 2 bytes must be sent to the LED driver. The first byte is an identifier byte that consists of the 7-bit address and one read-only bit. For writing, the read-only bit must be set to logic 0. The second byte is the data that is written into the register, so an SPI access consists of at least 16 bits.

The SPI frame format is shown in Figure 9, Table 36 and Table 37.
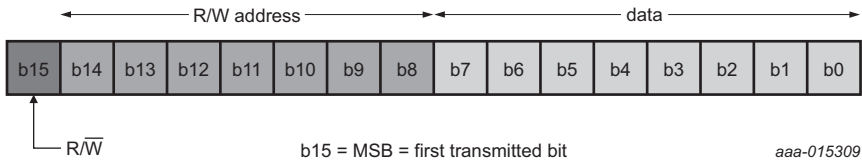


**Fig 9.    SPI frame format**

**Table 36.    SPI frame format for a transition to the device**

| Bit | Symbol | Description | Value | Function |
|---|---|---|---|---|
| 15 | b15 | R/W bit | 0 | write access |
| | | | 1 | read access |
| 14 to 8 | b14:8 | address bits | XXX XXXX | address that is selected |
| 7 to 0 | b7:0 | data bits | XXXX XXXX | data that is transmitted |

ASL4501SHN

**Product data sheet** **Rev. 2 — 10 January 2018** **25 of 43**

**Table 37.   SPI frame format for a transition from the device**

| Bit | Symbol | Description | Value | Function[1] |
|-----|--------|-------------|-------|-------------|
| 15 to 8 | b8:15 | diagnostic register | XXXX XXXX | content of diagnostic register |
| 7 to 0 | b7:0 | data bits | XXXX XXXX | when previous command was a valid read command, content of the register that is supposed to be read |
| | | | XXXX XXXX | when previous command was a valid write command, new content of the register that was supposed to be written |

[1]   The first SPI command after leaving the off mode, will return 00h.

The master initiates the command sequence. The sequence begins with CSB pin pulled LOW and lasts until it is asserted HIGH.

The ASL4501SHN also tolerates SPI accesses with a multiple of 16 bits. It allows a daisy chain configuration of the SPI.



*aaa-024030*

**Fig 10.   Daisy chain configuration**

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

26 of 43

*aaa-024031*
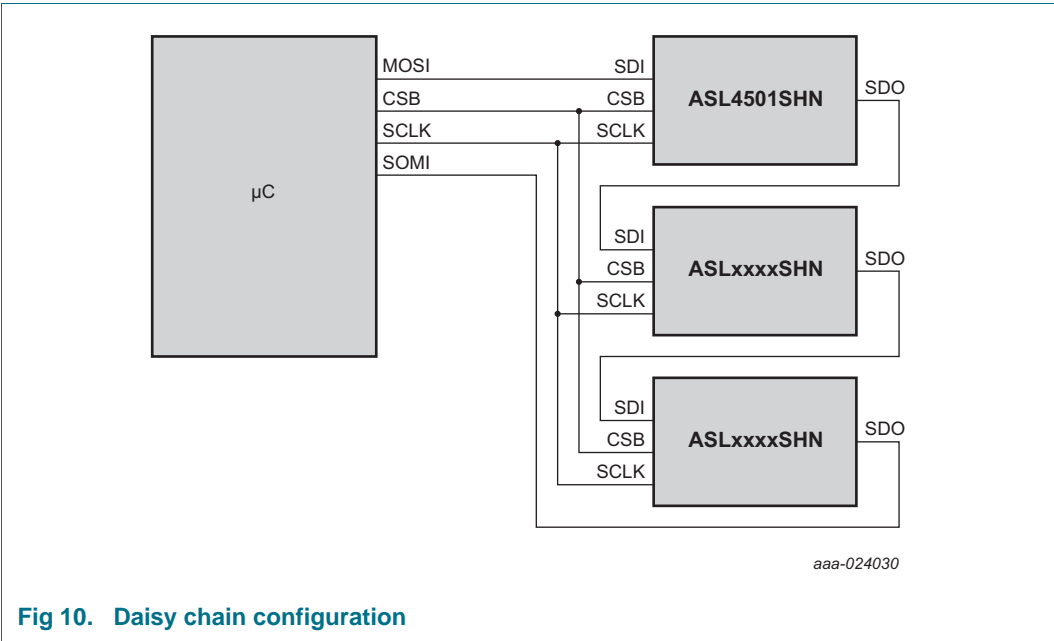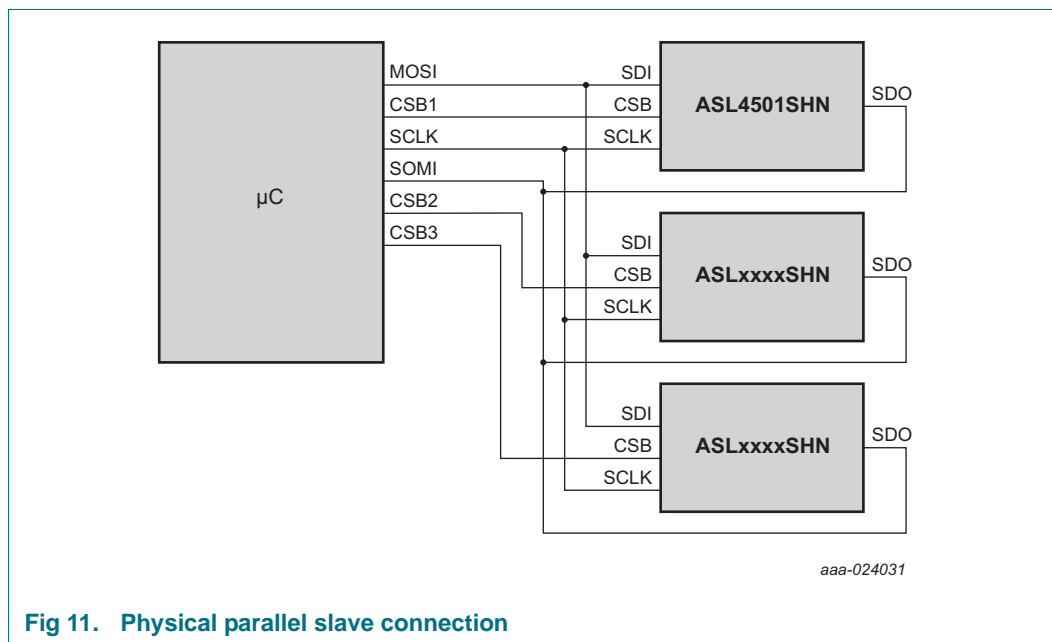
**Fig 11.   Physical parallel slave connection**

During the SPI data transfer, the identifier byte and the actual content of the addressed registers is returned via the SDO pin. The same happens for pure read accesses. Here the read-only bit must be set on logic 1. The content of the data bytes that are transmitted to the ASL4501SHN is ignored.

The ASL4501SHN monitors the number of data bits that are transmitted. If the number is not 16, or a multiple of 16, then a write access is ignored and the SPI error indication bit is set.

## 8.11.2   Typical use case illustration (write/read)

Consider a daisy chain scheme with one master connected to four slaves in daisy chain fashion. The following commands are performed during one sequence (first sequence):

- Write data FFh to the register 1Ah slave 1
- Read from register 02h of slave 2
- Write data AFh to the register 2Fh of slave 3
- Read from register 44h of slave 4
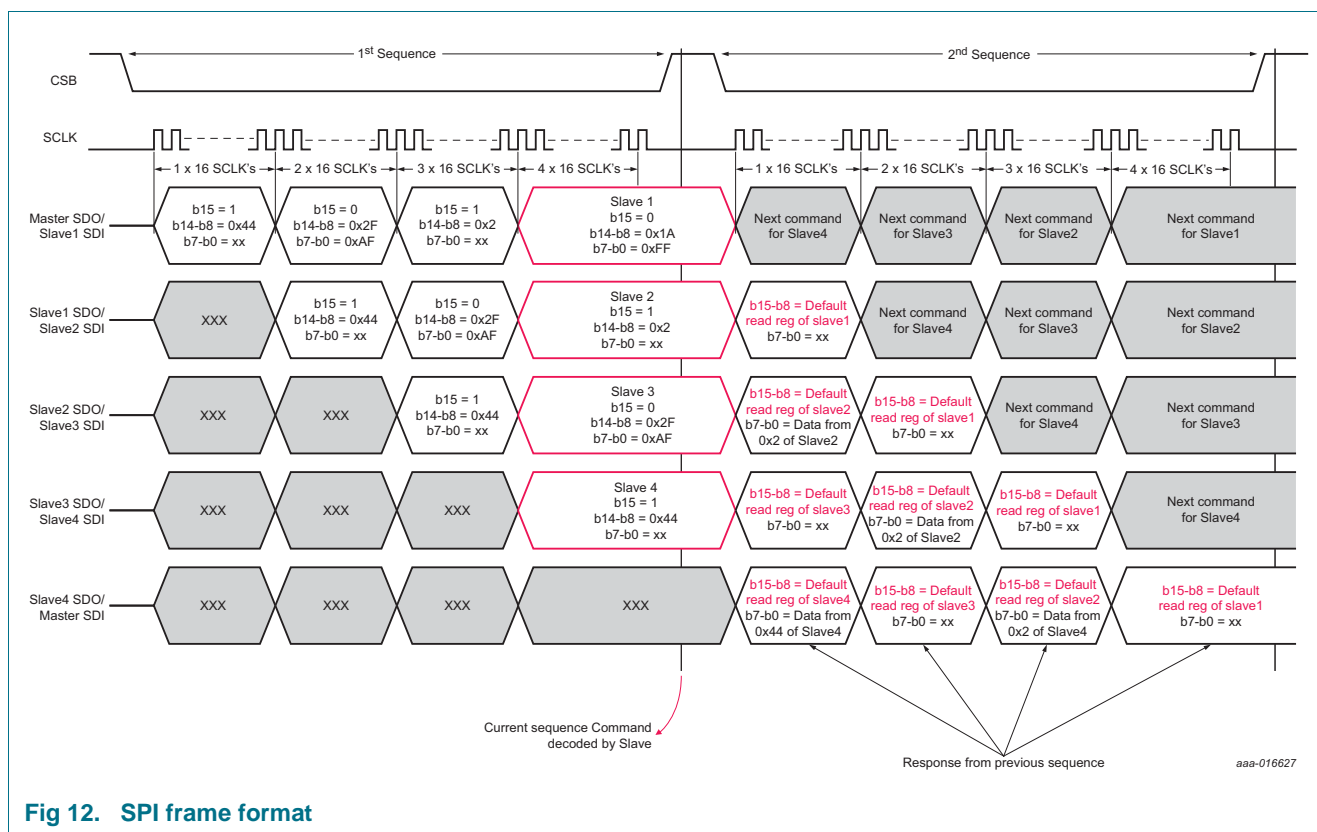
**Fig 12. SPI frame format**

### 8.11.3 Diagnostics for the SPI

The device is evaluating all SPI access to the device for the correctness of the commands. When the command is not allowed, the SPI_err bit is set.

The conditions that are considered as erratic accesses are:

- SPI write is attempted to a read-only location or reserved location
- SPI write is attempted during operation to a configuration register
- SPI read is attempted from a reserved location
- SPI command does not consist of a multiple of 16 clock counts

If an SPI access is considered to be erratic, no modifications to a SPI register are made. The access after the erratic SPI command returns the diagnostic register and zero in the data field.

For details concerning the SPI_err bit, see Section 8.10.

### 8.11.4 Register map

The addressable register space amounts to 128 registers from 00h to 7Fh. They are separated into two groups as shown in Table 38. The register mapping is shown in Table 39 and Table 42. The functional description of each bit can be found in the dedicated chapter.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**28 of 43**

**Table 38. Grouping of the register space**

| Address range | Description | Content |
|---|---|---|
| 00h to 1Fh | control registers | control registers |
| 20h to 7Fh | diagnostic registers | diagnostic information |

### 8.11.4.1 Control registers

**Table 39. Control register group overview**

| Address | Name | Reset value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | function control | 00h | - | - | - | - | Cnt_CSB | Vout2en[1] | Vout1en[1] | Cfg_dn |
| 01h | gate driver enable | 00h | - | - | - | - | EN_G4[2] | EN_G3[2] | EN_G2[2] | EN_G1[2] |
| 03h | target voltage output 1 | 00h | V_Vout_1[7:0] | | | | | | | |
| 04h | target voltage output 2 | 00h | V_Vout_2[7:0] | | | | | | | |
| 05h | limit voltage output 1 | 00h | Vmax_Vout_1[7:0] | | | | | | | |
| 06h | limit voltage output 2 | 00h | Vmax_Vout_2[7:0] | | | | | | | |
| 07h | maximum phase current Vout1 | 46h | I_max_per_phase_Vout_1[7:0] | | | | | | | |
| 08h | maximum phase current Vout2 | 46h | I_max_per_phase_Vout_2[7:0] | | | | | | | |
| 1Ch | frequency trimming register | 09h | - | - | Calib/Ftrim[4:0] | | | | | - |

[1] Bits are locked with bit Cfg_dn is HIGH. When bit Cfg_dn is LOW, bits can be changed. Read is always possible.

[2] Individual gate drivers that are enabled when Cfg_dn and VGG_ok are set HIGH, can be turned on and off during operation of the system. Gate drivers, disabled when bits Cfg_dn and VGG_ok are set HIGH, remain off, even when the gate enable bits are set HIGH later.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet** **Rev. 2 — 10 January 2018** **29 of 43**

#### 8.11.4.2 Configuration registers

The configuration registers inside the control block can only be written in configuration mode. In the other modes, this register can only be read.

**Table 40. Configuration register group overview**

| Address | Name | Reset value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------------|---|---|---|---|---|---|---|---|
| 02h | gate driver output | 00h | - | - | - | - | O_G4 | O_G3 | O_G2 | O_G1 |
| 09h | clock divider for output 1 | 0Fh | Clkdiv1[7:0] | | | | | | | |
| 0Ah | clock divider for output 2 | 0Fh | Clkdiv2[7:0] | | | | | | | |
| 0Bh | internal phases output 1 | 0Fh | - | - | - | - | EN_P4_1 | EN_P3_1 | EN_P2_1 | EN_P1_1 |
| 0Ch | internal phases output 2 | 0Fh | - | - | - | - | EN_P4_2 | EN_P3_2 | EN_P2_2 | EN_P1_2 |
| 0Dh | phase off and delay output 1 | 39h | Phdel1[4:0] | | | | | Phoff1[2:0] | | |
| 0Eh | phase off and delay output 2 | 39h | Phdel2[4:0] | | | | | Phoff2[2:0] | | |
| 0Fh | gate driver phase | 00h | - | - | - | - | O_GP4 | O_GP3 | O_GP2 | O_GP1 |
| 10h | phase selection configuration | E4h | Phsel4[1:0] | | Phsel3[1:0] | | Phsel2[1:0] | | Phsel1[1:0] | |
| 11h | loop filter proportional configuration | 00h | Prop2[3:0] | | | | Prop1[3:0] | | | |
| 12h | loop filter integral configuration | 00h | Integ2[3:0] | | | | Integ1[3:0] | | | |
| 13h | slope compensation configuration | 88h | Slpcmp2[3:0] | | | | Slpcmp1[3:0] | | | |
| 14h | current sense slope resistor configuration | 00h | Slpr4[1:0] | | Slpr3[1:0] | | Slpr2[1:0] | | Slpr1[1:0] | |
| 15h | gate driver control | FFh | VGG[7:0] | | | | | | | |
| 1Ah | overvoltage detection threshold | FFh | V_VIN_OV[7:0] | | | | | | | |
| 1Bh | undervoltage detection threshold | 00h | V_VIN_UV[7:0] | | | | | | | |

#### 8.11.4.3 Internal registers

The ASL4501SHN uses the SPI registers to control some internal functions. In order to avoid any unintended behavior of the device, do not modify these registers but leave them all at their default value.

**Table 41. Internal register group**

| Address | Name | Reset value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------------|---|---|---|---|---|---|---|---|
| 19h | internal 1 | 82h | - | - | - | - | - | - | - | - |
| 25h | internal 2 | 27h | - | - | - | - | - | - | - | - |
| 26h | internal 3 | 3Bh | - | - | - | - | - | - | - | - |
| 2Fh | internal 4 | E8h | - | - | - | - | - | - | - | - |
| 30h | internal 5 | 09h | - | - | - | - | - | - | - | - |

#### 8.11.4.4 Diagnostic registers

The ASL4501SHN provides diagnostic data via some SPI registers. These registers are read only, but error bits can be cleared via a write access to the register.

**Table 42. Diagnostic register group overview**

| Address | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|---|---|---|---|---|---|---|
| 41h | CSB count low | CSB_cnt[7:0] | | | | | | | |
| 42h | CSB count high | CSB_cnt[15:8] | | | | | | | |
| 45h | battery voltage | V_VBAT[7:0] | | | | | | | |
| 46h | junction temperature | T_junction[7:0] | | | | | | | |
| 4Ch | calibration result register | Calib_value[7:0] | | | | | | | |
| 5Fh | diagnostic register | Vout1_ok | Vout2_ok | VGG_ok | Tj_err | VIN_UV | VIN_OV | SPI_err | VGG_err |

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

Rev. 2 — 10 January 2018

31 of 43

# 9. Limiting values

**Table 43. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | battery supply voltage | EN = LOW | | −0.3 | +60 | V |
| | | EN = HIGH | | −0.3 | +40 | V |
| $V_{VCC}$ | voltage on pin VCC | | | −0.3 | +5.5 | V |
| $V_{GND}$ | ground supply voltage | voltage between ground pins | | −0.6 | +0.6 | V |
| $V_{FBx}$ | voltage on feedback pins | FB1 and FB2 | | −0.3 | +90 | V |
| $V_O$ | output voltage | programmed target voltage according to registers 0x03h and 0x04h | | 10 | 80 | V |
| $V_{I(dig)}$ | digital input voltage | voltage on digital pins SDO, SDI, CSB, SCLK and EN | | −0.3 | +5.5 | V |
| $V_{VGG}$ | voltage on pin VGG | VGG1 | [1] | −0.3 | +20 | V |
| | | VGG2 | [1] | −0.3 | +20 | V |
| $V_{sense}$ | sense voltage | voltage on sense pins SNH1, SNH2, SNH3, SNH4, SNL1, SNL2, SNL3 and SNL4 | | −0.3 | +1.8 | V |
| $V_{Gx}$ | voltage on gate pins | voltage on gate pins G1, G2, G3 and G4 | | −0.3 | +10 | V |
| $T_j$ | junction temperature | | | −40 | +175 | °C |
| $T_{stg}$ | storage temperature | | | −55 | +175 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | | [2] | −2 | +2 | kV |
| | | | [3] | −500 | +500 | V |

[1] VGG1 and VGG2 are IC internally connected (shorted).

[2] HBM according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[3] CDM according to AEC-Q100-011 (field induced charge; 4 pF).

# 10. Thermal characteristics

**Table 44. Thermal characteristics**

| Symbol | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $R_{th(tot)}$ | total thermal resistance | | [1] | 37 | K/W |

[1] In accordance with JEDEC, JESD51-2, JESD51-5 and JESD51-7 with natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array, under the exposed pad connected to the first inner copper layer.

## 11. Static characteristics

**Table 45. Static characteristics**

*Minimum and maximum values are specified for the following conditions: $V_{BAT}$ = 5.5 V to 40 V, $V_{EN}$ = 4.5 V to 5.5 V, $V_{VCC}$ = 4.5 V to 5.5 V and $T_j$ = −40 °C to +175 °C[1]. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at $V_{VIN}$ = 40 V, $V_{EN}$ = 5 V, $V_{VCC}$ = 5 V and $T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply pin VBAT** | | | | | | | |
| $I_{DD}$ | supply current | operating; no load on VGG; gate pins LOW; one phase; one output | | 5 | 13 | - | mA |
| | | operating; no load on VGG; gate pins low; four phases; two outputs | | - | 20 | - | mA |
| $I_{off}$ | off-state current | EN = LOW | | - | - | 5 | μA |
| $V_{th(det)pon}$ | power-on detection threshold voltage | | | - | - | 4.5 | V |
| **Supply pin VCC** | | | | | | | |
| $I_{VCC}$ | supply current on pin VCC | EN = HIGH; CSB = LOW | | - | - | 250 | μA |
| **Supply pin EN** | | | | | | | |
| $I_{EN}$ | supply current on pin EN | EN = HIGH | | - | - | 225 | μA |
| **Output voltage** | | | | | | | |
| $V_{O(acc)}$ | output voltage accuracy | Vout1: operating accuracy 1 | | $-0.03 \times$ Vout1 $- 0.711$ | - | $+0.03 \times$ Vout1 $+ 0.711$ | V |
| | | Vout2: operating accuracy 2 | | $-0.03 \times$ Vout2 $- 0.711$ | - | $+0.03 \times$ Vout2 $+ 0.711$ | V |
| $V_O$ | output voltage | bit Vout1_ok/Vout2_ok is set when $V_O$ is within the range regarding the target value | | −5.4 | - | +2.4 | V |
| **Regulated voltage output** | | | | | | | |
| $V_{VGG}$ | voltage on pin VGG | $V_{BAT} \geq V_{VGG} + V_{do(reg)VGG}$ | [2] | 4.46 | - | 10.04 | V |
| | | bit VGG_ok is set when $V_{VGG}$ is within the range regarding the target value | [2] | −2.4 | - | +2.4 | V |
| $V_{do(reg)VGG}$ | regulator dropout voltage on pin VGG | $I_{VGG} \leq$ 50 mA; regulator in saturation | | - | 0.5 | 1.0 | V |
| | | $I_{VGG} \leq$ 160 mA; regulator in saturation | | - | 1.6 | 3.2 | V |
| $V_{reg(acc)VGG}$ | regulator voltage accuracy on pin VGG | 25 °C to $T_{j(max)}$ | | −5 | - | +5 | % |
| | | −40 °C to +25 °C | | −7 | - | +5 | % |
| $C_{VGG}$ | capacitor on pin VGG | ESR $\leq$ 0.1 Ω | | - | 1 | - | μF |
| $\Delta V$ | voltage variation | deviation from average peak current value at sense pins; before subtracting slope compensation 160 mV, corresponding to a peak set value of 16 A at 10 mΩ $R_{sense}$ | [3] | −2.5 | - | +2.5 | % |

**Table 45.** **Static characteristics** *…continued*

*Minimum and maximum values are specified for the following conditions: $V_{BAT}$ = 5.5 V to 40 V, $V_{EN}$ = 4.5 V to 5.5 V, $V_{VCC}$ = 4.5 V to 5.5 V and $T_j$ = −40 °C to +175 °C[1]. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at $V_{VIN}$ = 40 V, $V_{EN}$ = 5 V, $V_{VCC}$ = 5 V and $T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{slope}$ | slope voltage difference | deviation from average slope voltage value at sense pins; subtraction of slope compensation is 10.9 mV, equal to 10.9 A at 10 mΩ $R_{sense}$ and $R_{slope}$ setting of 1 kΩ [3] | −8 | - | +8 | % |
| **Serial peripheral interface inputs; pins SDI, SCLK and CSB** | | | | | | |
| $V_{th(sw)}$ | switching threshold voltage | | $0.3V_{CC}$ | - | $0.7V_{CC}$ | V |
| $R_{pd(int)SCLK}$ | internal pull-down resistance on pin SCLK | | 40 | - | 80 | kΩ |
| $R_{pd(int)CSB}$ | internal pull-down resistance on pin CSB | | 40 | - | 80 | kΩ |
| $R_{pd(int)SDI}$ | internal pull-down resistance on pin SDI | | 40 | - | 80 | kΩ |
| **Serial peripheral interface data output; pin SDO** | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −4 mA; $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = −4 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.4 | V |
| $I_{LOZ}$ | OFF-state output leakage current | $V_{CSB}$ = $V_{CC}$; $V_O$ = 0 V to $V_{CC}$; $V_{CC}$ = 4.5 V to 5.5 V | −5 | - | +5 | μA |
| **Temperature protection** | | | | | | |
| $\Delta T_j$ | junction temperature variation | measurement provided via register 46h; $T_j$ = 130 °C | −20 | - | +20 | °C |
| $T_{sd(otp)}$ | overtemperature protection shutdown temperature | [4] | 150 | 175 | 200 | °C |
| **$V_{BAT}$ monitoring** | | | | | | |
| $V_{VBAT}$ | accuracy of voltage measurement on pin VBAT | | $-0.035 \times V_{BAT}$ − 0.3555 | - | $+0.035 \times V_{BAT}$ + 0.3555 | V |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] VGG refers to both VGG1 and VGG2.

[3] For a given system with $V_{BAT}$ = 13.5 V, Voutx = 50 V, L = 15 μH, $R_{sense}$ = 10 mΩ, $f_{sw}$ = 400 kHz, optimized device configuration and 30 W output power per phase, the maximum current deviation will be less than 225 mA from the average value.

[4] Additional features include protection against load dump transient voltages of up to 60 V and thermal shutdown when the junction temperature of the ASL4501SHN exceeds 175 °C.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**34 of 43**

## 12. Dynamic characteristics

**Table 46.  Dynamic characteristics**

*Minimum and maximum values are specified for the following conditions: $V_{BAT}$ = 5.5 V to 40 V, $V_{EN}$ = 4.5 V to 5.5 V, $f_{osc}$ = 130 MHz to 200 MHz, $V_{CC}$ = 4.5 V to 5.5 V and $T_j$ = −40 °C to +175 °C[1]. All voltages are defined with respect to ground. Positive currents flow into the IC. Typical values are given at $V_{BAT}$ = 12 V, $V_{EN}$ = 5 V, $V_{CC}$ = 5 V and $T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DCDC}$ | DC-to-DC converter frequency | | 125 | - | 700 | kHz |
| $f_{DCDC(acc)}$ | DC-to-DC converter frequency accuracy | operating; trimmed | −5 | - | +5 | % |
| $f_{osc}$ | oscillator frequency | internal oscillator; untrimmed | 130 | - | 250 | MHz |
| | | target frequency for trimmed operation | - | 180 | - | MHz |
| $t_{startup}$ | start-up time | EN = HIGH until SPI write access | - | - | 150 | µs |
| | | EN = HIGH until SPI read access | - | - | 2000 | µs |
| **Serial peripheral interface timing; pins CSB, SCLK, SDI and SDO** | | | | | | |
| $f_{clk(int)}/f_{SPI\_CLK}$ | internal clock frequency to SPI clock frequency ratio | | - | 20 : 1 | - | 1 |
| $t_{cy(clk)}$ | clock cycle time | | 250 | - | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | | 50 | - | - | ns |
| $t_{SPILAG}$ | SPI enable lag time | | 50 | - | - | ns |
| $t_{clk(H)}$ | clock HIGH time | | 125 | - | - | ns |
| $t_{clk(L)}$ | clock LOW time | | 125 | - | - | ns |
| $t_{su(D)}$ | data input set-up time | | 50 | - | - | ns |
| $t_{h(D)}$ | data input hold time | | 50 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | pin SDO; $C_L$ = 20 pF | - | - | 130 | ns |
| $t_{WH(S)}$ | chip select pulse width HIGH | | 250 | - | - | ns |
| **Gate driver** | | | | | | |
| $t_{ch(g)}$ | gate charge time | 20 % to 80 %; $V_{VGG}$ = 7.5 V; $C_{gate}$ = 2000 pF | - | - | 30 | ns |
| $t_{dch(g)}$ | gate discharge time | 80 % to 20 %; $V_{VGG}$ = 7.5 V; $C_{gate}$ = 2000 pF | - | - | 14 | ns |
| **Regulated voltage** | | | | | | |
| $t_{err(startup)}$ | start-up error time | of VGG; $f_{osc}$ = 180 MHz | - | 2.5 | - | ms |
| $t_{det(err)}$ | error detection time | for VGG during operation; $f_{osc}$ = 180 MHz | - | 31.5 | - | µs |
| $t_{fltr(Vo)}$ | output voltage filter time | for bit Vout1_ok and Vout2_ok; $f_{osc}$ = 180 MHz | - | 31.5 | - | µs |
| $t_{cal}$ | calibration time | bit VGG_ok = HIGH | - | - | 10 | ms |

[1]  All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

ASL4501SHN

**Product data sheet** Rev. 2 — 10 January 2018 35 of 43
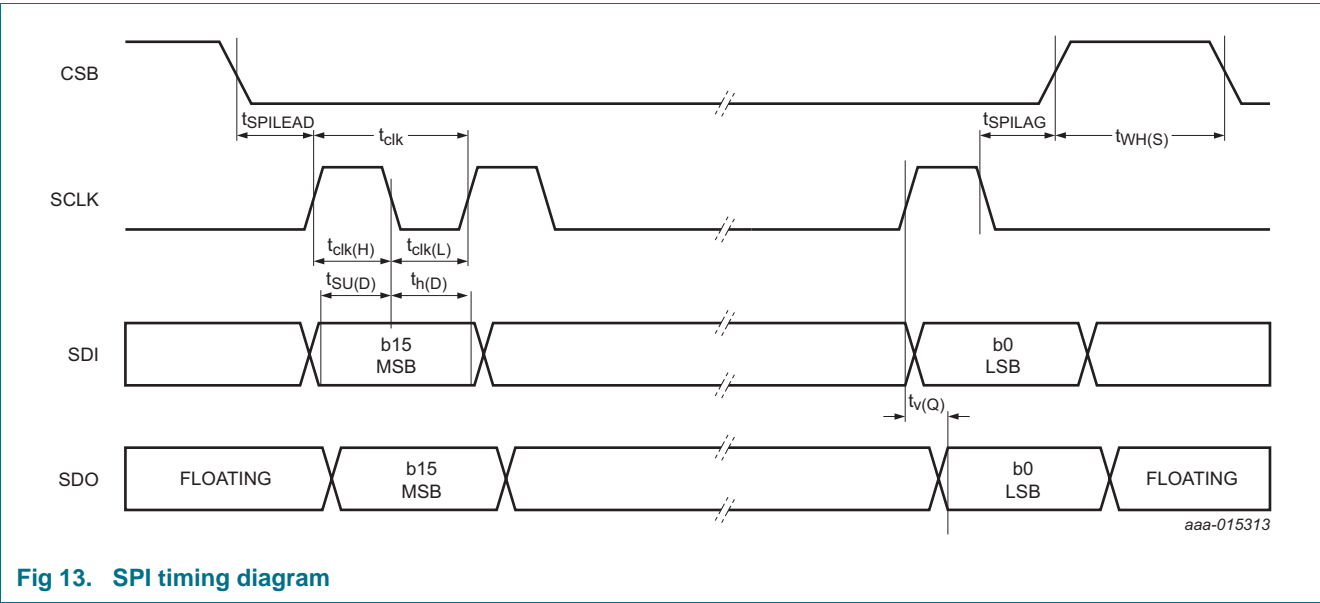
**Fig 13.  SPI timing diagram**

# 13. Application information

Figure 14 provides an application example for the ASL4501SHN in a typical four-phase boost converter IC with one output voltage.



**Fig 14. ASL4501SHN, configured as four-phase, single output boost converter**
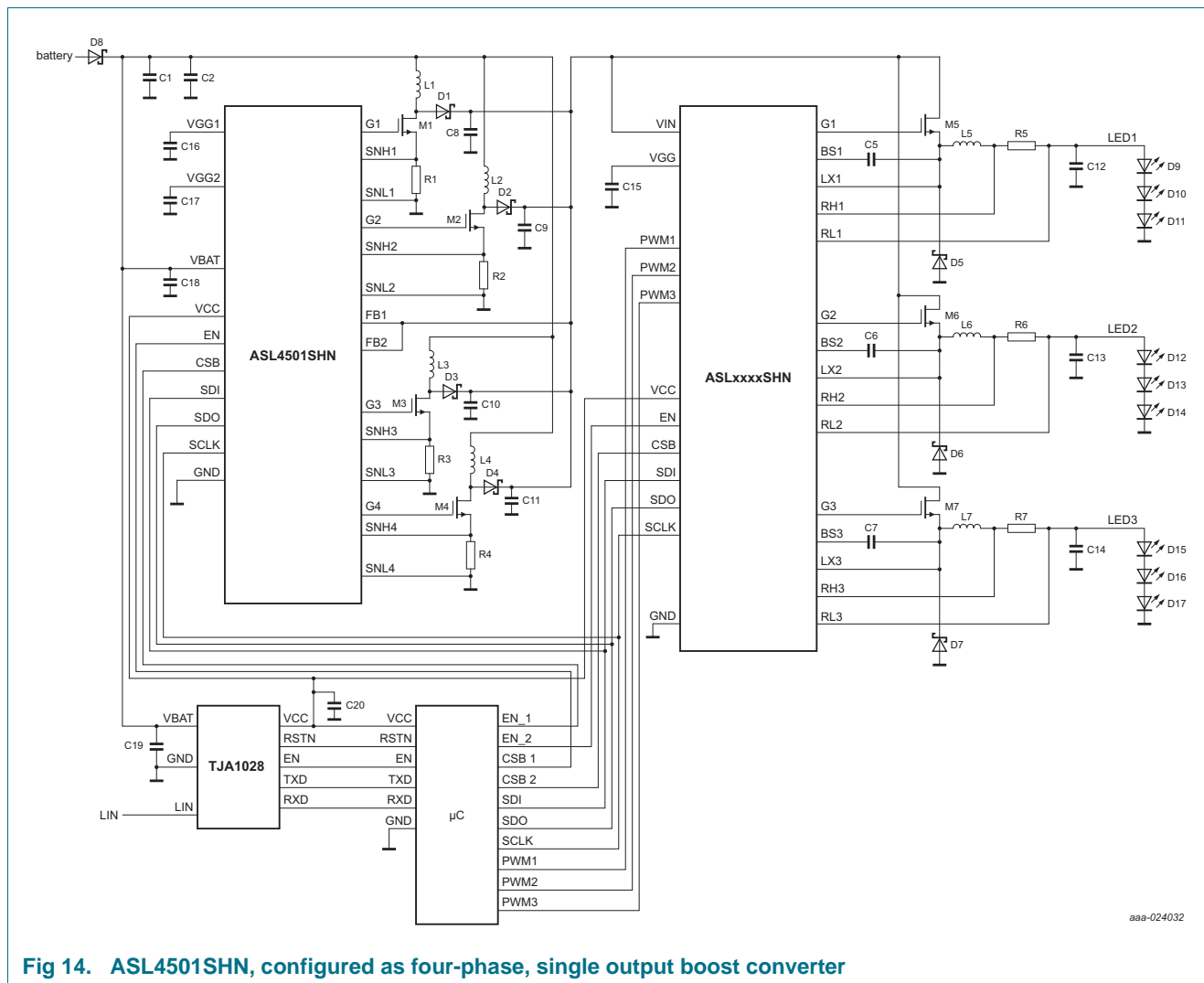
# 14. Test information

## 14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism-based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

37 of 43

## 15. Package outline

**HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;**
**32 terminals; body 5 x 5 x 0.85 mm**

SOT617-12



Dimensions (mm are the original dimensions)

| Unit | A | A₁ | b | c | D(1) | Dₕ | E(1) | Eₕ | e | e₁ | e₂ | k | L | v | w | y | y₁ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 5.1 | 3.1 | 5.1 | 3.1 | | | | | 0.50 | | | | |
| mm | nom | 0.85 | 0.02 | 0.21 | 0.2 | 5.0 | 3.0 | 5.0 | 3.0 | 0.5 | 3.5 | 3.5 | | 0.44 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 4.9 | 2.9 | 4.9 | 2.9 | | | | 0.5 | 0.30 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-12_po

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT617-12 | | MO-220 | | | | ~~13-10-14~~ 13-11-05 |

**Fig 15.  Package outline SOT617-12 (HVQFN32)**

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet** **Rev. 2 — 10 January 2018** **38 of 43**

## 16. Revision history

**Table 47.  Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| ASL4501SHN v.2 | 20180110 | Product data sheet | - | ASL4501SHN v.1 |
| Modifications: | • Updated formula for VGG setting: Table 30 "VGG control register (address 15h)" <br> • Updated formula for output voltage settings and input voltage measurements: <br>   – Table 18 "Output voltage 1 register (address 03h)" <br>   – Table 19 "Output voltage 2 register (address 04h)" <br>   – Table 20 "Limit voltage output 1 register (address 05h)" <br>   – Table 21 "Limit voltage output 2 register (address 06h)" <br>   – Table 31 "Battery voltage register (address 45h)" <br>   – Table 32 "Undervoltage threshold register (address 1Bh)" <br>   – Table 33 "Overvoltage threshold register (address 1Ah)" | | | |
| ASL4501SHN v.1 | 20170629 | Product data sheet | - | - |

ASL4501SHN

**Product data sheet** **Rev. 2 — 10 January 2018** **39 of 43**

# 17. Legal information

## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 17.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

ASL4501SHN

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2018. All rights reserved.

**Product data sheet**

**Rev. 2 — 10 January 2018**

**41 of 43**

## 19. Tables

## 20. Figures

## 21. Contents