Low Power PMIC With Integrated Linear Charger

BENEFITS and FEATURES

- **Wide Input Voltage Range**
  - 4V to 5.5V Input with 20V Protection
  - 2.7V to 4.5V Battery Range
- **Complete Integrated Power Solution**
  - Two 0.4A DC/DC Step-Down (Buck) Regulators
  - One 0.4A Buck-Boost Regulator
  - Three 100mA LDOs
  - Three 100mA Load Switches
  - One High Voltage Boost – 20V
  - 38mA Constant Current Sink LED Drive
  - 0.8A Linear Charger
- **Optimized Power for Portable Applications**
  - Active Power-Path Linear Charger (APLC)
  - Multiple Sleep Modes
  - Active-COT for Very Low Quiescent Current
  - 6µA Quiescent Current with 6 regulators and 3 load switches running
- **Space Savings**
  - Fully Integrated
  - Maximum Fsw = 3MHz for small size
  - Integrated Sequencing
- **Easy System Level Design**
  - Configurable Sequencing
  - Seamless Sequencing with External Supplies
  - Programmable Reset and Power Good GPIOs
- **Easy System Interface and Monitoring**
  - Four General Purpose I/O (4 X GPIOs)
  - I²C Serial Interface
  - Reset and Power Sequencing Control
  - Interrupt Controller and fault monitoring
  - Two configurable low power modes – SLEEP & DPSLP mode.
  - Watchdog Supervision
  - Hard/Soft Reset Functions
  - Multi-function Push button (PB) interface.
- **Highly Configurable**
  - uP interface for status and report and controllability
  - Flexible Sequencing and Fault Thresholds
  - Programmable GPIO Functions
  - GPIO/LED Current Sinks
  - Push Button Functionality (PB)
  - Contact Active Semi for PWREN Mode Startup

APPLICATIONS

- Consumer or medical wearables.
- Battery operated personal devices.
- IOT Modules.
- Cameras & DVRs

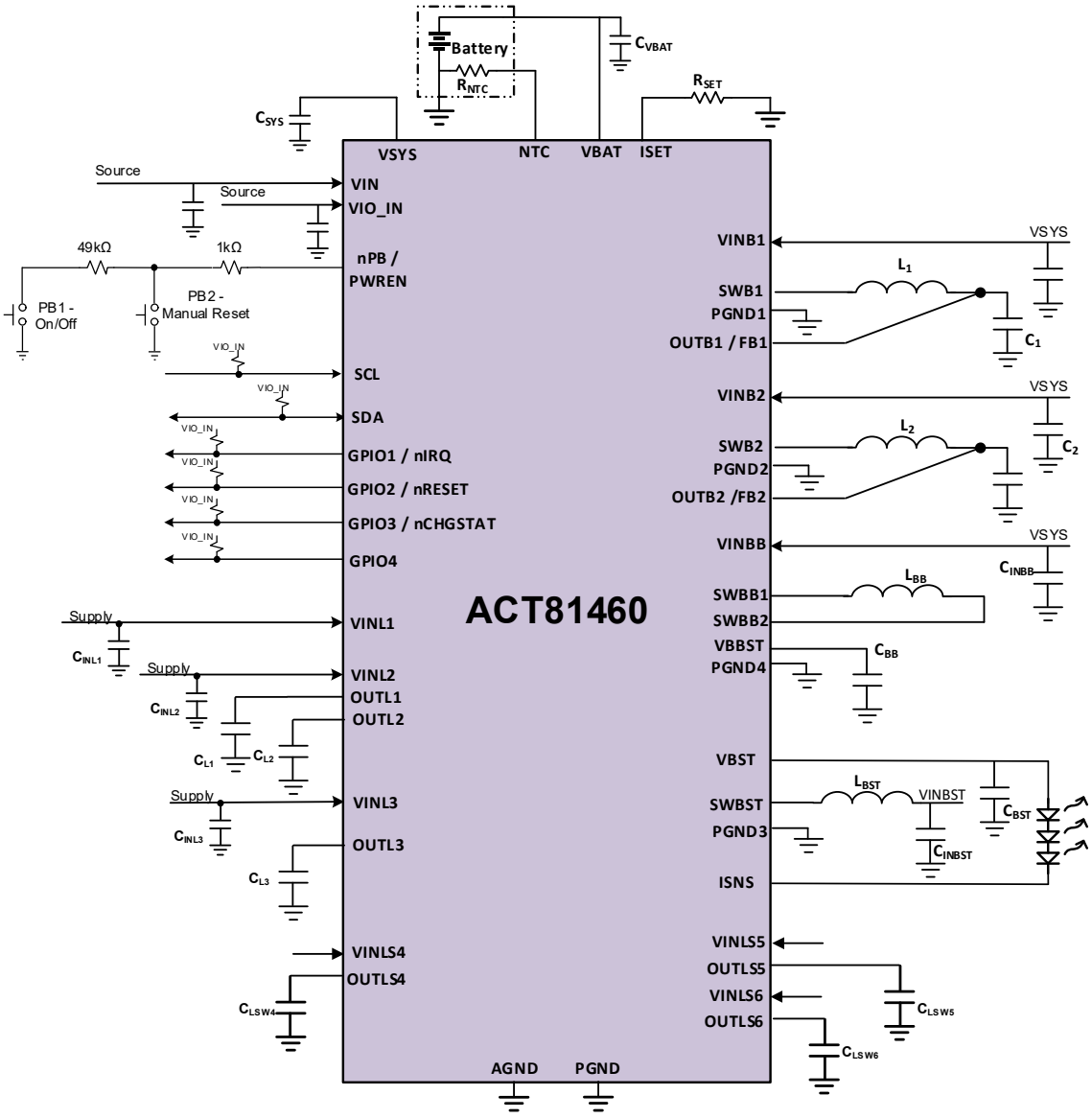
GENERAL DESCRIPTION

The ACT81460 is a low power PMIC (power management integrated circuit) that is specifically designed for battery operated systems and is suitable for a variety of processor applications. It features very low standby current that prolongs battery life between charges, especially in applications requiring long stand by or low power mode durations. It is a highly efficient PMIC that also enhances battery run time during normal operating modes. The number of regulators that can be turned OFF or left ON during low power modes is configurable and offers users flexibility to optimize system efficiency.

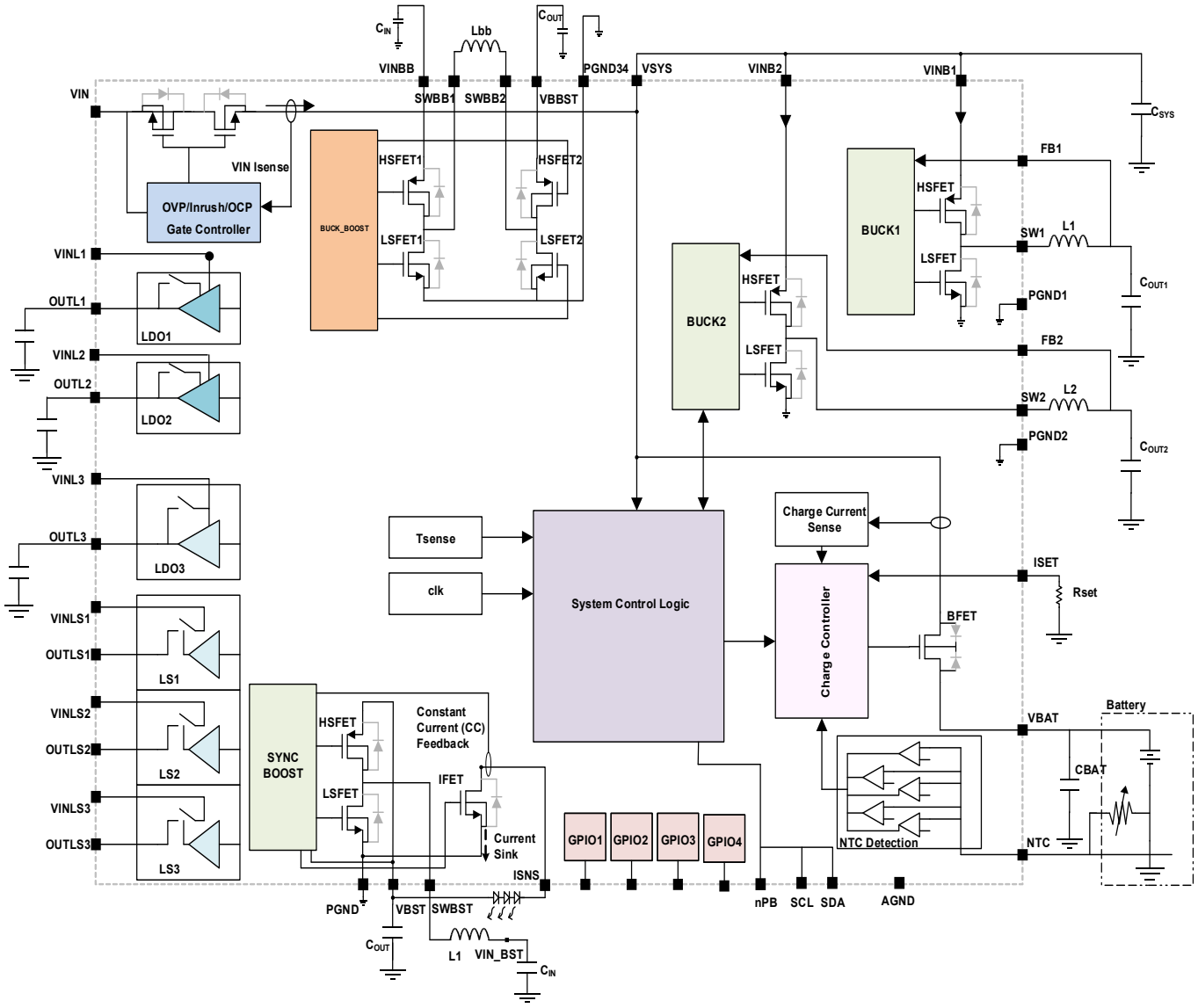
The IC includes four DC/DC converters with integrated power FETs, three low-dropout regulators (LDOs), and three load switches. Two of the DC/DC converters are step down buck regulators, one is a step up/down buck-boost regulator and the fourth is a high voltage step-up boost regulator capable of providing up to 20V. Each regulator can be configured for a wide range of output voltages through the I²C interface.

The ACT81460 is highly configurable. It offers configurable power sequencing combinations, startup timing, output voltage settings, fault monitoring, interrupt control, programmable GPIO options, and many more features. The device is pre-configured at the factory with default configuration settings that can be further adjusted though firmware via the standard I²C interface to suit individual system requirements. The IC also features the ability to sequence external power supply rails as part of the power up sequence by using GPIOs.

TYPICAL APPLICATION CIRCUIT

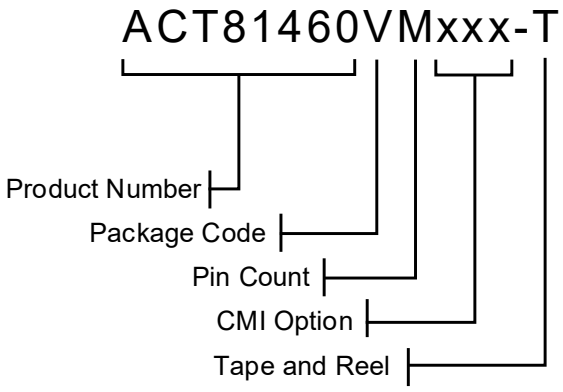


FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	V_{BUCK1}	V_{BUCK2}	V_{BUCK_BST}	V_{BOOST}	V_{LDO1}	V_{LDO2}	V_{LDO3}	Buck_Bst Mode	
ACT81460VM101-T	1.8V	1.2V	5.0V	12V (off)	3.2V	1.8V	1.2V	Boost	



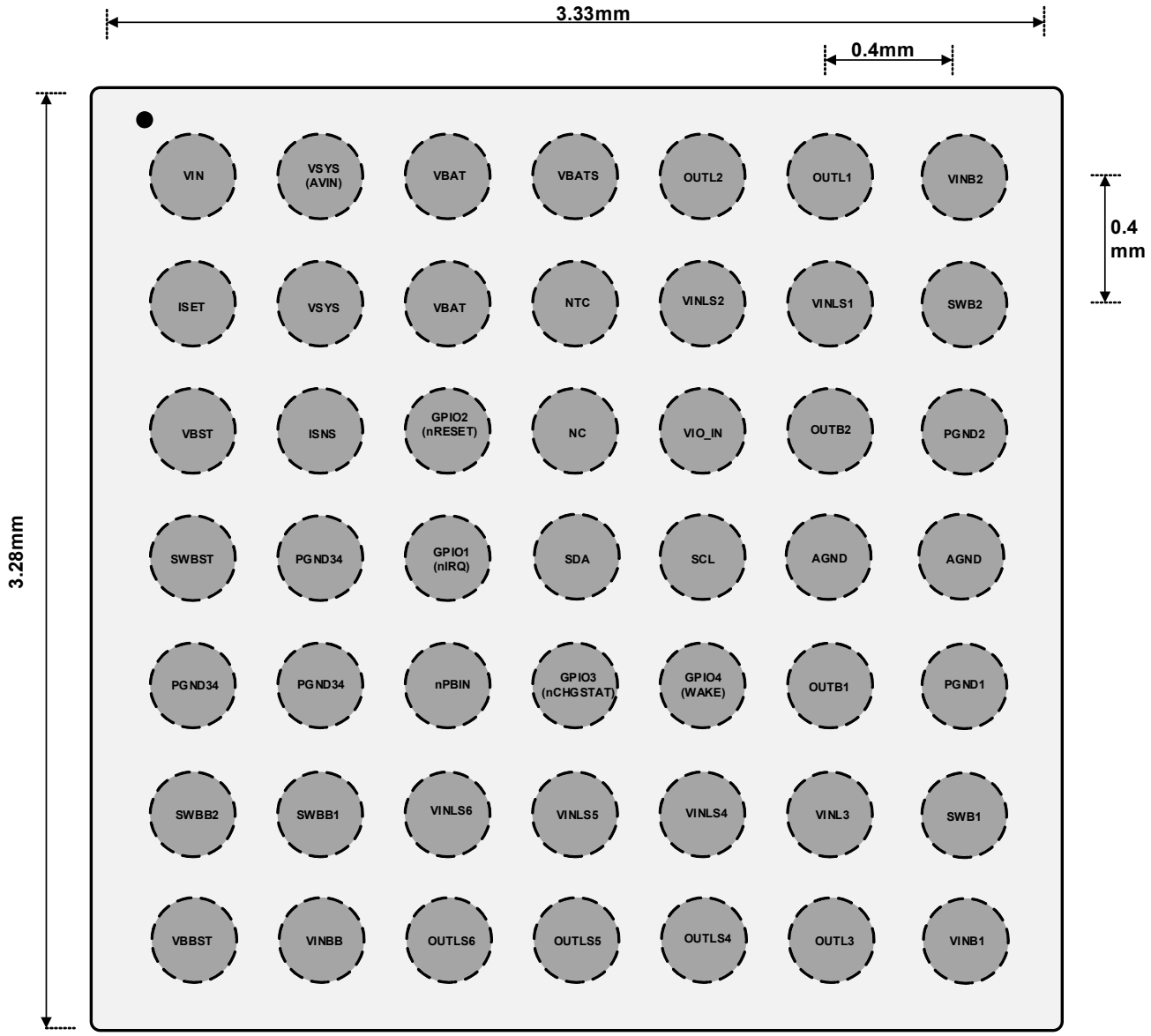
Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator "V" represents CSP

Note 4: Pin Count designator "I" represents 49 pins

PIN CONFIGURATION



Pin Configuration - Top View (bumps down): 49 Pin CSP

Figure 1: Pin Configuration – Top View – 49 Pin CSP (0.4mm pitch) 3.32mm x 3.27mm

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1	VIN	VIN power input
A2/B2	VSYS	System Voltage (system output of smart switch / linear charger). Input voltage to buck converters
A3/B3	VBAT	Charging Power Output pin. Positive side of battery connects to VBAT.
A4	VBATS	Sense Pin for Battery Voltage. Kelvin connect VBATS close the battery to sense the battery voltage.
A5	OUTL2	LDO2 output pin. This is also the LDO2 feedback pin.
A6	OUTL1	LDO1 output pin. This is also the LDO1 feedback pin.
A7	VINB2	Dedicated input pin for BUCK2
B1	ISET	Charge current setting pin. Connect a resistor from ISET to AGND to program the maximum charge current.
A2/B2	VSYS	System Voltage (system output of smart switch / linear charger). Input voltage to buck converters
A3/B3	VBAT	Charging Power Output pin. Positive side of battery connects to VBAT.
B4	NTC	Battery temperature sensing input. Connect a negative temperature coefficient thermistor from TH to AGND. This pin provides a constant current output and the voltage at this pin is used for temperature calculation.
B5	VINL2	Dedicated power input pin for LDO2
B6	VINL1	Dedicated power input pin for LDO1
B7	SW2	Switch pin for BUCK2
C1	VBST	Boost output pin
C2	ISNS	Back light LED current sense pin for Boost regulator
C3	GPIO2	GPIO2. Typically defined as nRESET, but can be configured for other functionality.
C4	NC	No Connection, this is floating so it can be tied to the adjacent VIO_IN or left floating
C5	VIO_IN	Digital Input Reference Voltage Input. Connect a 0.1uF ceramic capacitor between VIN_IN and AGND. Used for CMOS output reference voltage.
C6	FB_B2	Feedback pin for Buck2. Kelvin connect to the Buck2 output capacitors.
C7	PGND2	Power Ground pin for Buck2. The Buck2 input capacitor must be connected directly to PGND2.
D1	SWBST	Switch pin for Boost Regulator
D2	PGND34	Power Ground pin for the Buck-Boost and Boost. The Buck-Boost input and output capacitors must be connected directly to PGND34. The Boost output capacitors must be directly connected PGND34. All PGND34 pins must be connected together.
D3	GPIO1	GPIO1. Typically defined as nIRQ, but can be configured for other functionality
D4	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
D5	SCL	I^2C Clock Input. Needs an external pull up resistor.
D6	AGND	Analog Ground
D7	AGND	Analog Ground

E1	PGND34	Power Ground pin for the Buck-Boost and Boost. The Buck-Boost input and output capacitors must be connected directly to PGND34. The Boost output capacitors must be directly connected PGND34. All PGND34 pins must be connected together.
E2	PGND34	Power Ground pin for the Buck-Boost and Boost. The Buck-Boost input and output capacitors must be connected directly to PGND34. The Boost output capacitors must be directly connected PGND34. All PGND34 pins must be connected together.
E3	nPBIN	Push-Button Input Pin
E4	GPIO3	GPIO3. Typically configured as a charge status indicator, nCHGSTAT, but can be configured for other functionality
E5	GPIO4	GPIO4. Typically configured as a general input or output, but can be configured for other functionality.
E6	FB_B1	Feedback pin for Buck1. Kelvin connect to the Buck1 output capacitors.
E7	PGND1	Power Ground pin for Buck1. Buck1 input capacitors must be connected directly to PGND1.
F1	SWBB2	Switch pin 2 for Buck Boost
F2	SWBB1	Switch pin 1 for Buck Boost
F3	VINLS6	Input to Load Switch 6
F4	VINLS5	Input to Load Switch 5
F5	VINLS4	Input to Load Switch 4
F6	VINL3	Dedicated input power pin to LDO3.
F7	SW1	Switch pin for Buck 1
G1	VBBST	Output and feedback pin for Buck Boost (BBST) regulator
G2	VINBB	Dedicated input power pin to the Buck Boost regulator
G3	OUTLS6	Output of Load Switch 6
G4	OUTLS5	Output of Load Switch 5
G5	OUTLS4	Output of Load Switch 4
G6	OUTL3	Output and feedback pin for LDO3
G7	VINB1	Dedicated input power to pin to BUCK1

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

PARAMETER	VALUE	UNIT
All Pins to GND unless stated otherwise below	-0.3 to 6.0	V
nPBIN/PWREN, GPIO 1,2,3 (nIRQ, nRESET, nCHGSTAT), ISET, NTC	-0.3 to 6.0	V
VIN to PGNDx	-0.3 to 22.0	V
VSYS(AVIN), VBAT, VINLx, VINLSx, VINBx, VINBB to PGNDx	-0.3 to 6.0	V
OUTLS1,2,3 & OUTL1,2,3	-0.3 to VSYS voltage	V
VBBST	-0.3 to 6.0	V
SWBBx to PGNDx	-1.0 to VBBST + 1.0	V
VBST	-0.3 to 21	V
SWBST to PGNDx	-1.0 to VBST + 1.0	V
VIN_IO	-0.3 to 6.0	V
ISNS to PGNDx	-0.3 to VBST	V
FBx to PGNDx	-0.3 to VINBx	V
SWx to PGNDx	-1.0 to VINBx + 1	V
AGND, PGNDx	-0.3 to + 0.3	V
Junction to Ambient Thermal Resistance (Note 2)	40	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C

Note1: Do not exceed these limits to prevent damage to the IC. Exposure to absolute maximum rating conditions for long periods may affect IC reliability.

Note2: Measured on Active-Semi Evaluation Kit

ESD RATINGS

PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_ESD_HMB (All pins)	Human body Model per JEDEC JS-001	+/- 2000	V
V_ESD_CDM (All pins)	Charged device model per JEDEC JS-002	+/- 1000	V

SYSTEM CHARACTERISTICS

(VIN = 5V, VSYS = 3.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN Input Voltage	Charger Input	4.0		20	V
VIN Input UV Threshold, rising	Charger Input UV		3.8	4.0	V
VIN Input UV Threshold, hysteresis		0.1	0.2	0.3	V
VIN Input UV detection deglitch time		75	100	125	µs
VIN Input OV Threshold, rising	Charger Input OV		5.8		V
VIN Input OV Threshold, hysteresis		0.2	0.3	0.4	V
VIN Input OV detection deglitch time		150	200	250	µs
VIN OCP threshold level	Over current threshold (Configurable: 0.5/1/1.5/2A)	0.5	1	2.0	A
VSYS Voltage Ramp time	Soft Start time, V_{SYS}, C_{SYS} < 100 µF.	400	500	700	µs
System Voltage Range		2.7		5.7	V
VINL1,2 referenced to AGND		1.5		VSYS	V
VINL3 referenced to AGND		1.2		VSYS	V
VINLS4,5,6 referenced to AGND		0.8		VSYS	V
VSYS POR Level, Rising	IC Powers up at this voltage		1.4		V
VSYS POR Level, Rising	IC Powers down at this voltage		1.2		V
VSYS UVLO Threshold Falling		2.34	2.5	2.66	V
VSYS UVLO Hysteresis	Voltage above the UVLO Falling Threshold, above which all regulators turn on (device powers up)	75	100	150	mV
VSYS UV Warning Interrupt Threshold Falling	Configurable in 100mV steps from 1.85V to 3.35V Must be set above the VSYS UVLO Falling Threshold plus the Hysteresis	-0.2	Nominal	+0.2	V
VSYS UV Warning Interrupt Hysteresis	Voltage Rising	0.1	0.2	0.3	V
VSYS OV Threshold Rising	Overvoltage Set Point	5.5	5.7	5.9	V
VSYS OV Hysteresis	Voltage Falling	100	200	300	mV
VSYS UV Deglitch Time		80	100	120	µs

VSYS OV Deglitch Time		160	200	240	µs
Operating Supply Current	All regulators enabled but no load, boost regulator is disabled. Charger off, power supplied from VSYS.		6	8	µA
Operating Supply Current	LDO1 enabled but no load. BUCK1/2, Buck-boost, Boost, and Charger disabled. Battery FET enabled and supplied from VBAT. References and monitors enabled.		2.1	2.6	µA
Operating Supply Current	LDO1 and one BUCK regulator enabled with no load. Charger disabled. Power supplied from VSYS. References and monitors enabled.		2.7	3.2	µA
Thermal Low Power Threshold			70		°C
Thermal Warning Temperature	Temperature rising.	115	125	135	°C
Thermal Shutdown Temperature	Temperature rising.	140	155	170	°C
Thermal Shutdown Hysteresis			25		°C
Power Up Delay after initial VSYS	Time from VSYS > UVLO threshold to Internal Power-On Clear (POR)			5	ms
Startup Delay after initial VSYS	Time from VSYS > UVLO threshold to start of first regulator turning On.			10	ms
Transition time from Sleep State (SLEEP) to Active State	Time from I2C command to clear sleep mode to time when the first regulator turns ON with minimum turn on delay configuration.		90		µs
Turn Off Delay	Time from turn off event to when the first power rail turns off with minimum turn off delay configuration.		56		µs
Regulator Startup Delay Programmable Range between turn on events.	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111		0 0.5 1 2 5 10 15 20		ms
Regulator Turn Off Delay Programmable Range	Configurable in 4ms steps	0		60	ms
nRESET, Delay Timing	Configurable to 20, 40, 60 or 100ms.	20		100	ms

BUCK1 AND BUCK2 ELECRICAL CHARACTERISTICS

(VSYS = 3.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.7		5.5	V
Output Operating Voltage Range	Configurable in 50mV steps (Note 1)	0.6		3.6	V
Maximum Output Current	(Note 1)	0.4			A
Standby Supply Current, Low Power Mode Enabled	V_{OUTBx} >= 103% of setpoint, Regulator Enabled, V_{OUTBx} = 1.2V, No Load		0.6	0.8	µA
Shutdown Current	Regulator Disabled			0.1	µA
Output Voltage Accuracy	V_{OUTBx} > 1.2V, I_{OUT} = 0.4A (PWM mode)	-3	V_{NOM}	3	%
	V_{OUTBx} =< 1.2V, I_{OUT} = 0.4A (PWM mode)	-36	V_{NOM}	36	mV
	V_{OUTBx} > 1.2V, I_{OUT} = 1mA (PFM mode)	-4	V_{NOM}	4	%
	V_{OUTBx} =< 1.2V, I_{OUT} = 1mA (PFM mode)	-48	V_{NOM}	48	mV
	V_{OUTBx} > 1.2V, I_{OUT} < 0.01mA (LPM on)	-5	V_{NOM}	5	%
	V_{OUTBx} =< 1.2V, I_{OUT} < 0.01mA (LPM on)	-60	V_{NOM}	60	mV
Line Regulation	V_{IN_B1} = 3.0V to 5.0V, 200mA, PWM Regulation. (Note 2)		0.08		%/V
Load Regulation	PWM mode, 0.1A to 0.4A. (Note 2)		0.1		%/A
Power Good Threshold	V_{OUTBx} Rising, relative to regulation point	88	92	96	$\%V_{NOM}$
Power Good Hysteresis	V_{OUTBx} Falling, relative to regulation point		3		$\%V_{NOM}$
Switching Frequency, PWM Mode	Freq = 00, VIN = 3.6V, V_{OUTB1} = 1.8V. V_{OUTB2} = 1.2V, Note [1]		1.5		MHz
	Freq = 01, VIN = 3.6V, V_{OUTB1} = 1.8V. V_{OUTB2} = 1.2V, Note [1]		2.0		MHz
	Freq = 10, VIN = 3.6V, V_{OUTB1} = 1.8V. V_{OUTB2} = 1.2V, Note [1,2]		2.5		MHz
	Freq = 11, VIN = 3.6V, V_{OUTB1} = 1.8V V_{OUTB2} = 1.2V, Note [1,2]		3.3		MHz
Soft-Start Ramp	10% to 90% V_{NOM}		2.5		V/ms
T_{start}, Time from EN to POK	Time from enable to POK (92% VNOM)				µs

	Buck1 = 1.8V Buck2 =1.2V		3100 3500		
Current Limit, Cycle-by-Cycle (accuracy is valid at a CMI's default setting)	ILIM_SET = 0		0.6		A
	ILIM_SET = 1		1.2		A
Current Limit, Warning	2 consecutive switching cycles of 125% of cycle-by-cycle current limit.		125		%
Current Limit, Shutdown	8 consecutive switching cycles of 125% of cycle-by-cycle current limit.		125		%
PMOS On-Resistance	I_{SW} = -0.2A, V_{IN} = 5.0V		250		mΩ
NMOS On-Resistance	I_{SW} = 0.2A, V_{IN} = 5.0V		200		mΩ
SW Leakage Current	V_{IN} = 5.5V, V_{SW} = 0 or 5.5V, T_j < 60^{O}C			0.1	μA
Dynamic Voltage Scaling Rate			5		mV/us
Output Pull Down Resistance	Pull Down Enabled when the regulator is turned off. V_{OUTBX} = 0.1.	32		50	Ohms
Recommended Max Duty Cycle			85		%

Note1: L = 1uH, DCR = 80 mΩ, $C_{OUT\_effective}$ =10uF. If the user desires different VOUT configurations, from the default CMI, they should consult with active-semi Applications staff for proper setup of the device. Default CMI is what sets the output voltages of the regulators on POR event. Parts can be ordered with different CMI settings, to fit the specific customer output voltages in the application.

Note2: For heavy loads and high frequency settings, may need to use different VFFResSelect [2:0] setting for a stable switching frequency. Load may be limited when above 200mA, in order to keep the switch pin at a stable frequency Please consult with Applications for proper setup of different frequencies, and different output voltage settings.

BUCK-BOOST ELECTRICAL CHARACTERISTICS

(VSYS = 3.6V, Fsw = 2MHz, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VINBB, Operating Voltage Range		2.7		5.5	V
VBBST, Output Voltage Range	Configurable in 50mV steps	3.2		5.0	V
IBBST, Maximum Output Current	VBBST >= 4.2V	250			mA
	VBBST < 4.2V, (Note 1)	400			mA
No Load Input Current	VBBST = 5V, No Load		0.9	1.2	µA
Shutdown Current	Regulator Disabled			0.1	µA
Output Voltage Accuracy	I_{OUT} = 100mA (PWM), BB Mode	-3	V_{NOM}	3	%
	I_{OUT} = 1mA, BB Mode	-5	V_{NOM}	5	%
Line Regulation	V_{BBST} = 5V, V_{INBB} = 3.0V to 5.0V, 100mA, PWM Regulation. (Note 2)		0.03		%/V
Load Regulation	V_{BBST} = 5V, PWM Regulation, (Note 1)		0.4		%/A
Power Good Threshold	VBBST Rising	88	92	96	%VNOM
Power Good Hysteresis	VBBST Falling		3		%VNOM
Overvoltage Fault Threshold	VBBST Rising	105	110	115	%VNOM
Overvoltage Fault Hysteresis	VBBST Falling		3		%VNOM
Switching Frequency, PWM Mode	V_{INBB} = 3.6V, V_{BBST} = 5.0V. (Note 1,Note 3) Freq = 00 Freq = 01 Freq = 10 Freq = 11		 3.3 2.5 2.0 1.5		MHz
Soft-Start Period T_{SS}	10% to 90% V_{BBST} ramp time (Note 1)		800	1200	µs
T_{start}, Time from EN to PG	Time from enable to PGOOD / POK.		1500		µs
Current Limit, Cycle-by-Cycle	VBBST > 4.2V		0.85		A
	VBBST <= 4.2V, (Note 2)		1.2		A
Current Limit, Warning	2 consecutive switching cycles at 125% of cycle-by-cycle current limit.		125		%

Current Limit, Shutdown	8 consecutive switching cycles of 125% of cycle-by-cycle current limit.		125		%
VINBB to SWBB1 (HSFET1) Resistance	I_{SW} = -0.2A, V_{BBST} = 5.0V, T_j = 25^{O}C		210		mΩ
SWBB1 to PGND (LSFET1) Resistance	I_{SW} = 0.2A, V_{BBST} = 5.0V, T_j = 25^{O}C		185		mΩ
VBBST to SWBB2 (HSFET2) Resistance	I_{SW} = -0.2A, V_{BBTS} = 5.0V, T_j = 25^{O}C		170		mΩ
SWBB2 to PGND (LSFET2) Resistance	I_{SW} = 0.2A, V_{BBST} = 5.0V, T_j = 25^{O}C		170		mΩ
SWBB1 and SWBB2 Leakage Current	V_{SYS} = 5.5V, SWBB1 = SWBB2 = 0 or 5.5V			0.1	µA
Output Pull Down Resistance	Pull Down Enabled when the regulator is turned off. VBBST = 0.1V.	32		50	Ohms

Note 1: L = 2.2uH, DCR 80 mΩ, $C_{OUT\_effective}$ = 10uF. If the user desires different VOUT configurations from the default CMI, contact active-semi. Default CMI is what sets the output voltages of the regulators on POR event. Parts can be ordered with different CMI settings, to fit the specific customer output voltages in the application.

Note 2: Depends on ordering options (vout, ilim, etc), and external inductor selection.

Note 3: Device needs to be tuned for these frequencies. Contact active-semi for a different default operating frequencies or voltage.

BOOST ELECTRICAL CHARACTERISTICS

(VSYS = 3.6V, VBOOST = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{INBOOST}$, Operating Voltage Range		3.0		V_{SYS_OV}	V
VBST Programmable Output Voltage Range	Configurable in 250mV steps, VSET [5:0]	5.0		20.75	V
ISNS Programmable Boost Current Range	Constant current mode; 0.625mA per step across entire range	0.625		39.375	mA
ISNS Boost Current Accuracy	At default CMI setting.	-2		2	%
ISNS Voltage	Constant Current sense voltage		0.25		V
ISNS Programmable LED Current Sink Range	DISCC = 1, Disable CC mode and ISNS pin configured as a constant current sink. 0.625mA per step across the entire range.	0.625		39.375	mA
I_{VBST}, Maximum Output Current	Continuous boost output current, VBST=12V			39.375	mA
	Continuous boost output current, VBST=20V			32	mA
Standby Supply Current, Low Power Mode Enabled	VBST >= 103% of Nominal Voltage, Regulator Enabled, VBST = 12.0V, No Load		373		µA
Shutdown Current	Regulator Disabled		0.12		µA
Output Voltage Accuracy	VBST =12.0V, I_{OUT} = 0.02A	-3	V_{NOM}	3	%
Line Regulation	VBST = 12.0V, VSYS = 3.0V to 5.0V. 20mA (Note 1)		0.01		%/V
Load Regulation	VBST = 12.0V, I_{Boost} 2.0mA to 20mA. (Note 1)		0.005		%/mA
Power Good Threshold	VBST Rising	65	70	75	%VNOM
Power Good Hysteresis	VBST Falling		3		%VNOM
Overvoltage Fault Threshold	VBST Rising	105	110	115	%VNOM
Overvoltage Fault Hysteresis	VBST Falling		3		%VNOM
Switching Frequency, PWM Mode	VBST = 12.0V, I_{Boost} = 20mA, (Note 1)		1.125		MHz
Soft-Start Period T_{SS}	10% to 90% of setpoint. (Note 1)		80		ms
T_{start}, Time from EN to POK	70% of setpoint. (Note 1)		80		ms

Current Limit, Cycle-by-Cycle	LSILIM = 0 LSILIM = 1		1.0 1.35		A A
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	70	80	90	%
VBST to SWBST (HSFET) Resistance	I_{SWBST} = -0.2A, V_{SYS} = 5.0V, VBST = 5.0V, T_j < 85^{O}C		400		mΩ
SWBST to PGND (LSFET) Resistance	I_{SWBST} = 0.2A, V_{SYS} = 5.0V, VBST = 5.0V, T_j < 85^{O}C		250		mΩ
SWBST Leakage Current	V_{SWBST} = 20V, V_{SYS} = 3.6V			1	μA

Note1: L = 2.2uH, DCR = 10mΩ, C = 10uF

LDO1 AND LDO2 ELECTRICAL CHARACTERISTICS

(VINL1 =VINL2 = 3.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range	VINL1,2 (Input Voltage) to LDO1,2	1.5		VSYS	V
Output Voltage Programmable Range	Configurable in 50mV steps	0.6		3.6	V
Output Current	$V_{OUTL1,2}$ < VINL1,2 – 0.25V	100			mA
Output Voltage Accuracy	1.2V < $V_{OUTL1,2}$ < VINL1,2 – 0.25V	-3	V_{NOM}	3	%
	0.6V < $V_{OUTL1,2}$ < 1.2V	-36	V_{NOM}	36	mV
Line Regulation	VINL1,2 - $V_{OUTL1,2}$ > 0.25V, VINL1,2= 2.7V to VSYS. $I_{LDO1,2}$ = 10mA. (Note 2)		0.02		%/V
Load Regulation	I_{LDO1} = 1mA to 100mA		2.0		%/A
Power Supply Rejection Ratio	f = 1kHz, I_{LDO1} = 10mA		59.6		dB
	f = 10kHz, I_{LDO1} = 10mA		55.5		dB
	f = 2.25MHz, I_{LDO1} = 10mA		10.6		dB
I_{q1}, Supply Current	Regulator Enabled, no load, UV/OV and Current Limit Monitors are OFF.		0.4	0.5	µA
I_{q2}, Supply Current	Regulator Enabled, no load, UV/OV and Current Limit Monitors are ON.		0.5	0.6	µA
Soft-Start Ramp Rate			1.7		V/ms
Power Good Threshold	$V_{OUTL1,2}$ Rising	88	92	96	% V_{NOM}
Power Good Hysteresis	$V_{OUTL1,2}$ Falling		3		% V_{NOM}
Overvoltage Fault Threshold	$V_{OUTL1,2}$ Rising	105	110	115	% V_{NOM}
Overvoltage Fault Hysteresis	$V_{OUTL1,2}$ Falling		3		% V_{NOM}
Discharge Resistance	$V_{OUTL1,2}$ = 0.1V			80	Ω
Dropout Voltage	$I_{LDOL1,2}$ = 50mA,			100	mV
Output Current Limit	$V_{INL1,2}$ = 1.5V to VSYS	120			mA
T_{start}, Time from EN to POK	70% of setpoint. V_{OUTL1} = 3.2V V_{OUTL2} = 1.8V		 2300 1500		µs

LDO3 ELECTRICAL CHARACTERISTICS

(VINL3 = 3.6V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range	VINL3 (Input Voltage) to LDO3	1.2		VSYS	V
Output Voltage Programmable Range	Configurable in 50mV steps	0.6		3.6	V
Output Current	$V_{OUTL3} < V_{INL3} - 0.25V$, $V_{INL3} > 1.5V$	100			mA
Output Current	$V_{OUTL3} < V_{INL3} - 0.25V$, $1.5V > V_{INL3} > 1.2V$	40			mA
Output Voltage Accuracy	$1.2V < V_{OUTL3} < V_{INL3} - 0.25V$ $0.65V < V_{OUTL3} < 1.2V$	-3 -36	V_{NOM} V_{NOM}	3 36	% mV
Line Regulation	$V_{OUTL3} < V_{INL3} - 0.25V$, V_{INL3} = 1.5V to V_{SYS}, I_{LDO3} = 10mA.		0.02		%/V
Load Regulation	I_{LDO3} = 1mA to 100mA.		3.0		%/A
Power Supply Rejection Ratio	f = 1kHz, I_{LDO3} = 10mA,		64		dB
	f = 10kHz, I_{LDO3} = 10mA		56.9		dB
	f = 2.25MHz, I_{LDO3} = 10mA		13.9		dB
Supply Current per Output	Regulator Disabled			0.1	µA
I_{q1}, Supply Current	Regulator Enabled, no load, UV/OV and Current Limit Monitors are OFF.		0.4	0.5	µA
I_{q2}, Supply Current	Regulator Enabled, no load, UV/OV and Current Limit Monitors are ON.		0.5	0.6	µA
Soft-Start Period	Time from soft start “ON” to PGOOD		1000		µs
Power Good Threshold	V_{OUTL3} Rising	88	92	96	% V_{NOM}
Power Good Hysteresis	V_{OUTL3} Falling		3		% V_{NOM}
Overvoltage Fault Threshold	V_{OUTL3} Rising	105	110	115	% V_{NOM}
Overvoltage Fault Hysteresis	V_{OUTL3} Falling		3		% V_{NOM}
Discharge Resistance	V_{OUTL3} = 0.1V			80	Ω
Dropout Voltage	I_{OUT3} = 50mA, V_{OUT3} = 1.2V			140	mV
Output Current Limit	V_{INL3} = 1.5V to VSYS	120			mA
T_{start}, Time from EN to POK	70% of setpoint.		1100		µs

ACTIVE PATH LINEAR CHARGER (APLC) ELECTRICAL CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN Input Voltage		4.0		20	V
VIN Input UV Threshold, rising			3.8	4.0	V
VIN Input UV Threshold, hysteresis		0.1	0.2	0.3	V
VIN Input UV detection deglitch time		75	100	125	µs
VIN Input OV Threshold, rising		5.5	5.7	5.9	V
VIN Input OV Threshold, hysteresis		0.2	0.3	0.4	V
VIN Input OV detection deglitch time		75	100	125	µs
VIN OCP threshold level (current limit threshold)	IINSET [1:0] = 00 IINSET [1:0] = 01 IINSET [1:0] = 10 IINSET [1:0] = 11	0.45 0.9 1.35 1.7	0.55 1.0 1.5 1.9	0.55 1.1 1.65 2.1	A
VSYS Voltage Ramp time	Soft Start time, VSYS, C_{SYS} < 100 µF	400	500	700	µs
System Voltage Range: VSYS referenced to AGND		2.7		5.7	V
VSYS regulation voltage			4.8		V
VIN to VSYS Resistance	I_{VSYS} = 0.2A		160	200	mΩ
VSYS to VBAT (BFET) Resistance	VBAT = 3.6V, I_{SYS} = 0.2A		100	125	mΩ
VIN supply current	Charge disabled, I_{VSYS} = 0mA CHG_EN bit = 0		0.75	0.9	mA
VIN supply current	Charge enabled, I_{VSYS} = 0mA, I_{CHG} = 0 CHG_EN bit = 1		0.95	1.1	mA
VBAT supply current	VIN = 0V, I_{VSYS} = 0mA, BFET enabled. ILIM Disabled. VSYS powered from VBAT.		0.3	0.5	µA
VBAT supply current	VIN = 0V, Regulators disabled, References and VSYS monitors are On, BFET enabled. VSYS powered from VBAT.		1.4	1.7	µA
ISET pin voltage	VIN = 5.0V, VSYS – VBAT > 100mV			1.2	V

	ISET voltage is proportional to ICHRG, ISET max in CC.				
RSET, Allowable external resistor range	RSET sets the ISET pin current	1.2		15	kΩ
Charge Programmable Current Range	RSET resistor sets the ISET pin current and the charge current.	10		800	mA
ISET current ratio	VBAT = 3.8V, ICHG/ISET Ratio. ICHG < 200mA		10000		
Charge current accuracy	VBAT = 3.8V, ICHG at default charge current setting.	-10		+10	%
IPRE, Precondition Charge Current	IPRE is a percentage of ICHG (fast charge) IPRESET [1:0] = 00 IPRESET [1:0] = 01 IPRESET [1:0] = 10 IPRESET [1:0] = 11		 20 15 10 5		 % % % %
Precondition Voltage Threshold, VPRE, Programmable Range	Configure by VPRESET [3:0], 50mV step size	2.7		3.45	V
Precondition Voltage Threshold Hysteresis			0.1		V
Termination Voltage Threshold, VTERM, Programmable Range (Note 1)	Configure by VTERM [4:0], 20mV step size	3.9	4.4	4.5	V
Termination Voltage Threshold, VTERM, accuracy (Note 1)	Configure by VTERM [4:0], 20mV step size	-1	VTERM	1	%
Termination Current Threshold, ITERM (Note 1)	Percentage of IFCHG ITERM [1:0] = 00 ITERM [1:0] = 01 ITERM [1:0] = 10 ITERM [1:0] = 11		 20 15 10 5		 % % % %
Charge Restart Threshold	BAT_RECHG_THRESHOLD = 00 BAT_RECHG_THRESHOLD = 01 BAT_RECHG_THRESHOLD = 10 BAT_RECHG_THRESHOLD = 11		80 120 160 200		mV mV mV mV
Fast charge safety timer			12000		s
Precondition charge safety timer			4000		s
Thermal regulation threshold	Temperature range were charge current is proportionally reduced.	95	115	150	˚C
NTC pin pull up current	VBAT = 3.8V, NTC = 10kΩ resistor to AGND.		100		μA

NTC 60^0C Detection Voltage, V_{NTC}			0.300		V
NTC 60^0C Hysteresis			30		mV
NTC 50^0C Voltage Detection			0.416		V
NTC 50^0C Hysteresis			40		mV
NTC 45^0C Voltage Detection			0.492		V
NTC 45^0C Hysteresis			50		mV
NTC 10^0C Voltage Detection			1.792		V
NTC 10^0C Hysteresis			200		mV
NTC 0^0C Voltage Detection			2.720		V
NTC 0^0C Hysteresis			300		mV

Note1: For end of charge accuracy, (Bat_ESR*EOC Current) should be greater than 1mV

LOAD SWITCH 4,5,6 ELECTRICAL CHARACTERISTICS

(VSYS = 3.6V, VINLSx = 1.2V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	$V_{INLS456}$ (Input Voltage) to the LS4,5,6 EN_LSW_ILIM_COMPS=0	0.6		VSYS	V
Output Voltage Range	$V_{INLS456}$ (Input Voltage) to the LS4,5,6 EN_LSW_ILIM_COMPS=0	0.6		VSYS	V
Operating Input Voltage Range Current limit enabled normal range	$V_{INLS456}$ (Input Voltage) to the LS4,5,6 EN_LSW_ILIM_COMPS =1 EN_LOWVIN_ILIM_MODE = 0	0.8		VSYS	V
Operating Input Voltage Range Current limit enabled low vin range	$V_{INLS456}$ (Input Voltage) to the LS4,5,6 EN_LSW_ILIM_COMPS =1 EN_LOWVIN_ILIM_MODE = 1	0.6		VSYS-0.7	V
Maximum Output Current		100			mA
Current Limit voltage detection threshold (VINLS456 – VOUTL456)	$V_{OUTLS456}$ > 1.2V ILIM SET56[1:0] = 00 ILIM SET56[1:0] = 01 ILIM SET56[1:0] = 10 ILIM SET56[1:0] = 11	 35 75 125 175	 50 100 150 200	 65 125 175 225	 mV mV mV mV
Load Switch Resistance LSW4, LSW5 and LSW6	VINLS456 = 1.2V, $I_{VINLS456}$ = 50mA VSYS=3.6V		250	320	mΩ
Load Switch Resistance Load Switch Mode for LDO3	VINL3 = 1.2V, I_{OUTL3} = 50mA VSYS=3.6V		300	380	mΩ
Soft-start slew rate	Output start from 0 to 1.2V VSYS=3.6V, 10 – 90% measurement.		100		µs
Current limit deglitch time	Minimum time for current limit signal to be valid. (Note 1)	10			µs
Output Discharge Resistance	VSYS = 3.6V, $V_{OUTLS456}$ = 0.1V.			90	Ω
Startup Delay	Time from Enable to PG			1000	µs
Iq1, Total Current Condition 1	VSYS=3.6V, VIN=1.2V I_{SYS}+$I_{VINLS456}$ with no load current EN_LSW_ILIM_COMPS =0 EN_LOWVIN_ILIM_MODE = x		40		nA
Iq2, Total Current Condition 2	VSYS=3.6V, VIN=1.2V I_{SYS}+$I_{VINLS456}$ with no load current EN_LSW_ILIM_COMPS =1		225		nA

	EN_LOWVIN_ILIM_MODE = 0				
Iq3, Total Current Condition 3	VSYS=3.6V, VIN=1.2V I_{SYS}+$I_{VINLS456}$ with no load current EN_LSW_ILIM_COMPS =1 EN_LOWVIN_ILIM_MODE = 1		225		nA
Iq4, Total Current Condition 4	VSYS=3.6V, VIN=1.2V I_{SYS}+$I_{VINLS456}$ with no load current ON LSW = 0 EN_LSW_ILIM_COMPS =X EN_LOWVIN_ILIM_MODE = X			10	nA

Note 1: Guarantee by design

GPIO ELECTRICAL CHARACTERISTICS

(VIO_IN = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1,2,3,4 Input Low	VIO_IN = 1.8V			0.4	V
GPIO1,2,3,4 Input High	VIO_IN = 1.8V	1.35			V
GPIO1,2,3,4 Input Low	VIO_IN = 3.3V			1.2	V
GPIO1,2,3,4 Input High	VIO_IN = 3.3V	2.4			V
GPIO Open Drain Leakage Current	Output = 5V			1	µA
GPIO Open Drain Output Low	I_{OL} = 1mA			0.35	V
Output Low	I_{OL} = 0.25mA, CMOS output configuration.			0.35	V
Output High	I_{OH} = 0.25mA, CMOS output configuration.	VIO_IN-0.35			V
VIO_IN Operating Range		1.2		VSYS	V
PBIN Deglitch Time	1kΩ/50kΩ Ohm Pull down on PB pin		32		ms
PBIN Soft Reset Time	1kΩ Ohm Pull down on PB pin	2000		3999	ms
PBIN Power Cycle/ Hard Reset Time	1kΩ Ohm Pull down on PB pin	4000			ms
PBIN Programmable Turn on Time Range	Configurable to 32ms, 500ms, 1000ms or 2000ms	32		2000	ms
PBIN Power Cycle Time	Configured as power cycle / hard reset with long PB press. (50k Ohm Pull Down)	10000			ms
PBIN Turn Off Time	Configured as power off with long PB press. (50kΩ Ohm Pull Down, can disable)	14000			ms
PBIN Master Reset Rising Threshold	PBIN rising		1.25		V
PBIN Internal pull up resistance	Pull up to internal supply VSYS		0.5		MΩ

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VSYS = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{ILO}	V_{IO_IN} = 1.8V			0.4	V
SCL, SDA Input High	V_{IHI}	V_{IO_IN} = 1.8V	1.25			V
SDA Leakage Current	I_{OH}	SDA = 3.6V			0.1	μA
SDA Output Low	V_{OL}	I_{OL} = 5mA			0.35	V
SCL Clock Frequency	f_{SCL}		0		1000	kHz
SCL Low Period	t_{SCL_LOW}		0.5			us
SCL High Period	t_{SCL_HI}		0.26			us
SDA Data Setup Time	t_{SU}		50			ns
SDA Data Hold Time	t_{HD}		0			ns
Start Setup Time	t_{ST}		260			ns
Stop Setup Time	t_{SP}		260			ns
SDA Fall Time, T_{off}	Device requirement				120	ns
Capacitance on SCL or SDA PIN	C_{IN}				10	pF
Noise suppression on SCL and SDA	$t_{DEGLITCH}$				50	ns

Note1: Comply with I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering COLD, SLEEP, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the IC.

Note4: IC Address is factory configurable to 0x24h, 0x26h, 0x66h, 0x6Ah.

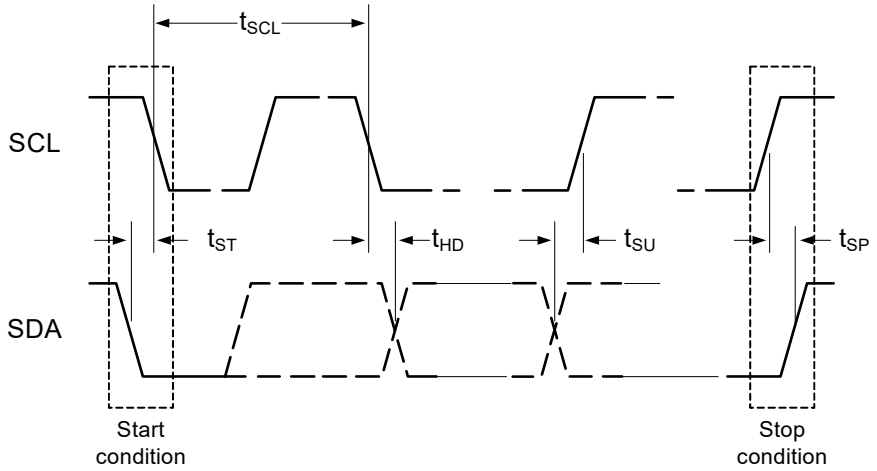


Figure 2: I²C Data Transfer

FUNCTIONAL DESCRIPTION

General

The ACT81460 is optimized for low power battery applications, but can also be used in higher power applications requiring small size with high integration.

The ACT81460 has one main power input, the VIN pin. This input supply is passed through the Smart Switch which serves three functions: VSYS softstart, VSYS linear regulator, and VIN overvoltage blocking. VSYS is the system voltage, which is limited to a maximum of 5.5V by the Smart Switch. The VSYS output powers the rest of the system and the other converters. The smart-switch doubles as a linear regulator to regulate VSYS to voltages lower than VIN.

The ACT81460 powers the system with several buck converters, a buck-boost converter, a boost converter, three LDOs, and three load switches. All of these are fully integrated and highly configurable. The buck converters each provide 400mA. The buck-boost can be configured in either buck-boost mode or boost mode and provides up to 400mA of output current. The boost converter provides up to 20V and can be configured in either voltage or current mode. In voltage mode, it powers higher voltage loads. In current mode, it regulates a constant current to a string of LEDs. The three LDOs provide up to 100mA. LDO3 is also configurable as a load switch. All three LDOs have dedicated input power pins to help optimize overall system efficiency. The three load switches provide very flexible system level power sequencing and allow the user to design voltage “islands” to turn off parts of the system in low power modes.

The ACT81460 also contains a configurable linear charger that provides up to 800mA. It is fully JEITA compliant and autonomously charges a single cell Li-Ion battery. It contains a full complement of charging protection features to ensure safe and reliable operation.

The ACT81460’s four GPIOs can be configured for a variety of functions. They can be used as standard digital inputs, push-pull outputs, open drain outputs, LED drivers, or as analog input/outputs. Typical configurations include nRESET, Power Good (PG), interrupt request or interrupt pin (nIRQ), digital output from power okay (POK) signal from individual regulators, digital input to control power sequencing or regulator ON/Off, digital inputs to put the IC into SLEEP and DPSLP modes, input/output lines to sequence external regulators as part of the power sequence, Dynamic Voltage Scaling (DVS) inputs, and as LED drivers.

The ACT81460 is highly flexible and contains many I²C configurable functions. The IC’s default functionality is defined by its default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. I²C functionality includes OV and UV fault thresholds, switching frequencies, current limits, precharge and fast charge current settings, charging termination voltage, JEITA settings, and more. The CMI Options section shows the default settings for each available CMI option. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT81460 uses standard I²C commands. It supports clock speeds up to 1MHz. The ACT81460 always operates as a slave device, and can be factory configured to one of four 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC’s slave address

Table 1: ACT2861 I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics. For more information regarding the I²C 2-wire serial interface, refer to the NXP website: http://www.nxp.com.

I²C Registers

The ACT81460 has an array of internal registers that contain the IC’s basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status

such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected IC behavior.

STATE MACHINE

The ACT81460 contains an internal state machine with five internal states: POWER OFF, START POWER SEQUENCE, SLEEP/STANDBY, DPSLP (DEEP SLEEP), and POWER ON.

POWER OFF State

The POWER OFF state is a PMIC “safe state” or “shutdown” state. In this state, all the regulator outputs are turned off. The user cannot configure any of the power supplies to remain ON in the POWER OFF state and this is therefore different from the SLEEP and DPSLP states that allows users to configure these states via firmware.

The ACT81460 enters POWER OFF at initial power on when input power is applied to the IC and VIN is within a valid range defined by the VIN_UV and VIN_OV thresholds. nRESET is asserted low and all volatile and non-volatile registers are reset to defaults. If the input voltage drops below the VIN_UV threshold voltage, the IC transitions from any other state to the POWER OFF state. It is important to note that a transition to POWER OFF due to VIN_UV returns all volatile and non-volatile registers to their default states. The ACT81460 can also enter POWER OFF from any other state due to an nPBIN press that initiates the power off sequence. The ACT81460 momentarily enters POWER OFF during a power cycle sequence. The IC exits the POWER OFF state when the I²C bit POWER OFF is cleared to 0, or the nPB pin is pulled low for > 32ms

START POWER SEQUENCE State

The START POWER SEQUENCE state is a transitional state to power on the regulators. The IC is not intended to operate in this state. When entering START POWER SEQUENCE from the SLEEP and DPSLP states, the IC transitions to the POWER ON state after all regulators are in regulation.

When entering START POWER SEQUENCE from the POWER OFF state due to an nPBIN press, the IC remains in START POWER SEQUENCE until nPBIN is released AND the regulators are in regulation. If nPBIN is released before the regulators are in regulation, the IC transitions back to the POWER OFF state. If nPBIN is still pressed and the regulators enter regulation and one of them has a fault before nPBIN is released, the IC transitions back to the POWER OFF state.

When entering START POWER SEQUENCE from the POWER OFF state due to a power cycle sequence, the IC stays in START POWER SEQUENCE for 0.5s before exiting to the ACTIVE state.

POWER ON State

The POWER ON state is the main active operating state when the input voltage is within the allowable operating range and there are no faults. Each power supply and load switch output can be programmed to be either ON or OFF in this state.

The ACT81460 enters the POWER ON state from START POWER SEQUENCE with a normal nPBIN startup, an I2C startup, or a power cycle sequence.

The IC can transition to the SLEEP and DPSLP states with proper control of the I2C bits and external GPIO inputs. It can transition to the POWER OFF state by setting the I2C MR bit or by the nPBIN pin.

SLEEP State

The SLEEP state is a low power mode for the operating system. Each output can be programmed to be on or off in the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the SLEEP state. Buck1/2 can be programmed to regulate to their VSET0 voltage, VSET1 voltage, or be turned off in the SLEEP state. The Buck-Boost, LDOs, Load Switches, and Boost converter can be programmed to regulate to their VSET0 voltage or can be programmed to be turned off. Note that the LDOs, Load Switches, and Boost converter do not have a VSET1 voltage.

The IC enters SLEEP state via I²C register bits SLEEP, SLEEP EN, and SLEEP MODE, plus a GPIO input pin.

The IC's specific CMI determines the specific combination of these inputs to enter SLEEP state. The ACT81460's I²C stays enabled in SLEEP state.

The I²C bit SLEEP MODE is set at factory and cannot be changed by the user. It controls the logical combination of the GPIO input and the SLEEP register bit to enter SLEEP state. When the SLEEP MODE bit is factory configured to 1, the logical combination is an "OR" function and when SLEEP MODE is factory configured to a 0, the logical combination is an "AND" function.

The IC exits the SLEEP state when the conditions to enter SLEEP state are no longer present. The IC also exits the SLEEP state when nPBIN is pulled low for >32ms. This also clears the SLEEP register bits. When the IC exits the SLEEP state, it goes through a full power ON sequence before entering the POWER ON state.

If no GPIOs are configured as a control input to enter and exit SLEEP state then only the SLEEP register bit controls the entry and exit of the SLEEP state.

Tables 1a and 1b show the conditions to enter SLEEP state.

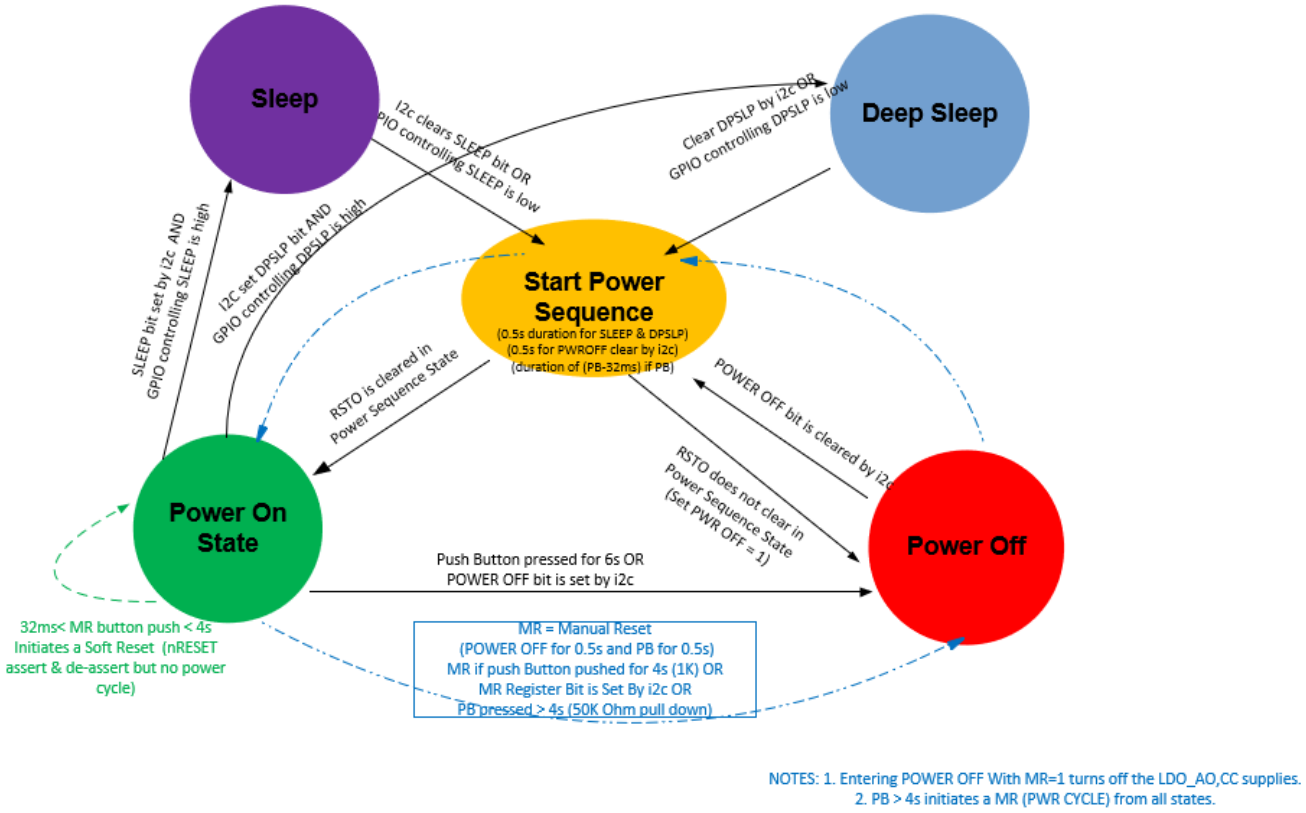


Figure 1: ACT81460 State Diagram

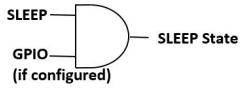
ACT81460 SLEEP MODE TRUTH TABLE					
SLEEP MODE (Reg Bit)	nPB Pin	SLEEP EN (Reg Bit)	SLEEP (Reg Bit)	GPIO CONTROL Pin	ENTER SLEEP State
0	not asserted	x	0	0	No
0	not asserted	x	0	1	No
0	not asserted	x	1	0	No
0	not asserted	x	1	1	Yes
0	not asserted	x	0	GPIO not configured	No
0	not asserted	x	1	GPIO not configured	Yes
Note: Asserting nPB >32ms brings the IC out of SLEEP State & clears the SLEEP register bit to 0.					
					

Table 1a. SLEEP Mode Truth Table (SLEEP MODE bit is configured to 0)

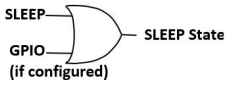
ACT81460 SLEEP MODE TRUTH TABLE					
SLEEP MODE (Reg Bit)	nPB Pin	SLEEP EN (Reg Bit)	SLEEP (Reg Bit)	GPIO CONTROL Pin	ENTER SLEEP State
1	not asserted	x	0	0	No
1	not asserted	x	0	1	Yes
1	not asserted	x	1	0	Yes
1	not asserted	x	1	1	Yes
1	not asserted	x	0	GPIO not configured	No
1	not asserted	x	1	GPIO not configured	Yes
Note: Asserting nPB >32ms brings the IC out of SLEEP State & clears the SLEEP register bit to 0.					
					

Table 1b. SLEEP Mode Truth Table (SLEEP MODE bit is configured to 1)

DPSLP State

The DPSLP state is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP mode. It is similar to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can only be programmed to be on or off in the DPSLP state. The DPSLP state does not allow the automatic use of the VSET1 registers. This programming can be different and independent from the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state.

The IC enters DPSLP state via I²C register bits DPSLP, DPSLP EN, and DPSLP MODE, plus a GPIO input pin. The IC's specific CMI determines the specific combination of these three inputs to enter DPSLP state. ACT81460's I²C stays enabled in DPSLP state.

The I²C bit DPSLP MODE is set at factory and cannot be changed by the user. It controls the logical combination of the GPIO input and the DPSLP register bit to enter DPSLP state. When DPSLP MODE is factory configured to 1, the logical combination is an "OR" function and when DPSLP is factory configured to a 0, the logical combination is an "AND" function.

The IC exits the DPSLP state when the conditions to enter DPSLP state are no longer present. The IC also exits the DPSLP state when nPBIN is pulled low for >32ms. This also clears the DPSLP register bits. When the IC exits the DPSLP state, it goes through a full power ON sequence before entering the POWER ON state.

If no GPIOs are configured as a control input to enter and exit DPSLP state then only the DPSLP register bit controls the entry and exit of the DPSLP state.

Table 2a and 2b show the conditions to enter DPSLP state.

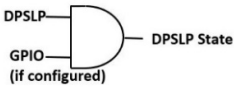
ACT81460 DPSLP MODE TRUTH TABLE					
DPSLP MODE (Reg Bit)	nPB Pin	DPSLP EN (Reg Bit)	DPSLP (Reg Bit)	GPIO CONTROL Pin	ENTER DPSLP State
0	not asserted	x	0	0	No
0	not asserted	x	0	1	No
0	not asserted	x	1	0	No
0	not asserted	x	1	1	Yes
0	not asserted	x	0	GPIO not configured	No
0	not asserted	x	1	GPIO not configured	Yes
Note: Asserting nPB >32ms brings the IC out of DPSLP State & clears the DPSLP register bit to 0.					
					

Table 2a. DPSLP Mode Truth Table (DPSLP MODE factory bit is configured to 0)

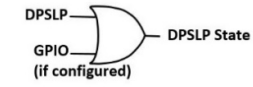
ACT81460 DPSLP MODE TRUTH TABLE					
DPSLP MODE (Reg Bit)	nPB Pin	DPSLP EN (Reg Bit)	DPSLP (Reg Bit)	GPIO CONTROL Pin	ENTER DPSLP State
1	not asserted	x	0	0	No
1	not asserted	x	0	1	Yes
1	not asserted	x	1	0	Yes
1	not asserted	x	1	1	Yes
1	not asserted	x	0	GPIO not configured	No
1	not asserted	x	1	GPIO not configured	Yes
Note: Asserting nPB >32ms brings the IC out of DPSLP State & clears the DPSLP register bit to 0.					
					

Table 2b. DPSLP Mode Truth Table (DPSLP MODE factory bit is configured to 1)

SLEEP and DPSLP State Configurability

The ACT81460 provides highly configurable low power modes that allow the user to fully optimize their system in any operating condition. This allows the user to configure the IC for many different microprocessor needs. The SLEEP and DPSLP states allow the user to optimize system efficiency. The configuration can be redefined prior to each time the states are entered. If the configuration is left unchanged, entering the state results in the same IC behavior every time SLEEP/DPSLP mode is activated. SLEEP/DPSLP can also be configured differently before entering the state each time and this empowers the user to control and change the SLEEP/DPSLP behavior by firmware in a variety of permutations and combinations. This gives the user immense control via firmware to configure the system state and behavior during low power states.

Each regulator's I²C SLEEP EN bit determines if that regulator is on or off in the SLEEP state. When the SLEEP EN bit = 0, that output ignores the SLEEP state. When the SLEEP EN bit = 1, that output responds to the SLEEP state. The same is true for each regulator's DPSLP EN bit.

SYSTEM FUNCTIONS

Startup/Shutdown

When power is applied, the IC enters the POWER OFF state and stays there indefinitely. This results in a very low power state. The IC starts up and sequences on the regulators when the user actively initiates a power on by either asserting nPBIN pin or by writing a 0 into the I²C POWER OFF bit. When powering on with the nPBIN pin, any fault that occurs before nPBIN is released transitions the IC back to the POWER OFF state. Any faults that occur after nPBIN is released and the IC is in the ACTIVE state are handled per the proper fault detection procedure as programmed by the IC's specific CMI. Once in the ACTIVE state, the IC can stay in that state or automatically transition to either the SLEEP or DPSLP state depending on the status of the inputs in Tables 1 and 2.

Shutdown is typically accomplished by forcing the system to transition to the DPSLP state. Shutdown can also be accomplished with the nPBIN pin or by setting the I²C POWER OFF bit to a 1.

Input Voltage Monitoring (VIN and VSYS UVLO)

The ACT81460 monitors the input voltage on the VIN pin to ensure it is within specified limits for system level operation. The IC also monitors the VSYS output. When VSYS rises above its POR (~1.4V), the IC wakes up and allows I²C communication. The outputs will not turn on until VSYS rises above UVLO (~2.5V). VSYS also has a UV Warning threshold that is I²C programmable between 1.85V and 3.35V. The IC asserts the nIRQ pin low if VSYS drops below the programmed threshold, but the outputs continue to operate normally. The IC turns off all outputs if VSYS drops below UVLO. I²C bit VSYSSTAT = 1 when VSYS < UV Warning and 0 when VSYS > UV Warning. This fault can be masked with I²C bit VSYSMSK.

Pushbutton Functionality

The ACT81460 nPBIN pin is a multi-functional input pin. It provides multiple system level functions based on its impedance to ground and "press" time. Power On and Power Cycle1 are typically implemented with a single normally open, momentary pushbutton switch to ground through 50kΩ. Power Off and Power Cycle2 are typically implemented with a single normally open, momentary pushbutton switch or a "pin hole" pushbutton to ground through 1kΩ.

Power On – This sequence starts up the IC and turns the outputs on. Initiate Power On by momentarily pulling nPBIN to ground through a 50kΩ resistor. The IC moves to the START POWER SEQUENCE and then starts turning on the outputs after a 32ms debounce time. The nPBIN pin must remain asserted for longer than the I²C PB_WAIT_TIME_SET register value for the IC to startup and move to the POWER ON state. The nPBIN wait time can be set to 32ms, 500ms, 1000ms, or 2000ms. If nPBIN is deasserted or a fault is detected before the wait time expires, the IC turns off the outputs and moves back to the POWER OFF state. Note that nPBIN remains asserted for > 8s, the IC follows the standard behavior described below.

Power Cycle1 – This sequence momentarily turns all outputs off and automatically restarts them. Initiate Power Cycle1 by momentarily pulling nPBIN to ground through a 50kΩ resistor for >8s, but <12s. When nPBIN transitions back high, the IC transitions from its current operating state to the POWER OFF state for 0.5s. It then transitions to the START POWER SEQUENCE state for 0.5s before going to the POWER ON state. If nPBIN is pulled low for <8s, no action is taken.

Power Off (Long Pushbutton Press) – This sequence turns all outputs off, and they stay off until the user actively initiates a Power On sequence. Initiate the Power Off sequence by pulling nPBIN to ground through a 50kΩ resistor for >12s. After 12s, the IC transitions from its current operating state to the POWER OFF state and turns all outputs off. Once in the POWER OFF state and

nPBIN is released high, the IC follows normal programmed functionality to leave the POWER OFF state. If nPBIN is pulled low for >8s but <12s, the IC follows the Power Cycle1 sequencing described above.

Soft Reset – This sequence pulls nRESET low to reset the system processor, but all ACT81460 outputs stay turned on. To initiate Soft Reset, pull nPBIN to ground through a 1kΩ resistor for 2s to 4s. nRESET asserts low after 2s. When nPBIN transitions back high, the IC de-asserts the nRESET pin high. The output voltages do not power cycle during a Soft Reset.

Power Cycle2 (Hard Reset) – This sequence momentarily turns all outputs off and automatically restarts them. Initiate Power Cycle2 by momentarily pulling nPBIN to ground through a 1kΩ resistor for >4s. When nPBIN transitions back high, the IC transitions from its current operating state to the POWER OFF state for 0.5s. It then transitions to the START POWER SEQUENCE START state for 0.5s before going to the POWER IN state. Unlike Power Cycle1, the Power Cycle2 sequence does not require any I²C register settings.

Software-Initiated Power Cycle

ACT81460 supports a software-initiated power cycle. This is initiated by setting I²C bit MR to 1. The IC then waits 8ms and initiates a power cycle to restart the system. MR is automatically reset to 0 after the power cycle.

Smart Switch – Softstart

The ACT81460 is specifically designed to system level handle hot plug events. It does this with a combination of the 20V input blocking capability and inrush current control at startup. When power is applied to the VIN pin, the IC monitors the VIN voltage after it is greater than approximately 1.5V. VIN is then monitored for under voltage (UV), ~4.0V, and over voltage (OV) conditions, ~5.8V. When VIN is in the valid range, the Smart Switch connects the VIN to VSYS. The Smart Switch slowly ramps up the VSYS by limiting the inrush current. The Smart Switch current limit is programmed by the I²C bit IN_ILIM_SETTING between 0.5A and 2A. The inrush controller thus limits inrush current while also adding monitoring and health check functions such as UV, OV and Over Current Protection (OCP) on the VIN input.

Smart Switch – Current Limit

The Smart Switch also provides input current limit circuit in normal operation. The Smart Switch current limit is programmed by the I²C bit IN_ILIM_SETTING between 0.5A and 2A. In the event of an overcurrent, the Smart Switch opens and disconnects VIN from VSYS. After a 20ms re-try timer expires, the Smart Switch restarts. During the softstart time, the Smart Switch limits the inrush current. During this time the current limit signal is masked to prevent false overcurrent conditions. The current limit is unmasked after the softstart time is complete and it then ready to detect over current faults.

Smart Switch – OVP

The Smart Switch also provides over voltage protection. When VIN goes above 5.8V, the IC generates a fault condition. The typical deglitch time for detecting an OV condition is 200us. The Smart Switch is latched open until the over voltage condition is removed. After the fault clears, the Smart Switch restarts. The typical retry time after the OV or any other fault condition clears is 20ms.

Watchdog Supervision

The ACT81460 features a watchdog supervisory function. This resets the system in the case where the host microprocessor get locked up or becomes unresponsive. Watchdog is disabled by default. Writing a 1 into I²C bits WDSREN or WDPCEN enables the watch dog functionality. Once enabled, the watchdog timer is reset whenever there is I²C activity. If there is no I²C communication for longer than 8s, the IC performs either a soft-reset if the WDSREN bit = 1 or a power cycle if the WDPCEN bit = 1. If both bits = 1, the IC performs Power Cycle

Fault Protection

The ACT81460 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit and short circuit

Thermal Shutdown

There are two types of I²C register bits associated with each fault condition: fault bits and mask bits. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. If a fault is masked, the fault bit shows the real-time fault status, but the fault does not assert nIRQ. Refer to Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

nIRQ (Interrupt)

nIRQ is an open-drain output that asserts low any time an interrupt is generated. This function can be configured on any of the GPIOs even though GPIO1 is

by default used for this function. Connect a pull-up resistor from the nIRQ pin to an appropriate voltage supply (typically VSYS or VIO_IN). nIRQ is typically used to drive the interrupt input of the system processor. Many of the ACT81460's functions support interrupt-generation. These are typically masked by default to block unnecessary interrupts but may be unmasked via the I²C interface per the user's choice through firmware. In general every output can generate interrupts due to current limits, UV or OV conditions. GPIOs can also be configured to generate interrupts when the GPIO is configured as a digital input. Push button function, manual reset, input UV/OV, thermal shutdown and other such functions can also trigger interrupts and these are available in the register map of the master control core, also referred to as the master tile. Examples of conditions that can cause nIRQ to trigger are:

1. Die temperature warning generated
2. Any buck regulator exceeding peak current limit for 8 cycles after soft start or a UV/OV condition.
3. Any LDO regulator exceeding current limit for more than 20uS after soft start or a UV/OV condition.
4. Input goes above OVP threshold or falls below the UV threshold.
5. Watch Dog timer expiring.
6. Push Button status when the nPBIN pin is asserted. The PB status register bit and PB counter register can then be used to check the PB time and take appropriate action.

If any of the faults occur and the nIRQ output is enabled, the nIRQ pin will be driven low. Following the nIRQ pin being asserted, a read operation of the interrupt causing status bit will clear the interrupt, so the interrupt is cleared upon reading provided the interrupt causing condition is removed.

nRESET

The ACT81460 provides a reset function to issue a master reset to the system CPU/controller. nRESET is immediately asserted low when either the VIN voltage is above or below the UV or OV thresholds or any power supply that is connected to the nRESET functionality goes below its Power Good threshold. The IC's specific CMI configures which power supplies are connected to the nRESET functionality. After startup, nRESET de-asserts after a programmable delay time when VIN and all connected power supply outputs are above their respective UVLO thresholds. The reset delay time, 20ms to 100ms, is controlled by the I²C TRST_DLY register bits. The IC's CMI programs the specific GPIOx pin used for the reset functionality. The CMI also programs which regulators outputs are monitored for the reset functionality.

Output Under/Over Voltage

The ACT81460 monitors the output voltages for under voltage and over voltage conditions. If an output enters an UV/OV fault condition, the IC asserts IRQ and nRESET and shuts down all outputs for 100ms and then restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If this behavior is not desired, mask the appropriate fault bit. If the fault is masked, the fault status bit shows the real-time fault status. Note that the IC's specific CMI sets the defaults for which regulators mask the UV and OV fault conditions.

Output Current Limit

The ACT81460 incorporates overcurrent for all converters and load switches. Refer to each section for the details.

Thermal Warning and Thermal Shutdown

The ACT81460 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Warning Threshold of typically 125 deg C. It shuts down all outputs when the temperature increases above 155 deg C. The Thermal Warning can be masked via I²C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

The IC includes a Thermal Low Power mode. When the die temperature goes above 70°C, the IC places a 100kΩ resistor on the output of the LDOs to ground. This prevents the output voltages from increasing due to leakage through the internal FETs.

Sequencing

The ACT81460 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each output has four basic sequencing parameters: input trigger, turn-on delay, turn-off delay, and output voltage. Each of these parameters is controlled via the ICs internal registers. The specifics for this IC as well as others are detailed at the end of the datasheet. Contact sales@active-semi.com for custom sequencing configurations. Refer to the Active-Semi Application Note AN116, ACT81460VM101 Register Definitions, for full details on the I²C register map functionality and programming ranges.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the

internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to an input pin such as EXT_PG or GPIO. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with an external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The GPIOx outputs can be connected to an internal power supply's POK signal and used to trigger external supplies in the overall sequencing scheme. The GPIOx inputs can also be connected to an external power supply's power good output and used as an input trigger for an ACT81460 supply.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ON DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between an input trigger going inactive and the output starting to turn off. Each output's turn-off delay is configured via its I²C bit OFF DELAY. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled. Turn-off delays are valid when entering SLEEP mode, DPSLP mode, and when turning off the IC. Turn-off delays are not implemented in fault conditions.

Output Voltage. The output voltage is each regulator's desired voltage. Each buck's output voltage is programmed via its I²C bits VSET0 and VSET1. The output regulates to VSET0 in ACTIVE mode. They can be programmed to regulate to VSET1 in DVS, SLEEP, and DSPSLP modes. Each LDO has a single register, VSET, to set its output voltage. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault thresholds are immediately changed, but the output takes time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for the two buck converters is available via either the I²C interface or a GPIO. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. Each buck converter operates at its VOUT0 voltage in normal operation and operates at its VOUT1 voltage when the DVS input trigger is active. DVS can be implemented three ways.

The first method is to individually put each buck converter in DVS by manually writing a new voltage regulation setpoint into its VOUT0 register.

DVS can also be implemented for both buck converters at one time via a single GPIO input. The IC's default CMI determines the specific GPIO used for the DVS input. Refer to the CMI Options section at the end of this datasheet. This setting can be modified with a custom CMI.

DVS can also be implemented for both buck converters at one time via I²C. One of three I²C registers controls each buck converters DVS function. Writing a 1 into the appropriate register puts the buck converter into DVS. The register choices are DVS_FROM_I2C_DB9, DVS_FROM_I2C_DB10, and DVS_FROM_I2C_DB11. Each buck's DBSTBY register programs which register enables its DVS function. The user can change the default settings after power up.

For CMI 101, Buck1 DVS is disabled by default. Buck2 is controlled by DVS_FROM_I2C_DB9. Writing a 1 into this register puts Buck2 into DVS, but does not affect Buck1. Note that each specific CMI allows DVS contro by either a GPIO or I²C, but not both.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

PIN FUNCTIONS

VIN

VIN is the ACT81460 input power pin. The VIN operating range is 4.0V to 5.5V, but it withstands voltage surges up to 20V.

VIN power the Smart Switch, two back-to-back protection FETs that actively disconnect VIN from VSYS when the input voltage goes above 5.8V. The Smart Switch also acts as a linear regulator to control the VSYS voltage, which powers the linear charger and other power rails. The regulated Smart Switch regulates VSYS to 4.8V.

Connect a 1uF ceramic input bypass capacitor directly between VIN and PGNDx

VSYS

VSYS is the output of the Smart Switch. It powers the rest of the system, the linear charger, and the switching converters. Connect a 10uF ceramic bypass capacitor from VSYS to PGND.

VBAT

The VBAT pins are the output of the linear charger. Note that the battery voltage is not regulated at VBAT, but at the VBATS pin. Connect 10uF ceramic output bypass capacitor directly between VBAT and PGND.

VBATS

VBATS is the battery voltage sense pin. The battery voltage is regulated at the VBATS pin. Kelvin connect input VBATS as close to the battery input terminals as possible.

OUTLx

The OUTLx pins are the outputs of the LDO linear regulators. These are also LDO regulation points.

VINBx

The VINBx pins are the inputs to the buck and buck-boost regulators. Each pin is a dedicated input to its switching regulator. The VINBx pins must be directly connected to the VSYS output. Each VINBx pin must have a dedicated ceramic bypass capacitor that is connected to PGND. Proper capacitor selection and placement are critical to good power supply performance.

ISET

ISET sets the maximum battery charge current. Connect a 1.2kohm to 15kohm resistor between ISET and AGND to set the fast charge current. See the Active Path Linear Charger section for more information.

NTC

NTC is the battery temperature sense input. Connect a negative temperature coefficient thermistor from NTC to AGND. This pin provides a constant current output and the resulting voltage at this pin is used to calculate the battery temperature.

VINLx

The VINL123 pins are dedicated input pins for LDO1, LDO2, and LDO3. The three LDO inputs are independent from each other. They can be connected to the same or to different input voltage rails. The VINL123 voltages should be higher than their respective LDO output voltages to maintain regulation. Connect 1uF ceramic input bypass capacitor directly between each VINL123 pin and PGND.

SWx

The SWx pins are the switch nodes for their respective switching converters. Connect the inductors directly to the SWx pins.

VBST

VBST is the boost converter output pin. The VBST pin must have a dedicated ceramic bypass capacitor that is connected to PGND. Proper capacitor selection and placement are critical to good power supply performance.

ISNS

ISNS is the current sensing input pin for the boost converter when it is configured for a constant current output. Connect the return side of the constant current load to ISNS. The load's return side is typically the cathode of an LED string. Note that ISNS is always regulated to 0.25V.

VINLSx

The VINLS456 pins are dedicated input pins for Load Switch 4, 5, and 6. Connect 1uF ceramic input bypass capacitor directly between each VINLS123 pin and ground. The capacitor's ground should be connected to load switch's input supply's output capacitor's ground.

GPIOx

The GPIOx pins can be configured as inputs, outputs, or other special functions. See the GPIO Functionality section of the DS for more details.

NC

This pin is not internally connected to the IC. It can be left open, shorted to GND, or shorted to the VIO_IN pin. Active Semi recommends shorting NC to VIO_IN.

VIO_IN

VIO_IN is the input bias supply for the IC. Apply an input voltage between 1.2V and the VSYS voltage. Bypass to AGND with a high quality, 1uF ceramic capacitor.

FBx

These are the regulation pins for the converters. Kelvin connect these pins to their respective output capacitors.

PGNDx

The PGNDx pins are dedicated power grounds for each switching converter. The input caps should be directly connected to the PGNDx pins.

SWBST

SWBST is the boost converter switch node. Connect the boost inductor directly to this pin.

SCL, SDA

SCL and SDA are the I²C clock and data pins to the IC They have standard I²C functionality. They are open-drain outputs and each require a pull-up resistor. The pull-up resistor is typically tied to the system's uP IO pins. The pullup voltage can range from 1.8V to 5.0V. SCL and SDA are open drain and are 5V compliant.

AGND

The AGND pins are the IC's analog ground. This is a "quiet" ground pin that is separate and isolated from the high power, high current carrying PGND ground plane. Connect the non-power components to AGND. AGND must be Kelvin connected to the PGND pin in a single location.

nPBIN

nPBIN is the push button input pin and provides multiple system level functions based on its impedance to ground and "press" time. See the Pushbutton Functionality section of the datasheet for more details.

nIRQ

nIRQ informs the host of any fault conditions. In general, any IC function with a status bit asserts nIRQ pin low if the status changes. The status changes can be masked by setting their corresponding register bits. If nIRQ is asserted low, the fault must be read before the IC deasserts nIRQ. If the fault remains after reading the status bits, nIRQ remains asserted. Refer to the **nIRQ Interrupt Pin (nIRQ)** section for more details.

nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor. nIRQ is 5V compliant.

GPIOx Configurability

The ACT81460 has four GPIO pins. These GPIOs allow a variety of functions to be implemented. They can be used as inputs, push-pull outputs, open drain outputs, LED drivers, or as analog input/output. These options allow implementation of a variety of system functions and also allow flexibility of functions tied to each pin. Some examples of system functions that can be implemented are nRESET, Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output from power okay (POK) signal from individual regulators, digital input to control power sequencing or regulator ON/Off, control input used to enter or exit sleep (SLEEP) and deep sleep (DPSLP) modes, input/output lines to sequence external regulators as part of the power sequence, to control Dynamic Voltage Scaling (DVS) in BUCK regulators or even as LED drivers.

The GPIOs are internally powered by the VIN_IO pin. The user should ensure that the resulting input and output voltages are compatible with their system level inputs and outputs.

GPIO1 (pin D3). GPIO1 can be programmed for any of the above functions except the LED drivers. It can be programmed as an input or an open drain or push-pull output.

GPIO2 (pin C3). GPIO2 is the same as GPIO1

GPIO3 (pin E4). GPIO3 can be programmed for all the above functions including the LED drivers. It can be programmed as an input or an open drain output.

GPIO4 (pin E5). GPIO4 is the same as GPIO3

The GPIOs are 5.5V tolerant meaning they can go to 5.5V even if VIN_IO is less than 5.5V.

When GPIO1 and GPIO2 are configured as LED drivers, they sink a constant current. The constant current is defined by the I²C bits ILED_SET per Table 3.

		ISET [5:3]	
		0	1
ISET [2:0]	000	0	8
	001	1	10
	010	2	12
	011	3	14
	100	4	16
	101	5	18
	110	6	20
	111	7	22

Table 3. Constant Current vs ISET Register

STEP-DOWN DC/DC REGULATORS

General Description

The ACT81460 contains two fully integrated step-down converters. Buck1 and Buck2 both provide 0.4A outputs. They operate with the Active-On-Time control loop, which is a hybrid topology of a Constant ON-Time (COT) synchronous step-down converter and a hysteretic converter. This combination allows them to achieve very low quiescent current during extremely light load operation. The regulators can achieve peak efficiencies of up to 95%. They are internally compensated, requiring only three external components (Cin, Cout, and L) for operation. They allow the use of small external components while emulating a constant frequency PWM mode regulator during continuous mode high load current situations. Additionally, all regulators are available with a variety of standard and custom output voltages and may be software-controlled via the I²C interface for systems that require advanced power management functions.

The ACT81460 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

Low Power Mode On/Off control

Overcurrent Thresholds

Refer to the Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Operating Mode

The Buck regulators operate in a fixed frequency Active-On-Time, fixed-frequency PWM mode at medium to heavy loads. This results in a fixed frequency, PWM mode with a constant on-time. The control loop automatically adjusts the on-time with changes in input voltage, output voltage, and load to maintain a fixed switching frequency. At lighter loads, the inductor current goes discontinuous and the control loop increases the off-time. This reduces the switching frequency and minimize switching losses. At extremely light loads, the IC continues to decrease the off-time, further reducing switching losses.

85% Duty Cycle Operation

The maximum duty cycle is limited to 85%. The maximum duty cycle must be considered when calculating the maximum allowable output voltage.

Synchronous Rectification

Each BUCK regulator features an integrated synchronous rectifier (or low side FET), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

The BUCK regulators include a fixed 2.5V/ms soft-start ramp which limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition.

Output Voltage Setting

The buck converters regulate to the voltage defined by I²C register VSET0 in normal operation and by VSET1 in DVS mode. They can be programmed between 0.6V and 3.6V in 50mV steps. The following equation calculates the output voltage based on the VSETx register setting.

Vbuck1 = 0.6V + VSETx * 0.05V

Where VSETx is the decimal equivalent of the value in each regulator's I²C VSETx register. The VSETx registers contain an unsigned 6-bit binary value. As an example, if Buck 1's VSET0 register contains 100110b (38 decimal), the output voltage is 2.5V.

Table 4 shows the output voltage in voltage as a function of the VSETx register settings.

		Buck Output Voltage (V)							
		VSETx [5:3]							
		000	001	010	011	100	101	110	111
VSETx [2:0]	000	0.60	1.00	1.40	1.80	2.20	2.60	3.00	3.40
	001	0.65	1.05	1.45	1.85	2.25	2.65	3.05	3.45
	010	0.70	1.10	1.50	1.90	2.30	2.70	3.10	3.50
	011	0.75	1.15	1.55	1.95	2.35	2.75	3.15	3.55
	100	0.80	1.20	1.60	2.00	2.40	2.80	3.20	3.60
	101	0.85	1.25	1.65	2.05	2.45	2.85	3.25	3.60
	110	0.90	1.30	1.70	2.10	2.50	2.90	3.30	3.60
	111	0.95	1.35	1.75	2.15	2.55	2.95	3.35	3.60

Table 4. Vout vs VSETx Register Setting

Active Semi recommends that the buck converter's output voltage be kept within +/- 20% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 20% may require different factory trim settings (new CMI) to maintain accuracy.

Dynamic Voltage Scaling

Each buck converter supports Dynamic Voltage Scaling (DVS). In normal operation, each output regulates to the voltage programmed by its VSET0 register. During DVS, each output can be programmed to regulate to its VSET0 or VSET1 voltage.

When DVS is enabled via I²C, the IC's digital core steps the output setting through each voltage step between the initial and final settings. This ensures a constant and controlled slew rate. During a high to low voltage transition, the regulator switches in an internal 40Ω resistor to ensure the output voltage maintains a constant slew rate under light load conditions.

When switching between VSET0 and VSET1 in DVS mode, the digital core steps the output voltage between the two values one register step at a time. During this transition, the regulator's OV and UV faults are ignored to prevent false fault conditions. Also for DVS, it is recommended to keep the range within +-20% of the nominal CMI set point. In some cases, greater than 20% deviation would be allowed.

Note that if the user changes the VSETx register while the buck converter is regulating to that register setting, the IC does not mask out the OV and UV faults. Either make small voltage steps or mask OV and UV fault registers to prevent a fault condition.

Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I²C interface by writing to that regulator's ON bit. Note that disabling a regulator that is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. Each buck converter has a load discharge function designed to quickly pull the output voltage to ground when the converter is disabled. The circuit connects an internal resistor (41ohm) from the output to PGND when the converter is disabled.

POK and Output Fault Interrupt

Each DC/DC features a Power-OK (POK) status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically 8.0% below the programmed regulation voltage, that regulator's POK bit will be 0.

If a DC/DC's nFLTMSK bit is set to 1, the ACT81460 interrupts the processor if the DC/DC's output voltage falls below the Power-OK (POK) threshold. In this case, nIRQ asserts low and remains asserted until either the regulator is turned off or the output goes back into regulation, and the POK bit has been read via I²C. The POK interrupt is cleared when the register is read and the fault is no longer present.

Minimum On-Time

ACT81460 does not have minimum on-time limitations that prevent the use of any desired switching frequency.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits.

If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle. If the load current continues to increase, this condition results in shutdown due to an UV condition from the shortened switching cycle.

If the short circuit or overload condition occurs quickly, the cycle-by-cycle current can exceed the programmed threshold. When it reaches 125% of the programmed current for two consecutive switching cycles, the IC issues an overcurrent warning and asserts nIRQ low. When it reaches 125% of the programmed current for eight consecutive switching cycles, the buck converter shuts down.

Compensation

The BUCK regulators utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

Each buck converter has a dedicated input pin and power ground pin. Each buck converter must have a dedicated input capacitor that is optimally placed to minimize the power routing loops for each buck converter. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

Each regulator requires a high quality, low-ESR, ceramic input capacitor. 1uF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output

loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Where V_{ripple} is the input voltage AC voltage ripple, I_{out} is the output current, V_{out} is the output voltage, V_{in} is the input voltage, F_{sw} is the switching frequency, and C_{in} is the input capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VINBx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The Buck converters utilize a Constant ON-Time and a hysteretic mode hybrid topology and a proprietary internal compensation scheme to simultaneously simplify external component selection and to optimize transient performance over the entire operating range. The ACT81460 is designed to operate with 1.0μH Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The BUCK regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. They are designed to operate with 10μF to 44μF output capacitors over most of their output voltage ranges. In order to ensure stability, the Buck effective capacitance must be greater than 4.7uF. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance when the IC in in PWM mode.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

The output capacitance also affects output ripple in PFM mode as well as the output voltage discharge time when the converter is disabled.

LOW-DROPOUT LINEAR REGULATORS

General Description

ACT81460 contains three fully integrated, 100mA, low-noise, low-dropout linear regulators (LDOs). Each LDO has been optimized to achieve low quiescent current under no load conditions. LDO3 can also be configured in load switch mode to behave like a load switch.

The LDOs require only two small external components (Cin, Cout) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. The LDO ramp rate is fixed at 1.7V/ms.

Output Voltage Setting

The LDOs regulate to the voltage defined by their I²C registers LDO1_VSET, LDO2_VSET, and LDO3_VSET. The LDOs do not have a second VSET register like the buck converters. They can be programmed between 0.6V and 3.6V in 50mV steps. The following equation calculates the output voltage based on the LDOx_VSET register setting.

VLDOx = 0.6V + LDOx_VSET * 0.050V

Where LDOx_VSET is the decimal equivalent of the value in each regulator's I²C LDOx_VSET register. These registers contain an unsigned 6-bit binary value. As an example, if LDO1's LDO1_VSET register contains 11000b (24 decimal), the output voltage is 1.8V.

Active Semi recommends that the LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Table 5 shows the output voltage in voltage as a function of the LDOx_VSET register settings.

		LDO Output Voltage (V)							
		LDOx_VSET [5:3]							
		000	001	010	011	100	101	110	111
LDOx_VSET [2:0]	000	0.60	1.00	1.40	1.80	2.20	2.60	3.00	3.40
	001	0.65	1.05	1.45	1.85	2.25	2.65	3.05	3.45
	010	0.70	1.10	1.50	1.90	2.30	2.70	3.10	3.50
	011	0.75	1.15	1.55	1.95	2.35	2.75	3.15	3.55
	100	0.80	1.20	1.60	2.00	2.40	2.80	3.20	3.60
	101	0.85	1.25	1.65	2.05	2.45	2.85	3.25	3.60
	110	0.90	1.30	1.70	2.10	2.50	2.90	3.30	3.60
	111	0.95	1.35	1.75	2.15	2.55	2.95	3.35	3.60

Table 5. Vout vs LDOx_VSET Register Setting

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I²C interface by writing to that regulator's ON bit. Note that disabling an LDO that is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. Each LDO has a load discharge function designed to quickly pull the output voltage to ground when the LDO is disabled. The circuit connects an internal resistor (50ohm) from the output to AGND when the LDO is disabled.

POK and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the Power-OK (POK) threshold, typically 8% below the programmed regulation voltage, the value of that regulator's POK bit will be 0.

If a LDO's nFLTMSK bit is set to 1, the ACT81460 will interrupt the processor if that LDO's output voltage falls below the Power-OK (POK) threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the POK bit has been read via I²C. After removing the undervoltage condition, a read operation clears the interrupt.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent detection and short circuit protection featuring a current-limit foldback function. When current limit is reached, the IC can either shut the output off or limit the output current until the overload condition is removed. This is controlled by I²C bits LDOx_ILIM_SHUTDOWN_DIS.

The overcurrent threshold is fixed at 120mA. In both an overload and a short circuit condition, the LDO limits the

output current which causes the output voltage to drop. When LDOx_ILIM_SHUTDOWN_DIS = 1, the LDO turns off when it reaches current limit. When the register = 0, and the UV fault is masked, the output voltage drops based on the load resistance. When the output voltage drops below 1V, the current folds back to ~60mA to reduce power dissipation in the IC. If the UV fault is not masked, the LDO shuts off when the output voltage drops below the UV threshold, waits 100ms, and then tries to restart.

The LDO's real-time current limit status is reported in the ILIM_LDOx I²C registers. The contents of these registers are latched until read via I²C. When in current limit, the IC asserts nIRQ low provided the fault is not masked. Overcurrent and short circuit conditions can be masked via the I²C bit ILIM_FLTMSK_LDOx. When masked, the LDO still shuts down or limits current (based on the LDOx_ILIM_SHUTDOWN_DIS bit). If the IC shuts down due to current limit, it automatically restarts in 14ms.

Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

Input Capacitor Selection

Each LDO has a dedicated input pin, VINL1, VINL2, and VINL3. Each input pin requires a high quality, low-ESR, ceramic input capacitor. A 1uF capacitor to AGND is typically suitable, but this value can be increased without limit. The input capacitor should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor. A 2.2uF capacitor to AGND is typically suitable, but this value can be increased without limit. The output capacitor is should be a X5R, X7R, or similar dielectric. The LDO effective output capacitance must be greater than 0.8uF.

LDO3 in Load Switch Mode

LDO3 can be configured as a load switch. Configure LDO3 into LDO mode by setting I²C bit EN_LDOx_LOAD_SWITCH_MODE = 0. Configure it into load switch mode by setting the register = 1.

When LDO3 reaches current limit, the output turns off for 14ms and then restarts. It continues in the "hiccup" mode until the overcurrent condition is removed. LDO3 does not generate an interrupt in an overcurrent condition.

Note that LSW456 do generate an interrupt with an overcurrent condition.

BUCK-BOOST REGULATOR

General Description

ACT81460 contains a fully integrated, four-switch, buck-boost regulator. It operates from an input voltage range of 2.7V to 5.5V and provides an output range between 3.2V and 5.0V.

The four integrated MOSFETS minimize the cost and size of the solution with minimal external components needed for the buck-boost function. The buck-boost can be configured via I²C to operate in Buck Only mode, Boost Only mode, or Buck-Boost mode. These bits are not user accessible. Refer to the CMI Options section for each CMI's specific setting.

In CCM mode, there are four user-selectable frequencies between 1.5MHz and 3.3MHz. The buck-boost is available with a variety of standard and custom output voltages and may be software-controlled via the I²C interface for systems that require advanced power management functions.

Operating Mode

The buck-boost regulator emulates operation of a fixed-frequency regulator at medium to heavy loads. It transitions to a proprietary power-saving mode at light loads to save power and improve efficiency. The buck-boost is optimized to reduce its input current during off/shutdown and standby modes when there is no load current and the regulator is left on with the output regulating. The output voltage can be configured via I²C.

Synchronous Rectification

The buck-boost features an integrated full H-bridge with two high side (HS) and two low side (LS) power MOSFETs. The LS MOSFETS are used in a fully synchronous mode to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Note that an additional Schottky diode is required when the output voltage is greater than 4.7V. Connect the anode to SWBB2 and the cathode to VBBST. The diode should be placed on the top layer with direct connections to these two pins. Refer to the EVK for layout details.

Soft-Start

The buck-boost regulator includes an internal 800µs soft-start ramp which limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition and during retry after a fault.

Output Voltage Setting

Output voltage for the buck-boost regulator can be programmed in 50mV steps from 3.20V to 5.0V. The buck-boost regulates to the voltage defined by I²C register VSET0. It can be programmed between 3.2V and 5.0V in 50mV steps. The following equation calculates the output voltage based on the VSET0 register setting.

Vbuck-boost = 3.2V + VSET0 * 0.05V

Where VSET0 is the decimal equivalent of the value in the I²C VSET0 register. The VSET0 register contains an unsigned 6-bit binary value. As an example, if the VSET0 register contains 100100b (36decimal), the output voltage is 5.0V.

Changes to the output voltage are intended to be performed with CMI settings. The output voltage should not be changed in final production. For development and experimentation, the output voltage may be changed by +-20% from the default setting. Voltage changes larger than +/- 20% require different factory trim settings (new CMI). Programming the output voltage farther than 20% from the default setting may damage the IC.

Table 6 shows the output voltage as a function of the VSET0 register setting. Do not program the VSET0 registers to a value greater than 100100b. Programming higher than this may damage the IC.

		Buck-Boost Output Voltage (V)							
		VSET0 [5:3]							
		000	001	010	011	100	101	110	111
VSET0 [2:0]	000	3.20	3.60	4.00	4.40	4.80	N/A	N/A	N/A
	001	3.25	3.65	4.05	4.45	4.85	N/A	N/A	N/A
	010	3.30	3.70	4.10	4.50	4.90	N/A	N/A	N/A
	011	3.35	3.75	4.15	4.55	4.95	N/A	N/A	N/A
	100	3.40	3.80	4.20	4.60	5.00	N/A	N/A	N/A
	101	3.45	3.85	4.25	4.65	N/A	N/A	N/A	N/A
	110	3.50	3.90	4.30	4.70	N/A	N/A	N/A	N/A
	111	3.55	3.95	4.35	4.75	N/A	N/A	N/A	N/A

Table 6. Vout vs VSET0 Register Setting

DVS

The buck-boost does not have DVS functionality.

Enable / Disable Control

During normal operation, the buck-boost may be enabled or disabled via the I²C interface by writing to its ON bit. Note that disabling the buck-boost if it is used as an

input trigger to another regulator may or may not disable the other regulator following it, depending on the specific CMI settings. The buck-boost has a load discharge function designed to quickly pull the output voltage to ground when it is disabled. The circuit connects an internal resistor (41ohm) from the output to PGND34 when the buck-boost is disabled.

POK and Output Fault Interrupt

The buck-boost features a Power-OK (POK) status bit that can be read by the system microprocessor via the I²C interface. If the output voltage is lower than the power-OK threshold, typically 90% of the programmed regulation voltage, the POK bit will be 0.

If the nFLTMSK bit is set to 1, the ACT81460 interrupts the processor if the output voltage falls below the Power-OK (POK) threshold. In this case, nIRQ asserts low and remains asserted until either the regulator is turned off or goes back into regulation, and the POK bit has been read via I²C. The POK interrupt is cleared when the register is read and the fault is no longer present.

Overcurrent and Short Circuit Protection

The buck-boost converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is fixed at 0.85A.

If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle. If the load current continues to increase, this condition results in shutdown due to an UV condition from the shortened switching cycle.

If the short circuit or overload condition occurs quickly, the cycle-by-cycle current can exceed the programmed threshold. When it reaches 125% of the programmed current for two consecutive switching cycles, the IC issues an overcurrent warning and asserts nIRQ low. When it reaches 125% of the programmed current for eight consecutive switching cycles, the buck-boost converter shuts down.

Compensation

The buck-boost utilizes a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The buck-boost converter has a dedicated input pin, VINBB. Its ground pin, PGND34 is common with the boost converter. VINBB must have a dedicated input capacitor that is optimally placed to minimize the power routing loop. Note that even though the buck-boost converter has a separate input, the input must be connected to the same voltage potential as the buck regulators.

The VINBB pin requires a high quality, low-ESR, ceramic input capacitor. 1uF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VINBx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The ACT81460 is designed to be used with a 1μH to 2.2μH. Use 1μH for a 3.3V output and use 2.2μH for a 5V output. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Output Capacitor Selection

The buck-boost regulator is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. VBBST must have a dedicated low-ESR capacitor bypass directly to PGND34 that is optimally placed to minimize the power routing loop. It is designed to operate with 22μF to 44μF output capacitors over most of its output voltage range. In order to ensure stability, the Buck-Boost effective capacitance must be greater than 8uF. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

The buck-boost converter has a dedicated input pin and power ground pin. The converter must have a dedicated input capacitor that is optimally placed to minimize the power routing loops. Note that even though the buck-boost converter has a dedicated input, the converter input must be connected to the same voltage potential as the buck converters.

BOOST STEP-UP REGULATOR

General Description

The ACT81460 contains a fully integrated boost converter. It can boost the battery voltage up to 20V and provide up to 40mA of output current. The maximum allowable output current is dependent on the battery and output voltages. The boost is very versatile and can be used for many different applications such as driving a LED backlight, driving audio speakers, implementing audio functions such as audio beeps, or haptics for communicative feedback.

The boost operates with high efficiency and achieve a peak efficiency up to 95%. It is internally compensated, requiring only three external components (Cin, Cout, and L) for operation. The ACT81460 boost regulator is highly configurable and can be quickly and easily reconfigured via I²C. This allows it to support changes in hardware requirements without the need for PCB changes.

Operating Modes

The boost converter operates with a standard fixed frequency. It can be operated with voltage feedback, current feedback, or both.

Constant Voltage Feedback Mode

The boost can operate as a standard boost converter. Configure the boost for this mode by leaving the ISNS pin disconnected from the boost circuitry. The ISNS pin can be operated separately and independently from the boost converter.

In constant voltage (CV) mode, the boost can supply up to 40mA. The maximum current should be reduced to 25mA when the output voltage is > 17V.

Constant Current Feedback Mode

The boost can operate as a current sink. In this configuration, the boost is not needed. The ISNS pin sinks a constant current, regardless of the voltage applied to it. This mode is useful for driving LEDs that have another power source. Configure the boost for this mode by connecting the external circuit directly to the ISNS pin. The boost converter can be operated separately and independently from the ISNS pin. Note that the ISNS pin always regulates to 0.25V.

In constant current mode (CV) mode, the output can drive up to 40mA. The more LEDs, the higher the required output voltage. If the voltage across the LEDs exceeds 17V, the maximum current should be reduced to 25mA.

Constant Voltage/Current Feedback Mode

The boost can operate in a dual constant voltage/current mode. Either the voltage or current loop dominates, depending on the operating conditions. In this mode, both the voltage and current regulation loops are active. As long as the load current is less than the current regulation threshold, the voltage loop dominates and maintains a constant output voltage. If the load current increases to the current regulation threshold, the current loop takes over and reduces the output voltage to maintain a constant current. This mode is similar to a lab power supply with a fixed voltage output setting and a maximum current limit setting. The output voltage is sensed at the VBST pin. The current is sensed by the ISNS pin, which is always regulated to 0.25V

This mode is useful for driving LEDs that do not have their own power source. Configure the boost for this mode by connecting the output of the boost converter (VBST pin) to the load, which is typically the anode of an LED string. Then connect the cathode of the LED string to the ISNS pin.

Synchronous Rectification

The boost regulator features an integrated synchronous rectifier (or low side FET), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

The boost regulator includes a fixed 80ms soft-start ramp which limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the output. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition.

The boost converter's synchronous FET is connected between the BSTSW pin (switch node) and the VBST pin (output voltage). Because of this, there is no way to disconnect the output voltage from the input source. When the VSYS voltage softstarts, the VSYS voltage passes through the synchronous FET and charges up the boost converter output voltage. VBST then stays at the VSYS voltage until the boost converter is enabled. After the boost converter is enabled, the output voltage ramps to the setpoint with the 80ms softstart time.

Output Voltage Setting

The boost converter regulates to the voltage defined by I²C register VSET. It can be programmed between 5V and 20.75V in 250mV steps. The following equation calculates the output voltage based on the VSET register setting.

Vboost = 5V + VSET * 0.25V

Where VSET is the decimal equivalent of the value in the I²C VSET register. The VSET register contains an unsigned 6-bit binary value. As an example, if VSET register contains 011100 (28 decimal), the output voltage is 12.00V.

Table 7 shows the output voltage in voltage as a function of the VSET register setting.

		Boost Output Voltage (V)							
		VSET [5:3]							
		000	001	010	011	100	101	110	111
VSET [2:0]	000	5.00	7.00	9.00	11.00	13.00	15.00	17.00	19.00
	001	5.25	7.25	9.25	11.25	13.25	15.25	17.25	19.25
	010	5.50	7.50	9.50	11.50	13.50	15.50	17.50	19.50
	011	5.75	7.75	9.75	11.75	13.75	15.75	17.75	19.75
	100	6.00	8.00	10.00	12.00	14.00	16.00	18.00	20.00
	101	6.25	8.25	10.25	12.25	14.25	16.25	18.25	20.25
	110	6.50	8.50	10.50	12.50	14.50	16.50	18.50	20.50
	111	6.75	8.75	10.75	12.75	14.75	16.75	18.75	20.75

Table 7. Vout vs VSET Register Setting

Active Semi recommends that the boost converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy. Note that making large voltage steps will result in an UV/OV fault. If a large voltage change is required, change the voltage in multiple small steps. To prevent an UV/OV fault caused by changing the voltage when the boost is enabled, do not increase VSET in steps larger than 30% or decrease VSET in steps larger than 10% of the previous setting. Keeping the voltage steps smaller than these levels

Output Current Setting

The boost converter regulates to the sink current defined by I²C register ISET. It can be programmed between 0mA and 39.375mA in 0.625mA steps. The following equation calculates the sink current based on the ISET register setting.

Isink = ISET * 0.625mA

Where ISET is the decimal equivalent of the value in the I²C ISET register. The ISET register contains an unsigned 6-bit binary value. As an example, if ISET register contains 101000 (40 decimal), the sink current is 25mA.

Table 8 shows the sink current as a function of the ISET register setting.

		Boost Sink Current (mA)							
		ISET [5:3]							
		000	001	010	011	100	101	110	111
ISET [2:0]	000	0.00	5.00	10.00	15.00	20.00	25.00	30.00	35.00
	001	0.63	5.63	10.63	15.63	20.63	25.63	30.63	35.63
	010	1.25	6.25	11.25	16.25	21.25	26.25	31.25	36.25
	011	1.88	6.88	11.88	16.88	21.88	26.88	31.88	36.88
	100	2.50	7.50	12.50	17.50	22.50	27.50	32.50	37.50
	101	3.13	8.13	13.13	18.13	23.13	28.13	33.13	38.13
	110	3.75	8.75	13.75	18.75	23.75	28.75	33.75	38.75
	111	4.38	9.38	14.38	19.38	24.38	29.38	34.38	39.38

Table 8. Boost Sink Current vs ISET Register

Dynamic Voltage Scaling

The boost does not have dynamic voltage scaling.

Enable / Disable Control

During normal operation, boost voltage and current sink can be independently enabled or disabled via the I²C interface. The voltage enable is controlled by the boost's ON bit. Note that disabling a the boost if it is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. The constant current can be disenabled by writing a value of 0mA to the ISET bits. It is enabled by writing a non-zero value.

POK and Output Fault Interrupt

The boost converter contains an internal Power-OK (POK) signal that can be used to sequence other power supplies. This status is not available to the I²C interface. POK threshold is typically 30% below the programmed regulation voltage.

The boost converter does have I²C register undervoltage and overvoltage fault bits. These bits can be masked. When masked, they provide real-time fault status. If the nFLTMSK bits are set to 1, the ACT81460 interrupts the processor if the boost output voltage goes above or below the fault thresholds. In this case, nIRQ asserts low and remains asserted until either the regulator is turned off or goes back into regulation and the fault bit has been read via I²C. The fault bit is cleared when the register is read and the fault is no longer present.

Overcurrent and Short Circuit Protection

The boost converter features a cycle-by-cycle current limit on the low side MOSFET. As with any standard

synchronous boost converter, this limits the maximum allowable output current in normal operation, but does not limit short circuit current. Short circuit current is not limited because the synchronous FET does not block current flow from the SWBST pin to the output. The VSYS voltage is always connected to VBST.

The user must take care to not load or leave a load connected to the boost regulator output when it is disabled. The output of the boost regulator cannot be discharged to 0V due to these constraints and any load left connected to the boost regulator can continue to draw power because the boost regulator output voltage always trails the input voltage by one diode voltage.

Maximum Output Current

The maximum allowable output current is a function of the peak switch current, the input voltage, and the output voltage. The peak switch current limit can be set to 1.0A or 1.35A. This setting is not user adjustable. See the CMI Options section of the datasheet for each CMI's setting. The following equation approximates the maximum available output current. Note that this is the boost output current. The constant current into the ISNS pin is still limited to 39.375mA.

$$I_{Boost\_max} = \frac{I_{SW\_peak}}{2} * \frac{V_{IN}}{V_{OUT}}$$

Compensation

The boost converter utilizes a proprietary internal compensation scheme. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The boost converter requires dedicated input capacitor. It should be a high quality, low-ESR, ceramic input capacitor. 1uF capacitors are typically suitable, but this value can be increased without limit.

Inductor Selection

The boost converter requires a 2.2µH inductor. Ensure that the inductor is rated for at least 1A peak current. The inductor's peak current is much higher than the average output current.

Output Capacitor Selection

The boost converter is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. It is designed to operate with a 10µF output capacitor. In order to ensure stability, the Boost effective capacitance must be greater than 4µF and less than 22µF. The maximum allowable capacitance includes both the capacitance at the boost's output and at the load's input.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

LOAD SWITCHES

General Description

The ACT81460 features three, 100mA load switches. They operate from 0.6V to the VSYS voltage. The Load Switches allow a power rail to be switched on or off to create a power “island” for system loads. This “island” can be turned off to minimize power consumption when those loads are not needed. Each Load Switch can also be incorporated into the ICs startup sequencing with programmable turn-on and turn-off delay times. They can also be programed to be turned on or off in SLEEP and DPSLP states.

Softstart

The load switch outputs are slew rate controlled to minimize inrush current during turn on. The rise time is approximately 9.6mV/µs.

Enable / Disable Control

During normal operation, the load switches may be enabled or disabled via the I²C interface by writing to their ON bits. Note that disabling a load switch if it is used as an input trigger to another regulator may or may not disable the other regulator following it, depending on the specific CMI settings. The load switches have a load discharge function designed to quickly pull the output voltage to ground when it is disabled. The circuit connects an internal resistor (50ohm) from the output to PGND34 when the load switch is disabled.

Current Limit

The load switches provide output current limiting. They implement current limit by measuring the voltage drop across their internal FETs. With an overload or short circuit condition, the excessive current causes the voltage drop across the load switch to exceed the current limit threshold. The current limit circuit senses this voltage and shuts down the load switch. Following a 14ms wait time, the load switch turns on again and goes through a soft start. When sensing the current limit, a minimum deglitch time is used before shutting down the load switch. The deglitch time and retry time set the duty cycle of the load switch turning on and off under an output short circuit conditions and this is chosen to protect the load switch from electrical over stress.

For extremely light load conditions, the load switch current limit functionality can be disabled to reduce the IC’s quiescent current. The I²C bit EN_34_OK_OV_ILIM controls the functionality for LSW4 and LDO3 when in load switch mode. The I²C bit EN_LSW_ILIM_COMPS controls the functionality for LSW5 and LSW6.

Note, there is a difference between stand-alone load switches and LDO load switch modes when it comes to detecting a current limit event. When the LDO123 are configured as a load switch, there is no interrupt when ILIM triggers. The switch retries to power up after 14ms. If the current limit is still present it continues this “hiccup” cycle until the high current condition is removed. This is different from stand-alone LSW456. For these load switches when ILIM triggers, they “hiccup” with 14ms cycle, but also generate an interrupt.

Input Capacitor Selection

The load switches each require a quality, low-ESR, ceramic input capacitor. 1uF capacitors are typically suitable, but this value can be increased without limit.

Output Capacitor Selection

The load switches each require a quality, low-ESR, ceramic input capacitor. 1uF capacitors are typically suitable, but this value can be increased without limit.

LDO3 Load Switch

Note that LDO3 can also be configured to operate as a load switch. Refer to the LDO section of the datasheet for more information on this functionality.

ACTIVE PATH LINEAR CHARGER (APLC)

General Description

The ACT81460 low power PMIC incorporates Active-Semi's proprietary ActivePath linear battery charging architecture. It is a full featured charger that performs a variety of advanced battery management functions, including fault protection and management, thermal regulation, and temperature monitoring. It includes an 800mA, linear, single cell Li-Ion battery charger and a Smart Switch. It interfaces to the host microprocessor via I²C to provide very flexible functionality with its built in programmability.

The charger is capable of status and fault monitoring and is designed to work with many different host processors via interrupt generation and status and fault reporting. Host processor interrupts are generated for any change in battery charging state:

1) JEITA temp threshold crossed

2) Battery voltage low

3) Battery removed/inserted

4) Charge source plugged/unplugged

5) Charge condition / state change – Precondition, fast charge, top off and end of charge reached.

ActivePath Architecture

The ActivePath architecture provides a system level charging architecture that dynamically optimizes battery charging while ensuring that power delivery to the system is not interrupted.

At the input of the ActivePath charger is a high voltage LDO that can withstand input voltages as high as 20V. There are variety of protection features such as input over voltage (OV), input under voltage (UV), input current limit. The ActivePath circuity provides a very simple means of implementing a solution that maximizes available power from the input source without overloading the source. An example would be a 0.5A current limited USB input source. The ActivePath circuit ensures that the full 0.5A current is used.

ActivePath circuitry automatically detects the state of the input supply, the battery and the system and then reconfigures itself to optimize the system power. A higher priority is always given to system power to ensure uninterrupted power to the system. It does this by independently managing the input current and the charge current. This allows the battery to charge as quickly as possible while ensuring that the total ACT81460 input current does not exceed the input source capability. This is ideal for weak, or current limited input sources.

The ActivePath architecture operates in two separate modes, dynamic charge current control (DCCC) and dynamic voltage charge current control (DVCCC).

The DCCC mode can be used for a "weak" input source when the maximum available current is known. In DCCC mode, the ACT81460 regulates the total input current into VIN. This allows the user to set the total input current below the power source's maximum current rating. This ensures that the input power source's current rating is not exceeded and that its voltage does not collapse.

The DCCC loop regulates the input current to the programmed current limit setting. The system consumes its required current, and the remaining current is used to charge the battery. The charging current is dynamically adjusted as the system current changes.

If the system current exceeds the maximum programmed input current due to current spikes, the charger stops charging and goes into supplement mode. In supplement mode, the battery supplies current to the system. This maintains the maximum allowable input current while still allowing the system to run properly.

This maximum input current is programmable to 0.5A, 1A, 1.5A, or 2A via I²C register bits IN_ILIM[1:0]

DVCCC mode can be used to maximize the total available power from the input source, even when the current capability is not known. It also prevents "weak" input sources from collapsing.

The DVCCC loop regulates the input voltage on VIN. If the system current plus charging current is greater than the input source's current capability, the input voltage collapses. The DVCCC loop becomes active and limits the VIN current. It also prioritizes the system current over the charging current. The DVCCC loop starts limiting the charge current when VIN drops to the programmed threshold. It linearly decreases the charge current until VIN drops to 0.7V below the threshold. If the system current continues to increase, the charger goes into supplement mode and the battery provides current to the system.

The VDCCC threshold is programmable to "Disable", 4.25V, 4.5V, or 4.75V via I²C register bits VDCCC[1:0]. When set to "Disable", the control loop does not limit the input voltage drop.

Smart Switch

The Smart Switch serves three functions: VSYS softstart, VSYS linear regulator, and VIN overvoltage blocking. VSYS is the system voltage, which is limited

to a maximum of 5.5V by the Smart Switch. The VSYS output powers the rest of the system and the other converters. The Smart Switch doubles as a linear regulator to regulate VSYS to voltages lower than VIN.

Softstart

The Smart Switch provides softstarting to the VSYS output when input power is applied. This provides a 500µs controlled ramp time to limit inrush currents.

Overvoltage Blocking

The Smart Switch continuously monitors the VIN voltage. If VIN goes above the 5.7V overvoltage threshold, the switch opens to protect the VSYS bus and all downstream loads. It has a 20V blocking capability to handle extreme overvoltage conditions. When an overvoltage condition occurs, the ACT81460 opens the Smart Switch to protect VSYS from the overvoltage condition.

VSYS Regulator

The Smart Switch regulates VSYS to 4.8V. This provides a constant VSYS operating voltage, even when VIN varies. Contact Active Semi if a different VSYS regulation voltage is required. If VIN is lower than the programmed regulation voltage, the Smart Switch fully turns on with a resulting resistance of 200mΩ.

Linear Charger

The ACT81460 autonomously charges a single cell Li-Ion battery. The IC automatically detects the battery's state of charge and starts charging in the proper charge state. It completes full or partial charging cycles without host intervention. The charger includes all Li-Ion charging modes and protection including trickle charging, precharge, fast charge, over and under voltage protection, JEITA charging profiles, and thermal regulation. It also includes Active Semi's ActivePath Architecture.

Charger Enable

The charger is automatically enabled when the VSYS voltage is greater than the battery voltage by > 100mV. The charger can be enabled and disabled by I²C bit CHG_EN.

Battery Charging Profile

The IC follows the standard Li-Ion battery charge profile with four charging phases: trickle charge, preconditioning, constant current, and constant voltage. The battery charge current is a function the battery voltage and the IC's hardware and register settings. Figure 2 shows the charge profile and Table 9 shows these available settings.

VBAT	Charging Current	Current set by
< $V_{TRICKLE}$	$I_{TRICKLE}$	I²C Configurable: 10mA, 25mA
$V_{TRICKLE}$ ~ V_{PRE}	I_{PRE}	I²C Configurable: 5%, 10%, 15%, 20% of I_{CHG} current
V_{PRE} ~ V_{TERM}	I_{CHG}	Hardware Configurable: 10mA to 800mA
> V_{TERM}	0A	None

Table 9: Charging Current Settings

Trickle Charge – When the battery voltage is lower than the battery short threshold voltage, V_{BAT_SHORT}, the battery can only accept very low charge currents. The charger supplies a trickle charge current, $I_{TRICKLE}$, to condition the battery and bring a shorted battery pack "back to life" by allowing the battery protection circuitry to close its protection FETs. The battery can then be safely charged to bring the voltage up to a level where preconditioning can begin.

$V_{TRICKLE}$ is set to 2.0V, 2.2V, 2.4V, or 2.5V via I²C register bits V_TRICKLE[1:0].

$I_{TRICKLE}$ is set to 10mA or 25mA via I²C register I_TRICKLE_SET.

Precondition Charge - When the battery voltage is higher than the trickle voltage threshold, the precondition charge phase begins. In this phase, the IC charges the battery at a reduced charge current. This safely conditions the battery chemistry to prepare the battery to accept the full charging current.

The precondition voltage threshold, VPRE, is set via I²C register bits VPRE[3:0]. The precharge voltage is programmable between 2.7V to 3.4V. The following equation calculates the precharge voltage.

$$VPRE = 2.7V + 50mV * VPRE[3:0]$$

Where VPRE[3:0] is the decimal equivalent value in this register. For example, if VPRE[3:0] = 0110 (6 decimal), the precharge voltage = 3.0V.

The precharge current, I_{PRE}, is set by I²C register bits IPRE[1:0]. The constant current is set to 5%, 10%, 15% or 20% of the fast charge current setting.

The constant current, precondition phase continues until the battery voltage increases to the precondition voltage threshold.

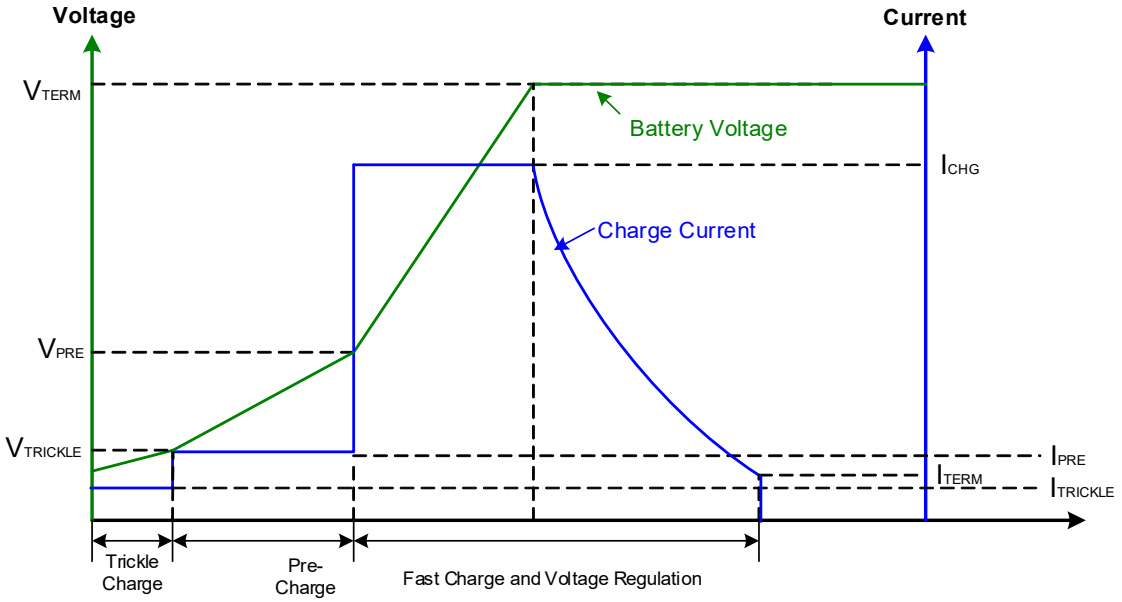


Figure 3: APLC Charging Profile

Fast Charge – When the battery voltage is higher than the precharge voltage, the Fast Charge phase begins. In this phase, the battery chemistry is ready to accept the full charging current and the charger applies the full fast charge current, I_{CHG}.

The ACT81460 fast charge current is set by placing a resistor from the ISET pin to ground. The following equation calculates the correct R_{ISET} resistor value in ohms

$$R_{ISET} = \frac{1.2V}{I_{CHG}} * 10{,}000$$

Where I_{CHG} is the desired fast charge current in amps. R_{ISET} should stay between 15kΩ and 1.2MΩ to keep the fast charge current between 10mA and 800mA.

During fast charge, the charger regulates a constant current until the battery voltage reaches the termination voltage, VTERM. When the battery reaches VTERM, the charger changes from constant current regulation to constant voltage regulation. During this time, the charger keeps the battery at the VTERM voltage and the charging current starts to drop. When the current drops below the termination current, ITERM, charging is terminated and the battery is considered to be at the end of charge (EOC).

The termination voltage threshold, VTERM, is set via I²C register bits VTERM[4:0]. VTERM is programmable between 3.9V to 4.52V. The following equation calculates VTERM.

$$VTERM = 3.9V + 20mV * VTERM[4:0]$$

Where VTERM[4:0] is the decimal equivalent value in this register. For example, if VTERM[4:0] = 01111 (15 decimal), the termination voltage = 4.2V.

The termination current, ITERM, is set to 5%, 10%, 15%, or 20% (note that ERD has different values in different places) of I_{CHG} by I²C register bits ITERM[1:0].

End of Charge – When the charge current drops below ITERM, the charger considers the battery fully charged. The charge current drops to 0A and the charger continues to monitor the battery voltage. With no charging current, the battery can drop due to self-discharge or due to being externally loaded. If the battery voltage drops below the recharge voltage, V_{RECHG}, the charger re-enters the Fast Charge phase. V_{RECHG} is a function of the termination voltage and I²C register BAT_RECHG_THRESHOLD[1:0]. The BAT_RECHG_THRESHOLD[1:0] register sets V_{RECHG} to 80mV, 120mV, 160mV, or 200mV below the termination voltage.

Input Voltage and Current Control

If the input power source is not capable of supporting the charging current plus the system current, the VIN input voltage drops. The ACT81460 eliminates this

problem by providing an additional control loop that prevents VIN from dropping below 4.25V. This function allows the charger to maximize power drawn from the input source without collapsing the input voltage. This maximizes the power from VIN and minimizes current from the battery to increase battery life.

When the system current plus charging current is greater than the input source's current capability, the input voltage collapses. When it collapses below the VDCCC threshold, the charger reduces the charging current. This prioritizes the system current over the charging current. If VIN continues to drop, the charger continues to reduce the charging current in an attempt to keep VIN regulated to 4.25V or higher. If VIN drops to 3.8V, the charge current goes to 0A and the charger goes into supplement mode where it sources current to VSYS.

The VDCCC threshold is programmable to "Disable", 4.25V, 4.5V, or 4.75V via I²C register bits VDCCC[1:0]. When set to Disable, the control loop does not limit the input voltage drop.

In addition to the input voltage regulation, the ACT81460 can also regulate the total input current. This allows the user to set the total input current below the power source's maximum current rating. This ensures that the input power source that powers the charger is not subject to over current and subsequently collapsing the voltage on the input source. This function in combination with the input voltage regulation loop allows the system to maximize the power drawn from the VIN source for both charging the battery and powering the system as much as possible to conserve battery power and extend the battery life of the system.

This maximum input current is programmable to 0.5A, 1A, 1.5A, or 2A via I²C register bits IN_ILIM[1:0]

Die Thermal Regulation

The ACT81460 charger includes a maximum die temperature regulation loop. This feature maximizes charge current with high ambient thermal conditions. If the charging conditions increase the die temperature to 115°C, the thermal loop takes over and starts reducing the charge current. The charge current is linearly reduced until the die temperature reaches 150°C. At 150°C, the charging current is 0A. At 155°C the IC reports an interrupt, bit BAT_TEMP_STAT is set to 1, and Charge Fault is set to 1. Thermal regulation can be disabled by setting I²C bit DIS_THERM_REG to 1.

NTC Battery Temperature Detection

The ACT81460 NTC pin is used to monitor the battery temperature. An NTC resistor connected between NTC and AGND provides temperature information. This information is used by the charger to comply with the industry standard JEITA charging guidelines. The NTC monitoring is designed to work with a typical 10kΩ @ 25°C. Figure 4 shows that the NTC pin provides a constant current output that results in a voltage across the NTC resistor. Internal comparators monitor the NTC voltage and allow the IC to take the appropriate action if the measured temperature exceeds the thresholds defined in the JEITA Battery Temperature Control section of the datasheet. By detecting the pull-down resistor on the NTC pin, the ACT81460 shall be able to detect presence of the battery as well as the battery temperature during charging.

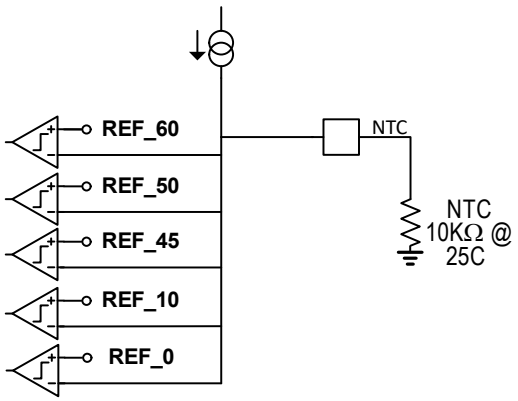


Figure 4: NTC Temperature Thresholds

JEITA Battery Temperature Control

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasizes the importance of avoiding a high charge current and high charge voltage at both extreme low and high temperature ranges. To comply with JEITA battery charging requirements, and to improve battery reliability and safety, the ACT81460 reduces the termination voltage and/or the charging current when the battery is at temperature extremes. When the battery temperature is outside the normal charging range, the IC either reduces the safety timer speeds or stops the timers until the temperature goes back into the normal charging range. When stopped, the timers are not reset. They hold their value and resume normal counting when charging restarts. Refer to the Safety Timer Speed Settings table for specific details.

$T_{battery}$ < 0°C: All battery charging is suspended until the temperature goes back above 0°C. Both the Fast Charge Safety Timer and the Low Battery Safety Timers are suspended.

0°C < $T_{battery}$ < 10°C: I_{PRE} and I_{CHG} Precharge and Fast Charge currents in this region can be programmed to either 50% or 100% of the fast charge current. Note that $I_{TRICKLE}$ is not affected. Set I²C register 0xD0 bit 6 to 0 for the 100% setting and set to 1 for the 50% setting. The termination voltage is not changed. The safety timer runs at half speed. Table 10 shows the resulting charge functionality and safety timer settings.

10°C < $T_{battery}$ < 45°C: Battery charging in this region operates at normal voltage and current levels.

45°C < $T_{battery}$ < 50°C: Battery charging is functional, but limited in this region. Setting I²C register 0xD0 bit 6 to 1 disables all charging. Setting it to 0 does not affect charge current, but reduces the termination voltage by 100mV from the normal termination voltage. The charge timers are not affected when charging.

50°C < $T_{battery}$ < 60°C: Battery charging is functional, but limited in this region. Setting I²C register 0xD0 bit 6 to 1 disables all charging. Setting it to 0 does not affect charge current, but reduces the termination voltage by 150mV from the normal termination voltage. The charge timers are not affected when charging.

$T_{battery}$ > 60°: All battery charging is suspended until the temperature goes back below 60°C. Both the Fast Charge Safety Timer and the Precondition Safety Timers are suspended.

Table 10 shows the resulting charge functionality and safety timer settings. Figure 5 shows this in graphical form.

Charging Safety Timers

The ACT81460 provides two internal charging safety timers: Precondition Safety Timer and Fast Charge Safety Timer.

The Precondition Timer is 4000s. It is activated when the charger is enabled and the battery voltage is less than the precharge voltage, VPRE.

If the Precondition timer expires, the charger goes into the Fault state charging stops.

The Fast Charge Timer is 12000s. It is activated when the battery voltage is above the precharge voltage, VPRE.

If the Fast Charge Timer expires, the charger goes into the Fault state charging stops.

Both safety timers are automatically stopped any time the charging is enabled but charging is suspended. This occurs when the battery temperature exceeds the allowable temperature limits.

Both safety timers run at ½ speed when VIN Input Regulation, IIN Current Regulation, or Die Thermal Regulation are active. This feature allows more time to charge without falsely triggering the fault timer.

Additionally, the Fast Charge Safety Timer runs at ½ speed in some JEITA charging modes. See the JEITA Battery Temperature Control paragraph for more details.

Temp	I²C register 0xD0 bit 6	Fast Charge Current	Fast Charge Safety Timer	Trickle Charge	PreCharge	Precondition Battery Safety Timer	Termination Voltage
<0C	X	Suspended	Stopped	Suspended	Suspended	Stopped	n/a
0C to 10C	0	100% of I_{CHG}	Full Speed	100% of $I_{TRICKLE}$	100% of I_{PRE}	Full Speed	V_{TERM}
	1	50% of I_{CHG}	½ Speed	100% of $I_{TRICKLE}$	50% of I_{PRE}	½ Speed	V_{TERM}
10C to 45C	x	100% of I_{CHG}	Full Speed	100% of $I_{TRICKLE}$	100% of I_{PRE}	Full Speed	V_{TERM}
45C to 50C	0	100% of I_{CHG}	Full Speed	100% of $I_{TRICKLE}$	100% of I_{PRE}	Full Speed	V_{TERM} – 100mV
	1	Suspended	Stopped	Suspended	Suspended	Stopped	n/a
50C to 60C	0	100% of I_{CHG}	Full Speed	100% of $I_{TRICKLE}$	100% of I_{PRE}	Full Speed	V_{TERM} – 150mV
	1	Suspended	Stopped	Suspended	Suspended	Stopped	n/a
> 60C	x	Suspended	Stopped	Suspended	Suspended	Stopped	n/a

Table 10: JEITA Mode Charging Safety Timer Configuration

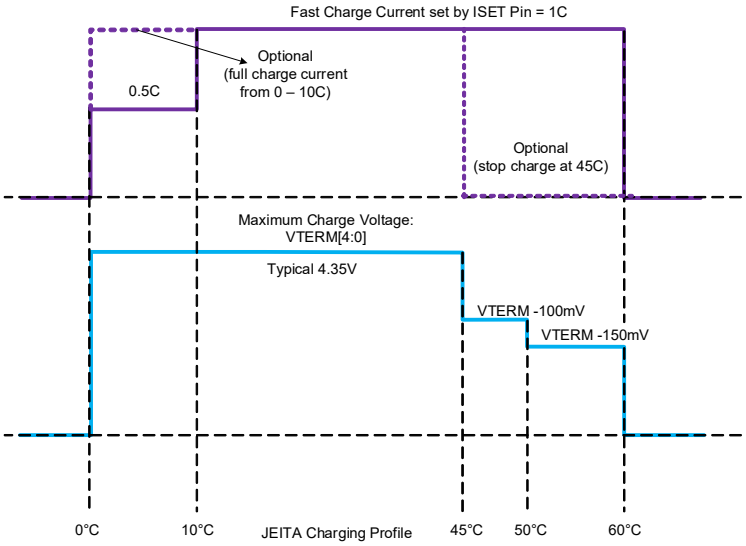


Figure 5: NTC Temperature Thresholds

Battery Path Impedance (Cord) Compensation

The ACT81460 includes a Battery Path Impedance Compensation (Cord Comp) feature that speeds the charging cycle. This feature compensates for system level voltage drops due to PCB, connector, wiring resistances, and battery pack current sense resistances.

These voltage drops effectively reduce the voltage at the battery. This results in the charger reaching the constant voltage portion of the charge cycle too soon. The Cord Comp feature allows the charger to stay in the constant current mode longer, which reduces the charging time.

The ACT81460 allows the user to compensate for the system level resistances by increasing the battery termination voltage, VTERM as a function of charge current according to the equation below. This feature is implemented with the I2C register: CORD_COMP_SETTING[2:0]. This register sets the system level resistance that is being accounted for. It can be programmed between 0mΩ and 420mΩ. Setting the value to 0mΩ effectively disables Cord Comp. The user should always pick a Cord Comp value lower than the actual system level resistance. The following equation shows the Cord Comp voltage, VCOMP.

$$V_{CORD} = CORD\_COMP\_SETTING * I_{CHG}$$

Where VCORD is the increase in VTERM, CORD_COMP_SETTING is nearest Cord Comp to the actual system resistance, and ICHG is the actual charging current.

As an example, if the actual system resistance is 320mΩ, select CORD_COMP_SETTING = 300mΩ. If ICHG = 800mA, and VTERM = 4.2V, the charger stays in fast charge mode until the battery voltage reaches 4.2V + 800mA*300mΩ = 4.44V.

It is important to note that the actual battery voltage never exceeds 4.2V because of the system level voltage drops.

It is also important to select a Cord Comp value that is LOWER than the actual system resistance. This ensures that the battery voltage never exceeds the VTERM voltage.

The charger is capable of status and fault monitoring and is designed to work with a host of host processor via interrupt generation and status and fault reporting. Host processor interrupts shall be generated for any change in battery charging state:

1) JEITA temp threshold crossed

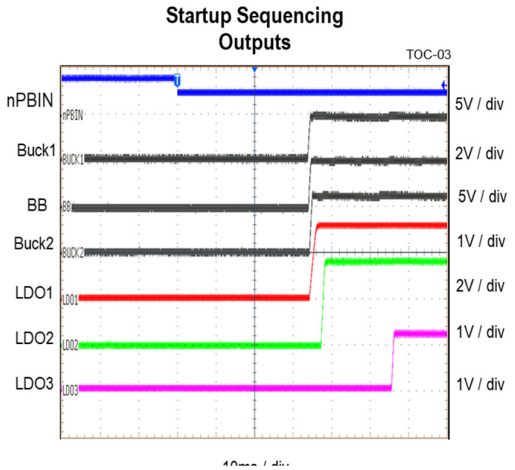
2) Battery voltage low

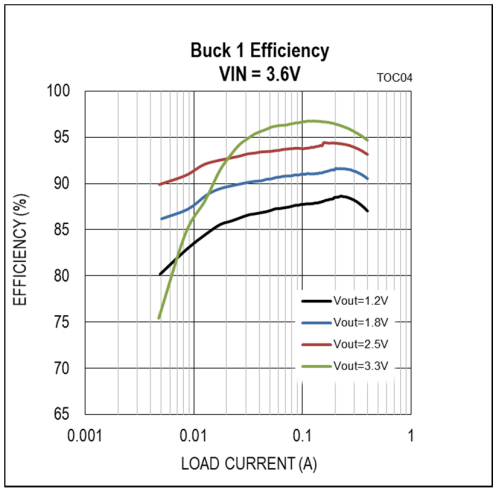
3) Battery removed/inserted

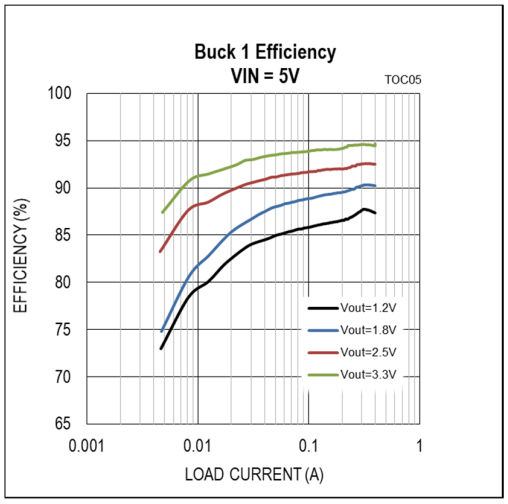
4) Charge source plugged/unplugged

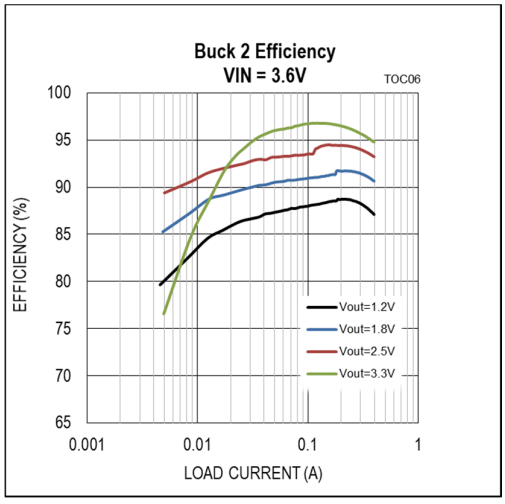
5) Charge condition / state change – Precondition, fast charge, top off and end of charge reached.

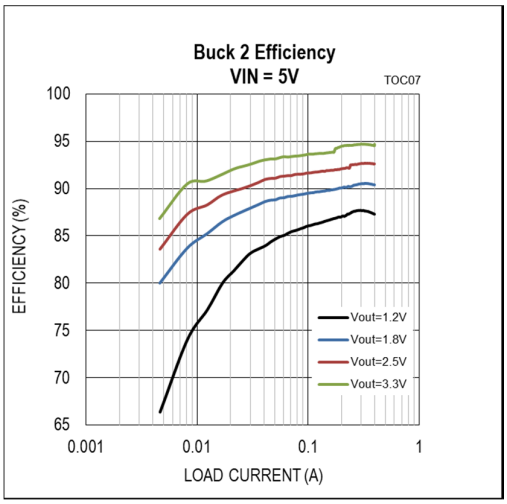
Typical Operating Characteristics

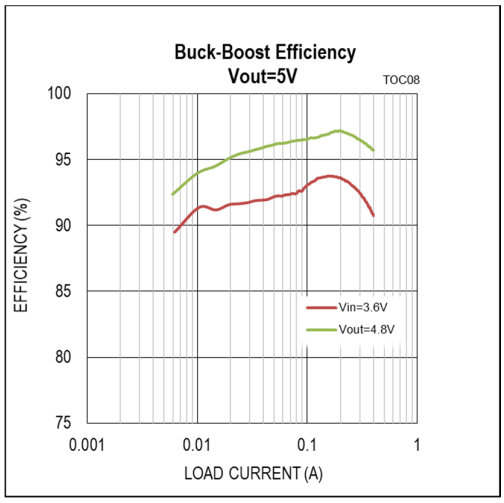


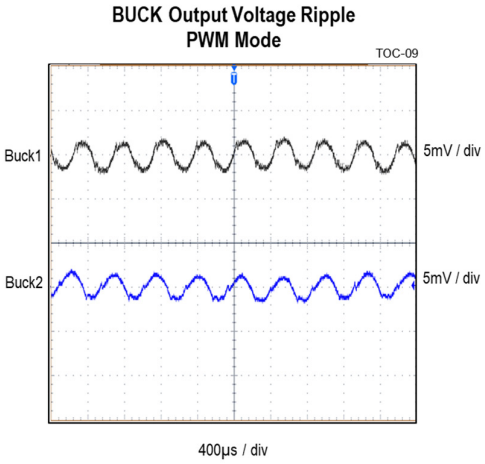


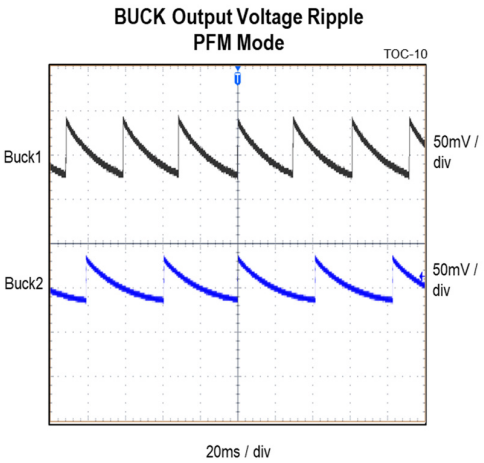


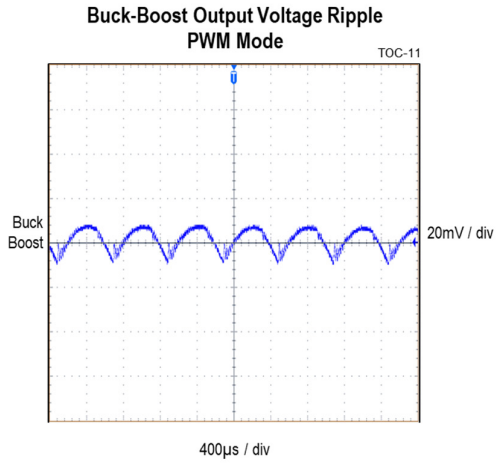


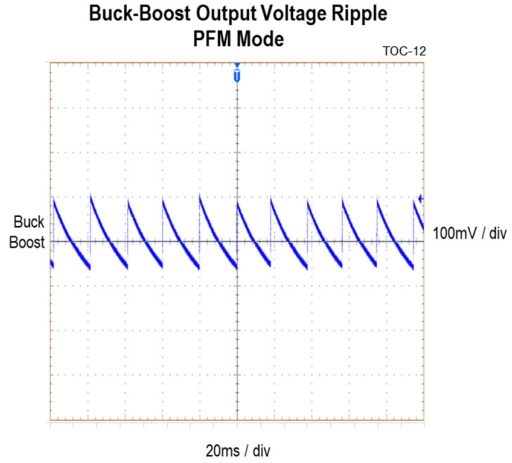


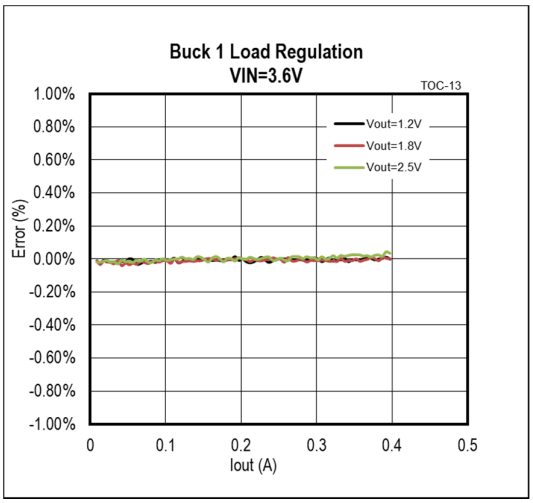


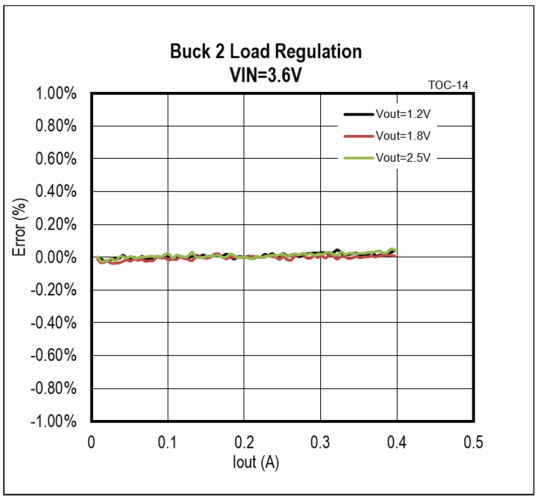


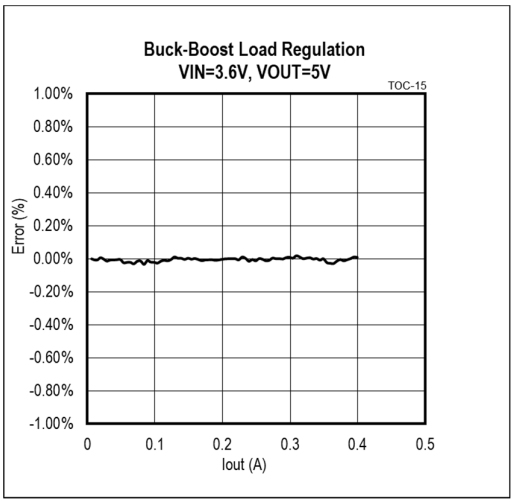


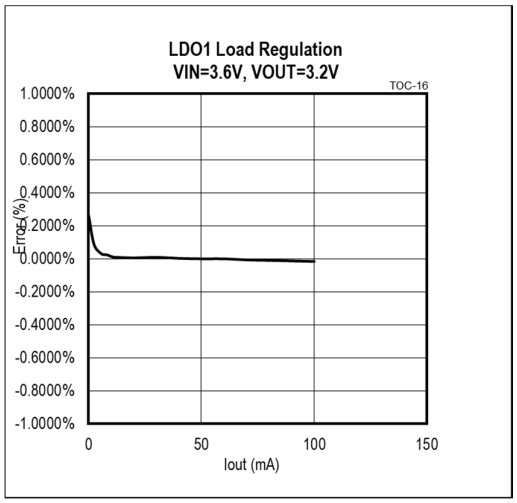


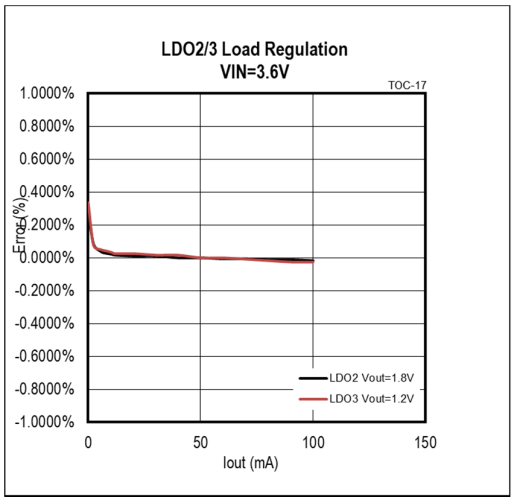


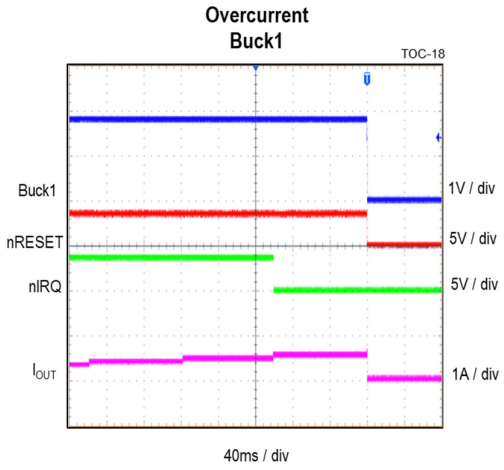




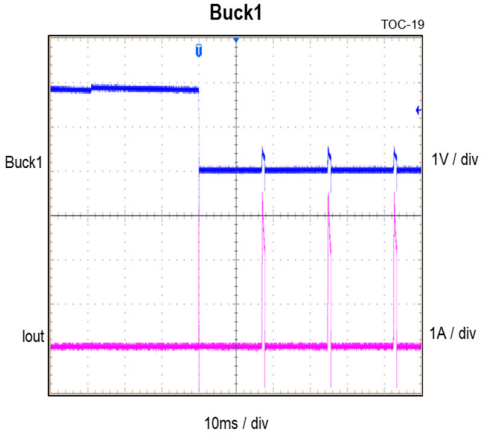




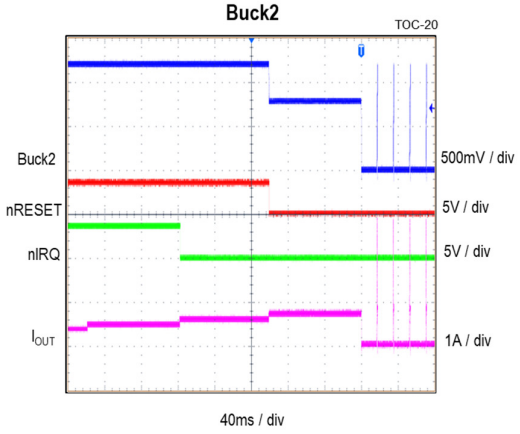




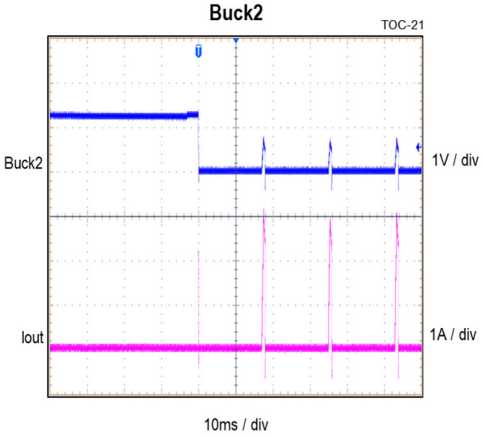
Short Circuit
Buck1



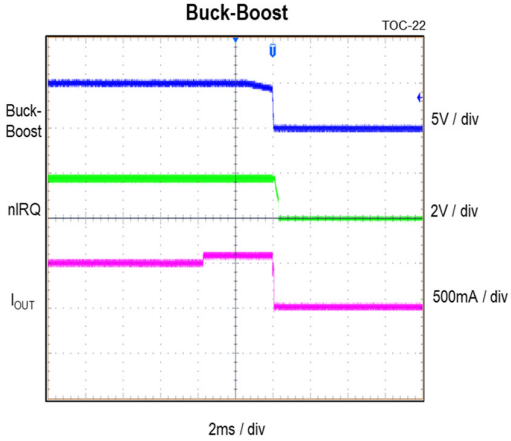
Overcurrent
Buck2



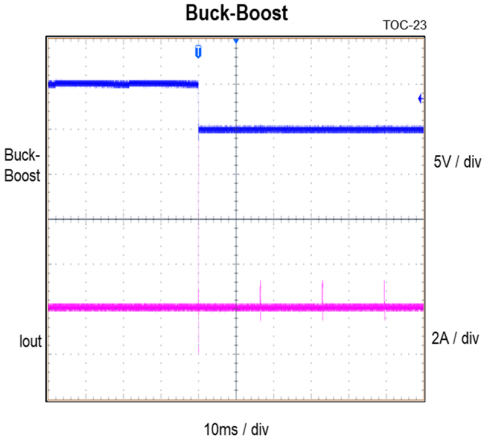
Short Circuit
Buck2



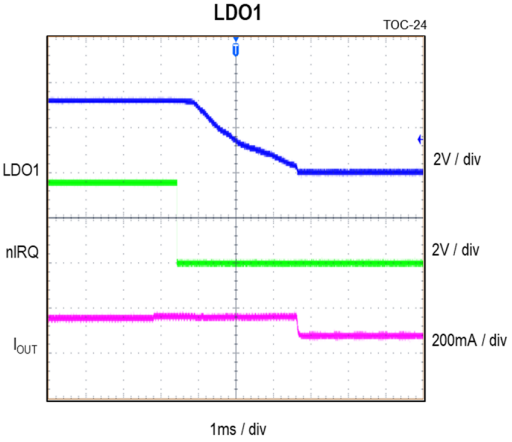
Overcurrent
Buck-Boost



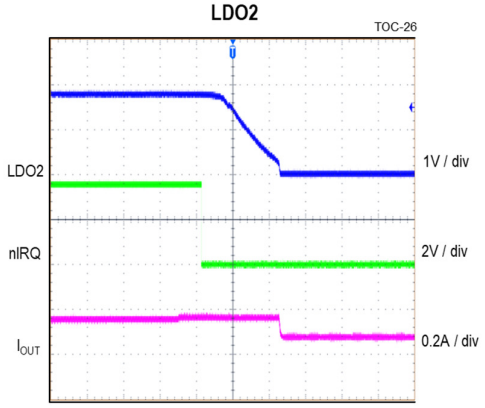
Short Circuit
Buck-Boost



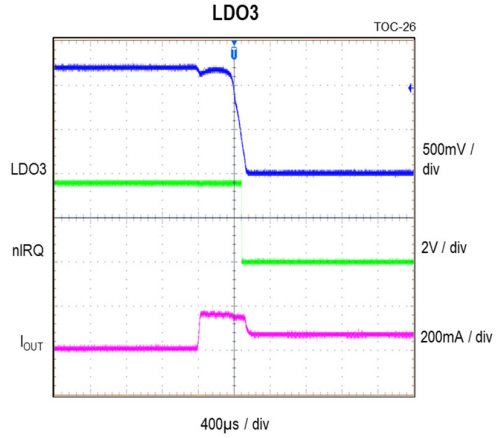
Overcurrent
LDO1



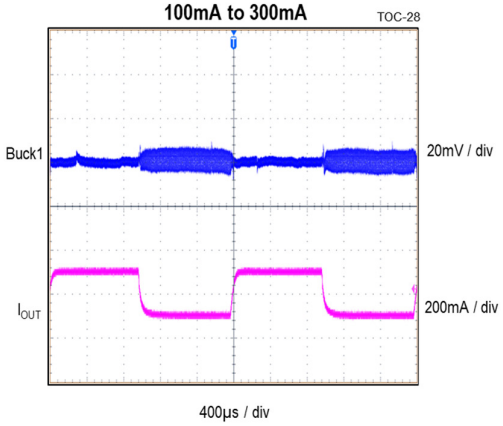
Overcurrent
LDO2



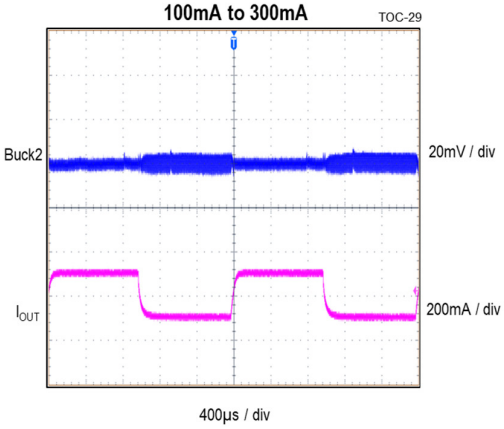
Overcurrent
LDO3



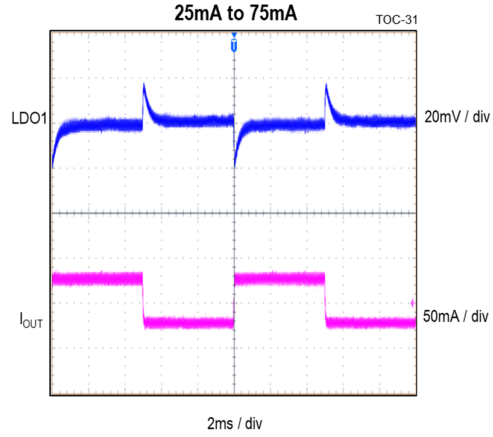
Load Transient
Buck1
100mA to 300mA



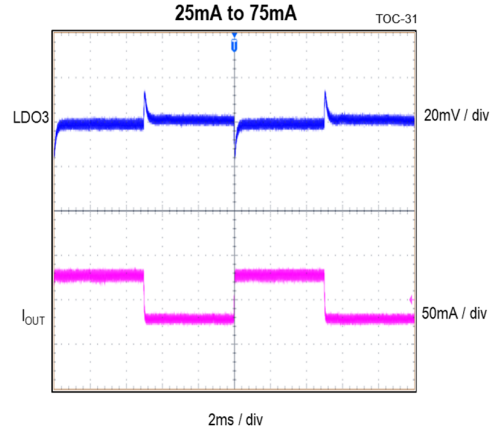
Load Transient
Buck2
100mA to 300mA



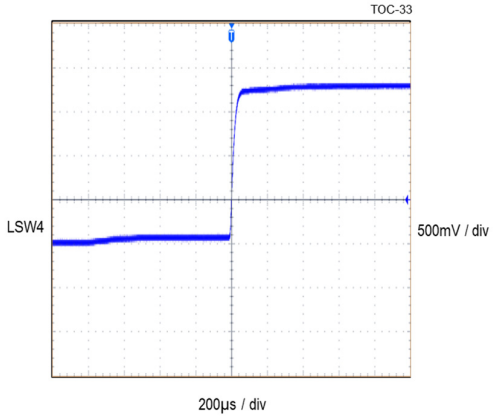
Load Transient
LDO1
25mA to 75mA



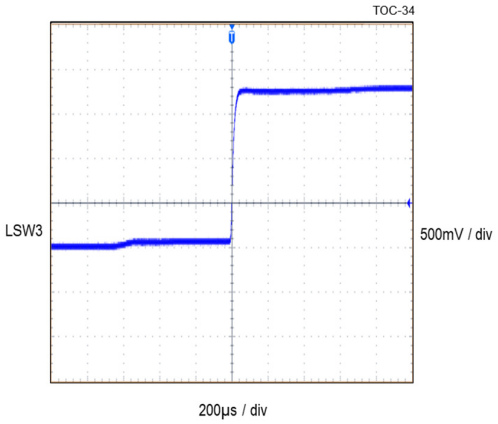
Load Transient
LDO3
25mA to 75mA



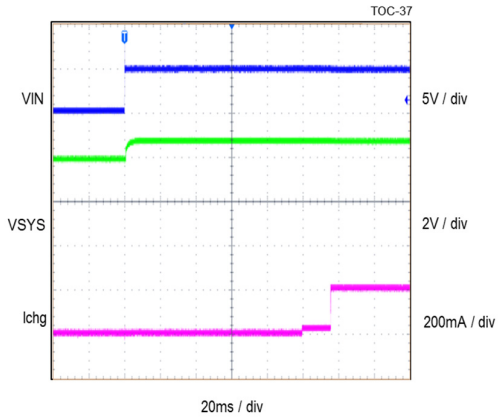
Load Switch Start up



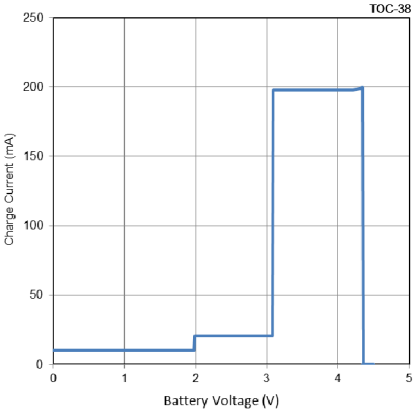
LDO3 Load Switch Mode Start up



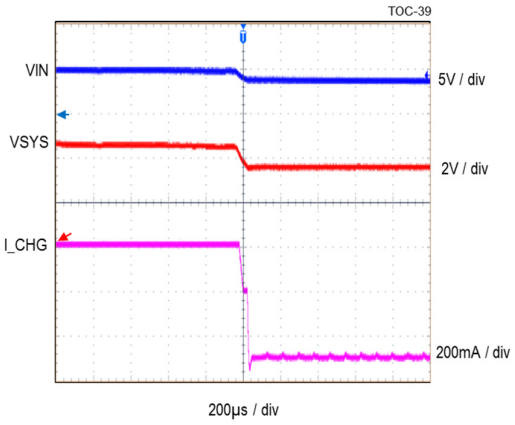
APLC Start up



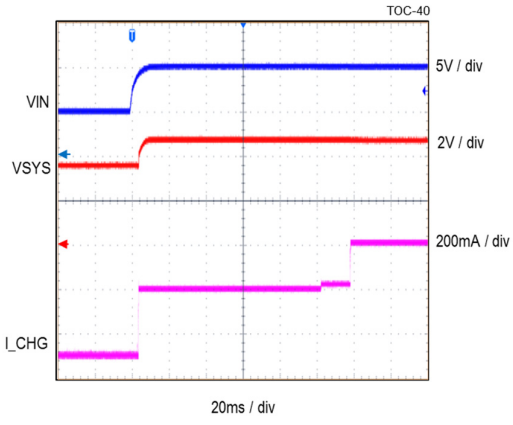
APLC V-I Curve



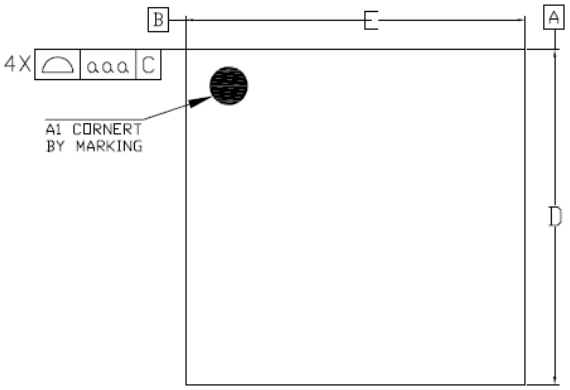
APLC VIN Removal



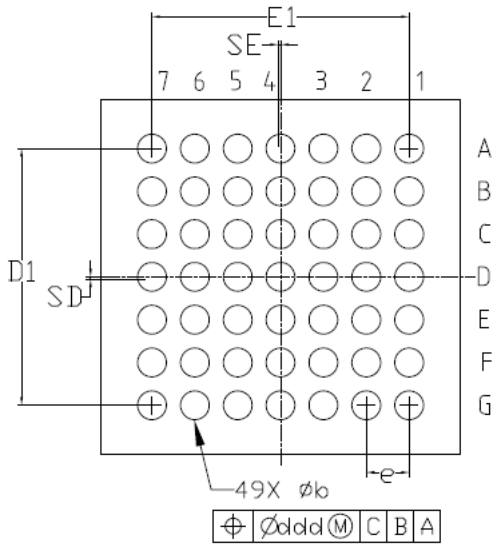
APLC VIN Applied



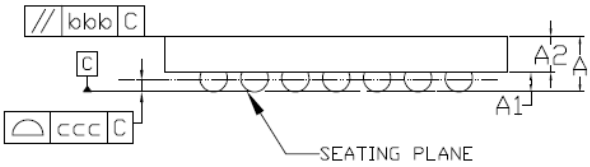
PACKAGE OUTLINE AND DIMENSIONS – 49 BALL WLCSP



Top View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.495	0.545	0.595
A1	0.165	0.190	0.215
A2	0.330	0.355	0.380
D	3.265	3.280	3.295
E	3.315	3.330	3.345
D1	2.350	2.400	2.450
E1	2.350	2.400	2.450
b	0.230	0.270	0.310
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		