TAOS Inc.

is now

ams AG

The technical content of this TAOS datasheet is still valid.

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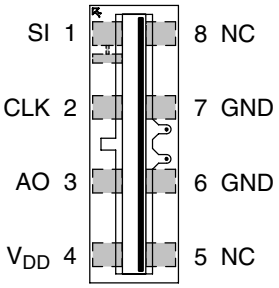
Please visit our website at **www.ams.com**

- **64 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 2000:1 (66 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 5 MHz**
- **Single 5-V Supply**
- **Replacement for TSL201, TSL201R, and TSL201R–LF**
- **RoHS Compliant**

CL PACKAGE
(TOP VIEW)



NC – No internal connection

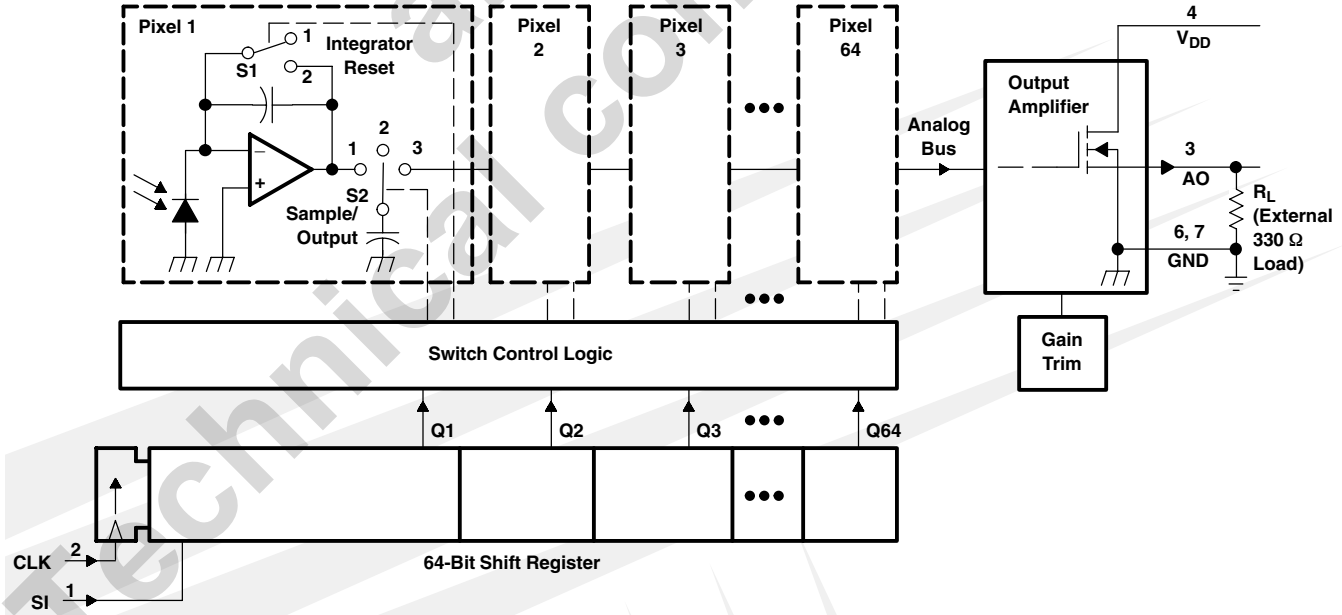
Package Drawing is Not to Scale

Description

The TSL201CL linear sensor array consists of a 64 × 1 array of photodiodes and associated charge amplifier circuitry. The pixels measure 120 μm (H) by 68 μm (W) with 125-μm center-to-center spacing and 57-μm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The TSL201CL is intended for use in a wide variety of applications including mark detection and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning as well as optical linear and rotary encoding.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	3	Analog output.
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
SI	1	Serial input. SI defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 64 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The integration time is the interval between two consecutive output periods.

The output and reset of the integrators is controlled by a 64-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI for one positive going clock edge (see Figures1 and 2)†. As the SI pulse is clocked through the 64-bit shift register, the charge on the sampling capacitor of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage output, AO. When the bit position goes low, the pixel integrator is reset. On the 65^{th} clock rising edge, the SI pulse is clocked out of the shift register and the output assumes a high-impedance state. Note that this 65^{th} clock pulse is required to terminate the output of the 64^{th} pixel and return the internal logic to a known state. A subsequent SI pulse can be presented as early as the 66^{th} clock pulse, thereby initiating another pixel output cycle.

The voltage developed at analog output (AO) is given by:

$$V_{out} = V_{drk} + (R_e)\ (E_e)\ (t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in $V/(\mu J/cm^2)$
- E_e is the incident irradiance in $\mu W/cm^2$
- t_{int} is integration time in seconds

AO is driven by a source follower that requires an external pulldown resistor (330-Ω typical). The output is nominally 0 V for no light input, 2 V for normal white-level, and 3.4 V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1 µF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

† For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . . –0.3 V to 6 V
Input voltage range, V_I . . . . . –0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . –20 mA to 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . –25 mA to 25 mA
Voltage range applied to any output in the high impedance or
power-off state, V_O . . . . . –0.3 V to V_{DD} + 0.3V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . –25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . . –40 mA to 40 mA
Analog output current range, I_O . . . . . –25 mA to 25 mA
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds‡ . . . . . 260°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Not recommended for solder reflow.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		5000	kHz
Sensor integration time, t_{int}	0.013		100	ms
Operating free-air temperature, T_A	0		70	°C
Load resistance, R_L	300		4700	Ω
Load capacitance, C_L			470	pF

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 16.5 μW/cm² (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 64 pixels)	see Note 1	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 64 pixels)	E_e = 0	0	50	120	mV
PRNU	Pixel response nonuniformity	See Notes 2 & 3		±4%	±7.5%	
	Nonlinearity of analog output voltage	See Note 3		±0.4%		FS
	Output noise voltage	See Note 4		1		mVrms
R_e	Responsivity (See Note 5)		18	23		V/(μJ/cm²)
SE	Saturation exposure	See Note 6		142		nJ/cm²
V_{sat}	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels, E_e = 0 See Note 7		25	120	mV
IL	Image lag	See Note 8		0.5%		
I_{DD}	Supply current, output idle			3.4	5	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			1	μA
I_{IL}	Low-level input current	V_I = 0			1	μA
$C_{i(SI)}$	Input capacitance, SI			5		pF
$C_{i(CLK)}$	Input capacitance, CLK			5		pF

NOTES:
1. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
2. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
3. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
4. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
5. $R_{e(min)} = [V_{out(min)} - V_{drk(max)}] \div (E_e \times t_{int})$
6. Minimum saturation exposure is calculated using the minimum V_{sat}, the maximum V_{drk}, and the maximum R_e.
7. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
8. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\,(IL)} - V_{drk}}{V_{out\,(white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 9)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 9 and Note 10)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns

NOTES:
9. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
10. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 10 pF		185		ns

TYPICAL CHARACTERISTICS

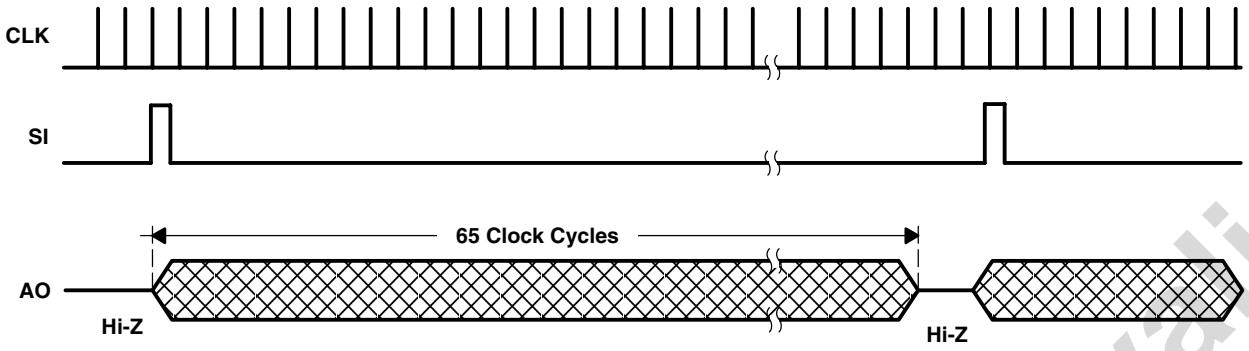


Figure 1. Timing Waveforms

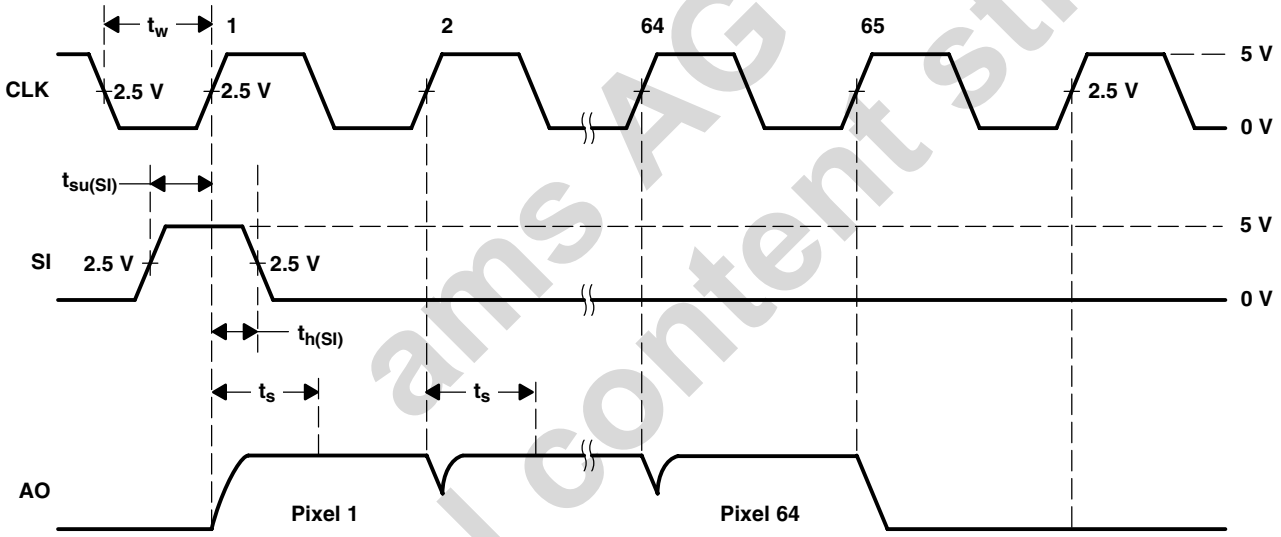


Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY

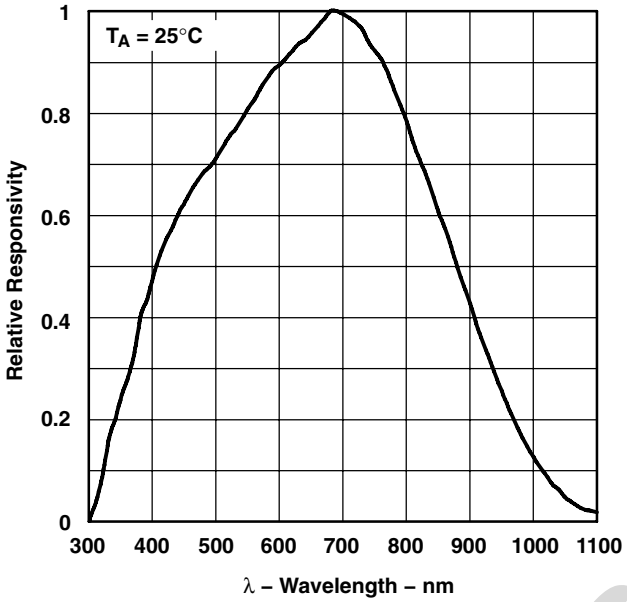


Figure 3

ANALOG OUTPUT SETTLING TIME vs LOAD CAPACITANCE AND RESISTANCE

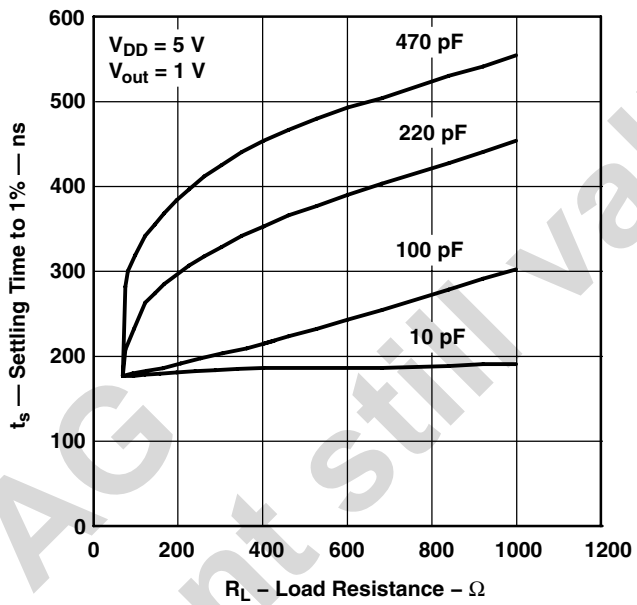


Figure 4

APPLICATION INFORMATION

Power Supply Considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads mounted close to the device package.

Integration Time

The integration time of the linear array is the period during which light is sampled and charge accumulates on each pixel's integrating capacitor. The flexibility to adjust the integration period is a powerful and useful feature of the TAOS TSL2xx linear array family. By changing the integration time, a desired output voltage can be obtained on the output pin while avoiding saturation for a wide range of light levels.

Each pixel of the linear array consists of a light-sensitive photodiode. The photodiode converts light intensity to a voltage. The voltage is sampled on the Sampling Capacitor by closing switch S2 (position 1) (see the functional block diagram on page 1). Logic controls the resetting of the Integrating Capacitor to zero by closing switch S1 (position 2).

At SI input (Start Integration), pixel 1 is accessed. During this event, S2 moves from position 1 (sampling) to position 3 (holding). This holds the sampled voltage for pixel 1. Switch S1 for pixel 1 is then moved to position 2. This resets (clears) the voltage previously integrated for that pixel so that pixel 1 is now ready to start a new integration cycle. When the next clock period starts, the S1 switch is returned to position 1 to be ready to start integrating again. S2 is returned to position 1 to start sampling the next light integration. Then the next pixel starts the same procedure. The integration time is the time from a specific pixel read to the next time that pixel is read again. If either the clock speed or the time between successive SI pulses is changed, the integration time will vary. After the final (n^{th}) pixel in the array is read on the output, the output goes into a high-impedance mode. A new SI pulse can occur on the (n+1) clock causing a new cycle of integration/output to begin. Note that the time between successive SI pulses must not exceed the maximum integration time of 100 msec.

The minimum integration time for any given array is determined by time required to clock out all the pixels in the array and the time to discharge the pixels. The time required to discharge the pixels is a constant. Therefore, the minimum integration period is simply a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time and reduces the maximum light level for saturation on the output. The minimum integration time shown in this data sheet is based on the maximum clock frequency of 5 MHz.

The minimum integration time can be calculated from the equation:

$$T_{int(min)} = \left(\frac{1}{maximum\ clock\ frequency}\right) \times n$$

where:

n is the number of pixels

In the case of the TSL201CL, the minimum integration time would be:

$$T_{int(min)} = 200ns \times 64 = 12.8\mu s$$

It is important to note that not all pixels will have the same integration time if the clock frequency is varied while data is being output.

APPLICATION INFORMATION

It is good practice on initial power up to run the clock (*n*+1) times after the first SI pulse to clock out indeterminate data from power up. After that, the SI pulse is valid from the time following (*n*+1) clocks. The output will go into a high-impedance state after the *n*+1 high clock edge. It is good practice to leave the clock in a low state when inactive because the SI pulse required to start a new cycle is a low-to-high transition.

The integration time chosen is valid as long as it falls in the range between the minimum and maximum limits for integration time. If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. If this occurs, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling window is active is to lower the output voltage level to prevent saturation. However, the integration time must still be greater than or equal to the minimum integration period.

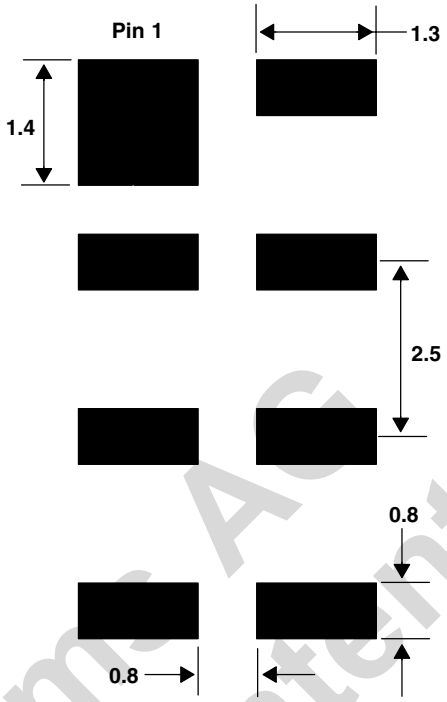
If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the integrating capacitors on the pixels can hold their accumulated charge. The maximum integration time should not exceed 100 ms for accurate measurements.

Although the linear array is capable of running over a wide range of operating frequencies up to a maximum of 5 MHz, the speed of the A/D converter used in the application is likely to be the limiter for the maximum clock frequency. The voltage output is available for the whole period of the clock, so the setup and hold times required for the analog-to-digital conversion must be less than the clock period.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested PCB pad layout guidelines for the CL package are shown in Figure 5.

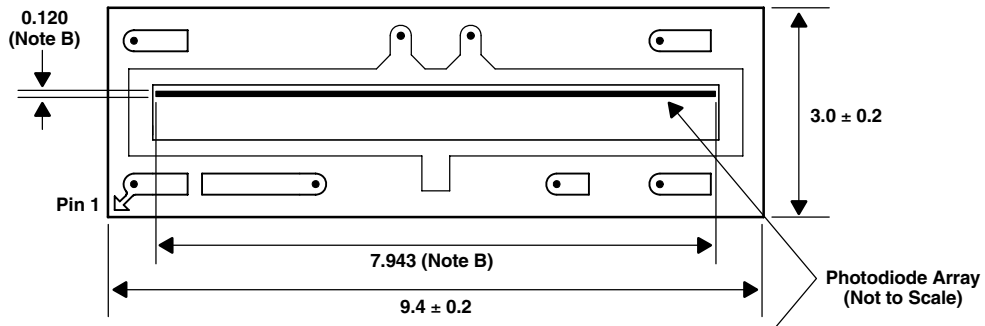


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

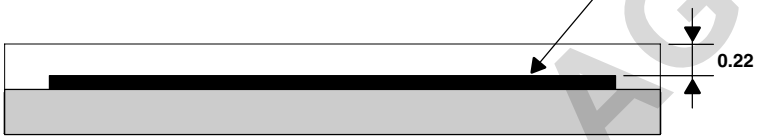
Figure 5. Suggested CL Package PCB Layout

PACKAGE INFORMATION

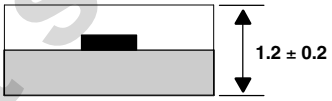
TOP VIEW



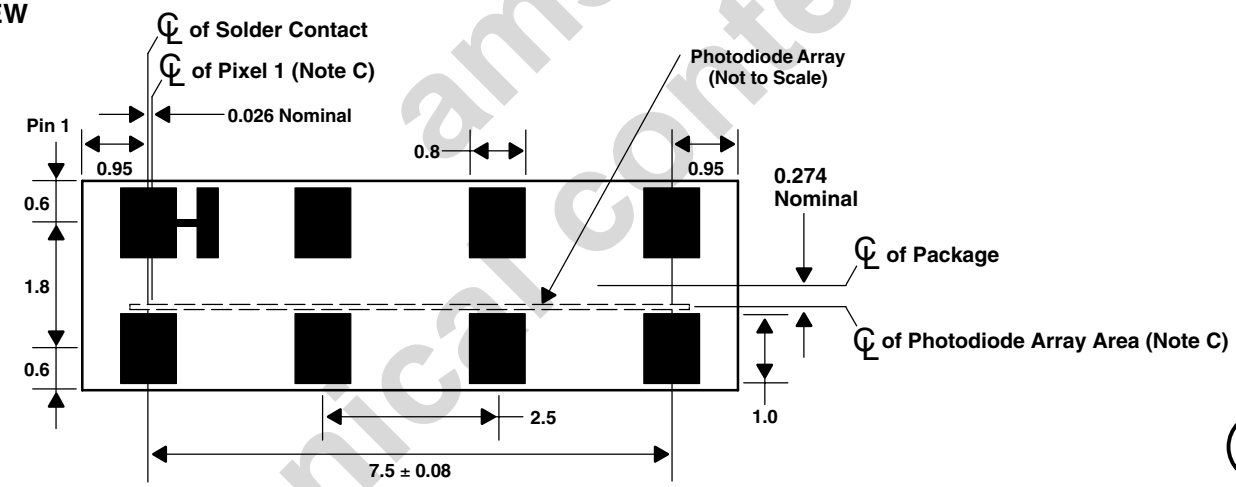
SIDE VIEW



END VIEW



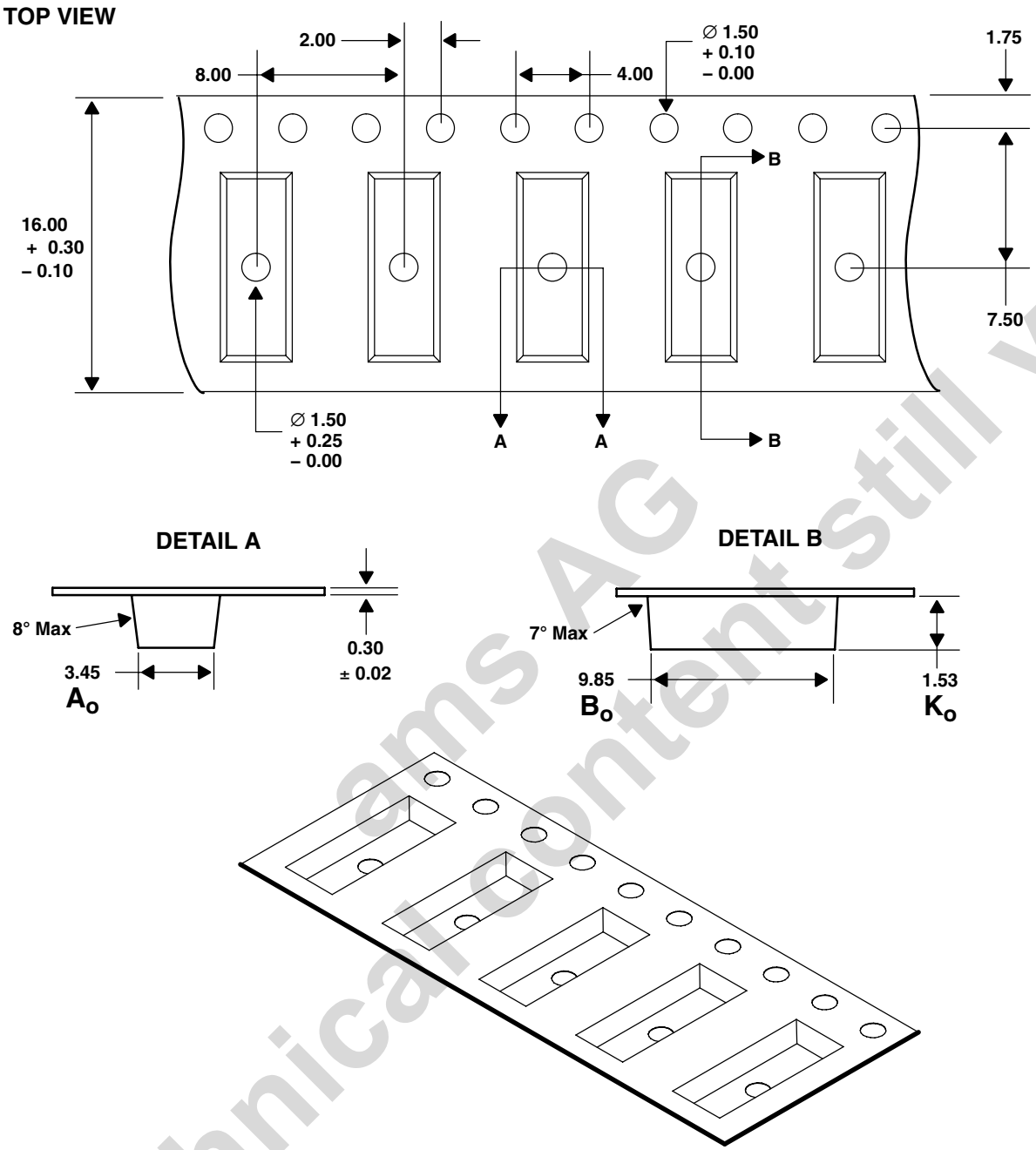
BOTTOM VIEW



NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
B. Nominal photodiode array dimension. The array is made up of 64 pixels with pixel #1 closer to Pin 1. Each pixel is 68 µm wide by 120 µm high, spaced on 125 µm centers.
C. The die is centered within the package within a tolerance of ± 0.05 mm.
D. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.56.
E. Contact finish is soft gold plated.
F. This package contains no lead (Pb).
G. This drawing is subject to change without notice.

Figure 6. Package CL Configuration

CARRIER TAPE AND REEL INFORMATION



NOTES:
A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 1000 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 7. Package CL Carrier Tape

SOLDERING INFORMATION

The CL package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 1. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

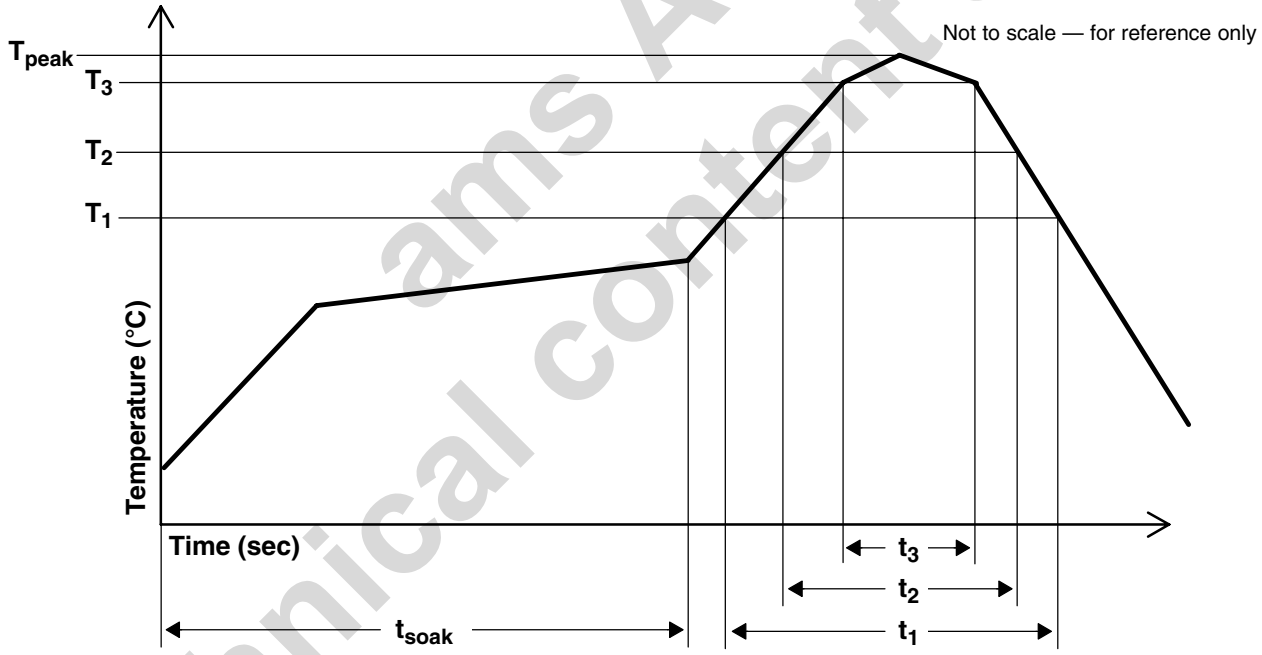


Figure 8. Solder Reflow Profile Graph

STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The CL package has been assigned a moisture sensitivity level of MSL 5a and the devices should be stored under the following conditions:

Temperature Range	5°C to 50°C
Relative Humidity	60% maximum
Total Time	6 months from the date code on the aluminized envelope — if unopened
Opened Time	24 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 24 hours. If rebaking is required, it should be done at 60°C for 24 hours.

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Green (RoHS & no Sb/Br) TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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