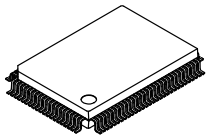
Compressed Audio Signal Processor IC with USB Host Controller

LC786820E

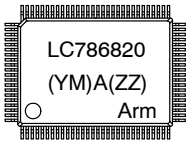
ON Semiconductor®

www.onsemi.com



PQFP100 14x20
CASE 122BV

MARKING DIAGRAM



LC786820	= Specific Device Code
Y	= Year of Production
M	= Assembly Operation
A	= Assembly Site
ZZ	= Assembly Lot Number

Overview

The LC786820E integrates Arm7TDMI−S®, USB host processing, SD memory card host processing, compressed audio decode processing, audio signal processing and a flash memory which stores the program for Arm7TDMI−S and the various data. The sophisticated programs in the flash memory for the USB host processing for the SD memory card processing or audio signal processing etc. make the process of external main microcontroller easier and very helpful to develop a much features/high performance audio player system.

Main Features

- USB Host/Device Function (Full Speed: 12 Mbps), SD Memory Card Host Function
- MP3*, WMA*, AAC*, FLAC*, SBC* Decoder Processing Function
- Audio Input Functions such as Analog (Stereo 3ch)/Digital 3ch Input (Sampling Rate Convertible)
- Audio Processing Functions such as 20 Bands Equalizer (Stereo 1ch), Subwoofer Processing, High−frequency Range Extendable Filter and etc.
- Audio Output Functions such as Electronical Volume Output 5 ch (for LF, LR, RF, RR, SW), or DAC Output 3ch (Lch, Rch, SW)
- Arm7TDMI−S as Internal CPU Core, Flash Memory for Program and Various Data Storage
- Operational Voltage Source: 3.3 V Single Power Supply
- Operational Temperature: −40 to +85°C
- Package: QIP100E (14×20) Pb−Free and Halogen Free type
- This Device is Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

- MP3
  MPEG Layer−3 Audio Coding
- WMA
  Windows Media Audio
- AAC
  Advanced Audio Coding
- FLAC
  Free Lossless Audio Codec

Detail Functions
[Compressed Audio Functions]

<Audio Processing Block>

- MP3 decode (ISO/IEC 11172−3, ISO/IEC 13818−3)
  - Supported sampling rate : MPEG1−Layer1/2/3 (32 kHz, 44.1 kHz, 48 kHz)
    MPEG2−Layer1/2/3 (16 kHz, 22.05 kHz, 24 kHz)
    MPEG2.5−Layer3 (8 kHz, 11.025 kHz, 12 kHz)
  - Supported bit rate : All Bit Rate (Variable Bit Rate support)
  - MPEG header read supported
- WMA decode (Version 9.2 standard)
  - Supported sampling rate : 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz
  - Supported bit rate : 5 kbps to 384 kbps (Variable Bit Rate support)
- AAC decode (ISO/IEC 14496−3, ISO/IEC 13818−7)
  - Profile : MPEG4−AAC−LowComplexity
  - Supported sampling rate : 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz
  - Supported bit rate : Monaural 8 kbps to 160 kbps (Variable bit rate support)
    Stereo 16 kbps to 320 kbps (Variable bit rate support)
  - *Depending on the condition, sampling rate can be supported up to 96kHz.
- FLAC decode (FLAC 1.3.0)
  - Supported format : Block size: up to 4608
    Quantized number of bits: 8/16/24 bit per sample
  - Supported sampling rate : 8 kHz to 48 kHz
  - Supported channel : 1/2ch

[Audio Processing Functions]

<Audio Data Digital Processing Block>

- Equalizer function
  Supports max of 20−band (stereo 1ch) and unused band can be used for not only the voice output but also used for other processing
- Supports signal processing for subwoofer
- Sampling conversion (Fs = 32/44.1/48 kHz) when playing compressed audio, High band extended processing supported
- Mute (−∞/−12 dB), attenuator
- De−emphasis filter
- Embedded level/peak hold circuit and can hold up to 8 data
- Noise cancel/Echo cancel function
  Supports noise cancel/echo cancel at Fs = 8 kHz
- Supports input/output of Fs = 16 kHz voice data

<Audio Input Processing Block>

- Analog Audio data input (3−channels by stereo)
  - Single Ended input : 2 channels
  - Differential input : 1 channel
  - Input Gain : −12.5 dB to +18.5 dB (1 dB step)
  - 24 bit accuracy AD converter
- Digital audio input (Stereo input: Max of 3 channels)
  - Supports digital 3−line (LR clock, bit clock, audio data) connection and clock can be master or slave
  - Data format supports IIS/MSB first right justified and etc.
  - Input data can support 8 kHz to 96 kHz, and by sampling conversion, converts to the suitable Fs (Playback Fs = 32/44.1/48 kHz etc.)

<Audio Output Processing Block>

- Analog Audio data output (One channel for stereo, and one channel for Sub−Woofer)
  - Eight−fold over−sampling digital filter (24 bit)
  - Secondary LPF for audio output
- Electronic Volume/Fader
  - 5ch outputs (Lch−Front (LF)/Rear (LR), Rch−Front (RF)/Rear (RR), Sub−Woofer)
  - Output Range: 0dB to −0dB, −∞
    - 0 dB to −32 dB : Analog control, 0.25 dB step
    - −32 dB to −70 dB : Analog control, 1.0 dB step
    - −70 dB to −90 dB : Digital attenuator control
  - Decrease the noise at the volume change timing by the digital and analog composite control.
  - Individual output for 5 channels control is available
- Digital Audio data output
  - Digital 3−line interface with IIS/MSB first right justification and etc.
    - LR clock, Bit clock, Data 1
    - Clock can be master or slave
    - Capable of outputting 384 Fs clock

[External Interface Functions]

<USB Host/Device Control Block>

- Open Host Controller Interface 1.0a
- Universal Serial Bus Specification 2.0 Full Speed
- Supports four kinds of transfer type (Control/Bulk/Interrupt/Isochronous)
- Supports 2 Ports. USB1 = Host or Device, USB2 = Host only
- USB Charger (USB1 only)
  - Supports detection of CDP (Charging Downstream Port) of USB Charger Specification 1.2
  - Charge (supplying current) is not supported
- PHY block: Internal Pull−Down/Pull−Up resistors built−in

<SD Memory Card Host Control Block>

- Multimedia Card Specification v2.11
- Secure Digital Memory Card Physical Layer Specification v0.96
  - * Individual contract is necessary to use SD memory card controller.

[Internal Microcontroller Functions]

<*Sequencer Control*>
- USB, SD memory card playback/write control
  USB/SD files analysis, etc.
- Audio playback control
  Compressed audio playback control, various filter control and etc.

<*Communication Control between Main Controller*>
- Main communication format is SIO (4−line)
- Capable of direct control of oscillation stop/start from main microcontroller
- Capable of some special command can be used even when oscillation is stopped

<*Peripheral Interface Block*>

♦ GPIO ports	37 ports maximum (Shared with other functions. Some part of pins can be used even when the clock is halted)	
♦ External interrupt pins	4 pins maximum (Shared with other functions)	
♦ Serial interface		
SIO	clock synchronized full duplex (3 lines)	3 channels
UART	full duplex	2 channels
IIC	master function	1 channel

<*Program Memory Block*>
- Program memory for the internal sequencer built−in
  Program version up from the external media (USB and etc.) or main controller is available.

<*Others*>
- Watch Dog Timer
  Notify to outside from the pin or internal reset.
- Sleep Mode (2 kinds)
  (1) Only CPU core operates at slow clock and clocks for other blocks are stopped.
  (2) All clocks are stopped by the main microcontroller control.

[Useful Functions for CD−DSP IC Connection Usage]

<*CD TEXT Processing Block*>
- Buffers CD−TEXT data
- Starts buffering from desired ID3/ID4 of CD−TEXT data.
  * Neeccessary to connect subcode synchronization signals (SBSY and SFSY), shift clock (SBCK) and data (PW).

<*CD−ROM Processing Block*>
- Up to 4× speed operation available
- Supports CD−ROM decoding (Mode1, Mode2 <form1, form2>)
- Supports output of CD−ROM decoded data
  * Neccessary to connect three signals (LRCK, BCK and DATA).
  It is possible if desired to connect C2 error flag.

[Others]

<*Internal Power Supply*>
- Regulator for internal blocks (V_{DD} for internal = 1.2 V, V_{DD} for Flash = 1.8 V) built−in

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Item	Symbol	Pin Name	Condition	Ratings	Unit
Maximum supply voltage	V_{DD} max	DVDD, AVDD1, AVDD2, XVDD, VVDD2		−0.3 to +3.95	V
Input voltage	V_{IN}	All digital input pins		−0.3 to DVDD+0.3	
Output voltage	V_{OUT}	All digital output/input−output pins		−0.3 to DVDD+0.3	
Allowable power dissipation	Pd max		Ta ≤ 85°C Mounted reference PCB(*)	519	mW
Operating temperature	Topr			−40 to +85	°C
Storage temperature	Tstg			−40 to +125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Reference PCB: 114.3mm × 76.1mm × 1.6mm, glass epoxy resin.

ALLOWABLE OPERATING RANGES at T_A = −40°C to 85°C, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Item	Symbol	Pin Name	Condition	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}1	DVDD, AVDD1, AVDD2, XVDD, VVDD2		3.00		3.60	V
High−level input voltage	V_{IH}	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, JTMS, JTRSTB, JTCK, JTDI, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	Schmitt	2.00		V_{DD}1	
Low−level input voltage	V_{IL}	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, JTMS, JTRSTB, JTCK, JTDI, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53, TEST0, TEST1	Schmitt	0.00		0.80	
Oscillator Frequency	FX	XIN	Oscillator circuit		12.0000		MHz
		XOUT					

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = −40°C to 85°C, $V_{DD}1$ = 3.0 V to 3.6 V, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Item	Symbol	Pin Name	Condition	MIN	TYP	MAX	Unit
Current drain	$I_{DD}1$	DVDD, AVDD1, AVDD2, XVDD, VVDD2			100	150	mA
High−level input current	I_{IH}	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, JTMS, JTRSTB, JTCK, JTDI, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	Schmitt $V_{IN} = V_{DD}1$ Built−in Pull−down resistor OFF			10.00	μA
Low−level input current	I_{IL}	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53, JTMS, JTRSTB, JTCK, JTDI, TEST0, TEST1	Schmitt V_{IN} = 0.0 V	−10.00			
High−level output voltage	V_{OH}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP15, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	CMOS I_{OH} = −2 mA	$V_{DD}1$ −0.6			V
	V_{OH}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, JTDO, JTRTCK	CMOS I_{OH} = −4 mA				
Low−level output voltage	V_{OL}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP15, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	CMOS I_{OL} = 2 mA			0.40	V
	V_{OL}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, JTDO, JTRTCK	CMOS I_{OL} = 4 mA			0.40	V
Built−in Pull−down resistor	RPD	SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53		50	100	200	kΩ

ELECTRICAL CHARACTERISTICS at T_A = −40°C to 85°C, $V_{DD}1$ = 3.0 V to 3.6 V, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Item	Symbol	Pin Name	Condition	MIN	TYP	MAX	Unit
Output off−leakage current	IOFF (1)	AFILT	Hi−Z Out	−10.00		10.00	μA
	IOFF (2)	SIFDO	Hi−Z Out	−10.00		10.00	
Charge pump output current	IAFH	AFILT			195.0		μA
	IAFL	AFILT			195.0		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Place an internal pull−down resistor or external pull−down resistor or external pull−up resistor to the SIFDO pin if its output condition is set to 3−State mode.

PIN ASSIGNMENT

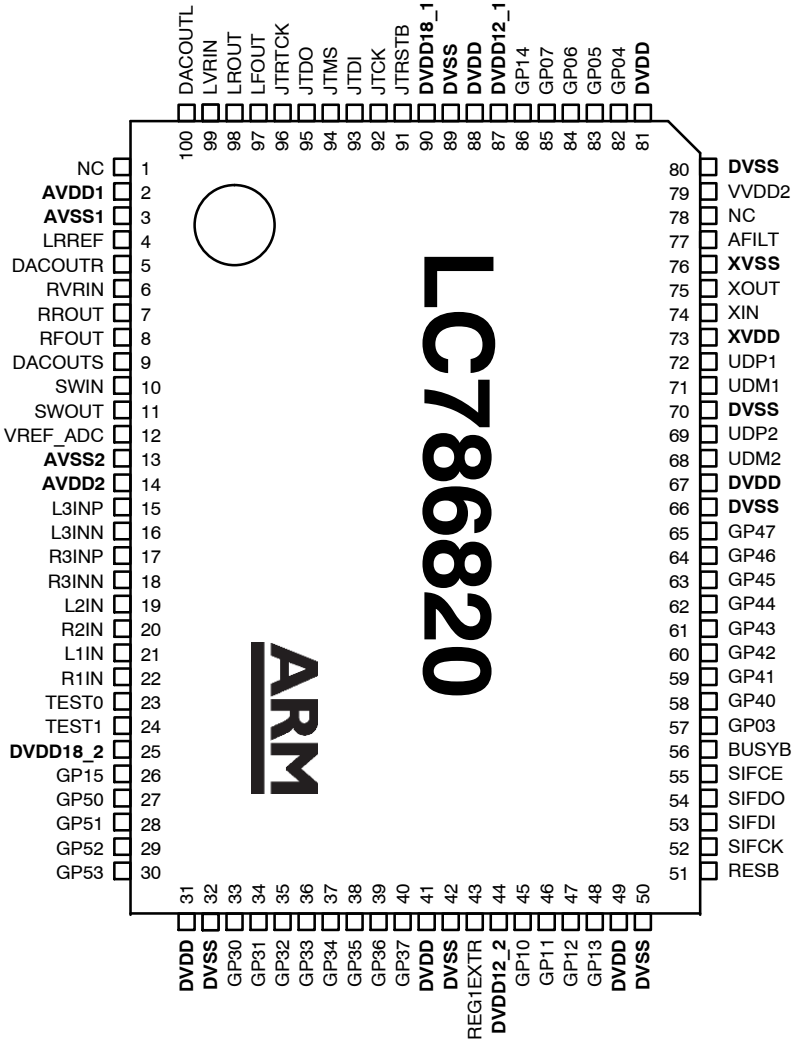


Figure 1. Pin Assignment

PIN DESCRIPTION

Pin No.	Pin name	I/O	State when "Reset"	Function
1	NC	–	–	NC pin. This pin must be left open
2	AVDD1	–	–	Analog system (ADC) power supply
3	AVSS1	–	–	Analog system (ADC) ground. This pin must be connected to the 0 V level
4	LRREF	AO	AVDD1/2	Capacitor connection pin for reference voltage for Audio DAC and Electronic Volume
5	DACOUTR	AO	Unknown	Audio DAC : Right channel output
6	RVRIN	AI	Input	Electronic Volume : Right channel volume input
7	RROUT	AO	Unknown	Electronic Volume : Right channel Rear output
8	RFOUT	AO	Unknown	Electronic Volume : Right channel Front output
9	DACOUTS	AO	Unknown	Audio DAC : Sub−Woofer output
10	SWIN	AI	Input	Electronic Volume : Sub−Woofer volume input
11	SWOUT	AO	Unknown	Electronic Volume : Sub−Woofer output
12	VREF_ADC	AO	AVDD2/2	Capacitor connection pin for audio ADC reference voltage
13	AVSS2	–	–	Analog system (ADC) ground. This pin must be connected to the 0V level
14	AVDD2	–	–	Analog system (ADC) power supply
15	L3INP	AI	Input	Analog stereo Left channel Differential input (Positive) / Analog stereo Left channel Single Ended input
16	L3INN	AI	Input	Analog stereo Left channel Differential input (Negative)
17	R3INP	AI	Input	Analog stereo Right channel Differential input (Positive) / Analog stereo Right channel Single Ended input
18	R3INN	AI	Input	Analog stereo Right channel Differential input (Negative)
19	L2IN	AI	Input	Analog stereo Left channel Single Ended input
20	R2IN	AI	Input	Analog stereo Right channel Single Ended input
21	L1IN	AI	Input	Analog stereo Left channel Single Ended input
22	R1IN	AI	Input	Analog stereo Right channel Single Ended input
23	TEST0	I	Input	Test input. This pin must be connected to the 0 V level.
24	TEST1	I	Input	Test input. This pin must be connected to the 0 V level.
25	DVDD18_2	AO	H	Capacitor connection pin for internal regulator (1.8 V for Flash)
26	GP15	I/O	Input(L)	General purpose I/O port with pull down resistor Various signal monitoring output
27	GP50	I/O	Input(L)	General purpose I/O port with pull down resistor LR clock input/output 1 for Audio interface LR clock input 1 for Stream data interface Transmit data output for serial communication 3 (exclusive with GP34) Over current detection signal input for USB 1 (exclusive with GP44)
28	GP51	I/O	Input(L)	General purpose I/O port with pull down resistor Bit clock input/output 1 for Audio interface Bit clock input/output 1 for Stream data interface Master clock output for serial communication 3 (exclusive with GP35) Power supply signal output for USB 1 (exclusive with GP45)
29	GP52	I/O	Input(L)	General purpose I/O port with pull down resistor Data input/output 1 for Audio interface Data input 1 for Stream data interface Receive data input for serial communication 3 (exclusive with GP36) Over current detection signal input for USB 2 (exclusive with GP46)
30	GP53	I/O	Input(L)	General purpose I/O port with pull down resistor Clock (Fs384) input/output 1 for Audio DAC Request flag input/output 1 for Stream data interface Power supply signal output for USB 2 (exclusive with GP47)

PIN DESCRIPTION (continued)

Pin No.	Pin name	I/O	State when "Reset"	Function
31	DVDD	–	–	Digital system power supply
32	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level
33	GP30	I/O	Input(L)	General purpose I/O port with pull down resistor UART2 data transmit (exclusive with GP46) External interruption function 3 (exclusive with GP13, GP31, GP43 and GP47) LR clock input/output 2 for Audio interface LR clock input 2 for Stream data interface
34	GP31	I/O	Input(L)	General purpose I/O port with pull down resistor UART2 data receive (exclusive with GP47) External interruption function 3 (exclusive with GP13, GP30, GP43 and GP47) Bit clock input/output 2 for Audio interface Bit clock input/output 2 for Stream data interface
35	GP32	I/O	Input(L)	General purpose I/O port with pull down resistor Data 1 input/output for SD memory card Data input/output 2 for Audio interface Data input/output 2 for Stream data interface
36	GP33	I/O	Input(L)	General purpose I/O port with pull down resistor Data 0 input/output for SD memory card Clock(Fs384) input/output 2 for Audio DAC Request flag input/output 2 for Stream data interface
37	GP34	I/O	Input(L)	General purpose I/O port with pull down resistor Clock output for SD memory card Transmit data output for serial communication 3 (exclusive with GP50) Block synchronization signal (SBSY) input for CD subcode (exclusive with GP44)
38	GP35	I/O	Input(L)	General purpose I/O port with pull down resistor Command input/output for SD memory card Master clock output for serial communication 3 (exclusive with GP51) Frame synchronization signal (SFSY) input for CD subcode (exclusive with GP45)
39	GP36	I/O	Input(L)	General purpose I/O port with pull down resistor Data 3 input/output for SD memory card Receive data input for serial communication 3 (exclusive with GP52) Data (PW) input for CD subcode (exclusive with GP46)
40	GP37	I/O	Input(L)	General purpose I/O port with pull down resistor Data 2 input/output for SD memory card Data transmit clock (SBCK) output for CD subcode (exclusive with GP47)
41	DVDD	–	–	Digital system power supply
42	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
43	REG1EXTR	AO	Unknown	Reserved pin for internal regulator. This pin must be left open.
44	DVDD12_2	AO	H	Capacitor connection pin for internal regulator (1.2 V for internal)
45	GP10	I/O	Input(L)	General purpose I/O port with pull down resistor UART1 data transmit (exclusive with GP06) IIC (master) clock output (exclusive with GP04 and GP40)
46	GP11	I/O	Input(L)	General purpose I/O port with pull down resistor UART1 data receive (exclusive with GP07) IIC (master) data input/output (exclusive with GP05 and GP41)

PIN DESCRIPTION (continued)

Pin No.	Pin name	I/O	State when "Reset"	Function
47	GP12	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 2 (exclusive with GP42 and GP46) Clock control input 1 Watch Dog Timer state monitor output
48	GP13	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 3 (exclusive with GP30, GP31, GP43 and GP47) Clock control input 2 Watch Dog Timer state monitor output
49	DVDD	–	–	Digital system power supply
50	DVSS	–	–	Digital system ground. This pin must be connected to the 0 V level
51	RESB	I	–	IC reset input ("L"−active) This pin must be set low once after power is first applied.
52	SIFCK	I	Input	Host−I/F Data transmit clock input for serial communication 1 Data transmit clock input for IIC communication
53	SIFDI	I/O	Input	Host−I/F Data input for serial communication 1 Data input/output for IIC communication
54	SIFDO	I/O	Input	Host−I/F Data output for serial communication 1 (CMOS or 3−State output) General purpose I/O port with pull down resistor (GP00)
55	SIFCE	I/O	Input	Host −I/F Enable signal input for serial communication 1 ("H"−active) General purpose I/O port with pull down resistor (GP01)
56	BUSYB	I/O	Input(L)	Host −I/F System busy signal output ("L"−active) General purpose I/O port with pull down resistor (GP02) External interruption function 0 (exclusive with GP40 and GP44)
57	GP03	I/O	Input(L)	General purpose I/O port with pull down resistor Watch Dog Timer state monitor output USB device detection flag output External interruption function 1 (exclusive with GP14, GP41 and GP45)
58	GP40	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 0 (exclusive with GP02 and GP44) IIC (master) clock output (exclusive with GP04 and GP10) LR clock input/output 3 for Audio interface LR clock input 3 for Stream data interface
59	GP41	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 1 (exclusive withGP03, GP14 and GP45) IIC (master) data input/output (exclusive with GP05 and GP11) Bit clock input/output 3 for Audio interface Bit clock input/output 3 for Stream data interface
60	GP42	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 2 (exclusive with GP12 and GP46) Watch Dog Timer state monitor output Data input/output 3 for Audio interface Data input/output 3 for Stream data interface

PIN DESCRIPTION (continued)

Pin No.	Pin name	I/O	State when "Reset"	Function
61	GP43	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 3 (exclusive with GP13, GP30, GP31 and GP47) Clock (Fs384) input/output 3 for Audio DAC Request flag input/output 3 for Stream data interface
62	GP44	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 0 (exclusive with GP02 and GP40) Over current detection signal input for USB 1(exclusive with GP50) Block synchronization signal (SBSY) input for CD subcode (exclusive with GP34)
63	GP45	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 1 (exclusive withGP03, GP14 and GP41) Power supply signal output for USB 1(exclusive with GP51) Frame synchronization signal (SFSY) input for CD subcode (exclusive with GP35)
64	GP46	I/O	Input(L)	General purpose I/O port with pull down resistor UART2 data transmit (exclusive with GP30) External interruption function 2 (exclusive with GP12 and GP42) Over current detection signal input for USB 2 (exclusive with GP52) Emphasis flag input/output for Audio (exclusive with GP14) Data (PW) input for CD subcode (exclusive with GP36)
65	GP47	I/O	Input(L)	General purpose I/O port with pull down resistor UART2 data receive (exclusive with GP31) External interruption function 3 (exclusive with GP13, GP30, GP31 and GP43) Power supply signal output for USB 2 (exclusive with GP53) CD_C2 error flag input (exclusive with GP14) Data transmit clock (SBCK) output for CD subcode (exclusive with GP37)
66	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
67	DVDD	–	–	Digital system power supply
68	UDM2	I/O	–	USB data input/output 2 D– signal connection
69	UDP2	I/O	–	USB data input/output 2 D+ signal connection
70	DVSS	–	–	Digital system ground. This pin must be connected to the 0 V level
71	UDM1	I/O	–	USB data input/output 1 D– signal connection Charge detection (CDP detection) input/output 1
72	UDP1	I/O	–	USB data input/output 1 D+ signal connection Charge detection (CDP detection) input/output 1
73	XVDD	–	–	Oscillator power supply
74	XIN	I	Oscillation	X'tal oscillator connection
75	XOUT	O	Oscillation	X'tal oscillator connection
76	XVSS	–	–	Oscillator ground. This pin must be connected to the 0 V level
77	AFILT	AO	Unknown	PLL2 charge pump output (for filter connection)
78	NC	–	–	NC pin. This pin must be left open.
79	VVDD2	–	–	PLL2 power supply
80	DVSS	–	–	Digital system ground. This pin must be connected to the 0 V level
81	DVDD	–	–	Digital system power supply
82	GP04	I/O	Input(L)	General purpose I/O port with pull down resistor Master clock output for serial communication 2 IIC (master) clock output (exclusive with GP10 and GP40)

PIN DESCRIPTION (continued)

Pin No.	Pin name	I/O	State when "Reset"	Function
83	GP05	I/O	Input(L)	General purpose I/O port with pull down resistor Receive data input for serial data communication 2 IIC (master) data input/output (exclusive with GP11 and GP41)
84	GP06	I/O	Input(L)	General purpose I/O port with pull down resistor Transmit data output for serial communication 2 UART1 data transmit (exclusive with GP10)
85	GP07	I/O	Input(L)	General purpose I/O port with pull down resistor UART1 data receive (exclusive with GP11)
86	GP14	I/O	Input(L)	General purpose I/O port with pull down resistor External interruption function 1 (exclusive with GP03, GP41 and GP45) Watch Dog Timer state monitor output USB device detection flag output Emphasis flag input/output for Audio (exclusive with GP46) CD_C2 error flag input (exclusive with GP47)
87	DVDD12_1	AO	H	Capacitor connection pin for internal regulator (1.2 V for internal)
88	DVDD	–	–	Digital system power supply
89	DVSS	–	–	Digital system ground. This pin must be connected to the 0 V level
90	DVDD18_1	AO	H	Capacitor connection pin for internal regulator (1.8 V for Flash)
91	JTRSTB	I	Input	JTAG reset input (Connect to pull−down resistor or 0 V level in normal mode)
92	JTCK	I	Input	JTAG clock input (Connect to pull−down resistor or 0 V level in normal mode)
93	JTDI	I	Input	JTAG data input (Connect to pull−down resistor or 0 V level in normal mode)
94	JTMS	I	Input	JTAG mode input (Connect to pull−down resistor or DVDD level in normal mode)
95	JTDO	O	L	JTAG data output (Leave open in normal mode)
96	JTRTCK	O	L	JTAG return clock output (Leave open in normal mode)
97	LFOUT	AO	Unknown	Electronic Volume : Left channel Front output
98	LROUT	AO	Unknown	Electronic Volume : Left channel Rear output
99	LVRIN	AI	Input	Electronic Volume : Left channel volume input
100	DACOUTL	AO	Unknown	Audio DAC : Left channel output

NOTES:

1. For unused pins :
   - The unused input pins must be connected to the GND (0 V) level if there is no individual note in the above table.
   - The unused output pins must be left open (No connection) if there is no individual note in the above table.
   - The unused input/output pins must follow the below conditions if there is no individual note in the above table:
     Input setting
     Leave open with internal pull−down resistor ON.
     With using internal pull−down resistor OFF, connect to GND (0 V) or connect to power pins for I/O.
     However, use of individual pull−up or pull−down resistor is recommended as fail−safe.
     Output setting
     Leave them open.
2. For power supply pins:
   - Same voltage level must be supplied to DVDD, AVDD1, AVDD2, XVDD and VVDD2 power supply pins.
     (Refer to "Allowable operating ranges")
3. For "Reset" condition:
   - This IC is not reset only by making the RESB pin "Low".
     Refer to "Power on and Reset control" for detail of "Reset" condition.
4. For "Analog Source" unused pins (15 pin to 22 pin) :
   - The "Analog Source" unused pins (15 pin to 22 pin) must be connected to the GND (0V) level through the input coupling capacitor or be left open (No connection).

BLOCK DIAGRAM

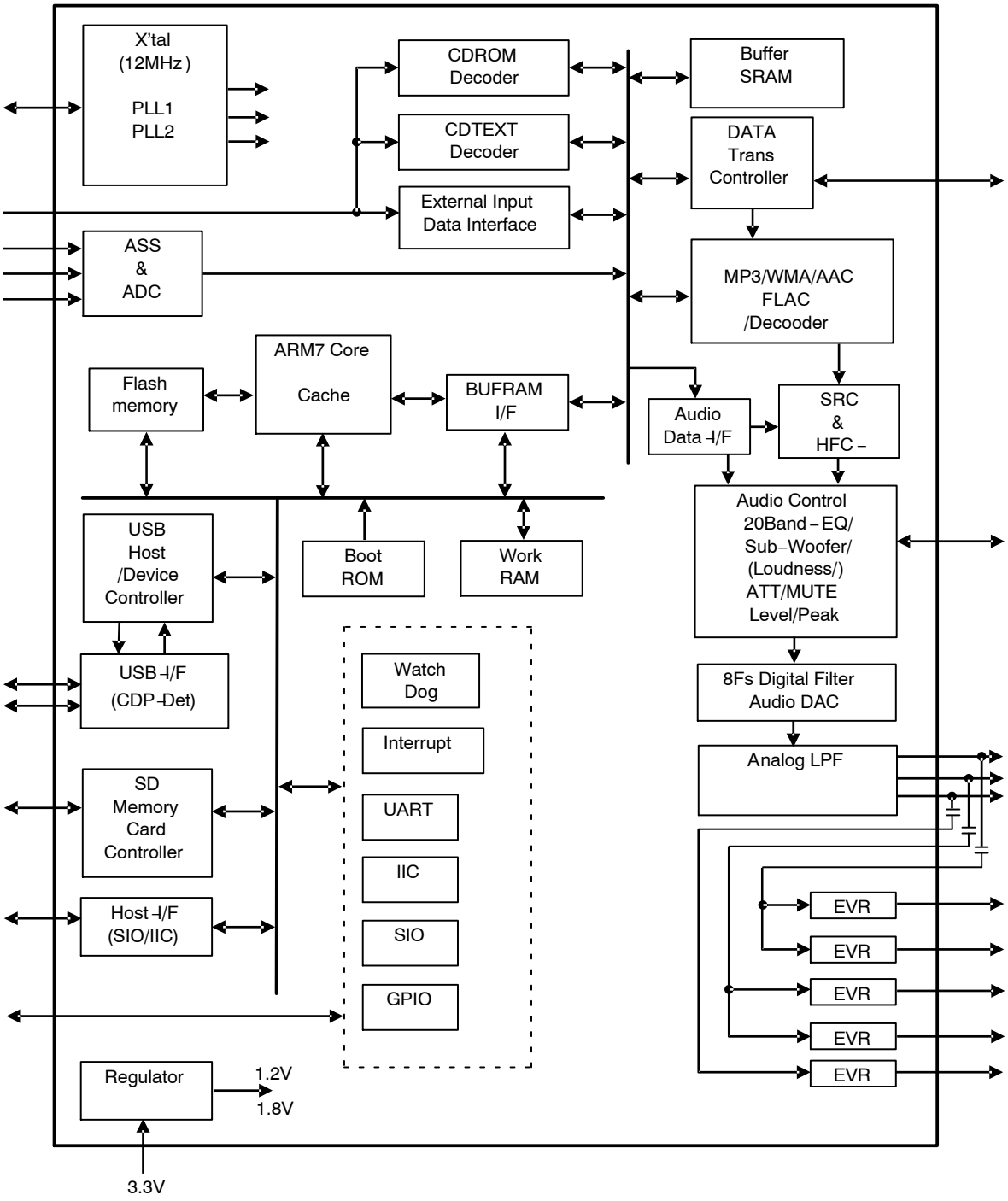


Figure 2. Block Diagram

Power−ON/Reset Control

- Notes on Power−On
  1. Regarding Reset Pin
     To stabilize the operation condition of the internal FlashROM, RESB pin must need to be “L”.
     If RESB pin is “H” at the Power−On, operation condition of the Flash memory becomes unstable and the operation of this LSI becomes unstable. In this case, Reset by RESET pin control does not return to the normal state, RESB pin must be “L” at the Power−On
  2. Regarding Volume Out
     Volume output becomes unknown state when Power−On, external circuit must care by muting/etc. from external circuit

Power−On/Power−Down/Reset Timing

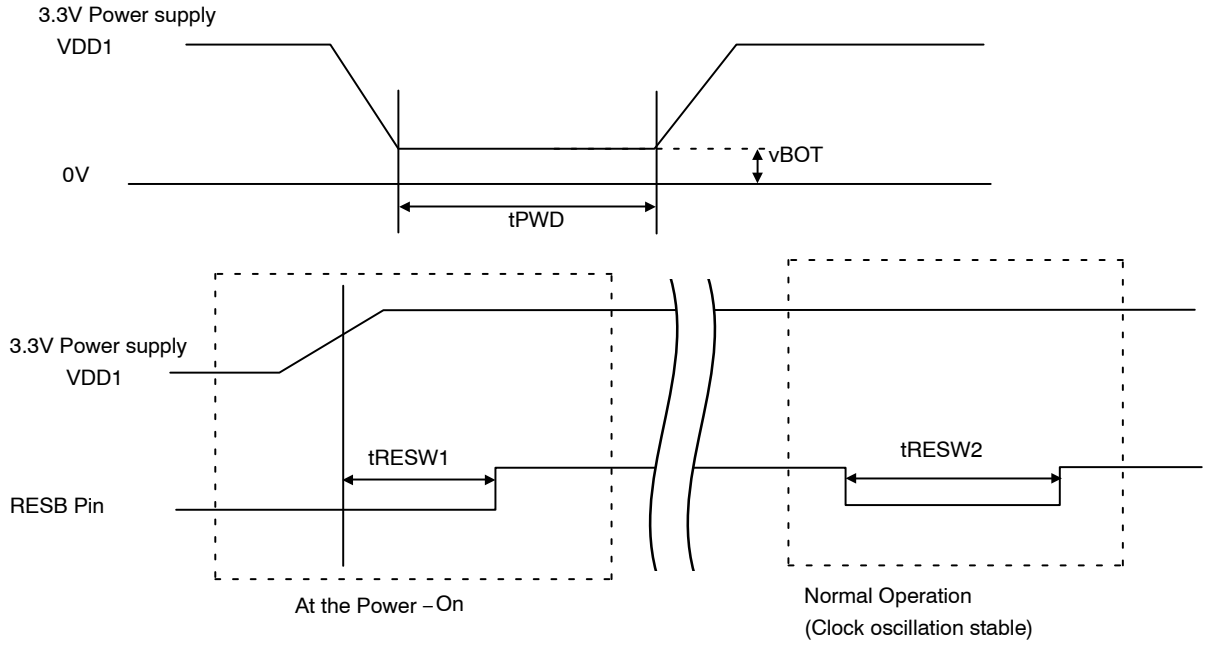


Figure 3.

Parameter	Symbol	Min	Typ	Max	Unit
Power−On rise time	tPWD	10			ms
Power−Down fall time	vBOT	0		0.2	V
Reset period (at Power−On)	tRESW1	20			ms
Reset period (When normal operation) (Note 5)	tRESW2	1			ms

5. Reset period at normal operation is the period that clock is stablely oscillating.
   Need to care about clock stable time when making clock OFF by commands.

− Regarding RESB pin control and internal Flash memory
  As stated above, reset of the operation state of the flash memory in this LSI cannot be controlled by only RESB pin, and needs Power−On−Reset. Therefore, when flash memory goes to runaway state during the power is on, Power−On−Reset must be done. In this case, users must power off the LSI and execute the Power−On−Reset.

On the other hand, reset control by RESB pin is effective to the circuit other than the flash memory. By making RESB pin to “L” for the time period stated above with the stable clock, the circuit except flash memory is initialized. Also, by this operation, flash memory becomes stand−by state and states of the memory cells are kept

Microcontroller Interface

Reception/Transmission from the host microcontroller is done by the SPI synchronous SIO communication.
The format of the data transmission is as below

- Code of M5 to M0 at the ModeCode transmission must be followed by the specification of the internal software inside this LSI.
  When data input in M5 to M0 and value in the internal register matches, SIFDO becomes “L” (Ack) and communication will be enabled. If no match, SIFDO becomes “H” (Nack) and communication will not be enabled.
- Judgement whether command transmission or reception will be done by the 7th bit data of the ModeCode transmission.
  “L” means command transmission and “H” means data reception
- Need to care the communication timing specification because the specification differs by operational mode (normal / low speed) of the internal microcontroller

Communication Interface with the Host Microcontroller

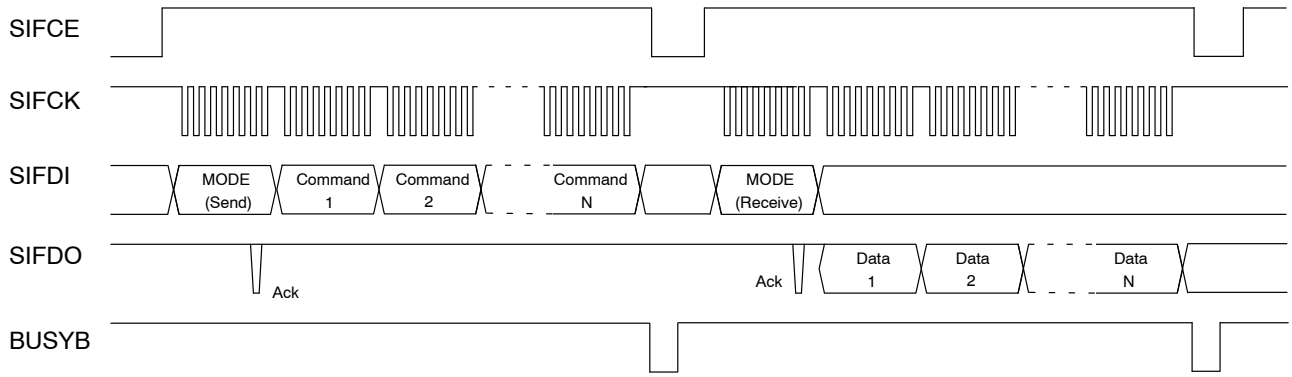


Figure 4.

Transmission/Reception Format with the Host Microcontroller

1. Host: Command Transmission

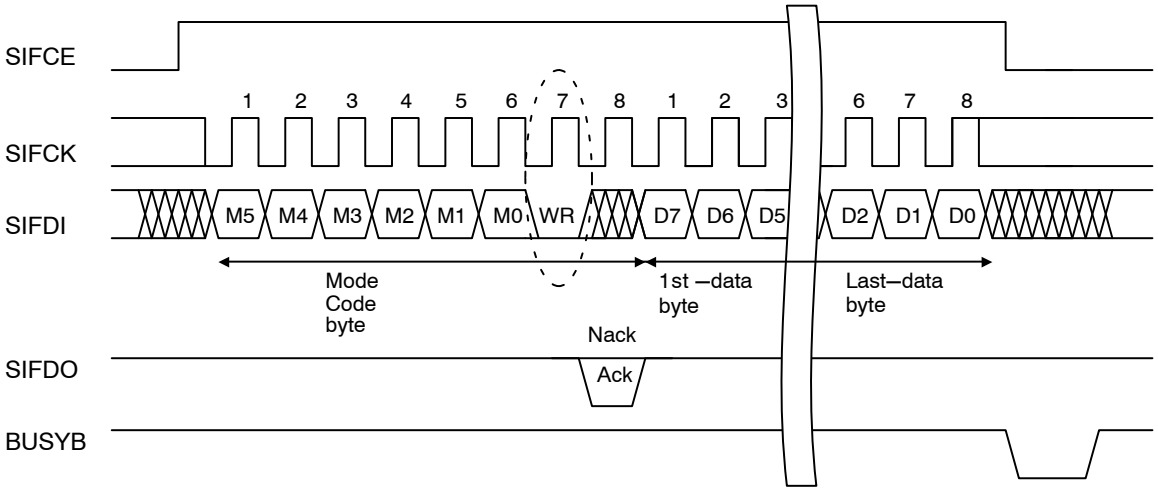


Figure 5.

2. Host: Data reception

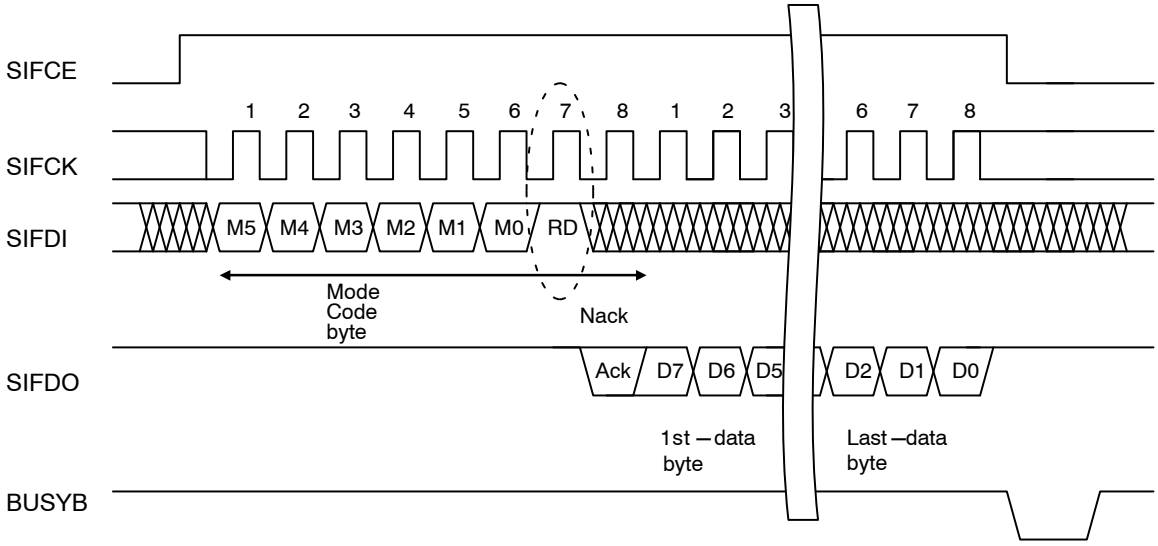


Figure 6.

Characteristics of Communication Timing With Host Microcontroller

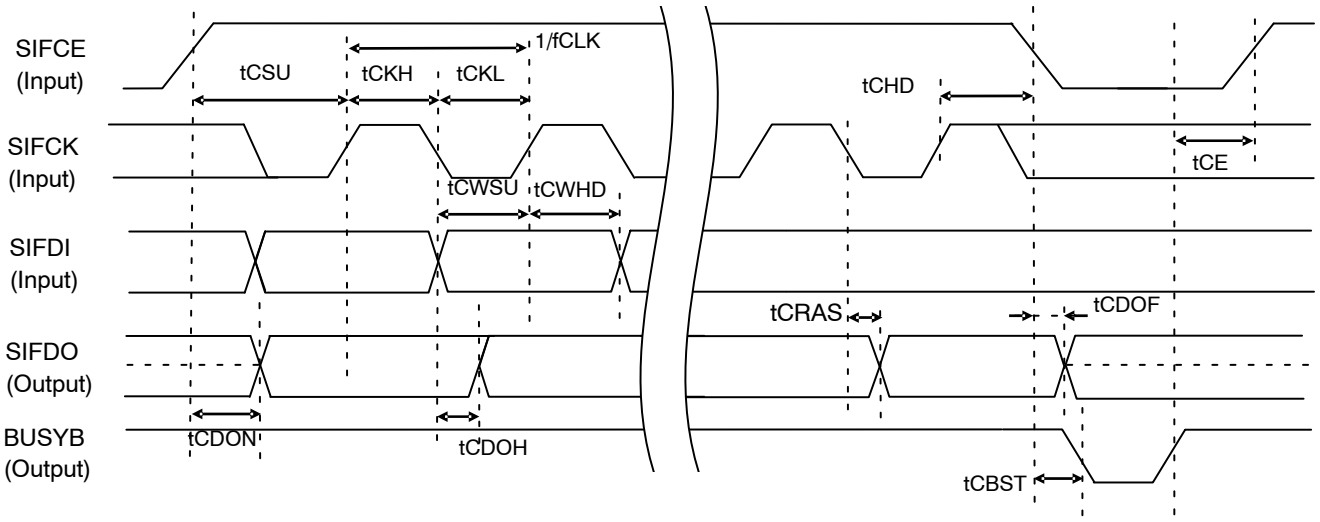


Figure 7.

Parameter	Symbol	Pin Names	Min	Typ	Max	Unit
Communication Clock Frequency	fCLK	SIFCK			3.3 0.725	MHz
Communication Clock “H” Period	tCKH	SIFCK	150 690			ns
Communication Clock “L” Period	tCKL	SIFCK	150 690			
Communication Start Allowable Time	tCE	BUSYB, SIFCE	0 0			
Communication Start Set Up Time	tCSU	SIFCE, SIFCK	100 200			
Communication End Hold Time	tCHD	SIFCE, SIFCK	100 200			
Data Input Set Up Time	tCWSU	SIFDI, SIFCK	75 75			
Data Input Hold Time	tCWHD	SIFDI, SIFCK	75 200			
Data Output “H” Level Rise Time	tCDOH	SIFDO, SIFCK			100 350	
Data Output Settle Time	tCRAS	SIFDO, SIFCK			100 350	
Output ON Settle Timer * (Note 6)	tCDON	SIFDO, SIFCE			100 100	
Output OFF Settle Timer * (Note 6)	tCDOF	SIFDO, SIFCE			150 150	
BUSYB “L” Level Settle Time	tCBST	BUSYB			150 350	

*Internal Microcontroller Operation Mode
Upper Value:
Normal Mode
Lower Value: Low Speed Mode
6. tCDON/tCDOF are available only when setting SIFDO pin to 3−State output.

IIC can be used for the transmission/reception from the host microcontroller.
Supported modes are;

Normal Mode : 100 kbps
High Speed Mode : 400 kbps

Slave address is 0x16 (7 bit value).

Condition for Communication(IIC) Timing With Host Microcontroller

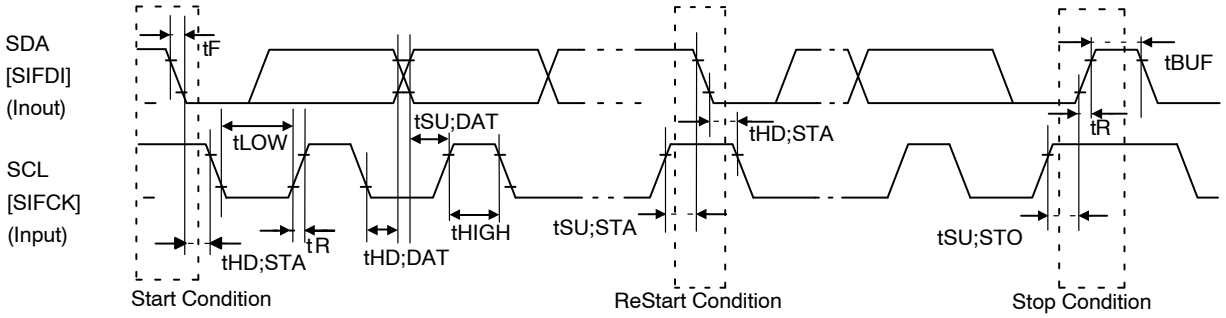


Figure 8.

Parameter	Symbol	Normal (100 kbps)		High Speed (400 kbps)		Unit
		Min	Max	Min	Max	
SCL Frequency	fSCL	0	100	0	400	kHz
Bus Open Time	tBUF	4.7		1.3		μs
SCL “L” Period	tLOW	4.7		1.3		μs
SCL “H” Period	tHIGH	4.0		0.6		μs
Start/ReStart Condition Hold Time	tHD;STA	4.0		0.6		μs
Start/ReStart Condition Set−Up Time	tSU;STA	4.7		0.6		μs
SDA Hold Time	tHD;DAT	0		0		s
SDA Set−Up Time	tSU;DAT	250		100		ns
SDA, SCL Rise Time	tR		1000	20+0.1Cb	300	ns
SDA, SCL Fall Time	tF		300	20+0.1Cb	300	ns
Stop Condition Set−Up Time	tSU;STO	4.0		0.6		μs

NOTE: Cb is the total capacity added to each bus (Unit: pF)

When using IIC, SIFDO/SIFCE/BUSYB pins can be used as GPIOs as below;

SIFDO : GP00
SIFCE : GP01
BUSYB : GP02

Serial Communication Ports

Characteristics of Serial Communication (SIO) Master Mode Input/Output Timing

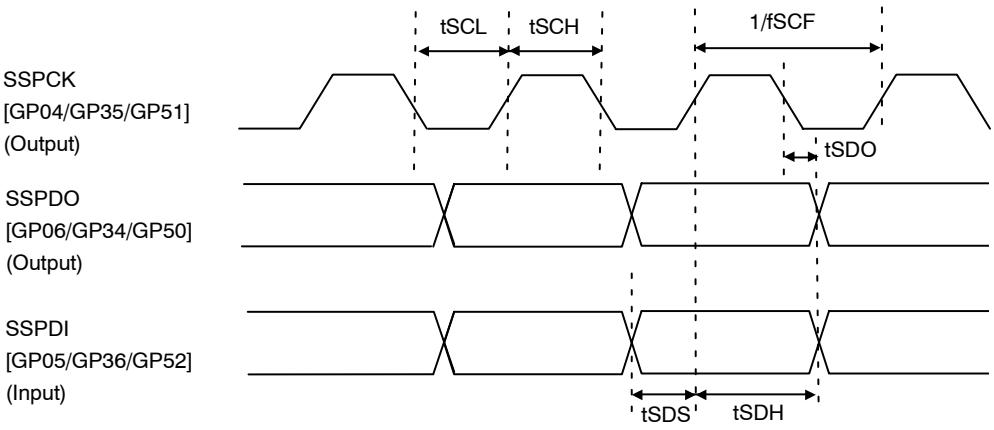


Figure 9.

Parameter	Symbol	Signal Names	Min	Typ	Max	Unit
SIO Clock Frequency	fSCF	SSPCK	0.008		5.0	MHz
SIO Clock “H” Period	tSCH	SSPCK	100		62500	ns
SIO Clock ”L” Period	tSCL	SSPCK	100		62500	
Data Output Settle Time	tSDO	SSPDO, SSPCK			90	
Data Input Set−Up Time	tSDS	SSPDI, SSPCK	50			
Data Input Hold Time	tSDH	SSPDI, SSPCK	75			

NOTE: In the case that internal microcontroller operates in normal mode.

Conditions for Input/Output Timing of Serial Communication (IIC) Master Mode

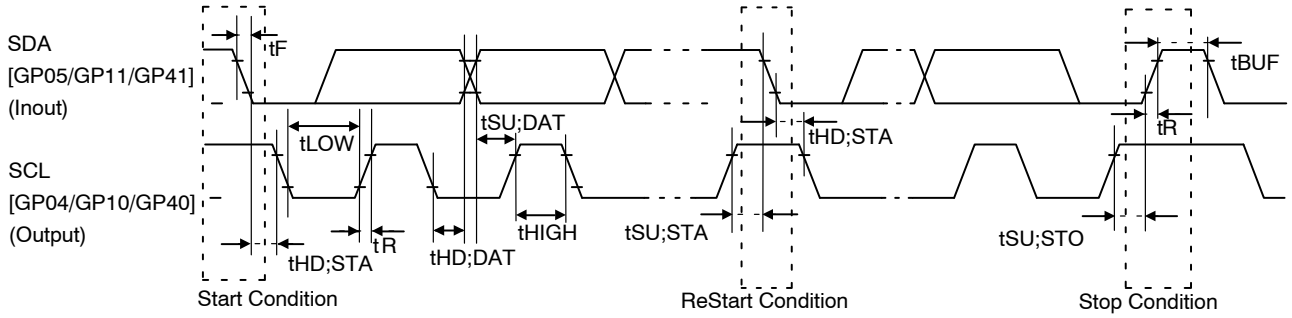


Figure 10.

Parameter	Symbol	Normal (100 kbps)		High Speed (400 kbps)		Unit
		Min	Max	Min	Max	
SCLFrequency	fSCL	0	100	0	400	kHz
Bus Open Time	tBUF	4.7		1.3		μs
SCL “L” Period	tLOW	4.7		1.3		μs
SCL “H” Period	tHIGH	4.0		0.6		μs
Start/ReStart Condition Hold Time	tHD;STA	4.0		0.6		μs
Start/ReStart Condition Set−Up Time	tSU;STA	4.7		0.6		μs
SDA Hold Time	tHD;DAT	0		0		μs
SDA Set−Up Time	tSU;DAT	250		100		ns
SDA,SCL Rise Time	tR		1000	20+0.1Cb	300	ns
SDA,SCL Fall Time	tF		300	20+0.1Cb	300	ns
Stop Condition Set−Up Time	tSU;STO	4.0		0.6		μs

NOTE: Cb is the total capacity added to each bus (Unit: pF)

USB SPECIFICATION at T_A = −40 to 85°C, $V_{DD}1$ = 3.0 to 3.6 V, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Parameter	Symbol	Pin Names	Conditions	MIN	TYP	MAX	Unit
High−level input voltage	VIH(USB)	UDM1, UDP1, UDM2, UDP2		2.0			V
Low−level input voltage	VIL(USB)					0.8	
Input leakage current	ILI		Output : OFF	−10.0		10.0	μA
Differential input sensitivity	VDI		|(UDP) − (UDM)|	0.2			V
Common mode voltage range	VCM		Includes VDI range	0.8		2.5	V
High−level output voltage	VOH(USB)			2.8		3.6	V
Low−level output voltage	VOL(USB)			0.0		0.3	V
Output signal Crossover voltage	VCR			1.3		2.0	V
USB data rising time	TUR		CL = 50pF	4.0		20.0	ns
USB data falling time	TUF			4.0		20.0	
D+/D− Pull−Down resistor	RPD			14.25		24.8	kΩ
D+ Pull−Up resistor	RPUI	UDP1	Idle	0.9		1.575	kΩ
	RPUR		Reception	1.425		3.09	
D− source voltage	VDMSRC	UDM1		0.5		0.7	V
	VLGC_SRC			0.8		2.0	V

- USB port peripheral circuit application

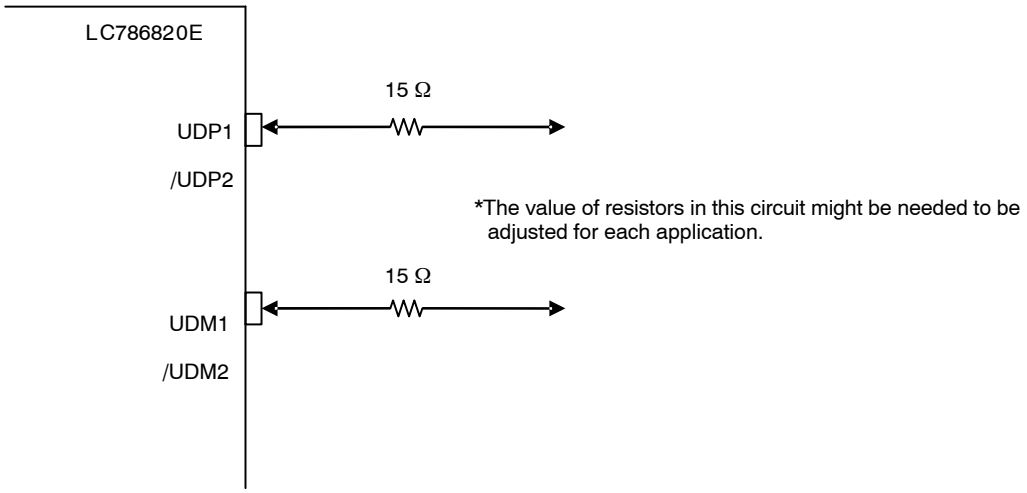


Figure 11.

SD Memory Card Interface

Characteristics of SD Memory Card Input/Output Timing

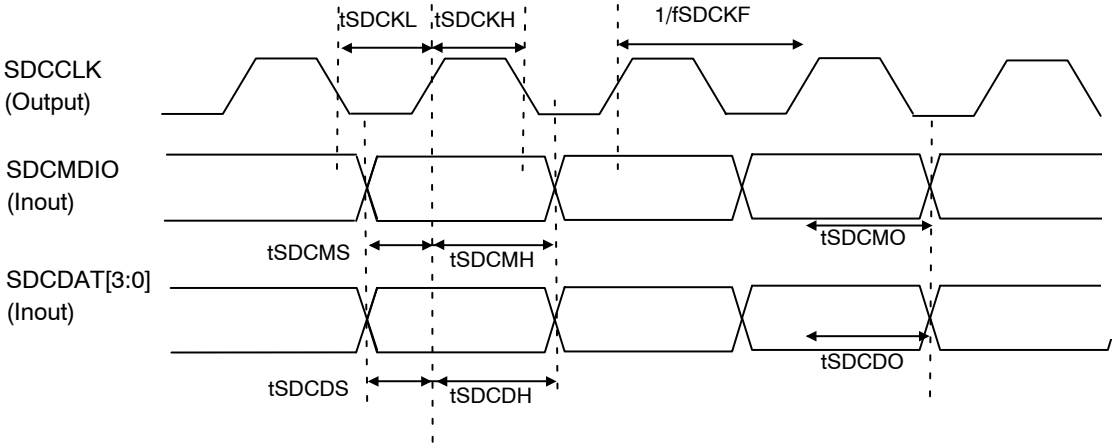


Figure 12.

*Relationship between signal name and pin

SDCCLK	: GP34	SDCMDIO	: GP35	SDCDAT[3]	: GP36
SDCDAT[2]	: GP37	SDCDAT[1]	: GP32	SDCDAT[0]	: GP33

Parameter	Symbol	Signal Names	Min	Typ	Max	Unit
SDCCLK Clock Frequency	fSDCKF	SDCCLK		6.0		MHz
SDCCLK ”H” Period	tSDCKH	SDCCLK		83.3		ns
SDCCLK ”L” Period	tSDCKL	SDCCLK		83.3		
Command Input Set−Up Time	tSDCMS	SDCMDIO, SDCCLK	30.0			
Command Input Hold Time	tSDCMH	SDCMDIO, SDCCLK	30.0			
Command Output Settle Time	tSDCMO	SDCMDIO, SDCCLK			30.0	
Data Input Set−Up Time	tSDCDS	SDCDAT[3:0], SDCCLK	30.0			
Data Input Hold Time	tSDCDH	SDCDAT[3:0], SDCCLK	30.0			
Data Output Settle Time	tSDCDO	SDCDAT[3:0], SDCCLK			30.0	

NOTE: Internal microcontroller (Arm7) must be used in normal mode. It cannot be used in low speed mode.

AUDIO DATA INPUT/OUTPUT FUNCTION

AC ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V_{DD}1$ = 3.3 V, DVSS = AVSS1 = AVSS2 = XVSS = 0 V
Fs = 44.1 kHz, Audio Signal Frequency: 1 kHz, Measurement Range: 10 Hz to 20 kHz

Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	Unit
(INPUT SELECTOR + ADC)							
Full scale Analog Input Level		L1IN, R1IN, L2IN, R2IN, L3INP, L3INN, R3INP, R3INN		2.605	2.805 ($0.85\times V_{DD}1$)	3.005	Vpp
Input Impedance				20	30		kΩ
Gain Setting Level				−12		19	dB
Gain Setting Step					1		dB
Gain Setting Step Error				−0.5		0.5	dB
Signal to Noise Ratio	S/N		0 dB Data, 20 kHz−LPF, A−filter	90	95		dB
Dynamic Range	DR		−60 dB Data, 20 kHz−LPF, A−filter	90	95		dB
Total Harmonic Distortion	THD+N		Input condition : −3 dBFS		−85	−80	dB
Cross Talk1	CT1		Between Channels		−100	−85	dB
Cross Talk2	CT2		Between Sources		−100	−85	dB
(ADC DIGITAL FILTER)							
Passband Frequency			±0.04 dB	0		0.4535	Fs
Stopband Frequency				0.5465			Fs
Passband Ripple						±0.04	dB
Stopband Attenuation			>24.1 kHz	−69			dB
HPF Cut Off Frequency for DC Offset cancelation					0.00002		Fs
(AUDIO DAC)							
Full scale Analog Output Level		DACOUTL, DACOUTR, DACOUTS		2.605	2.805 ($0.85\times V_{DD}$)	3.005	Vpp
Signal to Noise Ratio	S/N		0 dB Data, 20 kHz−LPF, A−filter		106		dB
Dynamic Range	DR		−60 dB Data, 20 kHz−LPF, A−filter		106		dB
Total Harmonic Distortion	THD+N		0 dB Data, 20 kHz−LPF		−85	−80	dB
Cross Talk	CT		0 dB Data, 20 kHz−LPF		−100	−85	dB
(DAC DIGITAL FILTER)							
Passband Frequency			±0.015 dB	0		0.4535	Fs
Stopband Frequency				0.5465			Fs

AC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD}1 = 3.3 V, DVSS = AVSS1 = AVSS2 = XVSS = 0 V
Fs = 44.1 kHz, Audio Signal Frequency: 1 kHz, Measurement Range: 10 Hz to 20 kHz (continued)

Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	Unit
(DAC DIGITAL FILTER)							
Passband Ripple						±0.015	dB
Stopband Attenuation				–62			dB
HPF Cut Off Frequency for DC Offset cancelation			–3 dB		0.0000385		Fs
(ELECTRONIC VOLUME)							
Input Impedance		LVRIN, RVRIN,		7.5	10		kΩ
		SWIN		15	20		kΩ
Volume Setting range		LFOUT, LROUT, RFOUT, RROUT, SWOUT		–70		0	dB
Mute Level				80	90		dB
Volume Setting Step			0 to –32 dB		0.25		dB
			–32 to –70 dB		1.0		dB
Volume Setting Step Error			0 to –32 dB	–0.125		0.125	dB
			–32 to –70 dB	–5		0.5	dB

Audio Digital Data Input/Output Function

AUDIO INPUT/OUTPUT SUPPORTED FORMAT

	Mode	Bit Length	Slot Length	Fs384 Clock
Input	IIS MSB First Right Aligned MSB First Left Aligned	16 bit 24 bit	32 fs, 48 fs, 64 fs	Internal Clock External Clock
Output	IIS MSB First Right Aligned MSB First Left Aligned	16 bit 24 bit	32 fs, 48 fs, 64 fs	Fs384 Clock Output

APPLIED PINS

	LRCK	BCK	DATA	Fs384 Clock
Input	GP30 GP40 GP50	GP31 GP41 GP51	GP32 GP42 GP52	GP33 GP43 GP53
Output	GP30 GP40 GP50	GP31 GP41 GP51	GP32 GP42 GP52	GP33 GP43 GP53

NOTE: When each pin is set as audio input simultaneously, they will be processed as below priority;
(1) GP30 to 33, (2) GP40 to 43, (3) GP50 to 53
For example, if set all pins to audio input mode, audio data will be processed on only data in GP30 to 33. Data in GP40 to 43, GP 50 to 53 will not be processed in the LSI.

Other

- Audio output can be supported in 3 kinds of Fs (32 kHz/44.1 kHz/48 kHz)
- When inputting external audio, GP14/GP46 can support input of emphasis signals

Characteristics of Audio Data Input Timing

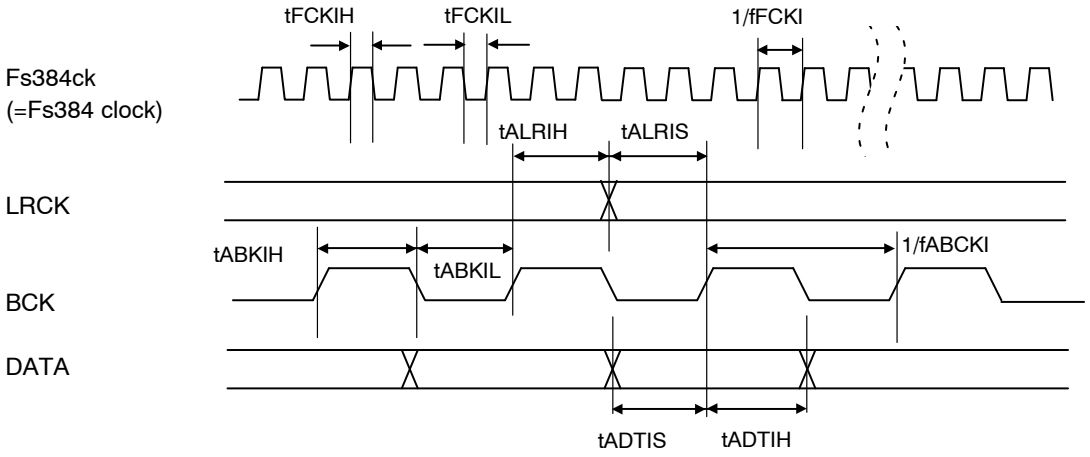


Figure 13.

Parameter	Symbol	Signal Names	Min	Typ	Max	unit
Fs384 Clock Frequency	fFCKI	Fs384ck			20.0	MHz
Fs384 Clock “H” Period	tFCKIH	Fs384ck	20			ns
Fs384 Clock “L” Period	tFCKIL	Fs384ck	20			ns
Bit Clock Frequency	fABCKI	BCK			3.3	MHz
Bit Clock “H” Period	tABKIH	BCK	120			ns
Bit Clock “L” Period	tABKIL	BCK	120			ns
LRCK Input Set−Up Time	tALRIS	LRCK, BCK	30			ns
LRCK Input Hold Time	tALRIH	LRCK, BCK	30			ns
DATA Input Set−Up Time	tADTIS	DATA, BCK	30			ns
DATA Input Hold Time	tADTIH	DATA, BCK	30			ns

Characteristics of Audio Data Output Timing

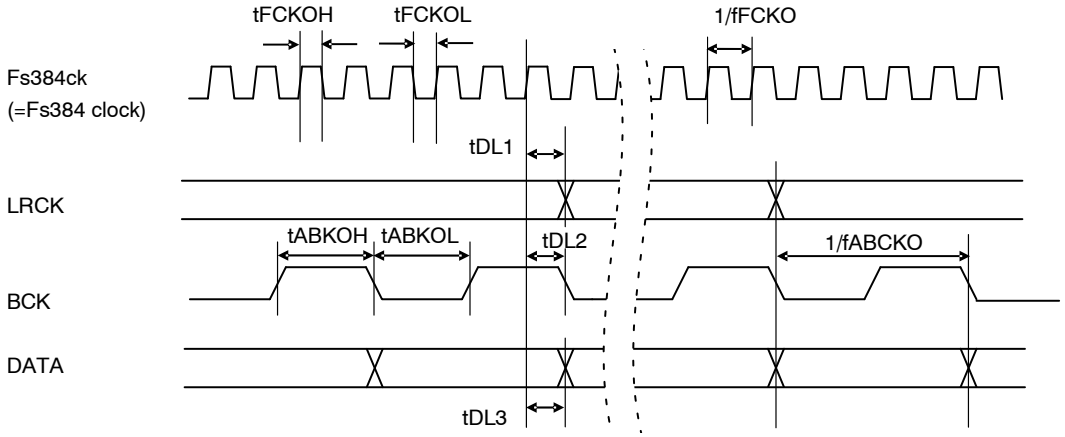


Figure 14.

Parameter	Symbol	Signal Names	Min	Typ	Max	unit
Fs384 Clock Frequency	fFCKO	Fs384ck		16.9344*		MHz
Fs384 Clock ”H” Period	tFCKOH	Fs384ck		29.5*		ns
Fs384 Clock ”L” Period	tFCKOL	Fs384ck		29.5*		ns
Bit Clock Frequency	fABCKO	BCK		2.1168*		MHz
Bit Clock ”H” Period	tABKOH	BCK		236.2*		ns
Bit Clock ”L” Period	tABKOL	BCK		236.2*		ns
LRCK Output Delay Time	tDL1	LRCK, Fs384ck	0		50	ns
BCK Output Delay Time	tDL2	BCK, Fs384ck	0		50	ns
DATA Output Delay Time	tDL3	DATA, Fs384ck	0		50	ns

*In the case that output Fs = 44.1 kHz and slot length of output format 48 fs.

Stream Data Input/Output Function

There are 2 ways to input/output the stream data.

1. 4−wire method

   Stream Input :During STREQO = “H” output, input STLRCKI/STBCKI/STDATI.
   In the case of 4−wire method, STLRCKI/STBCKI/STDATI (input state) are normal audio inputs/outputs. As same as the format, 4 byte (32 bit) data transmission/reception is done in one period of STLRCKI (input state).

2. 3−wire method

   Stream Input : Input STBCKI/STDATI while STREQO = “H” output.
   Stream Output : Output STBCKO/STDATO while STREQI = “H” input.
   In the case of 3−wire method, depending on the state of STREQO, only inputs the bit clock and data, or depending on the state of STREQI, only outputs the bit clock and data, and data communication unit becomes 2 byte (16 bit). Also in the 3−wire method of the stream output, it is possible that users just input the clock (STBCKI) and it will output the data only.

Characteristics of Stream Data Input Timing

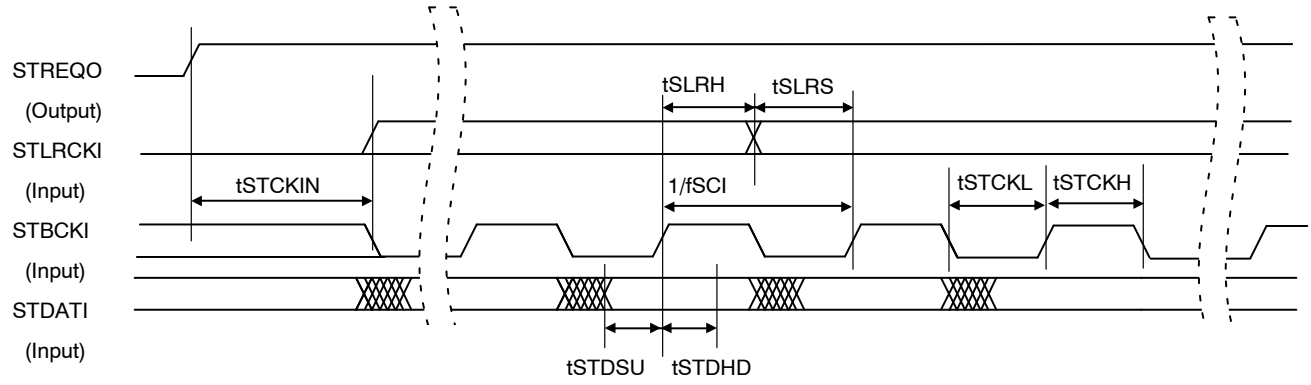


Figure 15.

*Relationship between signal name and pin

STREQO : GP33/GP43/GP53 STLRCKI : GP30/GP40/GP50
STBCKI : GP31/GP41/GP51 STDATI : GP32/GP42/GP52

NOTE: When each pin is set as stream input simultaneously, they will be processed as below priority;
(1) GP30 to 33, (2) GP40 to 43, (3) GP50 to 53
For example, if set all pins to stream input mode, stream data will be processed on only data in GP30 to 33. Data in GP40 to 43, GP 50 to 53 will not be processed in the LSI.

Parameter	Symbol	Signal Names	Min	Typ	Max	unit
STBCKI Clock Frequency	fSCI	STBCKI			4.24	MHz
Stream Input Start Time	tSTCKIN	STREQO, STBCKI, STLRCKI	50			ns
STBCKI “H” Period	tSTCKH	STBCKI	100			ns
STBCKI “L” Period	tSTCKL	STBCKI	100			ns
STLRCKI Set−Up Time	tSLRS	STLRCKI, STBCKI	75			ns
STLRCKI Hold Time	tSLRH	STLRCKI, STBCKI	75			ns
STDATI Set−Up Time	tSTDSU	STDATI, STBCKI	75			ns
STDATI Hold Time	tSTDHD	STDATI, STBCKI	75			ns

NOTE: Above diagram shows the case of data input at rising edge of STBCKI. The timing is the same if using falling edge synchronization.

Characteristics of Stream Data Output Timing: STBCK Output Mode

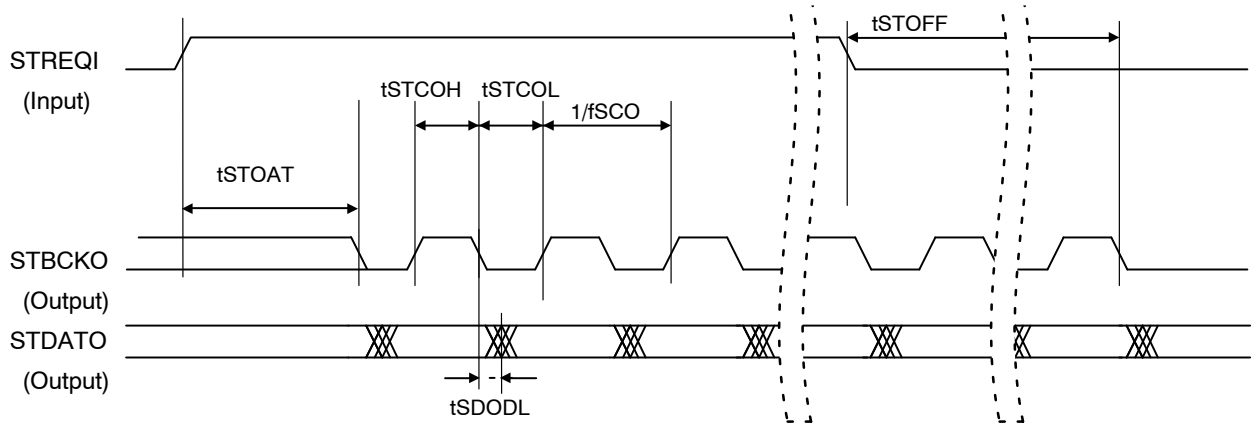


Figure 16.

*Relationship between signal name and pin
STREQI : GP33/GP43/GP53
STBCKO : GP31/GP41/GP51 STDATO : GP32/GP42/GP52

Parameter	Symbol	Signal Names	Min	Typ	Max	unit
STBCKO Clock Frequency	fSCO	STBCKO			4.24	MHz
Stream Output Start Time	tSTOAT	STREQI, STBCKO			(1/fSCO) × 48	ns
Stream Output Stop Time	tSTOFF	STREQI, STBCKO			(1/fSCO) × 48	ns
STBCKO “H” Period	tSTCOH	STBCKO	100			ns
STBCKO “L” Period	tSTCOL	STBCKO	100			ns
STDATO Output Delay Time	tSDODL	STDATO, STBCKO	0		50	ns

NOTE: Above diagram shows the case of data input at rising edge of STBCKO. The timing is the same if using falling edge synchronization.

Characteristics of Stream Data Output Timing: STBCK Input Mode

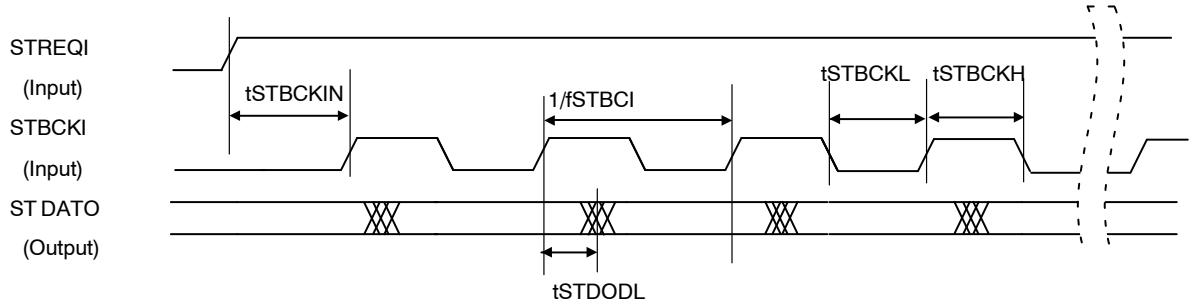


Figure 17.

*Relationship between signal name and pin
STREQI : GP33/GP43/GP53
STBCKI : GP31/GP41/GP51 STDATO : GP32/GP42/GP52

Parameter	Symbol	Signal Names	Min	Typ	Max	unit
STBCKI Clock Frequency	fSTBCI	STBCKI			1.25	MHz
STBCKI Input Start Time	tSTBCKIN	STREQI, STBCKI	1000			ns
STBCKI "H" Period	tSTBCKH	STBCKI	400			ns
STBCKI "L" Period	tSTBCKL	STBCKI	400			ns
STDATO Output Delay Time	tSTDODL	STBCKI, STDATO			250	ns

NOTE: Above diagram shows STBCKI is starting from "L".

<Additional Information>

Clock input mode supports 2 types and data output timing changes as below accordingly;

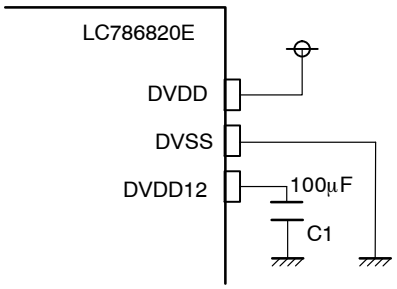
1. Starting from STBCKI = "L"
   STDATO will be output synchronizing with the rising edge of STBCKI.
2. Starting from STBCKI = "H".
   STDATO will be output synchronizing with the falling edge of SBCKI.
   Using each mode of (1) or (2) does not change the output characteristics.

INTERNAL VOLTAGE REGULATOR at T_A = −40 to 85°C, DVSS = AVSS1 = AVSS2 = XVSS = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	DVDD12	$V_{DD}1$ = 3.0 to 3.6 V	1.08	1.20	1.32	V
Load current	Iope	$V_{DD}1$ = 3.3 V			200	mA

NOTE: The specification of "load current" above is sum of the load current of two internal voltage regulator.

Example of 1.2 V Regulator Circuit

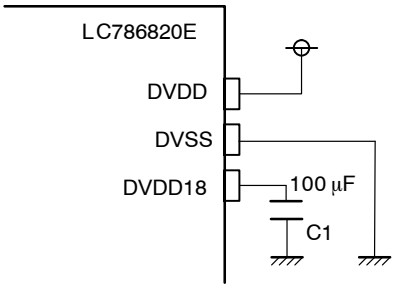


* Same circuit need to be mounted both for two regulator pins. (No.44 and No.87)
* C1 is for capacitor to stop oscillation. There is a possibility of oscillation due to temperature change and etc., so C1 must be greater than 50μF and low ESR at the operational temperature. (The recommended value is 100 μF)

Figure 18.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	DVDD18	$V_{DD}1$ = 3.0 to 3.6 V	1.65	1.80	1.95	V
Load current	Iope	$V_{DD}1$ = 3.3 V			50	mA

Example of 1.8V Regulator Circuit



* Build a circuit shown at left for the regulator pin No. 90.
* C1 is for capacitor to stop oscillation.
There is a possibility of oscillation due to temperature change and etc., so C1 must be greater than 50 μF and low ESR at the operational temperature.
(The recommended value is 100 μF)

Figure 19.

Oscillator

Example Circuit for Oscillator

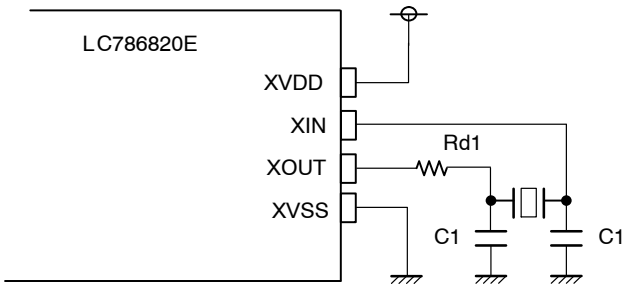


Figure 20.

XIN/XOUT: 12.0000 MHz

- For System Main clock and USB control
- Recommended Oscillator
  Nihon Dempa Kogyo Co., Ltd.

Type	Frequency	Recommended Constants
NX3225GA	12 MHz	Rd1 = 1 kΩ, C1 = 12 pF

<Notes>

- Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
- The precision of oscillator used in XIN/ XOUT should meet the USB standard.
- If oscillation clock is disturbed by noise or by the other factors, it may lead to operation failure. Hence, make sure to connect resistor and capacitor for oscillation circuit as close as XIN/ XOUT and the wire should be as short as possible. Also needs to select parts with caution so as to obtain stable external constant value within the guaranteed operating temperature range because the variation of external constant due to temperature change could affect the oscillation precision
- About internal circuit for XIN/XOUT, refer to the “Analog Pin Internal Equivalent Circuits” section

PLL Circuit

Example of PLL Circuit

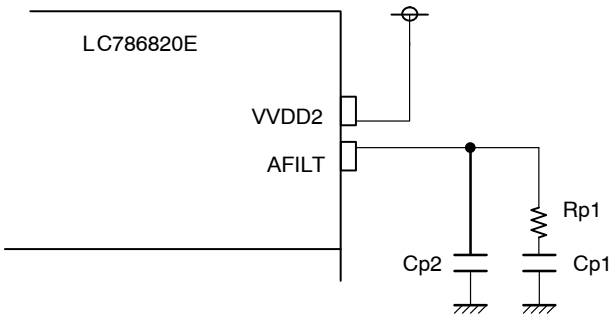


Figure 21.

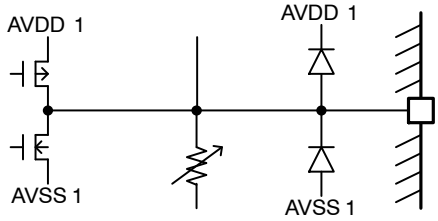
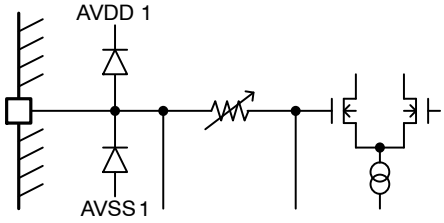
- About PLL
  LC786820E includes PLL1 and PLL2.
  PLL1 is for generating system clock and PLL2 is for generating Audio clock.
- External filter constant for PLL2

PLL2 constant
Rp1 = 3.3 kΩ / Cp1 = 3300 pF / Cp2 = 220 pF

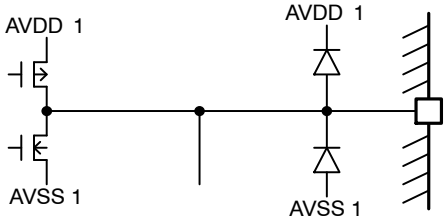
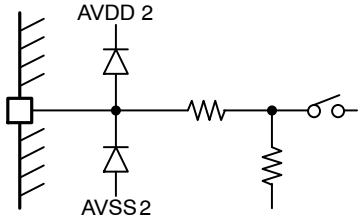
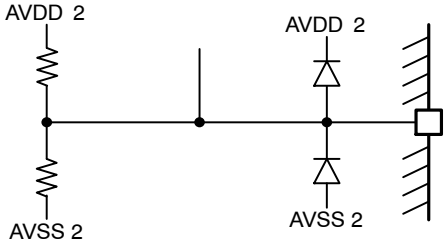
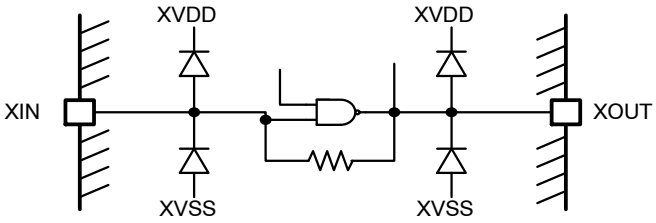
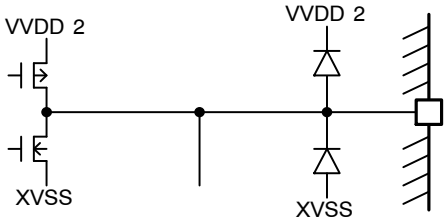
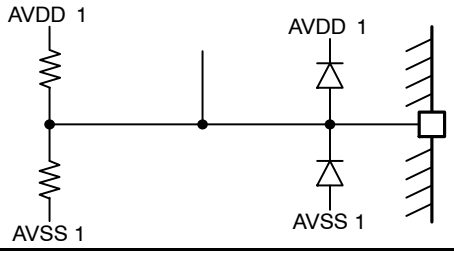
<Notes>

- This PLL filter circuit of resistor (Rp1) and capacitance (Cp1, Cp2), are for audio generation/system clock generation connected to AFILT. If oscillation clock is disturbed by noise or by the other factors, it may lead to operation failure. Hence, make sure to connect resistor and capacitor that constitute filter circuit as close as AFILT and the wire should be as short as possible. Also if filter constant changes due to temperature change, oscillation of PLL may become unstable and the following problem may occur:
- See section on ”Analog Pin Internal Equivalent Circuits” for the internal configuration of AFILT

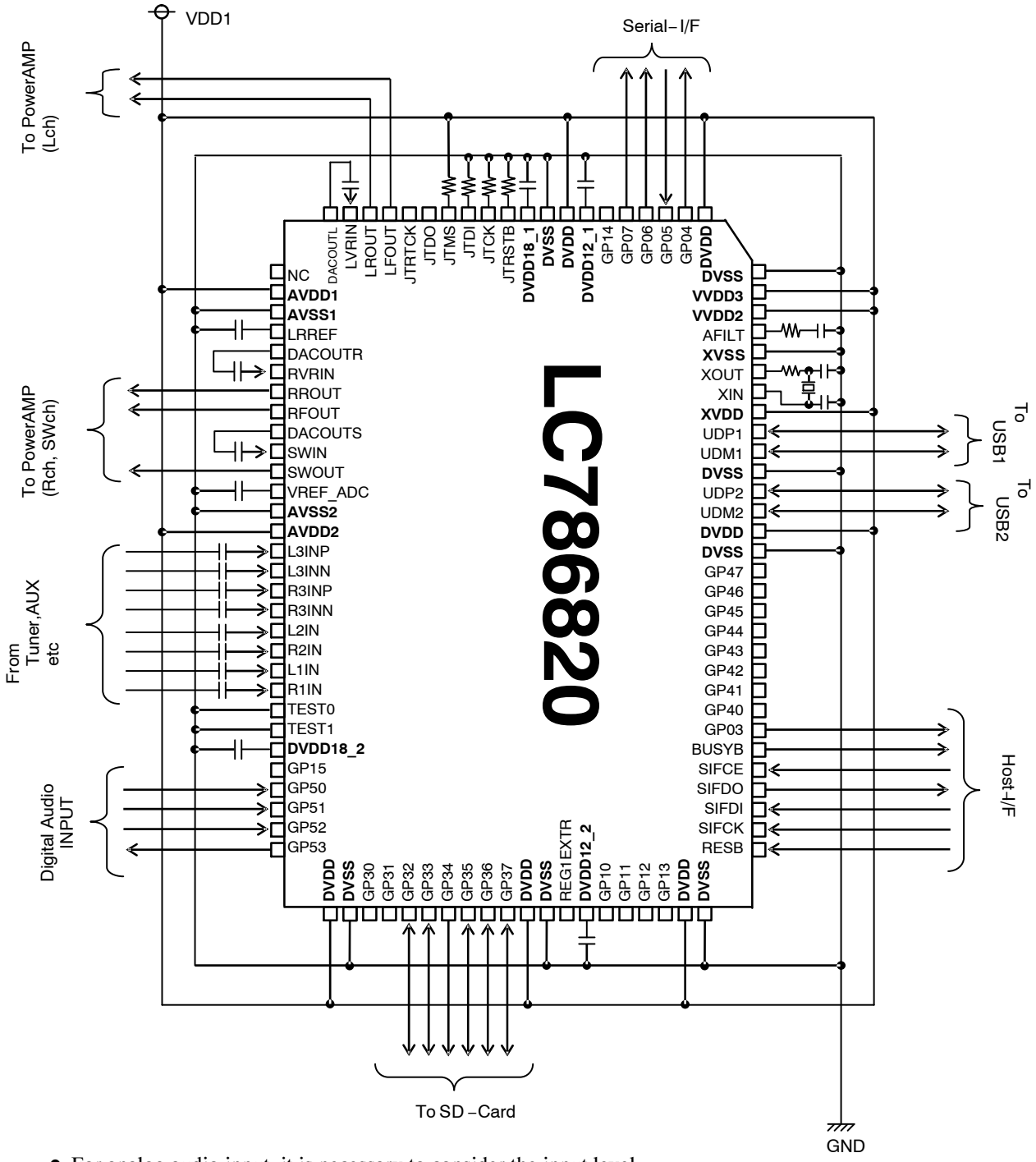
ANALOG PINS INTERNAL EQUIVALENT CIRCUIT

Pin Name ( ) shows pin #	Internal Equivalent Circuit
LFOUT (97) LROUT (98) RROUT (7) RFOUT (8) SWOUT (11)	
LVRIN (99) RVRIN (6) SWIN (10)	

ANALOG PINS INTERNAL EQUIVALENT CIRCUIT (continued)

Pin Name ( ) shows pin #	Internal Equivalent Circuit
DACOUTL (100) DACOUTR (5) DACOUTS (9)	
L1IN (21) R1IN (22) L2IN (19) R2IN (20) L3INP (15) L3INN (16) R3INP (17) R3INN (18)	
VREF_ADC (12)	
XIN (74) XOUT (75)	
AFILT (77)	
LRREF (4)	

Reference Circuit



- For analog audio input, it is necessary to consider the input level.
- Please refer to USB Specification table, Internal Voltage Regulator table and PLL Circuit for the detail of USB/Regulator/oscillator reference circuit.

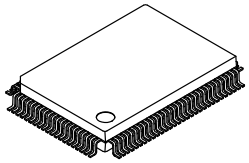
Figure 22.

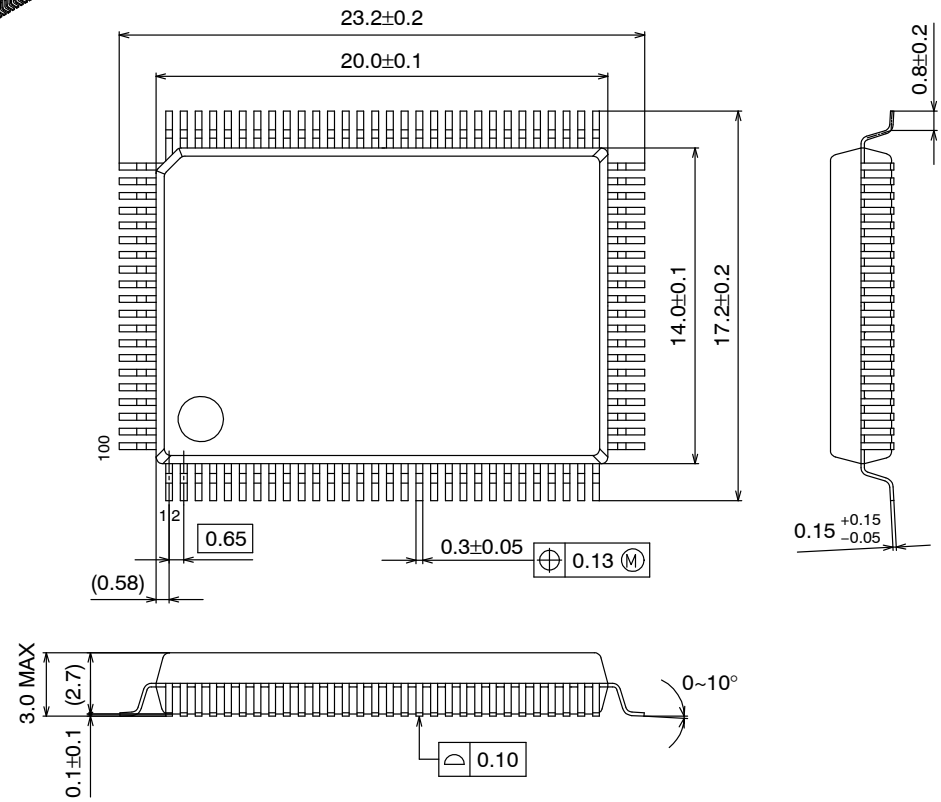
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

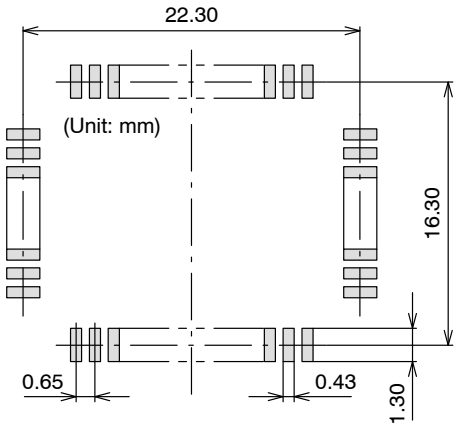
PQFP100 14x20 / QIP100E
CASE 122BV
ISSUE A

DATE 07 NOV 2013





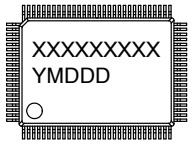
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON66026E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**PQFP100 / QIP100E 14X20**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊