Compact Flash Card

Oct. 19, 2010

FEATURES:

- **Compliant with Compact Flash specification version 4.1**
- **PC card ATA and True IDE Interface**
  - 512 bytes sector
  - ATA command set compatible
  - Support Data Transfer up to PIO Mode-6 /Multi-Word DMA 4/ Ultra DMA 5/ Ultra DMA 6
- **Capacities:**
  - 2GB – 32GB
- **RoHS Compliant**
- **Performance**
  - Max. performance up to 20MB/s for Read, 5MB/s for Write
- **Power Management Unit**
  - Auto Stand-by and Sleep Mode.
- **Temperature Ranges**
  - 0°C to +70°C for operating
  - -20°C to 85°C for storage
- **Support Voltage Read and Write Operation**
  - 3.3 V
  - 5.0 V
- **Support wear leveling function**
- **Support ECC function**
  - 4KB / 8KB data per page
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm

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PRODUCT DESCRIPTION

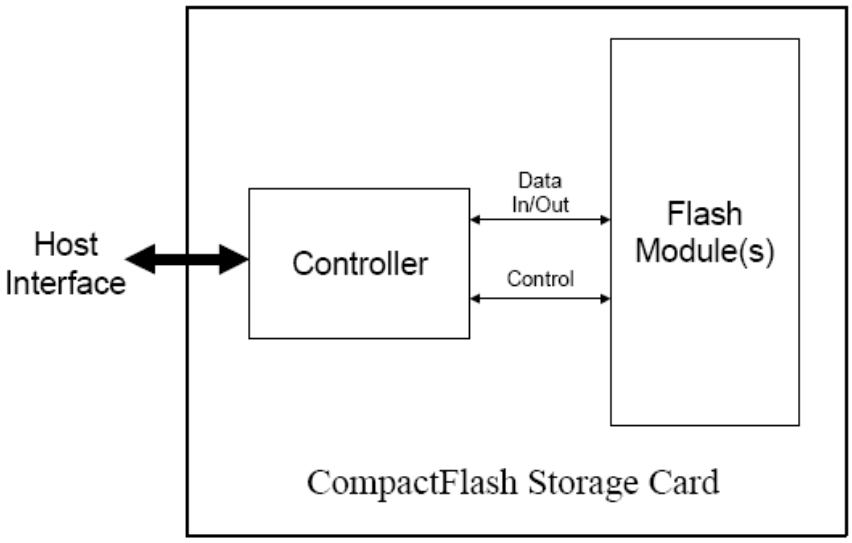
Apacer Photo Steno CompactFlash card is a high performance, removable flash memory data storage system. This product is well suited for solid-state mass storage portable applications offering new and expanded functionality while enabling smaller and lighter designs.

Apacer Photo Steno IV technology is widely used in a variety of consumer products such as portable computers, digital cameras, handheld data collection scanners, Personal Digital Assistants (PDAs), handy terminals, audio players, monitoring devices and set-top boxes. Also, it is special for high-end professional photographers who require the highest possible performance and the largest capacities for their SLR cameras.

Photo Steno IV CF card provides completes PCMCIA – ATA functionality and compatibility, besides, it supports Ultra DMA technology. This is achieved because the 50-pin CF card can be easily slipped into a passive 68-pin Type II adapter card that fully meets PCMCIA electrical and mechanical interface specifications.

1.0 GENERAL DESCRIPTION

The Compact Flash Storage Card contains a single chip controller and flash memory module(s) in a matchbook-sized package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27 mm) centers.



CompactFlash Storage Card Block Diagram

2.0 ELECTRICAL INTERFACE

2.1 Pin Assignment and Pin Type

The signal/pin assignments are listed in Table A Low active signals have a "-" prefix. Pin types are Input, Output or Input/ Output.

TABLE A: CARD PIN ASSIGNMENT

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O

28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD HSTROBE -HDMARDY	I	34	-IORD HSTROBE -HDMARDY	I	34	-IORD HSTROBE -HDMARDY	I
35	-IOWR STOP	I	35	-IOWR STOP	I	35	-IOWR STOP	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT -DOMARDY DSTROBE	O	42	-WAIT -DOMARDY DSTROBE	O	42	IORDY -DOMARDY DSTROBE	O
43	-INPACK -DMARQ	O	43	-INPACK -DMARQ	O	43	DMARQ	O
44	-REG DMACK	I	44	-REG DMACK	I	44	-DMACK	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

2.2 Signal Description

Signal Name	Type	Pin	Description
A10 – A0 (PC Card Memory mode)	I	8,10,11,12, 14,15,16,17 ,18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the Compact-Flash card, the memory mapped port address registers within the Compact Flash card, a byte in the card's information structure and its configuration control and status registers.
A10 – A0 (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal
A10 – A0 (True IDE mode)		18,19,20	In True IDE Mode only A[2:0] are used to select the one of eight (True IDE Mode) registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O mode)			This signal is asserted low to alert the host to changes in the RDY/- BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register
-PDIAG (True IDE mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1,-CD2 (PC Card Memory mode)	O	26,25	These Card Detect pins are connected to ground on the Compact Flash Storage Card. They are used by the host to determine that the Compact Flash Storage Card is fully inserted into its socket.
-CD1,-CD2 (PC Card I/O mode)			This signal is the same for all modes.
-CD1,-CD2 (True IDE mode)			This signal is the same for all modes.

Signal Name	Type	Pin	Description
-CE1,-CE2 (PC Card Memory mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0,-CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 30, Table 33, Table 35, Table 39, Table 41 and Table 42. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits.
-CE1,-CE2 (PC Card I/O mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
- CE1,- CE2 (True IDE mode)			In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave
D15 – D0 (PC Card Memory mode)	I/O	31,30,29, 28,27,49, 48,47,6,5, 4,3,2,23 ,22,21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 – D0 (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
D15 – D0 (True IDE mode)			In True IDE Mode, all Task File operations occur in Byte-Mode on the low order bus D00-D07 while all data transfers are 16 bit using D00- D15.
GND (PC Card Memory mode)	-	1,50	Ground.
GND (PC Card I/O mode)			This signal is the same for all modes.
GND (True IDE mode)			This signal is the same for all modes.

Signal Name	Type	Pin	Description
-INPACK ((PC Card Memory Mode except Ultra DMA Protocol Active)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge			The Input Acknowledge signal is asserted by the Compact Flash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the Compact Flash card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-) DMACK, i.e., the device shall wait until the host asserts (-) DMACK before negating (-) DMARQ, and re-asserting (-) DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.

Signal Name	Type	Pin	Description
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode except Ultra DMA Protocol Active)			This is an I/O Read strobe generated by the host. This signal gates I/ O data onto the bus from the Compact Flash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, this signal has the same function as in PC Card I/ O Mode.
-HDMARDY (All Modes - Ultra DMA Protocol DMA Read)			In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (All Modes - Ultra DMA Protocol DMA Write)			In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Compact Flash Storage Card controller registers when the Compact Flash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (All Modes – Ultra DMA Protocol Active)			In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the Compact Flash Storage Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE mode)			To enable True IDE Mode this input should be grounded by the host.

Signal Name	Type	Pin	Description
RDY/-BSY (PC Card Memory mode)	O	37	In Memory Mode, this signal is set high when the Compact Flash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the Compact Flash Storage Card has completed its power up or reset function. No access of any type should be made to the Compact Flash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O mode)			I/O Operation - After the Compact Flash card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device.
-REG (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device.
-DMACK (PC Card Memory Mode when Ultra DMA Protocol Active)			This is a DMA Acknowledge signal that is asserted by the host in response to (-) DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-) DMACK signal, including a floating condition.
DMACK (PC Card I/O Mode when Ultra DMA Protocol Active)			If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.
-DMACK (True IDE Mode)			A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

Signal Name	Type	Pin	Description
RESET (PC Card Memory mode)	I	41	The Compact Flash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The Compact Flash Storage Card s also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
RESET (True IDE mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory mode)	I-	13,38	+5.0V, +3.3V power.
VCC (PC Card I/O mode)			This signal is the same for all modes
VCC (True IDE mode)			This signal is the same for all modes
-VS1 -VS2 (PC Card Memory mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the Compact Flash Storage Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 -VS2 (PC Card I/O mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active)	O	42	The -WAIT signal is driven low by the Compact Flash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (All Modes – Ultra DMA Write Protocol Active)			In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.
DSTROBE (All Modes – Ultra DMA Read Protocol Active)			In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.

Signal Name	Type	Pin	Description
-WE (PC Card Memory mode)	I	36	This is a signal driven by the host and used for storing memory write data to the registers of the Compact Flash card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host
WP (PC Card Memory Mode) Write Protect	I	24	Memory Mode - The Compact Flash card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOCS16 (PC Card I/O mode)			I/O Operation - When the Compact Flash card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOCS16) function. A Low signal indicates that a 16 bit or Odd Byte only operation can be performed at the addressed port.
-IOCS16 (True IDE mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.0 ELECTRICAL SPECIFICATION

Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 6.5V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

Input Power

Voltage	Maximum Average Current	Measurement Method
3.3V ± 5%	75 mA	3.3V at 25°C
5.0V ± 10%	100 mA	5.0V at 25°C

Compact Flash interface I/O at 5.0V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	VCC	4.5	5.5	V	
High level output voltage	VOH	VCC-0.8		V	
Low level output voltage	VOL		0.8	V	
High level input voltage	VIH	4		V	Non-schmitt trigger
		2.92		V	Schmitt trigge
Low level input voltage	VIL		0.8	V	Non-schmitt trigger
			1.70	V	Schmitt trigge

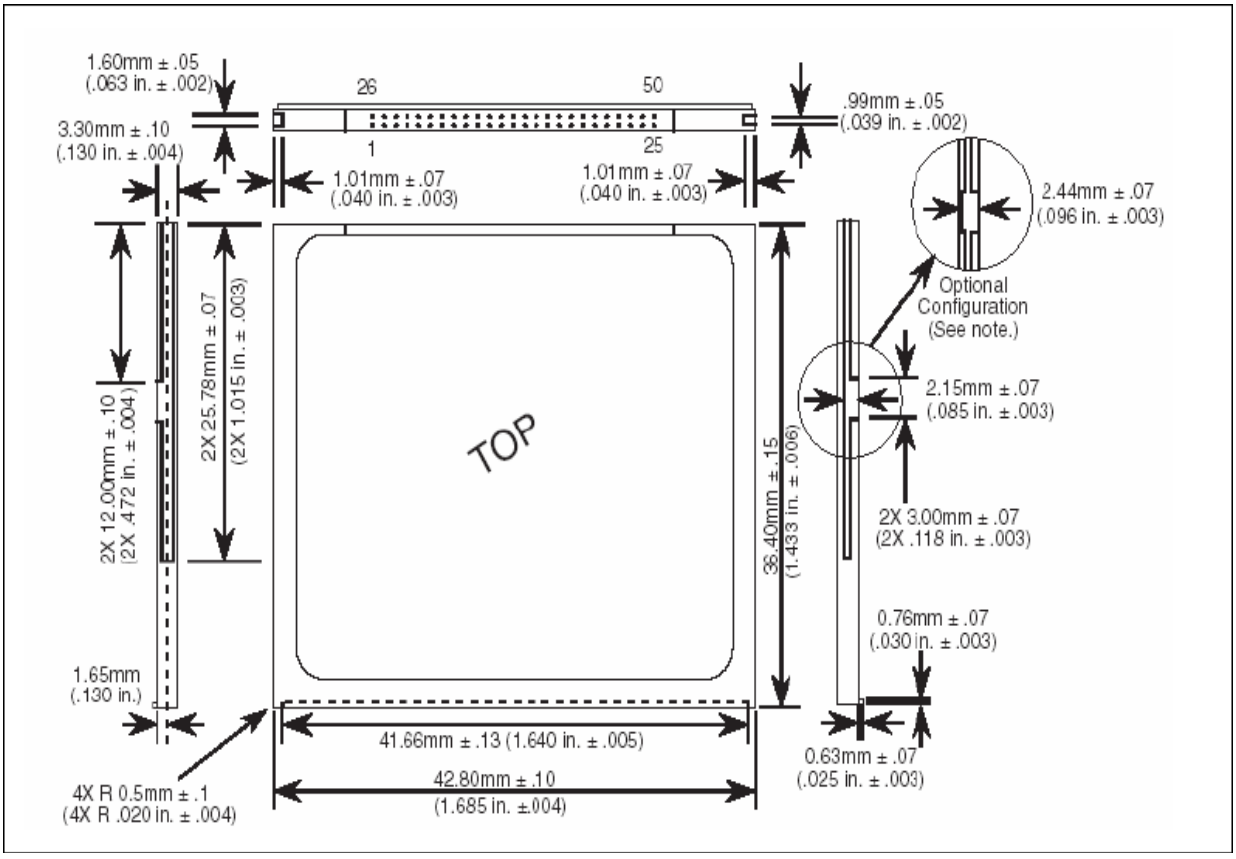
Compact Flash interface I/O at 3.3V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	VCC	2.97	3.63	V	
High level output voltage	VOH	VCC-0.8		V	
Low level output voltage	VOL		0.8	V	
High level input voltage	VIH	2.4		V	Non-schmitt trigger
		2.05		V	Schmitt trigge
Low level input voltage	VIL		0.6	V	Non-schmitt trigger
			1.25	V	Schmitt trigge

4.0 PHYSICAL DIMENSIONS

PHYSICAL MECHANICAL OUTLINE:

Length:	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
Width:	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
Thickness: **(Including Label Area)**	3.3mm+/-0.10mm (0.130+/-0.04in.)



REVISION HISTORY

Revision	Date	History	Remark
1.0	08/07/2007	Fist release	
1.1	05/11/2009	Capacity update	
1.2	10/19/2010	Format revised	