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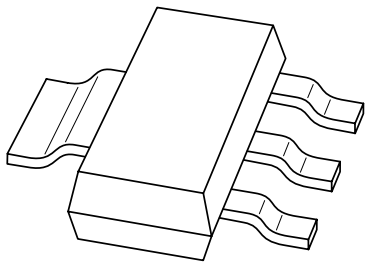
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Kind regards,

Team Nexperia

# DATA SHEET



## **BSP126**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
Supersedes data of 1997 Jun 23

2002 Feb 19

# N-channel enhancement mode vertical D-MOS transistor

**BSP126**

## FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

## APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

## DESCRIPTION

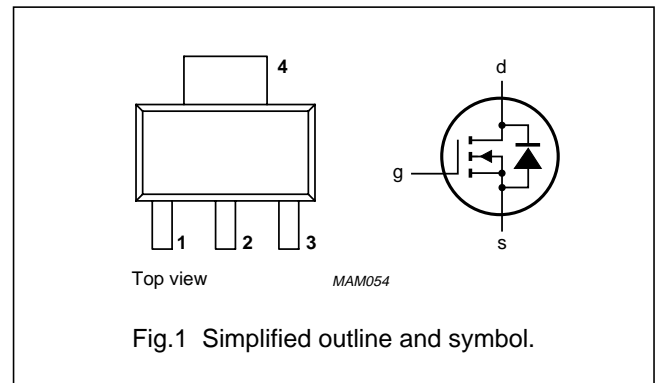
N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 package.

## MARKING

TYPE NUMBER	MARKING CODE
BSP126	BSP126

## PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	250	V
$I_D$	drain current (DC)		–	375	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	1.5	W
$R_{DSon}$	drain-source on-state resistance	$I_D = 300\text{ mA}; V_{GS} = 10\text{ V}$	2.8	5	$\Omega$
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	–	2	V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	250	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	375	mA
$I_{DM}$	peak drain current		–	1.3	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}; \text{note 1}$	–	1.5	W
$T_{stg}$	storage temperature		–55	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

## Note

1. Device mounted on a  $40 \times 40 \times 1.5\text{ mm}$  epoxy printed-circuit board; mounting pad for the drain tab minimum  $6\text{ cm}^2$ .

## N-channel enhancement mode vertical D-MOS transistor

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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	83.3	K/W

#### Note

1. Device mounted on a 40 × 40 × 1.5 mm epoxy printed-circuit board; mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0$	250	–	–	V
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	±100	nA
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 20\ \text{mA}; V_{GS} = 2.4\ \text{V}$	–	–	7.5	$\Omega$
		$I_D = 300\ \text{mA}; V_{GS} = 10\ \text{V}$	–	2.8	5	$\Omega$
$I_{DSS}$	drain-source leakage current	$V_{DS} = 200\ \text{V}; V_{GS} = 0$	–	–	1	$\mu\text{A}$
$ Y_{fs} $	transfer admittance	$I_D = 300\ \text{mA}; V_{DS} = 25\ \text{V}$	200	600	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	100	120	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	21	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	10	15	pF
<b>Switching times</b> (see Figs 2 and 3)						
$t_{on}$	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
$t_{off}$	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 10\ \text{to}\ 0\ \text{V}$	–	47	60	ns

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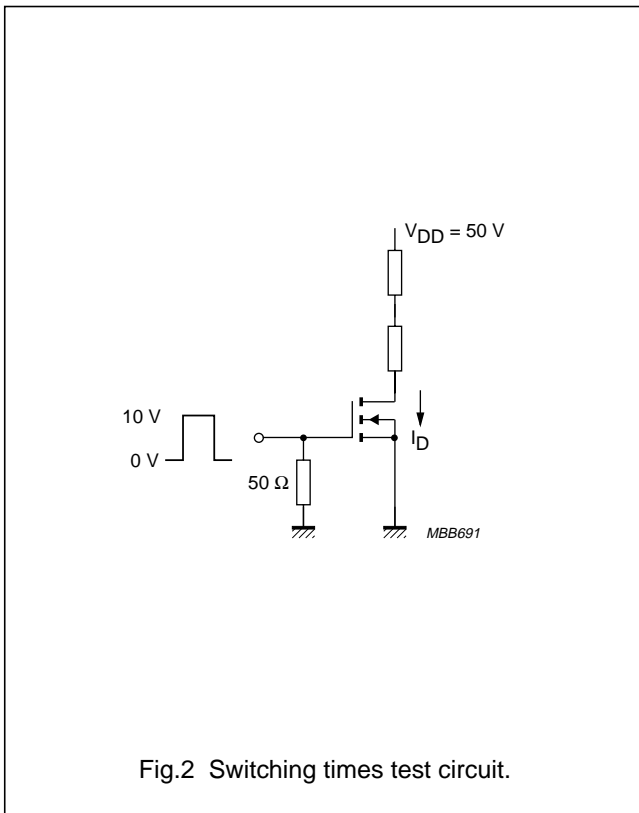


Fig.2 Switching times test circuit.

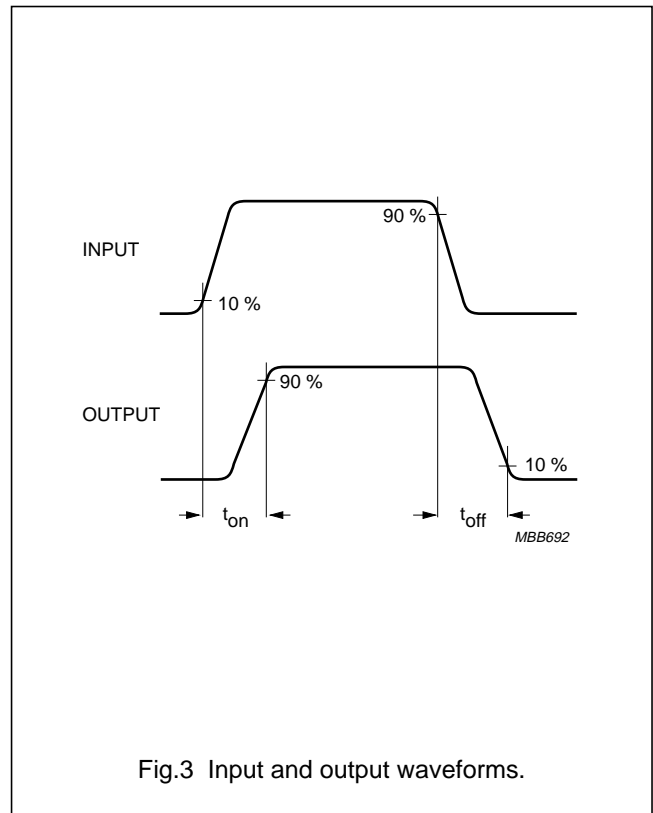


Fig.3 Input and output waveforms.

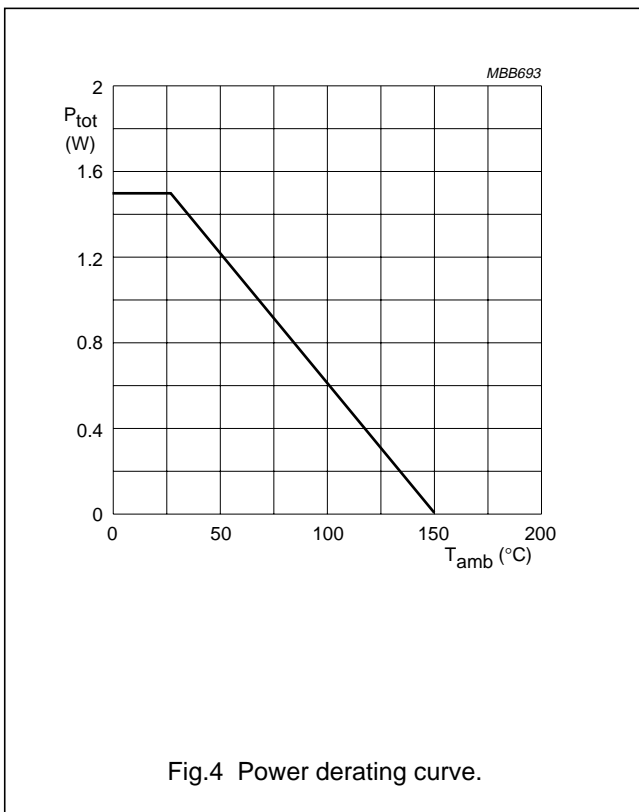
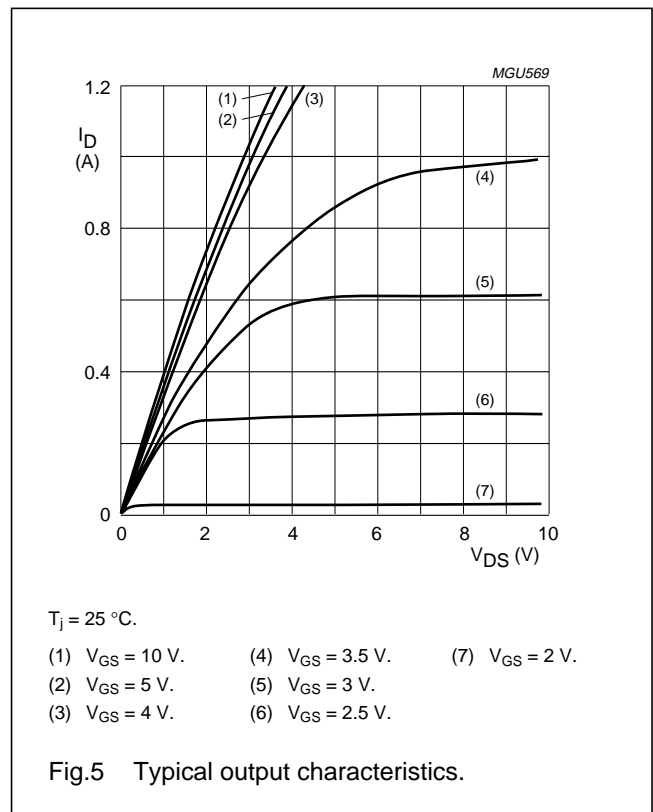


Fig.4 Power derating curve.



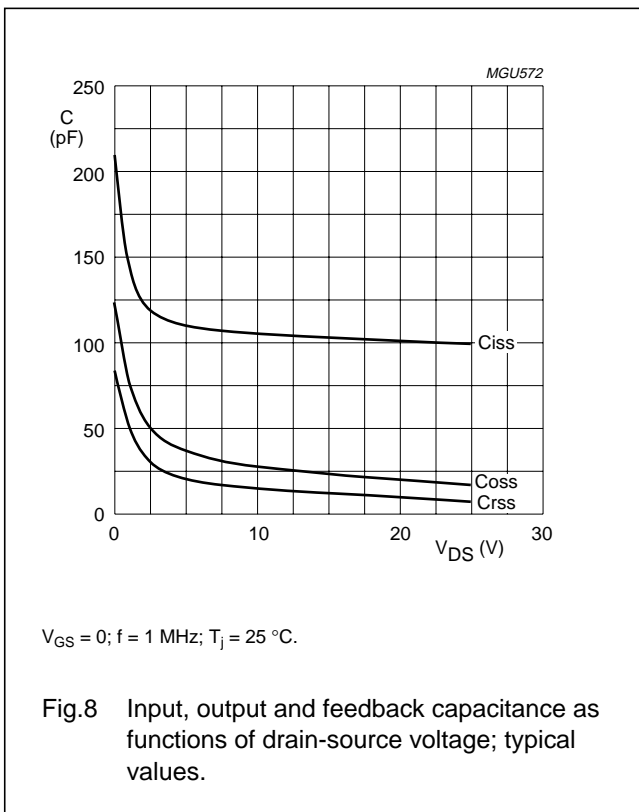
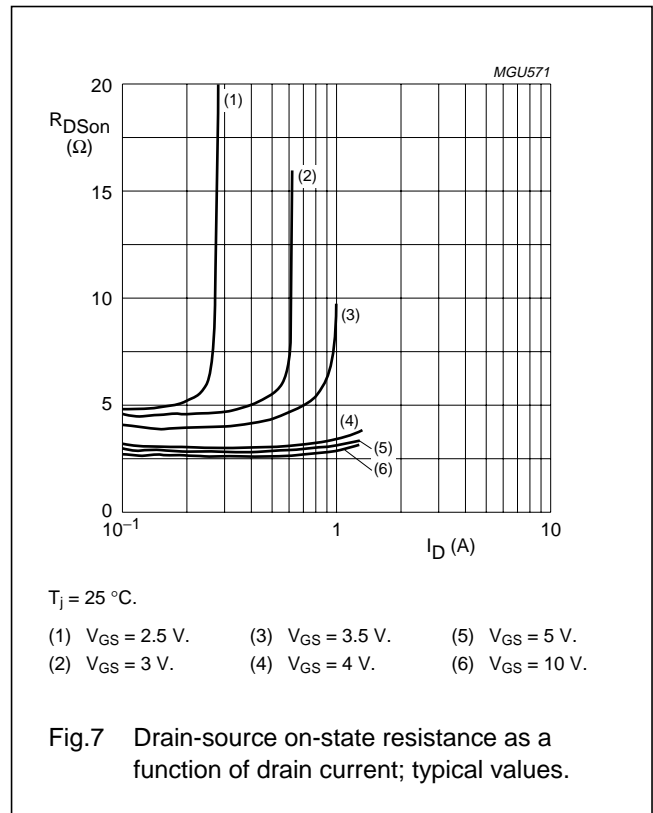
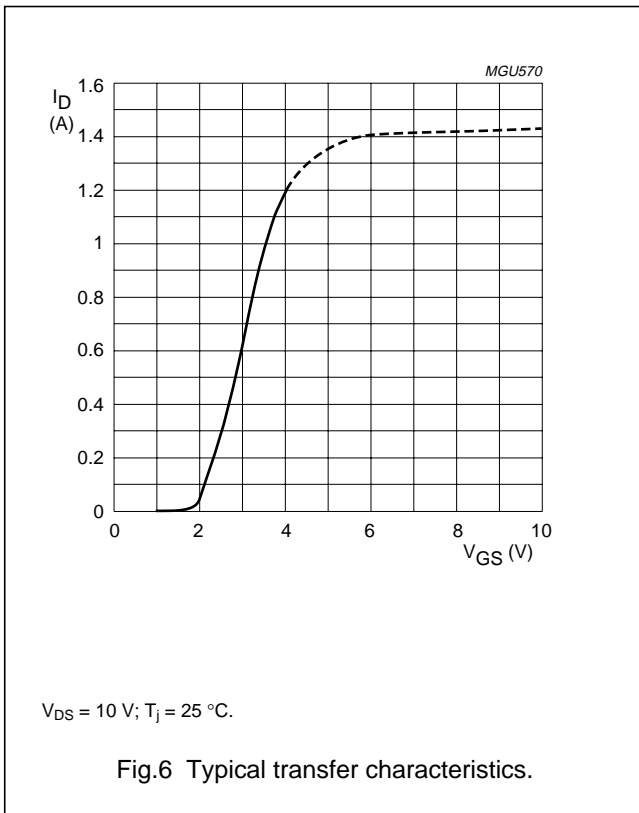
T<sub>j</sub> = 25 °C.

- (1) V<sub>GS</sub> = 10 V.
- (2) V<sub>GS</sub> = 5 V.
- (3) V<sub>GS</sub> = 4 V.
- (4) V<sub>GS</sub> = 3.5 V.
- (5) V<sub>GS</sub> = 3 V.
- (6) V<sub>GS</sub> = 2.5 V.
- (7) V<sub>GS</sub> = 2 V.

Fig.5 Typical output characteristics.

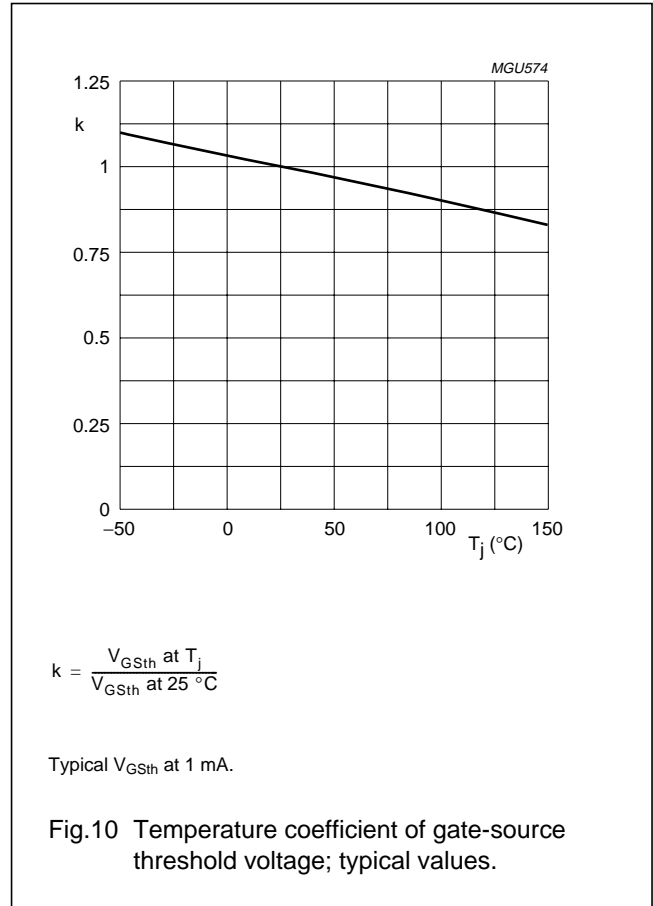
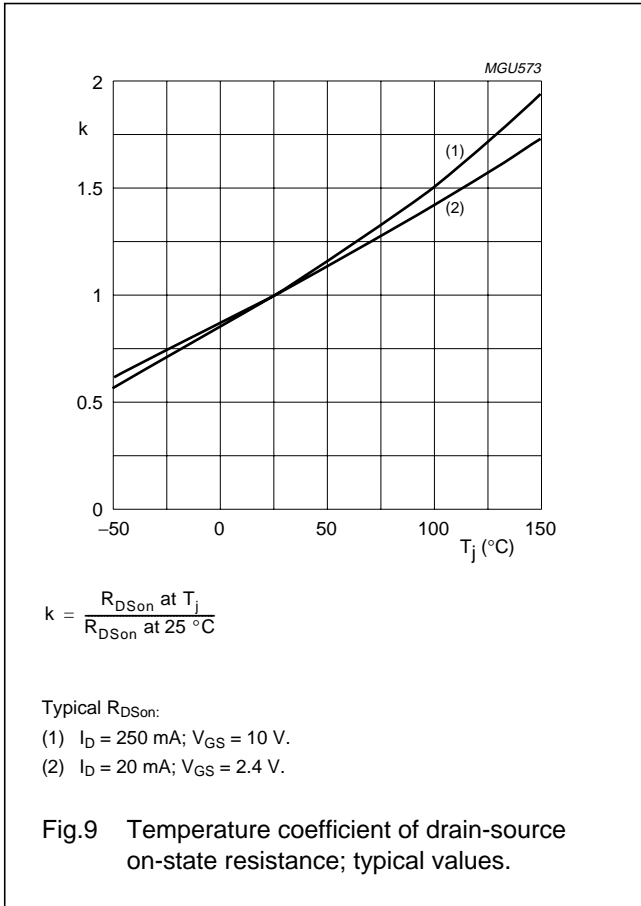
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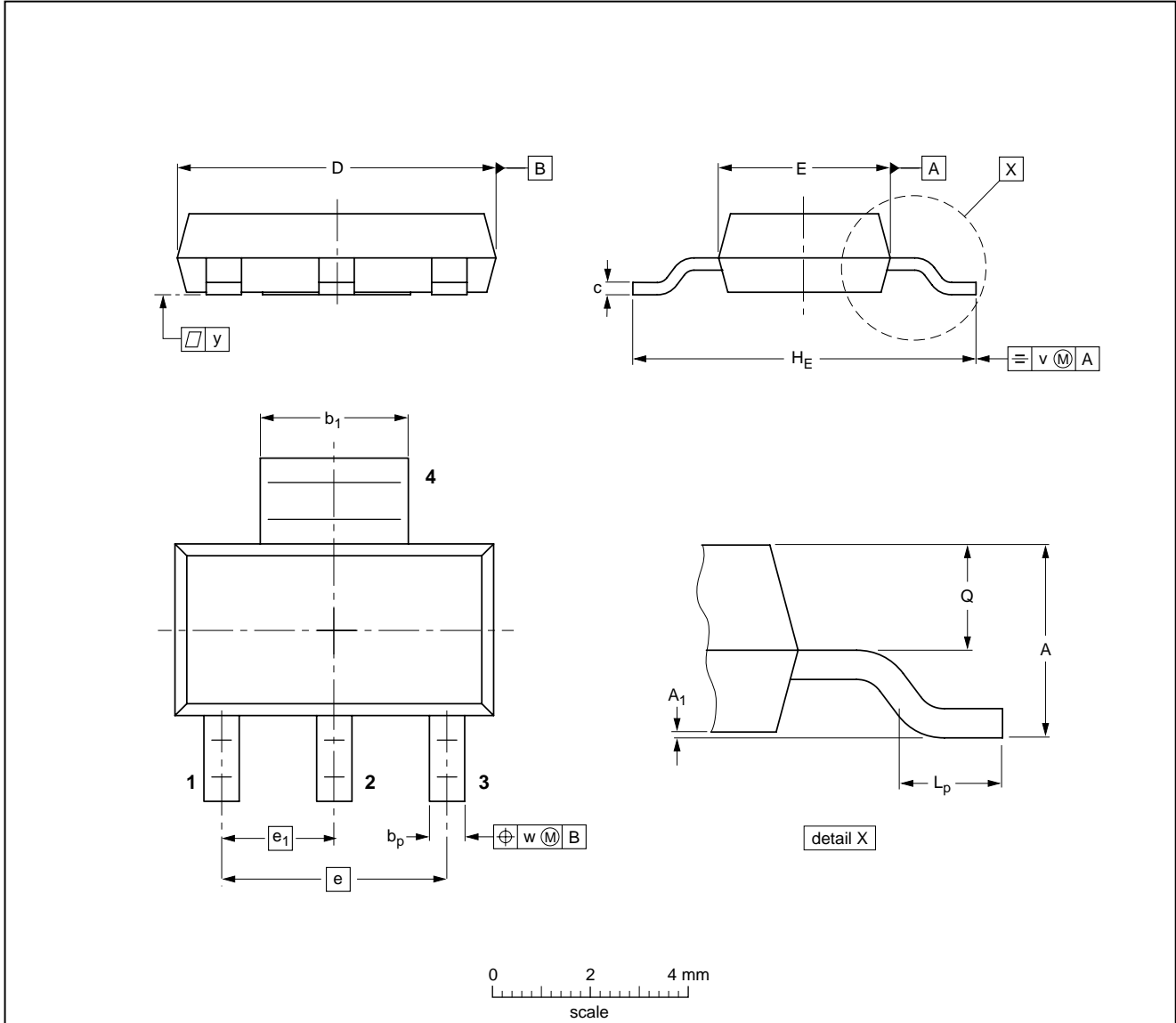
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT223			SC-73		97-02-28 99-09-13



# N-channel enhancement mode vertical D-MOS transistor

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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**NOTES**

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**NOTES**

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