



Description

The XR77103-A0R5 universal PMIC features three 2A synchronous high-efficiency, buck regulators with integrated power switches. They can operate in 5V, 9V and 12V powered systems with minimal required external component thus providing the smallest size solution possible. Two of the outputs may be paralleled for output currents up to 5A peak with steady state current of up to 4A.

The output voltage of each converter can be adjusted by external resistor divider down to voltage as low as 0.8V. With a nominal switching frequency of 500kHz, the regulators can also be synchronized to an external clock in applications where EMI control is critical.

XR77103-A0R5 features a supervisor circuit that monitors each converter output. PGOOD pin is asserted once sequencing is done, outputs are reported in regulation and the reset timer expires. The polarity of the signal is active high. A pulse skipping mode (PSM) reduces switching losses maintaining high efficiency when the system is unloaded or in standby mode.

FEATURES

- 4.5V to 14V wide input supply voltage range
- Built-in MOSFET and synchronous rectifier
- 0.8V, high accuracy reference (1%)
- Current-mode control with simple compensation circuit
- External synchronization
- Power good
- Protection
 - Thermal shutdown
 - Overvoltage transient protection
 - Overcurrent protection
- 32-pin 4mm x 4mm TQFN package

APPLICATIONS

- FPGA and DSP supplies
- Video processor supplies
- Applications processor power

Typical Application

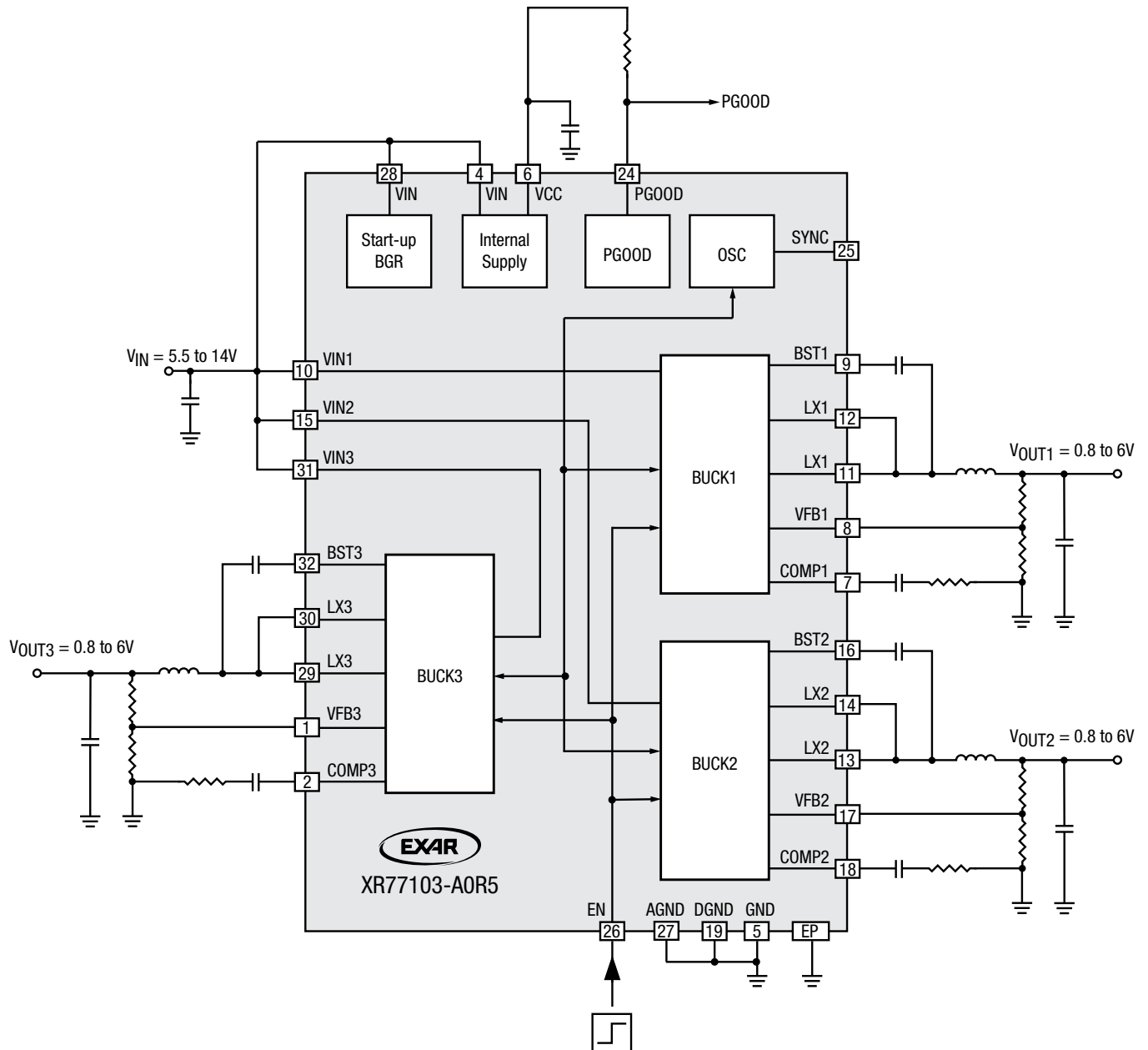


Figure 1. Typical Application

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

V_{IN1} , V_{IN2} , V_{IN3} , $LX1$, $LX2$, $LX3$	-0.3V to 18V
EN, V_{CC}	-0.3V to 7V
PGOOD, SYNC	-0.3V to 7V
BST# to LX#	-0.3V to 7V
AGND, DGND to GND.....	-0.3V to 0.3V
Storage temperature.....	-65°C to 150°C
Junction temperature.....	150°C
Power dissipation	Internally Limited
Lead temperature (soldering, 10 seconds).....	260°C
CDM	700V
ESD rating (HBM – human body model)	2kV

Operating Conditions

V_{IN}	4.5V to 14V
V_{CC}	4.5V to 5.5V
LX#	-0.3V to 14V ⁽¹⁾
Junction temperature range (T_J).....	-40°C to 125°C
XR77103 package power dissipation max at 25°C	3.4W
XR77103 thermal resistance θ_{JA}	30°C/W

NOTE:

1. LX# pins' DC range is from -0.3V, transient -1V for less than 10ns.

Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $EN = V_{CC}$, $f_{SW} = 500\text{kHz}$, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V _{IN}	Input voltage range		•	5.5		14	V
V _{IN}	Input voltage range	V _{CC} tied to V _{IN}	•	4.5		5.5	V
V _{UVLO}	UVLO threshold	V _{IN} rising/falling			4.22/4.1		V
UVLO _{DEGLITCH}	UVLO deglitch	Rising/falling			220		μs
I _{VIN}	V _{IN} supply current	EN = GND			250		μA
I _{VINQ}		EN = high, no load			2.6		mA
Internal Supply Voltage							
V _{CC}	Internal biasing supply	I _{LOAD} = 0mA	•	4.9	5	5.1	V
I _{CC}	Internal biasing supply current	V _{IN} = 12V	•			10	mA
V _{UVLO}	UVLO threshold for V _{CC}	V _{CC} rising			3.8		V
		V _{CC} falling			3.6		V
UVLO _{DEGLITCH}	UVLO deglitch for V _{CC}	Falling edge			220		μs

Electrical Characteristics (Continued)

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $EN = V_{CC}$, $f_{SW} = 500\text{kHz}$, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protections							
T _{SD}	Thermal shutdown temperature	Temperature rising, Non-latch off. T _{SD} release threshold, temperature = T _{SD} -HY _{TSD}			160		°C
HY _{TSD}	Thermal shutdown hysteresis				20		°C
T _{SD_DEGLITCH}	Thermal shutdown deglitch				220		μs
V _{OVBUCK}	Threshold voltage for buck over voltage	Output rising (HS FET will be forced off)			109		%
		Output falling (HS FET will be allowed to switch)			107		%
Buck Converter							
f _{SW}	Switching frequency				500		kHz
t _{SS}	Soft-start period				6		ms
I _{LIMx}	Peak inductor current limit				3.5		A
R _{ON_HSx}	HS switch on-resistance	V _{IN} = 12V			200		mΩ
R _{ON_LS1}	LS switch on-resistance of Buck1	V _{IN} = 12V			60		mΩ
R _{ON_LS2/3}	LS switch on-resistance of Buck2/3	V _{IN} = 12V			80		mΩ
I _{OX}	Output current capability	Continuous loading ⁽¹⁾			2		A
D _{MAX}	Maximum duty cycle				95		%
t _{ON MIN}	Minimum on time				120		ns
	Line regulation (ΔV _{OX} /ΔV _{INX})	V _{INX} = 5.5 to 14V, I _{OX} = 1A			0.5		%V _O
	Load regulation (ΔV _{OX} /ΔI _{OX})	I _O = 10 to 90%, I _O = MAX			0.5		%V _O /A
	Output voltage accuracy	V _{IN} = 12V	•	-1	Normal	1	%
		5.5V ≤ V _{IN} ≤ 14V	•	-2	Normal	2	
SYNC _{FREQ}	Synchronization frequency			525			kHz
SYNC _{D_MIN}	Synchronization signal minimum duty cycle		•	40			%
SYNC _{D_MAX}	Synchronization signal maximum duty cycle		•			60	%

NOTE:

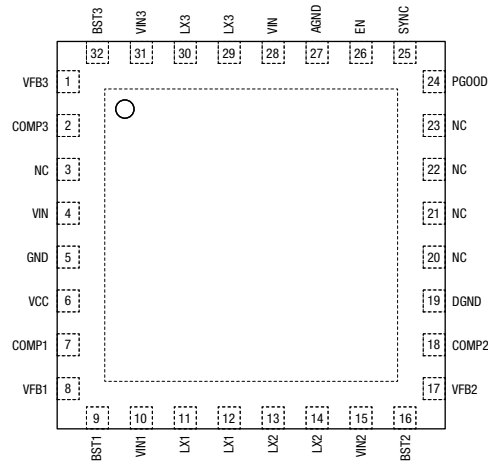
1. Subject to thermal derating. Design must not exceed the package thermal rating.

Electrical Characteristics (Continued)

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $EN = V_{CC}$, $f_{SW} = 500\text{kHz}$, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Good Reset Generator							
V_{UVBUCK}	Threshold voltage for buck under voltage	Output falling, (disabled after t_{ON_HICCUP})			85		%
		Output rising, (PG will be asserted)			90		
$t_{PG_DEGLITCH}$	Deglitch time	Rising and falling			22		ms
t_{ON_HICCUP}	Hiccup mode on time	$V_{UVBUCKX}$ asserted			24		ms
t_{OFF_HICCUP}	Hiccup mode off time	Once t_{OFF_HICCUP} elapses, all converters will start up again			30		ms
t_{RP}	Minimum reset period				2		s
R_{PG}	Power good pull-down on resistance				14	50	Ω
Input Threshold (SYNC, EN)							
V_{IH}	Input threshold high	V_{INPUT} rising	•	2.07		2.53	V
V_{IL}	Input threshold low	V_{INPUT} falling	•	1.36		1.67	V

Pin Configuration



Pin Functions

Pin Number	Pin Name	Description
1	VFB3	Buck 3 feedback pin.
2	COMP3	Compensation pin for Buck 3. Connect a series RC circuit to this pin for compensation.
3	NC	No connect.
4	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
5	GND	Ground.
6	VCC	Internal supply. Connect a ceramic capacitor from this pin to ground.
7	COMP1	Compensation pin for Buck 1. Connect a series RC circuit to this pin for compensation.
8	VFB1	Buck 1 feedback pin.
9	BST1	Bootstrap capacitor for Buck 1. Connect a bootstrap capacitor from this pin to LX1.
10	VIN1	Input supply for Buck 1. Connect a capacitor as close as possible to this pin.
11	LX1	Switching node for Buck 1.
12	LX1	Switching node for Buck 1.
13	LX2	Switching node for Buck 2.
14	LX2	Switching node for Buck 2.
15	VIN2	Input supply for Buck 2. Connect a capacitor as close as possible to this pin.
16	BST2	Bootstrap capacitor for Buck 2. Connect a bootstrap capacitor from this pin to LX2.
17	VFB2	Buck 2 feedback pin.
18	COMP2	Compensation pin for Buck 2. Connect a series RC circuit to this pin for compensation.
19	DGND	Digital ground.
20	NC	No connect.

Pin Functions (Continued)

Pin Number	Pin Name	Description
21	NC	No connect.
22	NC	No connect.
23	NC	No connect.
24	PGOOD	Power good output. Open drain output asserted after all converters are sequenced and within regulation.
25	SYNC	External clock input pin. Connect to signal ground when unused.
26	EN	Enable control input. Set EN high to enable converters.
27	AGND	Analog ground.
28	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
29	LX3	Switching node for Buck 3.
30	LX3	Switching node for Buck 3.
31	VIN3	Input supply for Buck 3. Connect a capacitor as close as possible to this pin.
32	BST3	Bootstrap capacitor for Buck 3. Connect a bootstrap capacitor from this pin to LX3.
-	E-PAD	Connect to power ground.

Typical Performance Characteristics

All data taken at $f_{SW} = 500\text{kHz}$, $T_A = 25^\circ\text{C}$, no airflow, unless otherwise specified.

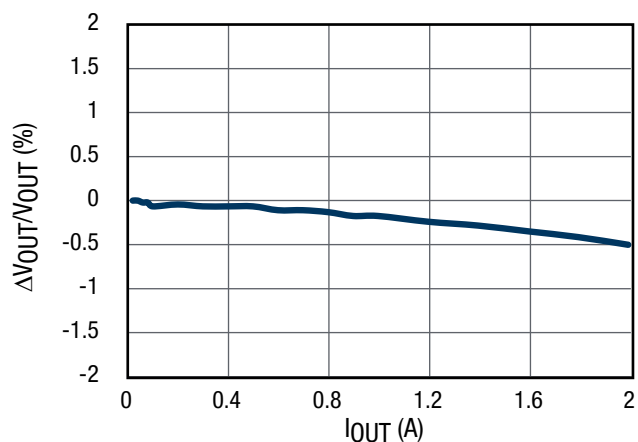


Figure 2. Load Regulation Channel 1,
12V_{IN}, 3.3V_{OUT}

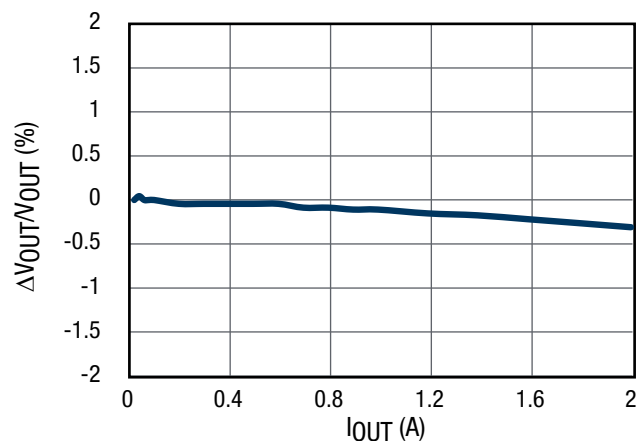


Figure 3. Load Regulation Channel 1,
5V_{IN}, 3.3V_{OUT}

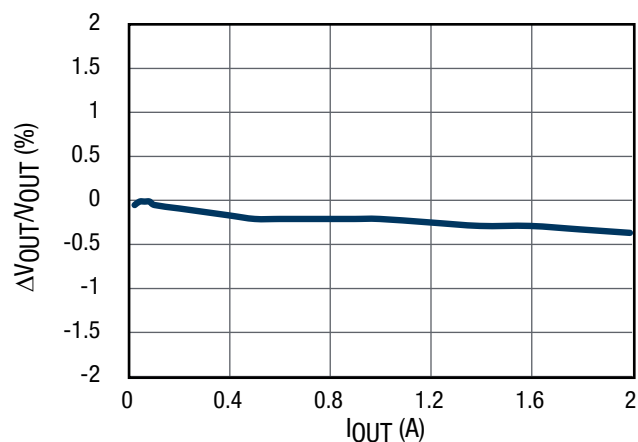


Figure 4. Load Regulation Channel 2,
12V_{IN}, 1.8V_{OUT}

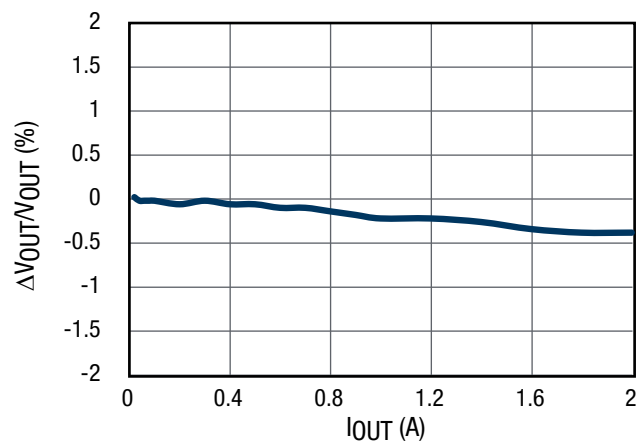


Figure 5. Load Regulation Channel 2,
5V_{IN}, 1.8V_{OUT}

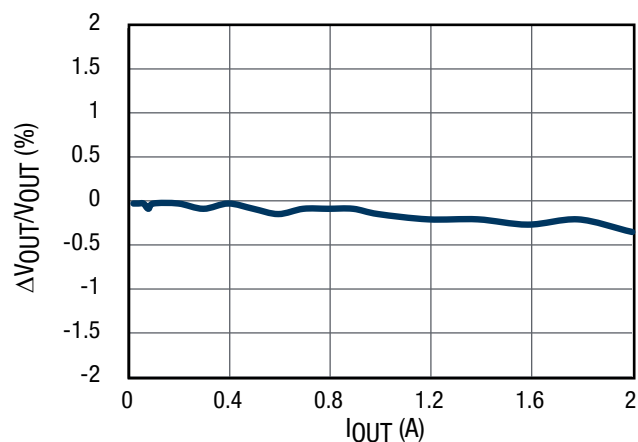


Figure 6. Load Regulation Channel 3,
12V_{IN}, 1.2V_{OUT}

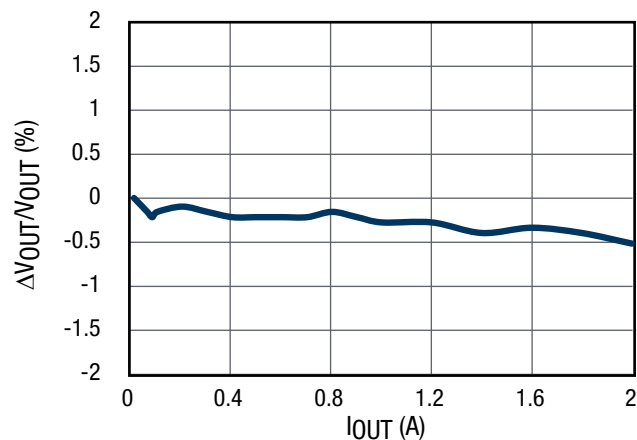


Figure 7. Load Regulation Channel 3,
5V_{IN}, 1.2V_{OUT}

Typical Performance Characteristics (Continued)

All data taken at $f_{SW} = 500\text{kHz}$, $T_A = 25^\circ\text{C}$, no airflow, unless otherwise specified.

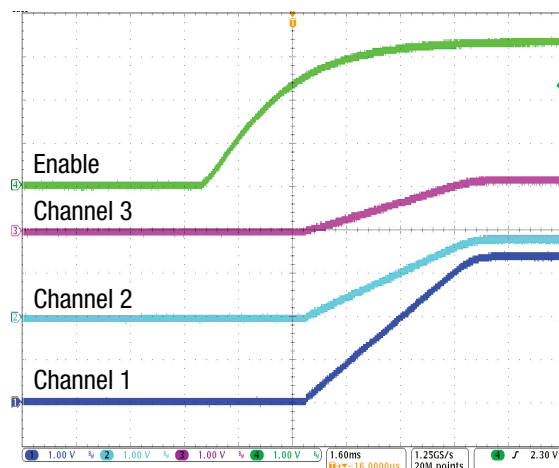


Figure 8. Power-up Sequence

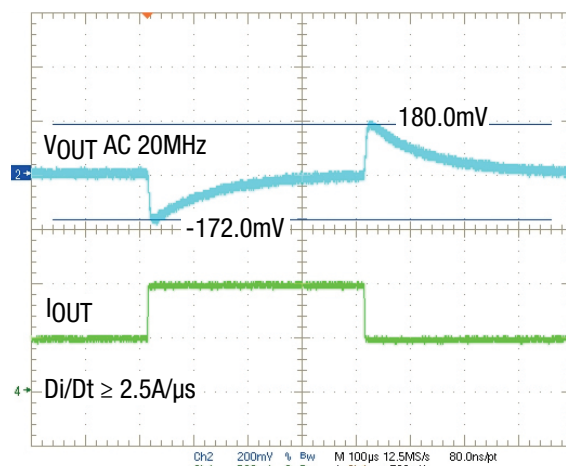


Figure 9. 12V_{IN} , 5.0V_{OUT} Transient Response, 0.5A to 1.0A

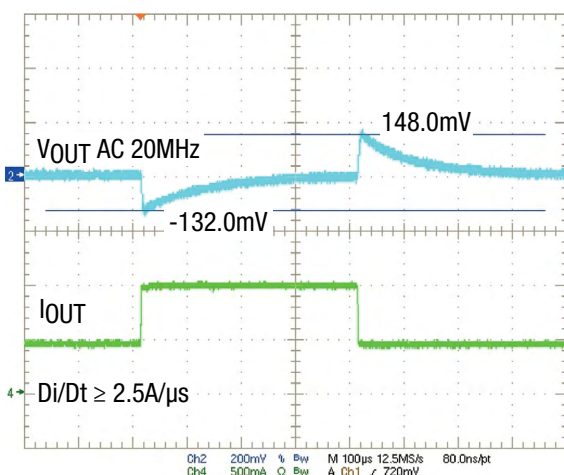


Figure 10. 12V_{IN} , 3.3V_{OUT} Transient Response, 0.5A to 1.0A

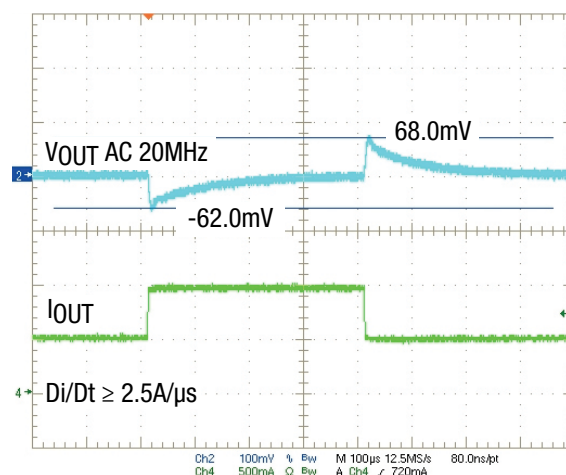


Figure 11. 12V_{IN} , 1.8V_{OUT} Transient Response, 0.5A to 1.0A

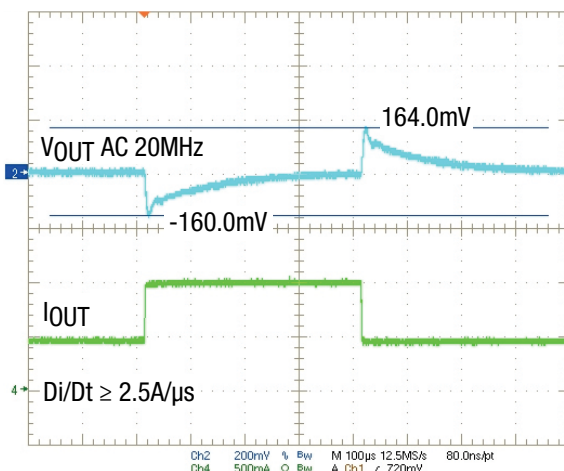


Figure 12. 5V_{IN} , 3.3V_{OUT} Transient Response, 0.5A to 1.0A

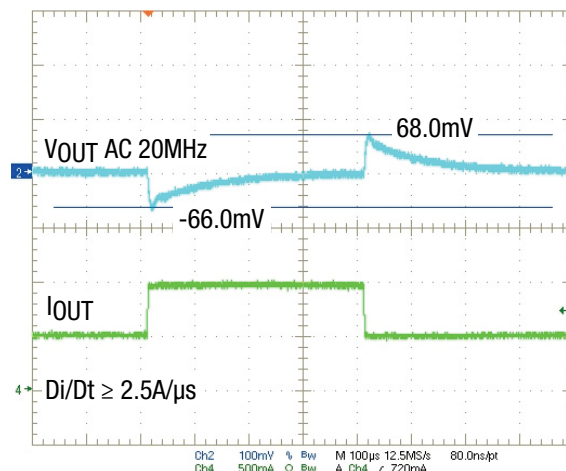


Figure 13. 5V_{IN} , 1.8V_{OUT} Transient Response, 0.5A to 1.0A

Typical Performance Characteristics (Continued)

Efficiency

$f_{SW} = 500\text{kHz}$, $T_A = 25^\circ\text{C}$, no airflow, only individual channel operating, inductor losses are included.

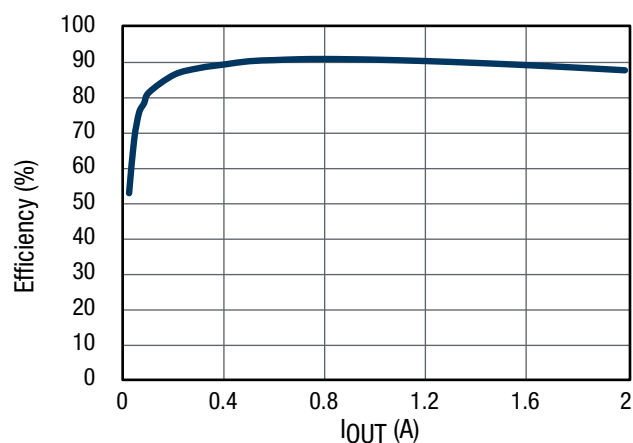


Figure 14. Efficiency Channel 1,
12V_{IN} 3.3V_{OUT}

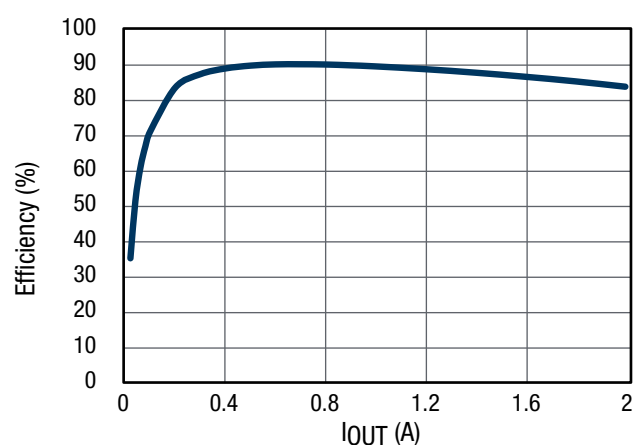


Figure 15. Efficiency Channel 1,
5V_{IN} 3.3V_{OUT}

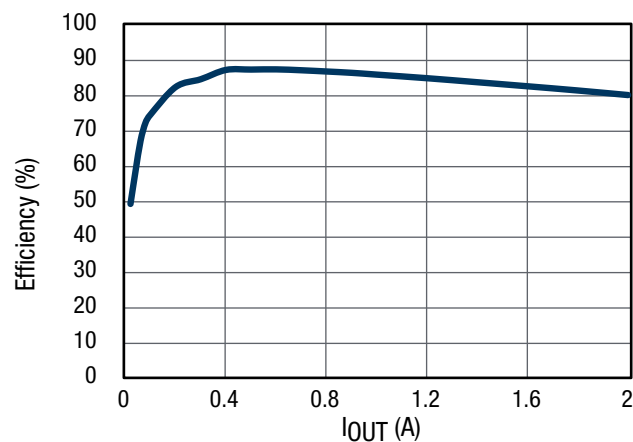


Figure 16. Efficiency Channel 2,
12V_{IN} 1.8V_{OUT}

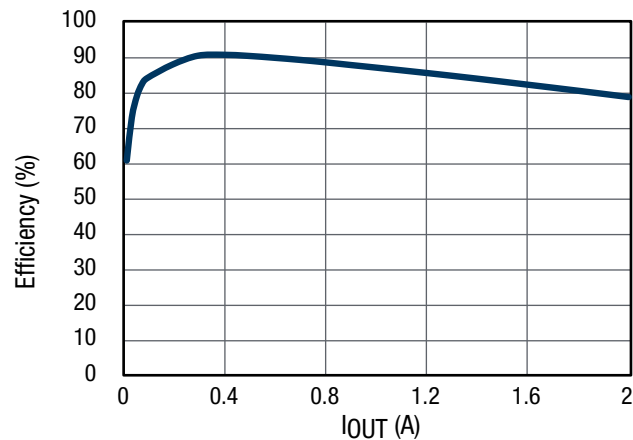


Figure 17. Efficiency Channel 2,
5V_{IN} 1.8V_{OUT}

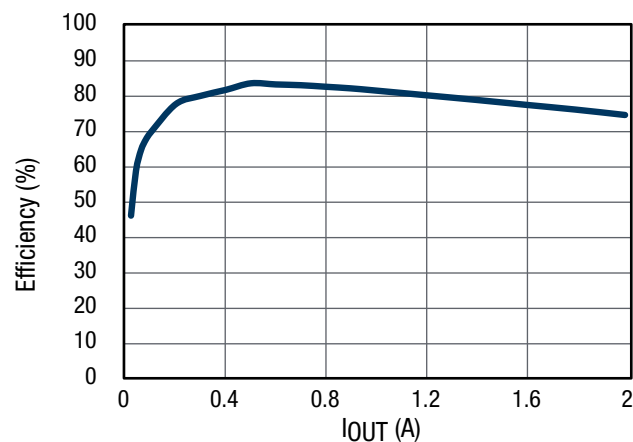


Figure 18. Efficiency Channel 3,
12V_{IN} 1.2V_{OUT}

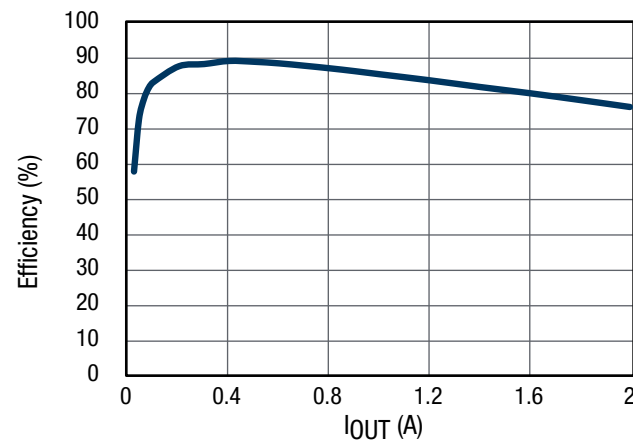


Figure 19. Efficiency Channel 3,
5V_{IN} 1.2V_{OUT}

Typical Performance Characteristics (Continued)

Thermal Characteristics

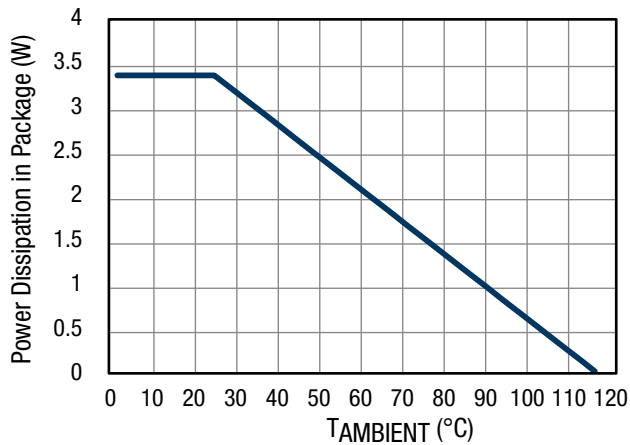
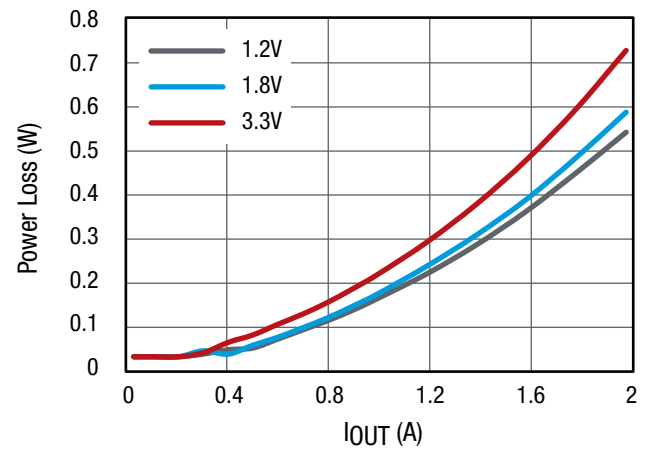
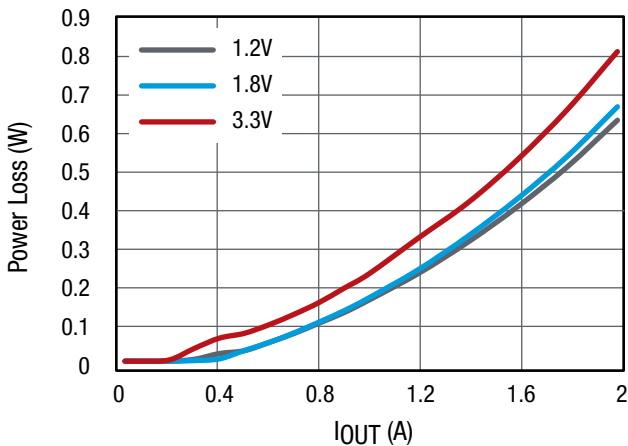
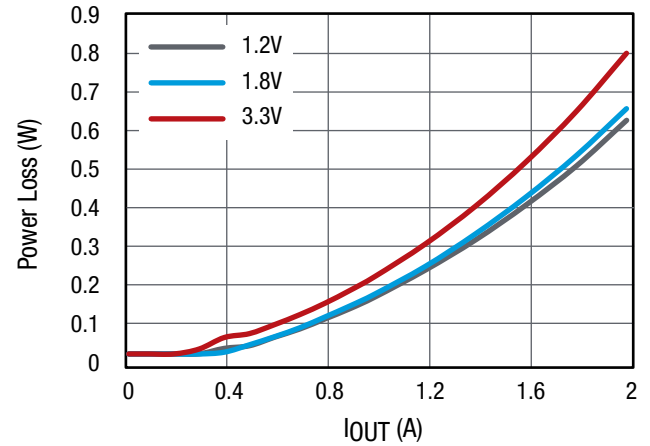
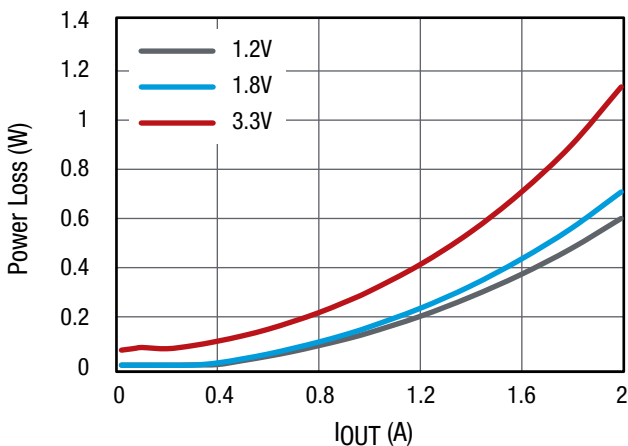
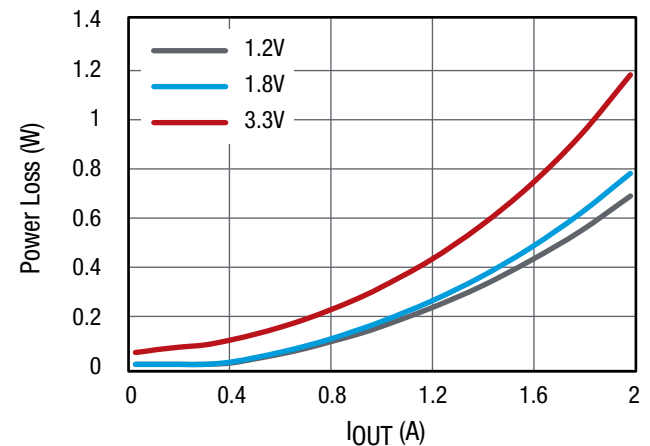


Figure 20. Package Thermal Derating

Figure 21. Channel 1 Power Loss at $f_{SW} = 500\text{kHz}$, $V_{IN} = 12\text{V}$, No AirflowFigure 22. Channel 2 Power Loss at $f_{SW} = 500\text{kHz}$, $V_{IN} = 12\text{V}$, No AirflowFigure 23. Channel 3 Power Loss at $f_{SW} = 500\text{kHz}$, $V_{IN} = 12\text{V}$, No AirflowFigure 24. Channel 1 Power Loss at $f_{SW} = 500\text{kHz}$, $V_{IN} = 5\text{V}$, No AirflowFigure 25. Channel 2 Power Loss at $f_{SW} = 500\text{kHz}$, $V_{IN} = 5\text{V}$, No Airflow

Typical Performance Characteristics (Continued)

Thermal Characteristics

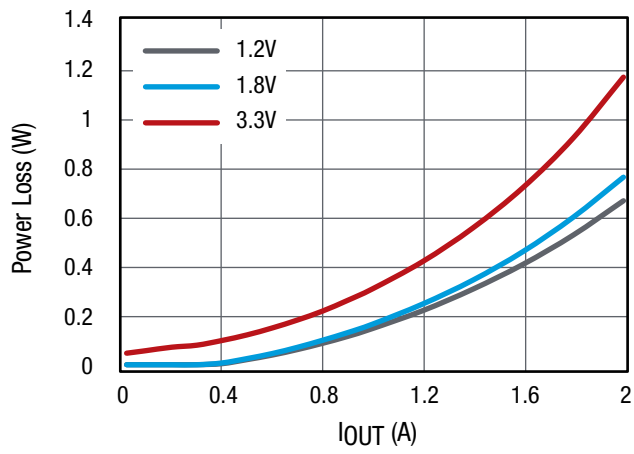


Figure 26. Channel 3 Power Loss at
 $f_{SW} = 500\text{kHz}$, $V_{IN} = 5\text{V}$, No Airflow

Functional Block Diagram

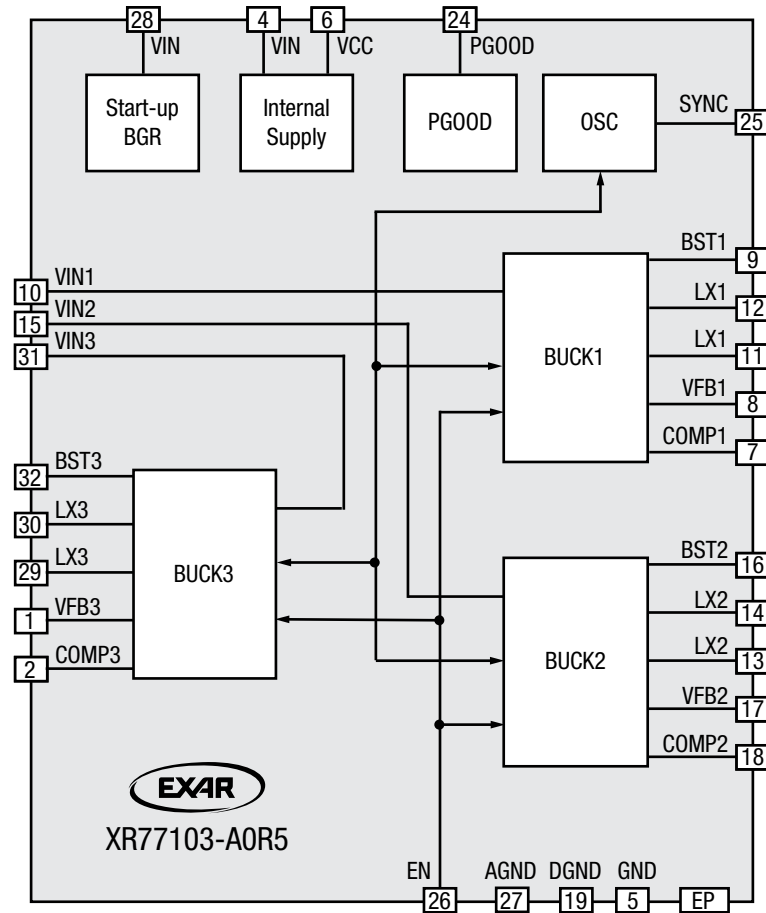


Figure 27. Functional Block Diagram

Applications Information

Operation

XR77103-A0R5 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. XR77103-A0R5 can support 4.5V to 14V input supply, high load current, 500kHz clocking. The buck converters have a PSM mode which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by 180 degree out-of-phase operation among converters. All three buck converters have peak current mode control which simplifies external frequency compensation. Each buck converter has peak inductor current limit of 3.5A. The device has a power good comparator monitoring the output voltage. Soft-start for each converter is 6ms. All outputs start up once EN pin is set high.

Output Voltage Setting

Output voltage is set externally using an external resistor divider. Output voltage is determined by the following equation.

$$V_{OUTX} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$

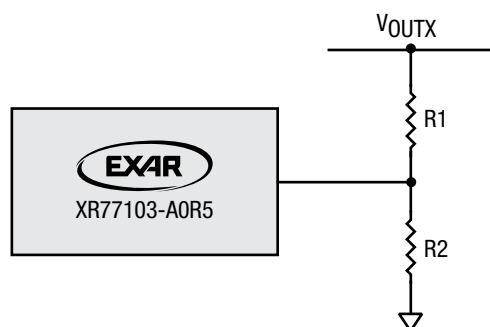


Figure 28. Output Voltage Setting

This can make the device applicable to AVS (automatic voltage scaling) system. Output voltage can be adjusted automatically by external DC voltage. Figure 29 shows application circuit of supply for AVS system.

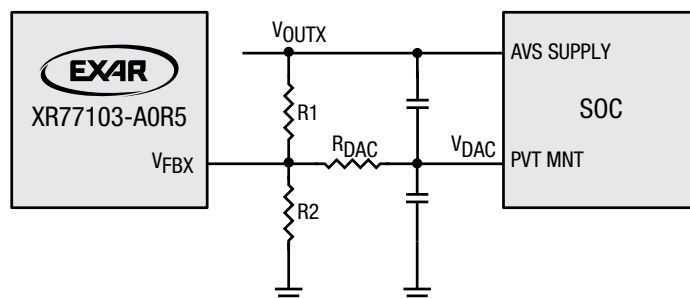


Figure 29. AVS Control

Frequency Compensation

In order to properly frequency compensate the device, the following component selection is recommended.

V _{IN} (V)	V _{OUT} (V)	L (μH)	C _{OUT} (μF)	R _{COMP} (kΩ)	C _{COMP} (nF)
12/5.0	1.0	2.2	22 x 3	10	4.7
12/5.0	1.2	2.2	22 x 3	10	4.7
12/5.0	1.5	3.3	22 x 3	20	4.7
12/5.0	1.8	3.3	22 x 2	20	4.7
12/5.0	2.5	4.7	22 x 2	20	4.7
12/5.0	3.3	4.7	22 x 1	20	4.7
12	5.0	6.8	22 x 1	20	4.7

Synchronization

The status of the SYNC pin will be ignored during start-up and the XR77103-A0R5's control will only synchronize to an external signal after the PGOOD signal is asserted. When synchronization is applied, the sync pulse frequency must be higher than the PWM oscillator frequency (525kHz) to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to signal ground.

Although the device can lock to external clock running up to 2.31MHz, doing this will alter the timing characteristics and degrade thermal performance.

Applications Information (Continued)

Out-of-Phase Operation

Channels 1 and 2 operate in phase while channel 3 operates 180 degrees out-of-phase with the other two converters (see Figure 30). This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

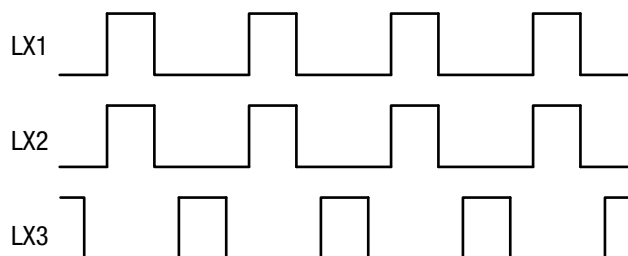


Figure 30. Out-of-Phase Operation

Two Buck Regulators in Parallel Operation (Current Sharing)

The XR77103-A0R5 can be used in parallel operation to increase output current capacity. To enable this, a user needs:

- To connect V_{OUT2} and V_{OUT3} together.
- To connect COMP2 and COMP3 together.
- Regulate the channels 2 and 3 to the same V_{OUT} .

Then, the channels 2 and 3 will run in parallel and load current is shared in average.

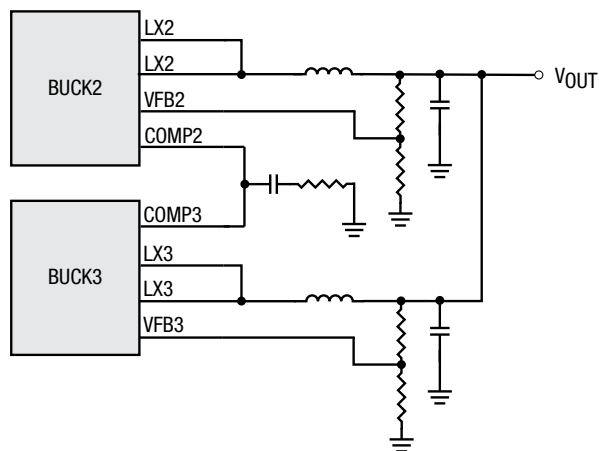


Figure 31. Parallel Operation

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of their nominal output voltage and the PGOOD reset timer expires. The polarity of the PGOOD is active high. The PGOOD reset time is 2s.

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR77103-A0R5 (30°C/W) is specified in the Operating Conditions section of this datasheet. The θ_{JA} thermal resistance specification is based on the XR77103-A0R5 evaluation board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

The package thermal derating and power loss curves are shown in Figures 20 through 26. These correspond to input voltages of 12V and 5V.

Layout Guidelines

Proper PCB layout is crucial in order to obtain a good thermal and electrical performance.

For thermal considerations it is essential to use a number of thermal vias to connect the central thermal pad to the ground layer(s).

In order to achieve good electrical and noise performance following steps are recommended:

- Place the output inductor close to the LX pins and minimize the area of the connection. Doing this on the top layer is advisable.
- Central thermal pad shall be connected to the power ground connections to as many layers as possible.
- Output filtering capacitor shall share the same power ground connection as the input filtering capacitor. Connection to the signal ground plane shall be done with vias placed at the output filtering capacitors.
- AC current loops formed by input filtering capacitors, output filtering capacitors, output inductors, and the regulator pins shall be minimized.
- GND, AGND, DGND pins shall be connected to the signal ground plane.
- Compensation networks shall be placed close to the pins and referenced to the signal ground.
- V_{CC} bypass capacitor shall be placed close to the pin.

Applications Information (Continued)

Typical Applications

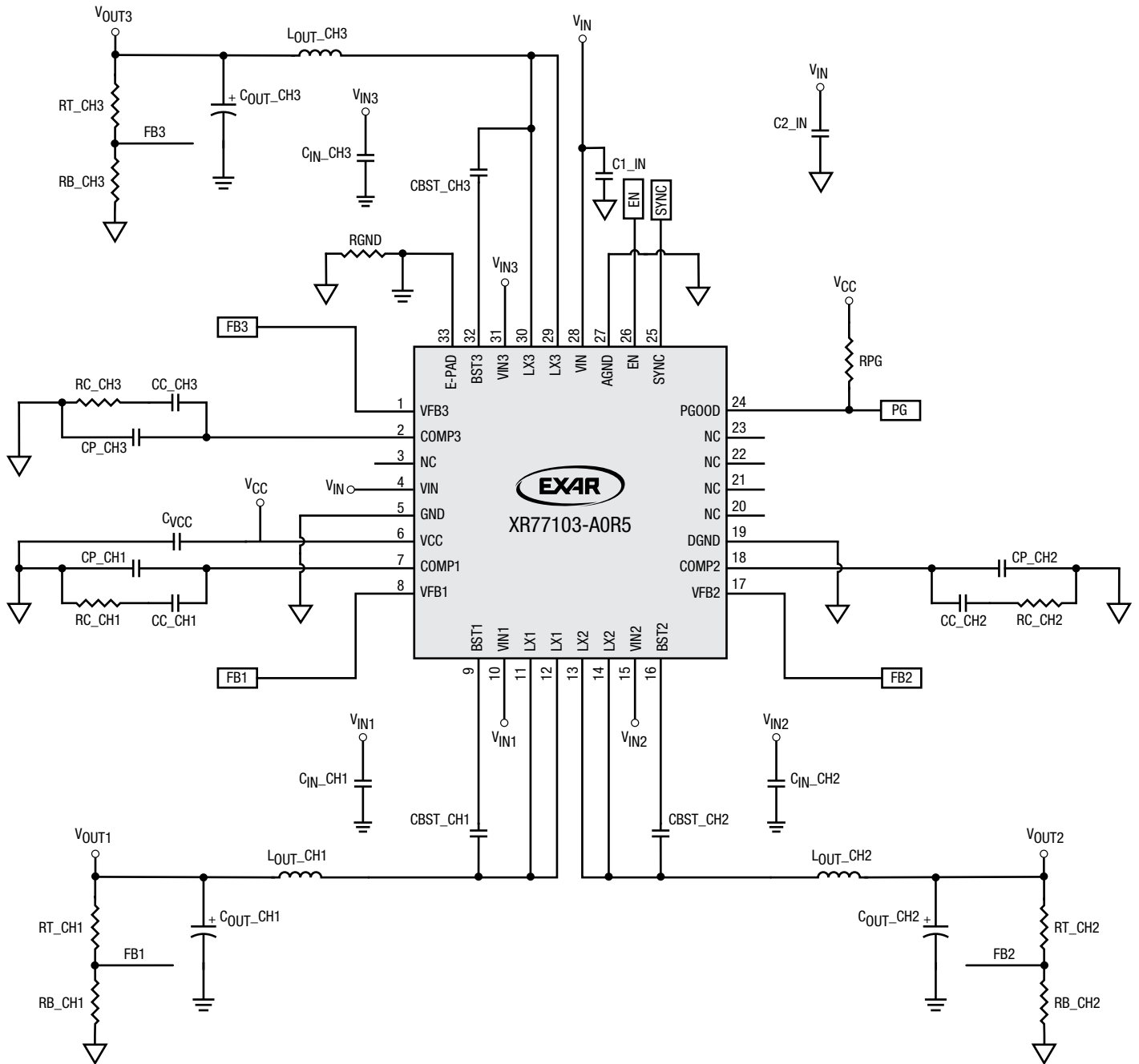
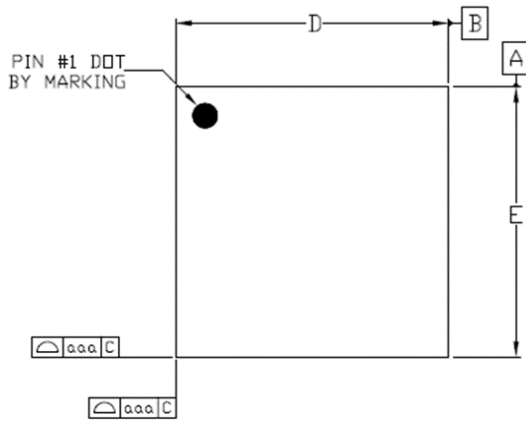


Figure 32. Typical Applications Schematic

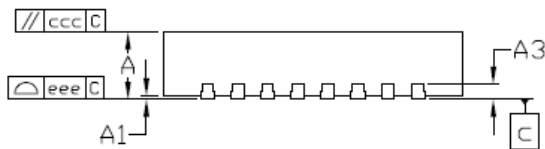
Package Description

Top View

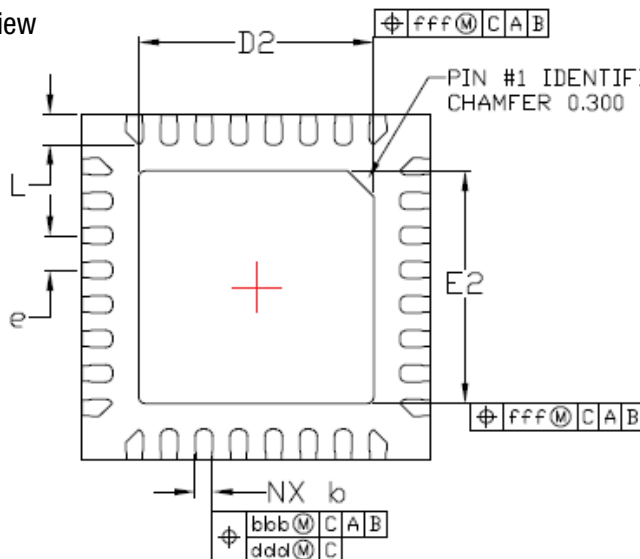


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	--	0.900
A1	0.000	--	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
b	0.150	0.200	0.250
L	0.300	0.350	0.400
e	0.400 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Side View



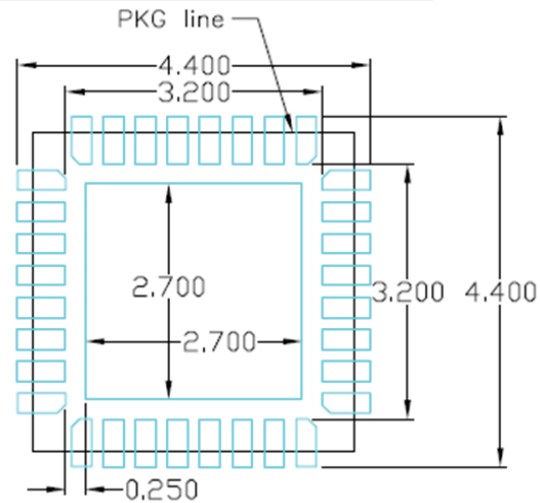
Bottom View



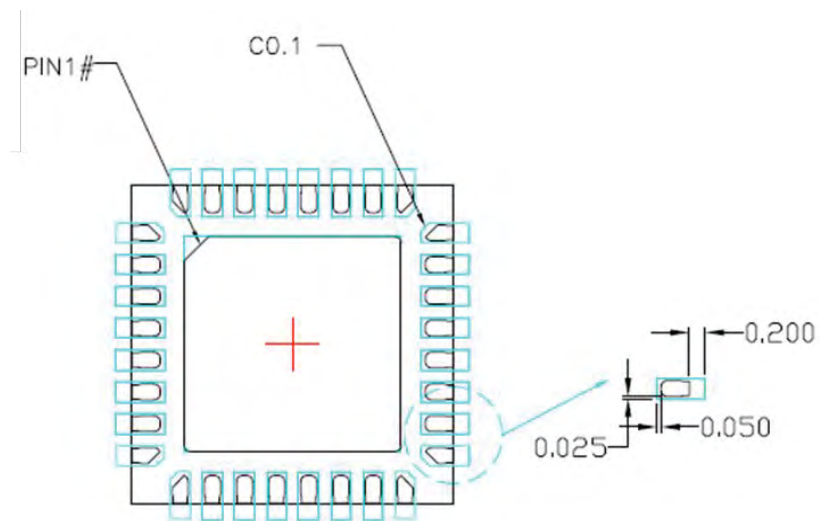
1. All dimensions are in millimeters
2. Dimensions and tolerance per Jedec MO-220

Package Description (Continued)

Recommended Land Pattern



Land Pattern

TOP VIEW

Overlap view

TOP VIEW

Order Information

Part Number	Operating Temperature Range	Environmental Rating	Package	Packaging Quantity	Marking
XR77103ELB-A0R5	-40°C ≤ T _J ≤ 125°C	RoHS compliant, halogen free	32-pin, 4mm x 4mm TQFN package	Bulk	EXAR XR77103
XR77103ELBTR-A0R5				3K/tape and reel	YYWWF01 XXXXXXX
XR77103EVB-A0R5	XR77103-A0R5 evaluation board				

NOTE:

YY = Year, WW = Work Week, XXXXXX = Lot Number.



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