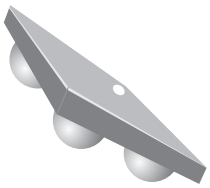
USBULC6-2F7

2-line Transil™ ultralow capacitance protection for high speed USB

Datasheet – production data



Flip Chip
(4 bumps)

Features

- Ultralow capacitance (1pF)
- Two data lines (D+ and D-) protected against ESD
- Breakdown voltage V_{BR} = 5.5 V min.
- Flip Chip 350 µm pitch, lead-free
- Very low leakage current
- Very small PCB area
- RoHS compliant

Benefits

- Minimized impact on rise and fall times for maximum data integrity
- Low PCB space occupation
- Higher reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
  - ±8 kV (contact discharge)
- MIL STD 883G - Method 3015.7
  - ±25 kV (Human body model)

Application

This device is designed to protect a high speed USB port in wireless handsets (up to 480 Mb/s according to USB 2.0 high speed specification).

Description

The USBULC6-2F7 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultra low line capacitance secures a high level of signal integrity without compromising the protection of downstream sensitive chips against the most stringently characterized ESD strikes.

Figure 1. Pin layout (bump side)

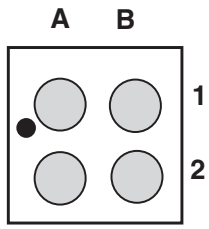
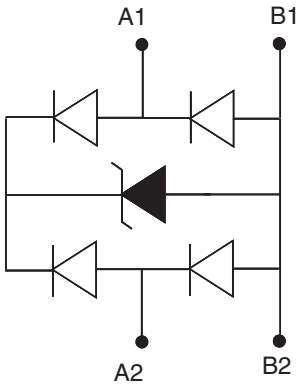


Figure 2. Device configuration



Note: B1 and B2 bumps must be grounded on the PCB together

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1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2: Contact discharge Air discharge	 10 30	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)	50	W
T_j	Operation junction temperature range	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L (1)	Maximum lead temperature for soldering during 10 s	260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 3. Electrical characteristics - definitions

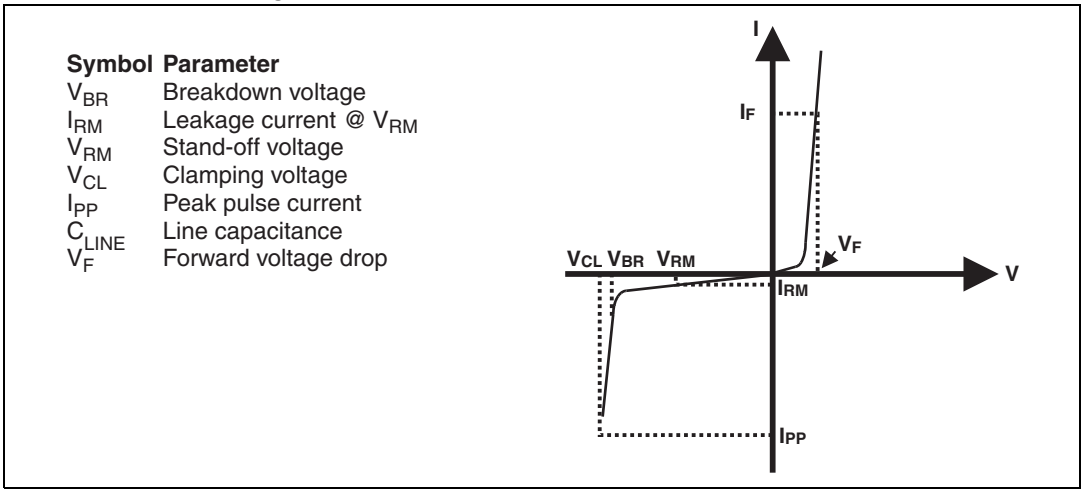


Table 2. Electrical characteristics - values (T_{amb} = 25 °C)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA		5.5	-	9	V
I_{RM}	V_{RM} = 3 V		-	-	70	nA
C_{line}	F = [200 MHz - 3000MHz], V_R = 0 V		-	1.0	1.35	pF
R_d	Dynamic resistance, pulse width 100 ns	I/O to GND		0.67		Ω
		GND to I/O		0.56		

Figure 4. Eye diagram, board only (according to USB high speed specification)

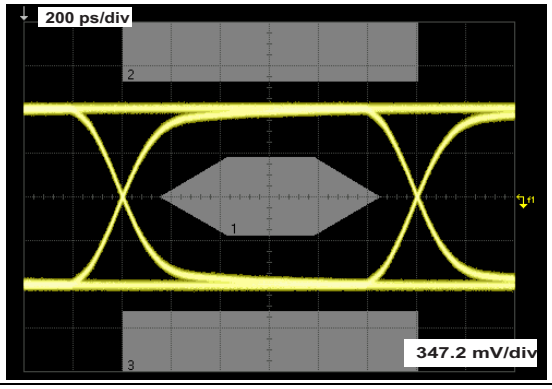


Figure 5. Eye diagram, board with USBULC6-2F7 (according to USB 2.0 high speed specification)

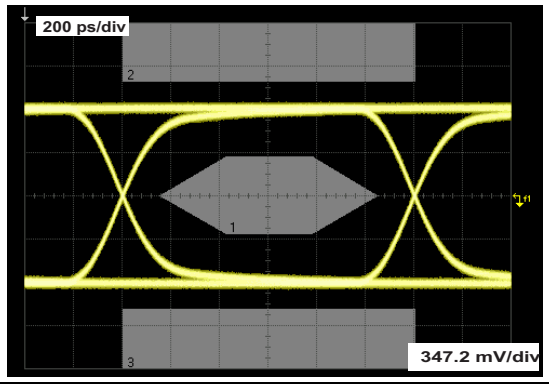


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)(1)

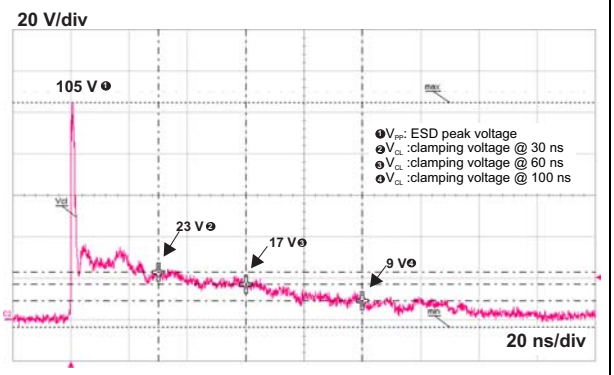
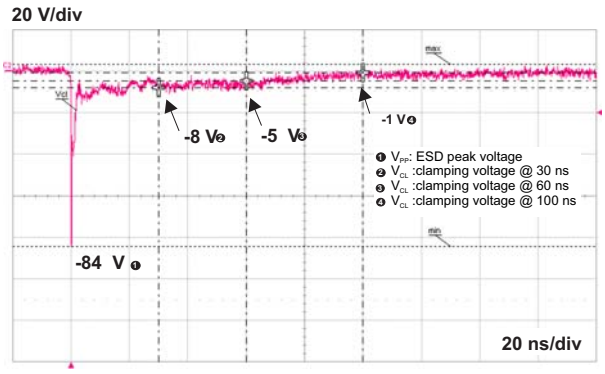


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)(1)



1. Test board connected to oscilloscope through 50 Ω cable and 20 dB + 6 dB attenuator. ESD generator return path connected to PCB ground plane.

Figure 8. Junction capacitance versus frequency (typical values)

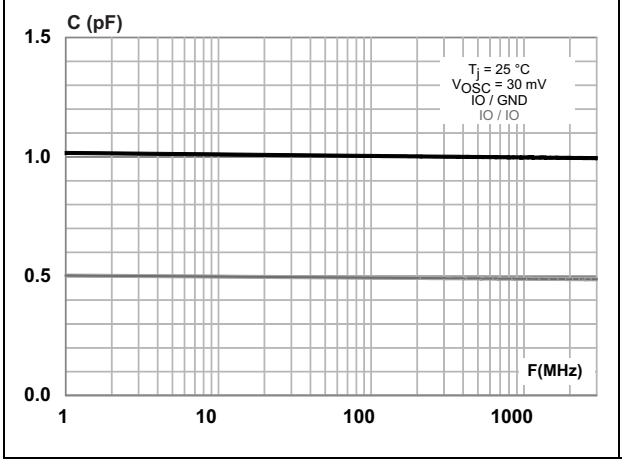


Figure 9. Analog crosstalk measurement

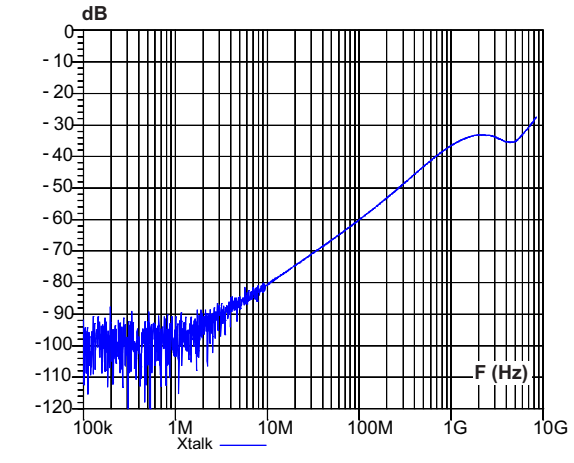


Figure 10. Peak pulse power versus initial junction temperature (maximum values)

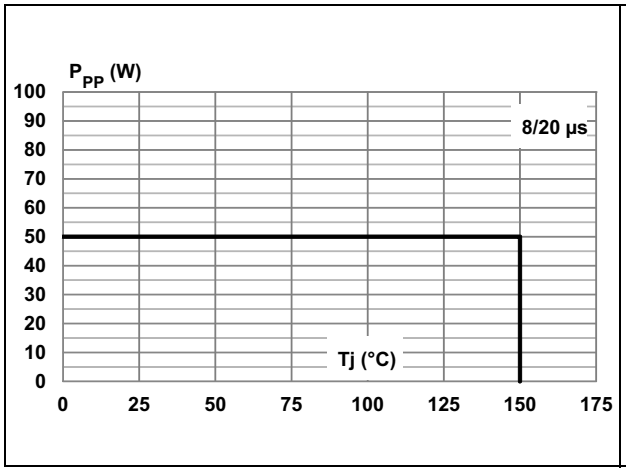


Figure 11. Peak pulse power versus exponential pulse duration (maximum values)

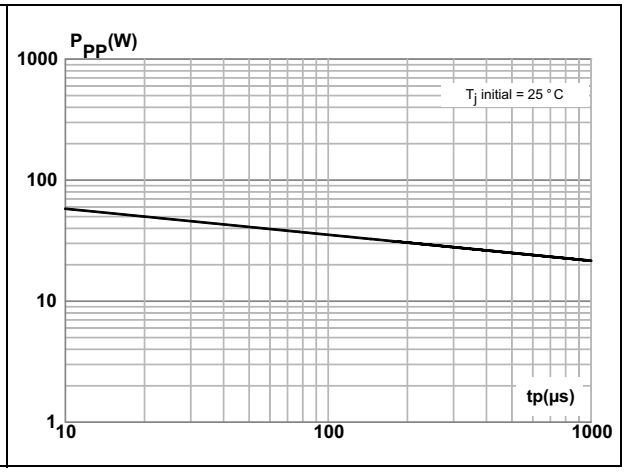


Figure 12. Clamping voltage versus peak pulse current (typical values)

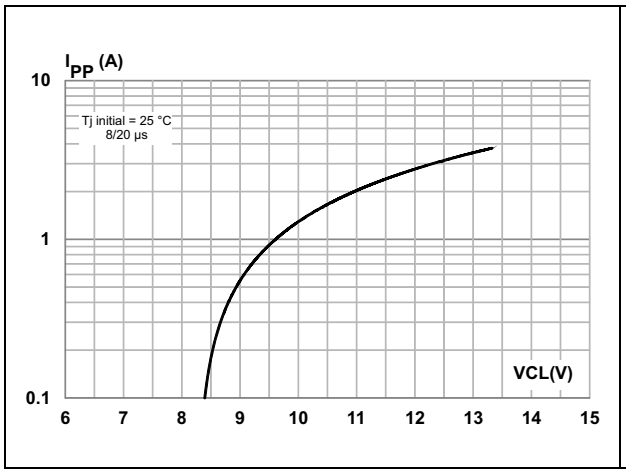


Figure 13. Leakage current versus junction temperature (typical values)

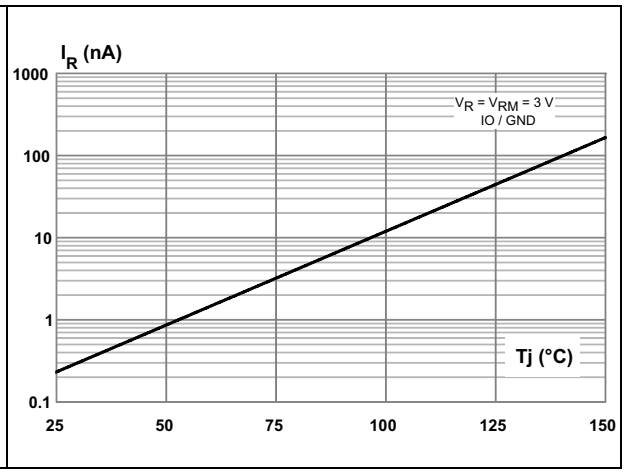


Figure 14. S21 (dB) attenuation measurement

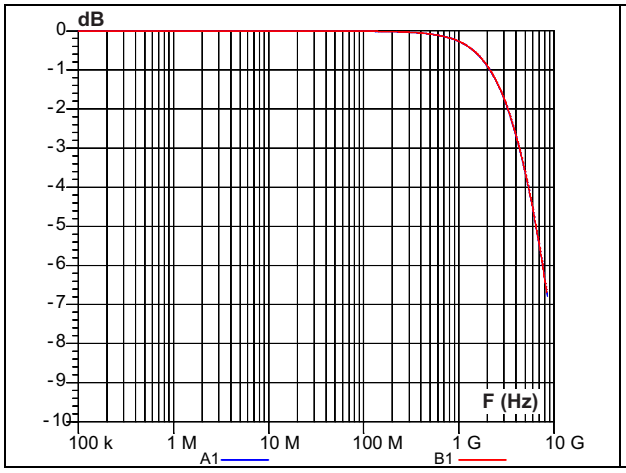
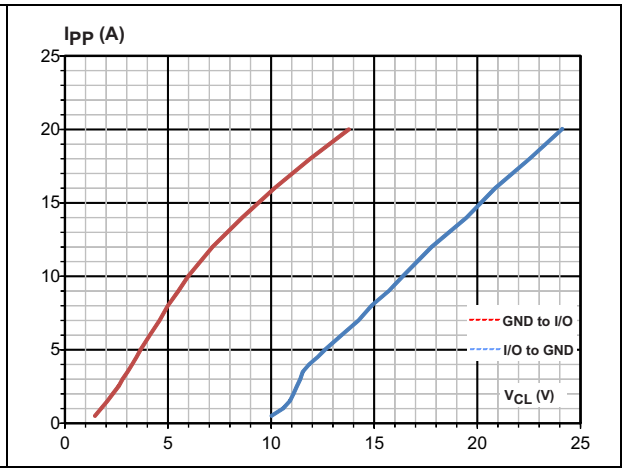
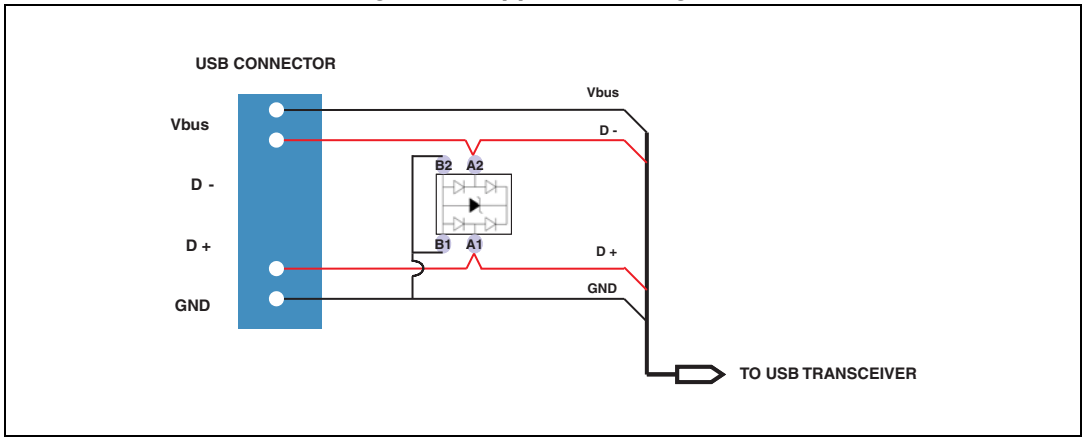


Figure 15. TLP measurement



2 Application information

Figure 16. Application diagram



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 17. Package dimensions

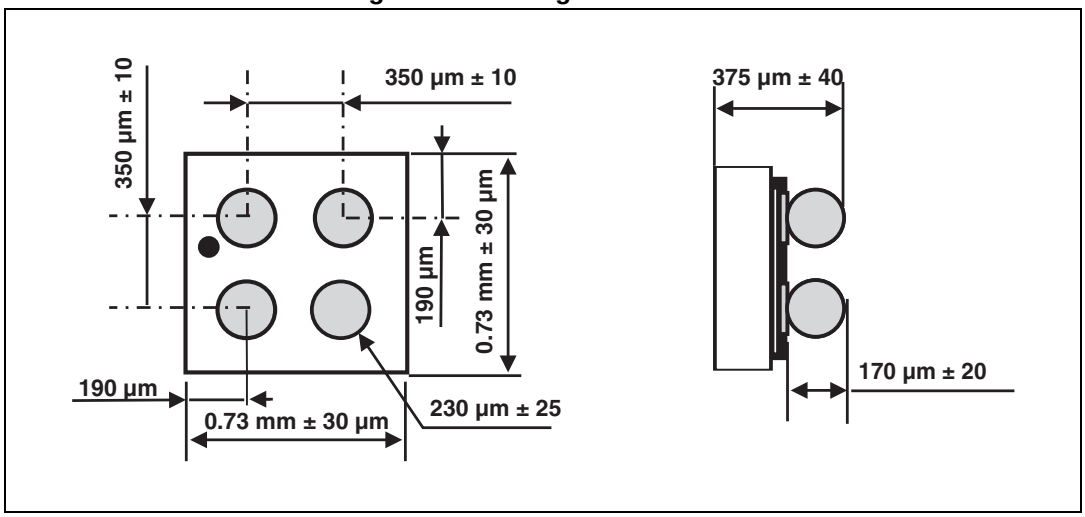


Figure 18. Footprint recommendations

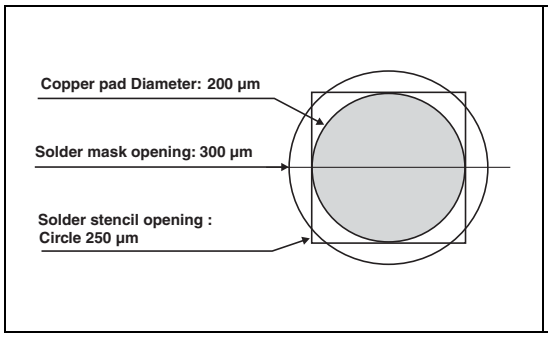


Figure 19. Marking

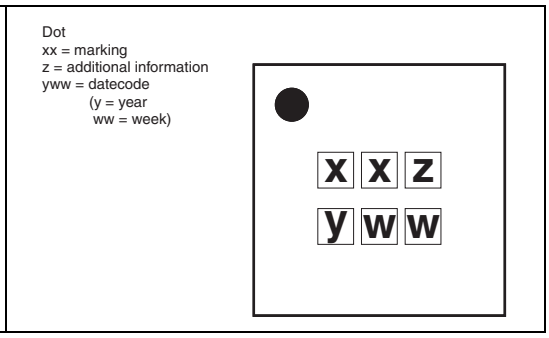
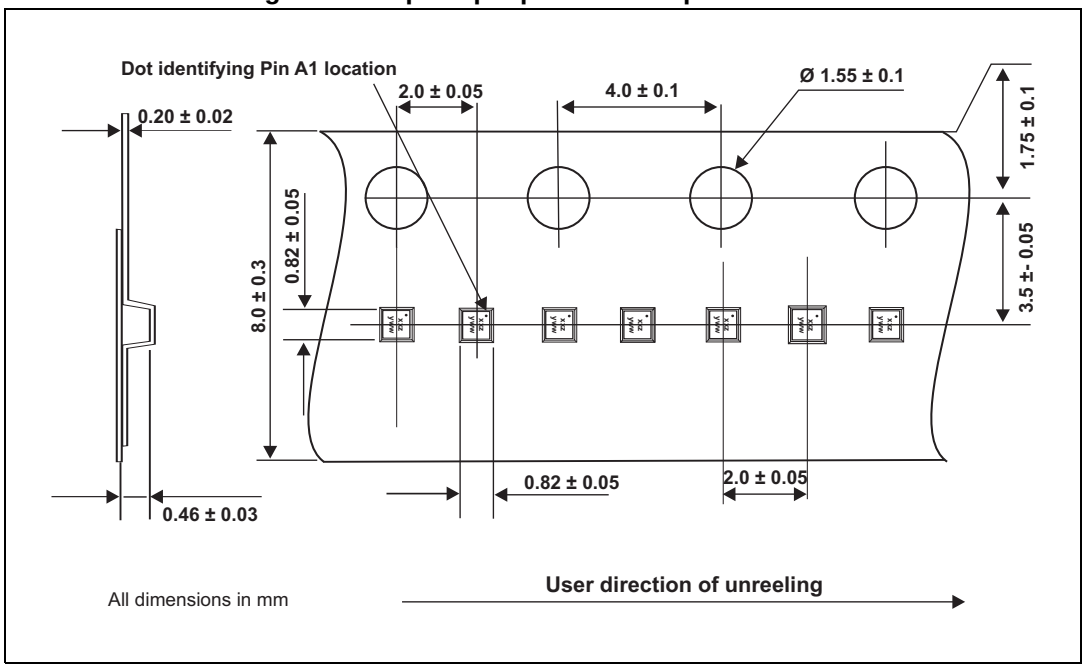


Figure 20. Flip-Chip tape and reel specifications



Note: More information is available in the STMicroelectronics Application notes:
AN4137: "350 µm Flip Chip: Package description and recommendations for use"
AN1826: "Transient protection solutions: Transil™ diode versus varistor"

4 Ordering information

Figure 21. Ordering information scheme

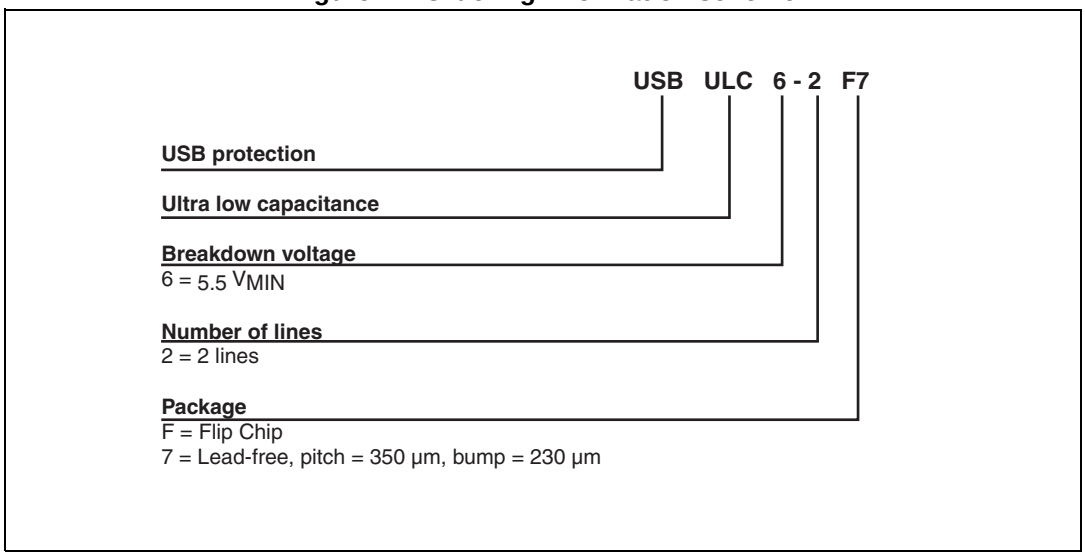


Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2F7	FA	Flip Chip	0.417 mg	14000	Tape and reel (7”)

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.

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