

## 6.5 mΩ, Bidirectional Battery Switch in Compact WCSP

### DESCRIPTION

The SiP32104 bidirectional switch feature reverse blocking capability to isolate the battery from the system. The internal switch has an ultra low 6.5 mΩ (typ. at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the devices ideal battery-disconnect switches for high capacity battery applications.

The SiP32104 has slew rate control, making it ideal in large load capacitor as well as high current load switching applications. The device is also highly efficient, consuming only 110 nA (typ.) current in shutdown and while operating.

The SiP32104 has an active low enable. It can interface directly with a low voltage control signal.

The SiP32104 is available in an ultra compact 12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

### FEATURES

- Bidirectional on and off
- 7 A continuous current capability
- Ultra-low  $R_{on}$ , 6.5 mΩ (typ.) at 3.3 V
- Wide input voltage, 2.3 V to 5.5 V
- Slew rate controlled turn on
- Low quiescent current: 110 nA
- Compact 12-bump, 1.3 mm x 1.7 mm x 0.55 mm WCSP package
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Smartphones and tablets
- Digital still / video cameras
- Portable meters and test instruments
- Communication devices with embedded batteries
- Portable medical and healthcare systems
- Data storage
- Battery bank

### TYPICAL APPLICATION CIRCUIT

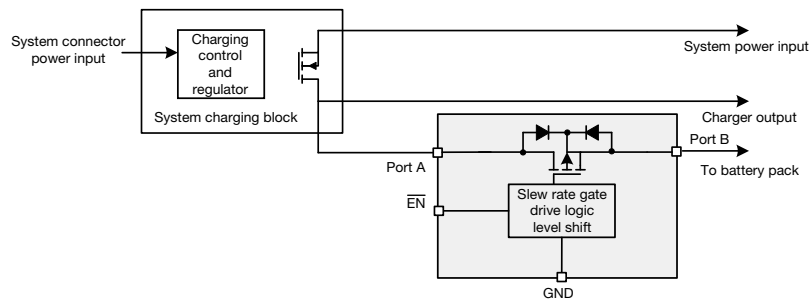


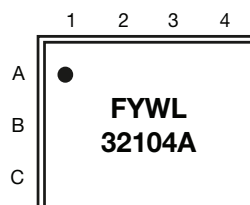
Fig. 1 - Typical Application Circuit

ORDERING INFORMATION					
PART NUMBER	MARKING	ENABLE	ENABLE PULL RESISTOR	PACKAGE	TEMPERATURE
SiP32104DB-T1-GE1	32104A	Low	No pull	12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package	-40 °C to +85 °C
SiP32104EVB	-	-	-	Evaluation board	-

#### Note

- GE1 denotes halogen-free and RoHS-compliant

### MARKING





ABSOLUTE MAXIMUM RATINGS			
PARAMETER	CONDITIONS	LIMIT	UNIT
$V_{PA}, V_{PB}$	Reference to GND	-0.3 to +6	V
	Pulse at 1 ms reference to GND <sup>a</sup>	-1.6	
$V_{EN}$	Reference to GND	-0.3 to +6	
Maximum continuous switch current		7	A
Maximum pulse current	100 $\mu$ s pulse	15	
ESD (HBM)		8000	V
Operating temperature		-40 to +85	°C
Operating junction temperature		125	
Storage temperature		-65 to +150	
Thermal resistance ( $\theta_{JA}$ ) <sup>b</sup>		73	°C/W
Power dissipation ( $P_D$ ) <sup>b, c</sup>	$T_A = 70$ °C	1096	mW

**Notes**

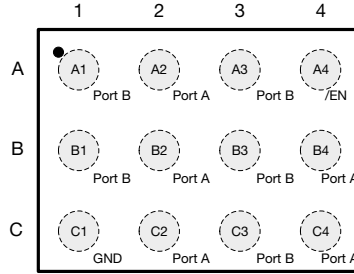
- a. Negative current injection up to 300 mA  
b. All bumps soldered to 1" x 1", 2 oz. copper, 4 layers PC board  
c. Derate 13.7 mW/°C above  $T_A = 70$  °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = V_{PA}/V_{PB} = 2.3$ V to 5.5 V, $T_A = -40$ °C to +85 °C (Typical values are at $V_{PA}, V_{PB} = 4.2$ V, $C_{PA}, C_{PB} = 0.1$ $\mu$ F, $T_A = 25$ °C)	LIMITS			UNIT
			MIN. <sup>a</sup>	TYP. <sup>b</sup>	MAX. <sup>a</sup>	
<b>Power Supply</b>						
Operating voltage <sup>c</sup>	$V_{PA/PB}$		2.3	-	5.5	V
Quiescent current	$I_Q$	$V_{EN} = 0$ V, no load	-	110	400	nA
Shutdown current	$I_{SHDN}$	$V_{EN} = V_{IN}$ , no load	-	110	400	nA
<b>Internal FET</b>						
On-resistance	$R_{DS(on)}$	$V_{PA}/V_{PB} = 2.3$ V, $I_L = 500$ mA, $T_A = 25$ °C	-	8	13	m $\Omega$
		$V_{PA}/V_{PB} = 3.3$ V, $I_L = 500$ mA, $T_A = 25$ °C	-	6.5	10	
<b>Control</b>						
$\overline{EN}$ Input logic-low voltage <sup>c</sup>	$V_{IL}$		-	-	0.4	V
$\overline{EN}$ Input logic-high voltage <sup>c</sup>	$V_{IH}$		1.4	-	-	
$\overline{EN}$ Input logic hysteresis	$V_{I(HYS)}$		-	> 200	-	mV
<b>Timing</b>						
Output turn-on delay time	$t_{d(on)}$	$V_{IN} = 4.2$ V, $R_L = 100$ $\Omega$ , $C_L = 0.1$ $\mu$ F, $T_A = 25$ °C	-	0.8	-	ms
Output turn-on rise time	$t_r$		-	1	-	
Output turn-off delay time	$t_{d(off)}$		-	0.12	-	
Output turn-off fall time	$t_f$		-	0.1	-	

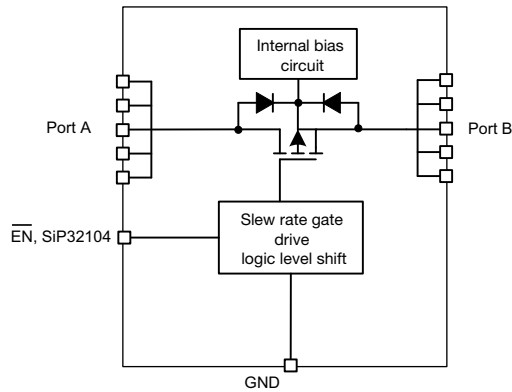
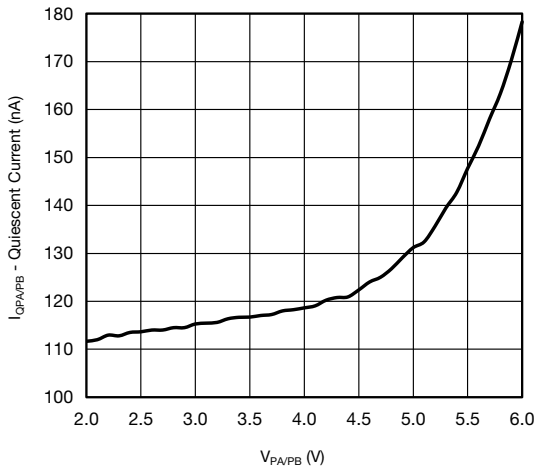
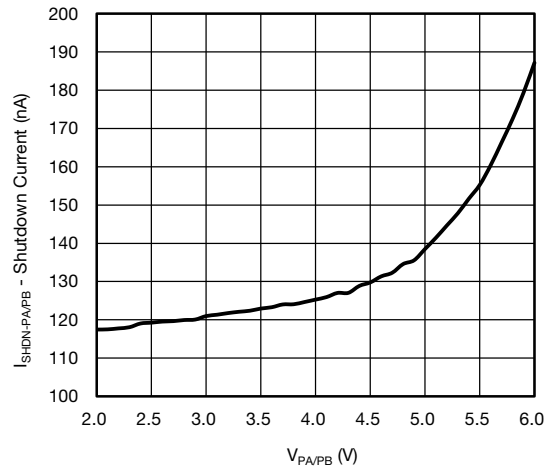
**Notes**

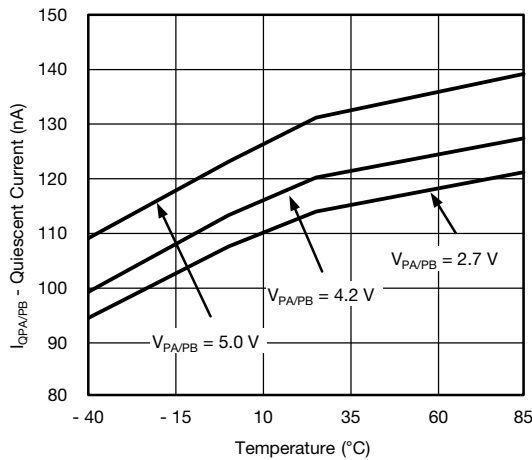
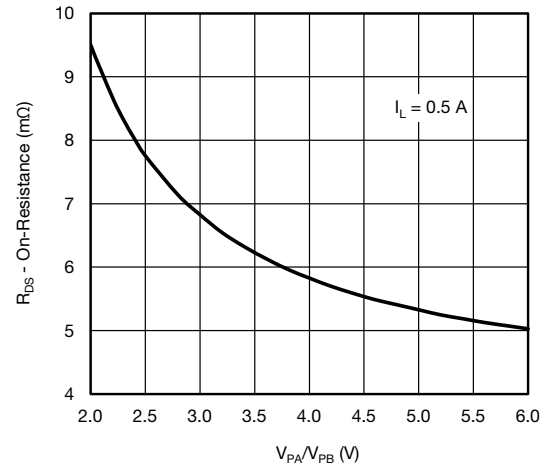
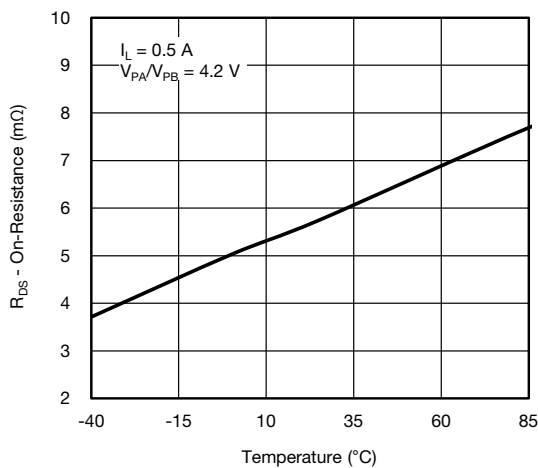
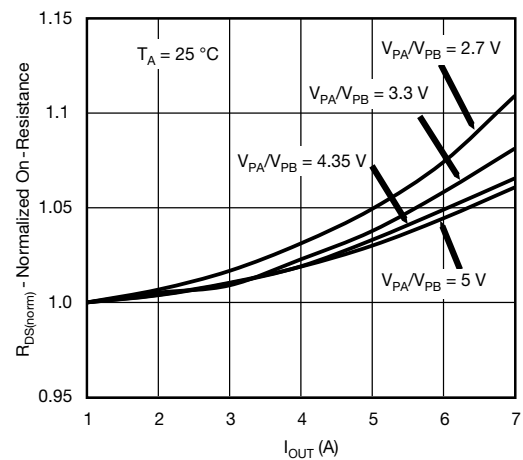
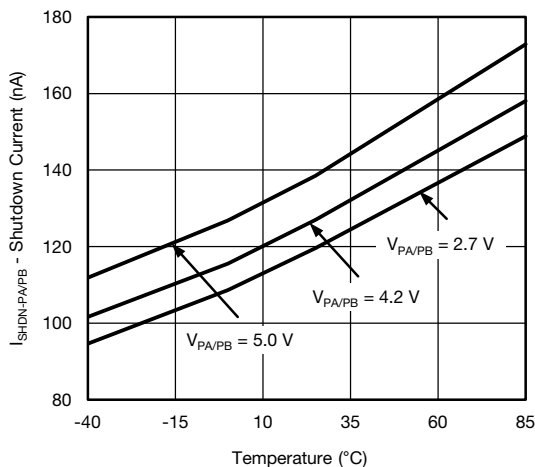
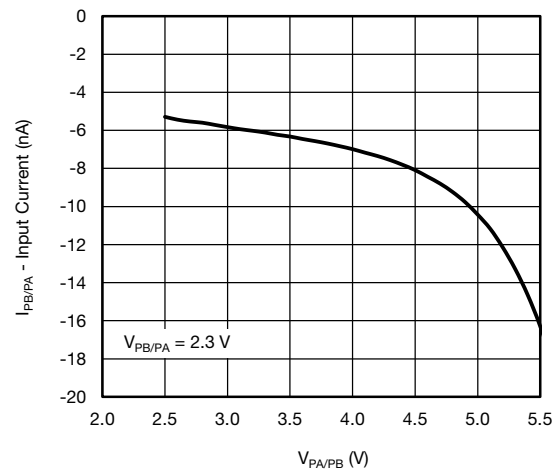
- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum  
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing  
c. For  $V_{IN}$  outside this range consult typical  $\overline{EN}$ , EN threshold curve

**BUMP CONFIGURATION**

 Top view  
(solder bumps on bottom)

**Fig. 2 - WCSP12, 1.3 mm x 1.7 mm**

BUMP DESCRIPTION		
BUMP NUMBER	NAME	FUNCTION
A1, B1, A3, B3, C3	PB	Power port B
C1	GND	Ground
A2, B2, C2, B4, C4	PA	Power port A
A4	$\overline{\text{EN}}$	Switch enable input, active low

**FUNCTIONAL BLOCK DIAGRAM**

**TYPICAL CHARACTERISTICS** (internally regulated 25 °C, unless otherwise noted)

**Fig. 3 - Quiescent vs. Input Voltage**

**Fig. 4 - Shutdown Current vs. Input Voltage**

**TYPICAL CHARACTERISTICS** (internally regulated 25 °C, unless otherwise noted)

**Fig. 5 - Quiescent vs. Temperature**

**Fig. 8 - On Resistance vs. Input Voltage**

**Fig. 6 - On Resistance vs. Temperature**

**Fig. 9 - Normalized On Resistance vs. Load Current**

**Fig. 7 - Shutdown Current vs. Temperature**

**Fig. 10 - Reverse Blocking Current ( $I_{RB}$ ) vs. Output Voltage**

**TYPICAL CHARACTERISTICS** (internally regulated 25 °C, unless otherwise noted)

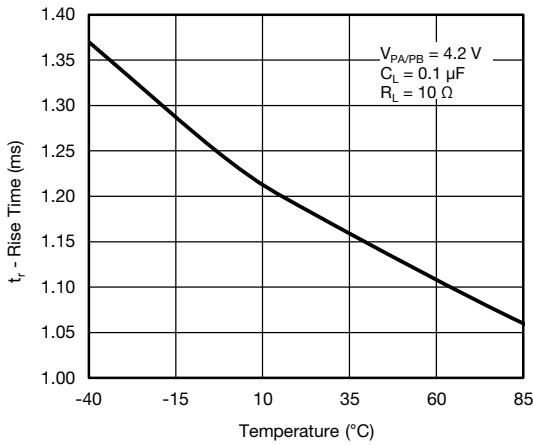


Fig. 11 - Rise Time vs. Temperature

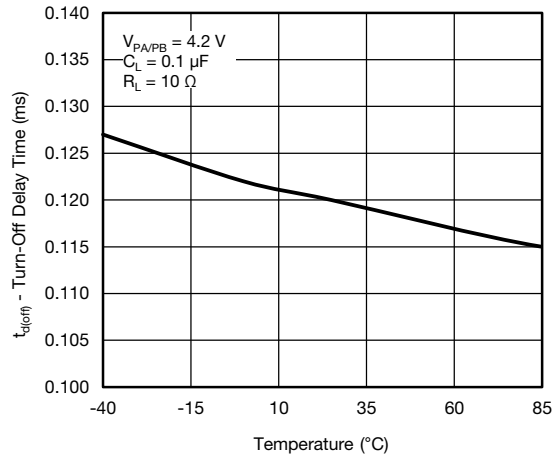


Fig. 14 - Turn-off Delay Time vs. Temperature

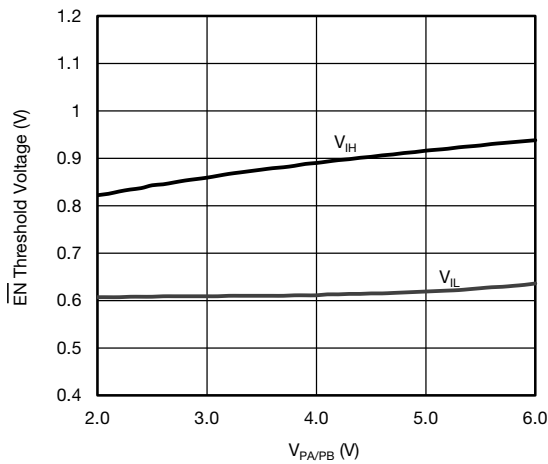


Fig. 12 - EN Threshold Voltage vs. Input Voltage

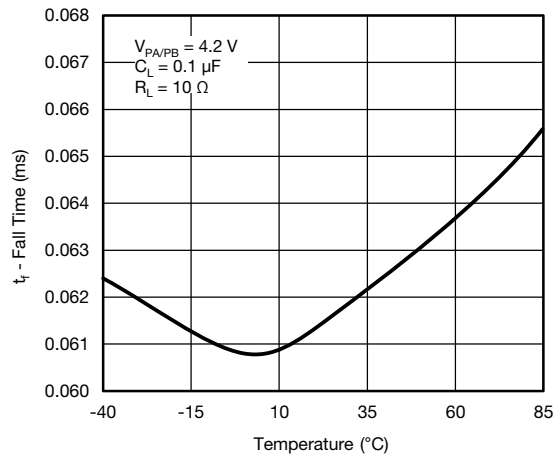


Fig. 15 - Fall Time vs. Temperature

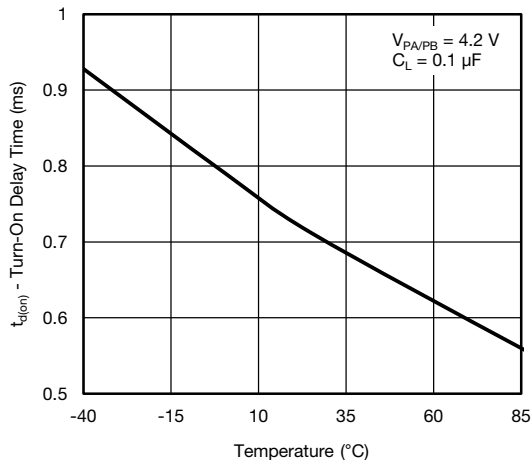


Fig. 13 - Turn-on Delay Time vs. Temperature

**DETAILED DESCRIPTION**

The SiP32104 bidirectional switch features reverse blocking capability to isolate the battery from the system. The internal switch has an ultra low 6.5 mΩ (typ. at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the device ideal battery-disconnect switch for high capacity battery applications. The parts can handle 7 A continuous current at both directions.

The SiP32104 has slew rate control, making it ideal in large load capacitor as well as high current load switching applications.

The SiP32104 is available in an ultra compact 12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

**REVERSE CURRENT BLOCKING**

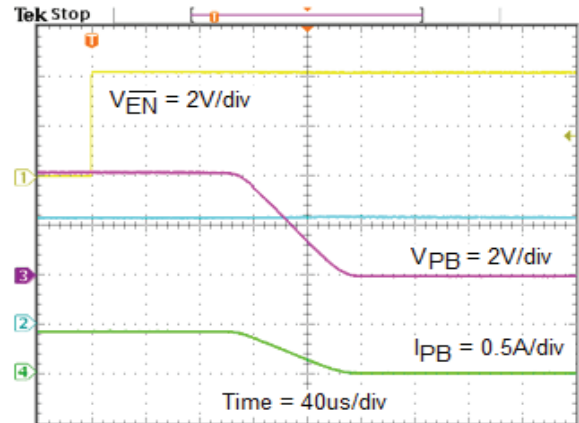
The SiP32104 is a bidirectional switch that prevent current flowing from either port to the other when the device is disabled.

**$\overline{EN}$  INPUT**

SiP32104 has an active-low enable pin which can interface with low voltage GPIO directly. The switch is on when EN is low and off when EN is high. The SiP32104  $\overline{EN}$  pin has no pull up or pull down resistor.

**SWITCH ON AND OFF PERFORMANCE**

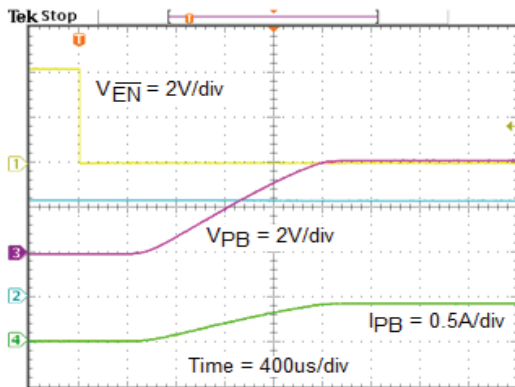
The SiP32104 has a slew rate control. This minimizes the inrush current and provides a soft turn on.



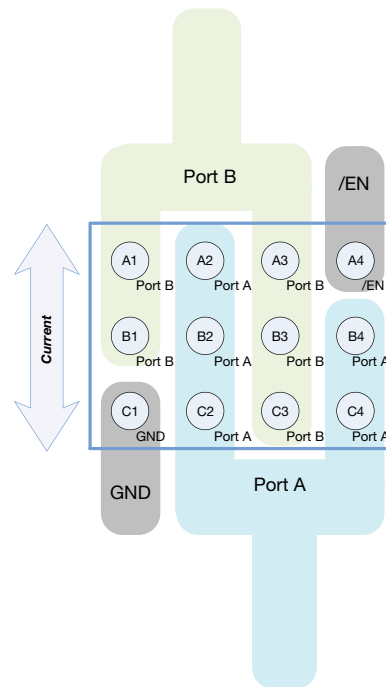
**Fig. 17 - Port B Turn-Off Time**  
( $V_{PA} = 4.2\text{ V}$ ,  $R_L = 10\ \Omega$ ,  $C_L = 0.1\ \mu\text{F}$ )

**DEVICE PIN OUT**

Device pin out is designed for ease of layout.



**Fig. 16 - Port B Turn-On Time**  
( $V_{PA} = 4.2\text{ V}$ ,  $R_L = 10\ \Omega$ ,  $C_L = 0.1\ \mu\text{F}$ )

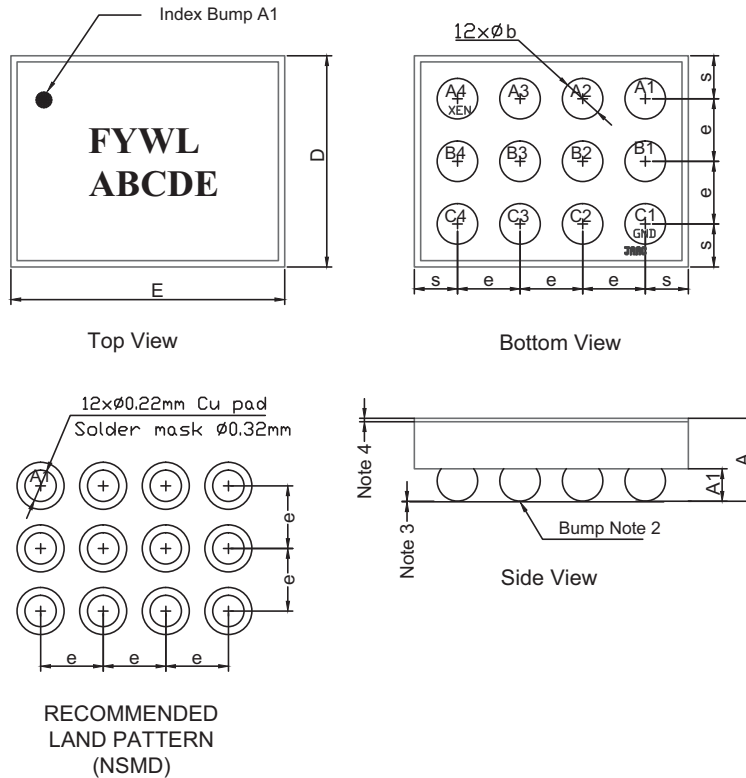


**Fig. 18 - Proposed Layout**

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## WCSP12: 12 Bumps

(3 x 4, 0.4 mm pitch, 208 μm bump height, 1.71 mm x 1.31 mm die size)



DIMENSION	MILLIMETERS <sup>(5)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0203	0.0209	0.0215
A1	0.183	0.208	0.233	0.0072	0.0082	0.0092
b	0.234	0.260	0.312	0.0092	0.0102	0.0123
e	0.400			0.0157		
s	0.235	0.255	0.275	0.0093	0.0100	0.0108
D	1.270	1.310	1.350	0.0500	0.0516	0.0531
E	1.670	1.710	1.750	0.0657	0.0673	0.0689

**Notes** (unless otherwise specified)

- (1) Laser mark on the silicon die back coated with an epoxy film.
- (2) Bumps are SAC396.
- (3) 0.050 max. co-planarity.
- (4) Laminate tape thickness is 0.022 mm.
- (5) Use millimeters as the primary measurement.

ECN: S13-2510-Rev. B, 16-Dec-13  
 DWG: 6017



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