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Kind regards,

Team Nexperia

# PDTA113Z series

PNP resistor-equipped transistors; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

Rev. 04 — 2 September 2009

**Product data sheet** 

### 1. Product profile

### 1.1 General description

PNP resistor-equipped transistors.

Table 1. Product overview

Type number	Package	Package		
	NXP	JEITA		
PDTA113ZE	SOT416	SC-75	PDTC113ZE	
PDTA113ZK	SOT346	SC-59	PDTC113ZK	
PDTA113ZM	SOT883	SC-101	PDTC113ZM	
PDTA113ZS[1]	SOT54 (TO-92)	SC-43A	PDTC113ZS	
PDTA113ZT	SOT23	-	PDTC113ZT	
PDTA113ZU	SOT323	SC-70	PDTC113ZU	

<sup>[1]</sup> Also available in SOT54A and SOT54 variant packages (see Section 2).

### 1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

### 1.3 Applications

- General purpose switching and amplification
- Inverter and interface circuits

#### Circuit drivers

#### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CEO}$	collector-emitter voltage	open base	-	-	-50	V
I <sub>O</sub>	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		0.7	1	1.3	$k\Omega$
R2/R1	bias resistor ratio		8	10	12	



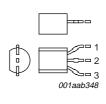
# 2. Pinning information

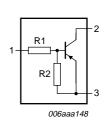
Table 3. Pinning

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)		
2	output (collector)		R1 2
3	GND (emitter)	001aab347	1 R2 3

#### SOT54A

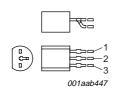
1	input (base)
2	output (collector)
3	GND (emitter)

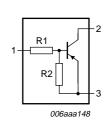




### **SOT54** variant

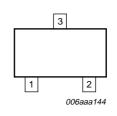
1	input (base)
2	output (collector)
3	GND (emitter)

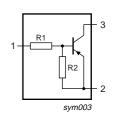




### SOT23, SOT323, SOT346, SOT416

1	input (base)
2	GND (emitter)
3	output (collector)

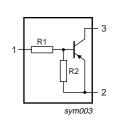




### **SOT883**

1	input (base)
2	GND (emitter)
3	output (collector)





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### 3. Ordering information

Table 4. Ordering information

Type number	Package				
	Name	Description	Version		
PDTA113ZE	SC-75	plastic surface mounted package; 3 leads	SOT416		
PDTA113ZK	SC-59	plastic surface mounted package; 3 leads	SOT346		
PDTA113ZM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 $\times$ 0.6 $\times$ 0.5 mm	SOT883		
PDTA113ZS[1]	SC-43A	plastic-single-ended leaded (through hole) package; 3 leads	SOT54		
PDTA113ZT	-	plastic surface mounted package; 3 leads	SOT23		
PDTA113ZU	SC-70	plastic surface mounted package; 3 leads	SOT323		

<sup>[1]</sup> Also available in SOT54A and SOT54 variant packages (see Section 2 and Section 9)

### 4. Marking

Table 5. Marking codes

indicate in the second	
Type number	Marking code <sup>[1]</sup>
PDTA113ZE	15
PDTA113ZK	27
PDTA113ZM	G3
PDTA113ZS	TA113Z
PDTA113ZT	*AM
PDTA113ZU	*16

<sup>[1] \* = -:</sup> made in Hong Kong

<sup>\* =</sup> p: made in Hong Kong

<sup>\* =</sup> t: made in Malaysia

<sup>\* =</sup> W: made in China

### 5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter	-	-50	V
$V_{CEO}$	collector-emitter voltage	open base	-	-50	V
$V_{EBO}$	emitter-base voltage	open collector	-	-5	V
$V_{I}$	input voltage				
	positive		-	+5	V
	negative		-	-10	V
Io	output current (DC)		-	-100	mA
I <sub>CM</sub>	peak collector current		-	-100	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$			
	SOT416		<u>[1]</u> -	150	mW
	SOT346		<u>[1]</u> -	250	mW
	SOT883		[2][3]	250	mW
	SOT54		<u>[1]</u> -	500	mW
	SOT23		<u>[1]</u> _	250	mW
	SOT323		<u>[1]</u> -	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C

<sup>[1]</sup> Refer to standard mounting conditions.

### 6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	SOT416		<u>[1]</u> _	-	833	K/W
	SOT346		<u>[1]</u> _	-	500	K/W
	SOT883		[2][3]	-	500	K/W
	SOT54		<u>[1]</u> -	-	250	K/W
	SOT23		<u>[1]</u> -	-	500	K/W
	SOT323		<u>[1]</u> -	-	625	K/W

<sup>[1]</sup> Refer to standard mounting conditions.

<sup>[2]</sup> Reflow soldering is the only recommended soldering method.

<sup>[3]</sup> Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 µm copper strip line.

<sup>[2]</sup> Reflow soldering is the only recommended soldering method.

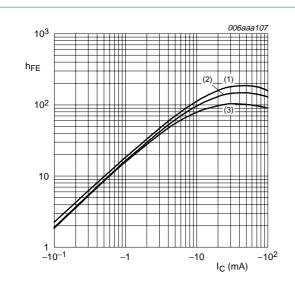
<sup>[3]</sup> Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 µm copper strip line.

### 7. Characteristics

Table 8. Characteristics

T<sub>amb</sub> = 25 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Unit
		141111	·yρ		
collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA
collector-emitter	$V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$	-	-	-1	μΑ
cut-off current	$V_{CE} = -30 \text{ V}; I_{B} = 0 \text{ A};$ $T_{j} = 150 ^{\circ}\text{C}$	-	-	<b>-50</b>	μΑ
emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$	-	-	-800	μΑ
DC current gain	$V_{CE} = -5 \text{ V}; I_{C} = -5 \text{ mA}$	35	-	-	
collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$	-	-	-150	mV
off-state input voltage	$V_{CE} = -5 \text{ V}; I_{C} = -100 \mu\text{A}$	-	-0.65	-0.3	V
on-state input voltage	$V_{CE} = -300 \text{ mV}; I_C = -20 \text{ mA}$	-2.5	-0.95	-	V
bias resistor 1 (input)		0.7	1	1.3	kΩ
bias resistor ratio		8	10	12	
collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	-	-	2	pF
	collector-emitter cut-off current  emitter-base cut-off current  DC current gain collector-emitter saturation voltage off-state input voltage on-state input voltage bias resistor 1 (input) bias resistor ratio	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{c} \text{collector-base cut-off} \\ \text{current} \\ \end{array} \begin{array}{c} V_{CB} = -50 \text{ V}; \text{ I}_{E} = 0 \text{ A} \\ \text{collector-emitter} \\ \text{cut-off current} \\ \end{array} \begin{array}{c} V_{CE} = -30 \text{ V}; \text{ I}_{B} = 0 \text{ A} \\ \hline V_{CE} = -30 \text{ V}; \text{ I}_{B} = 0 \text{ A}; \\ \hline V_{CE} = -30 \text{ V}; \text{ I}_{C} = 0 \text{ A} \\ \hline \end{array} \begin{array}{c} - \\ \hline \end{array} \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \end{array} \\ \begin{array}{c} - \\ \hline \end{array} \\ \begin{array}{c} - \\ \end{array} \\ \begin{array}{c} -$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$



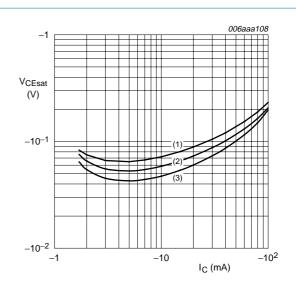
$$V_{CE} = -5 \text{ V}$$

(1) 
$$T_{amb} = 100 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3)  $T_{amb} = -40 \, ^{\circ}C$ 

Fig 1. DC current gain as a function of collector current; typical values



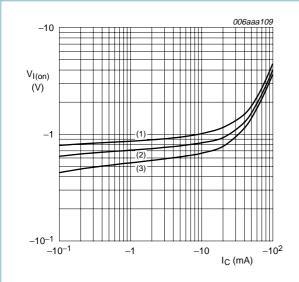
$$I_{\rm C}/I_{\rm B} = 20$$

(1) 
$$T_{amb} = 100 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3) 
$$T_{amb} = -40 \, ^{\circ}C$$

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values



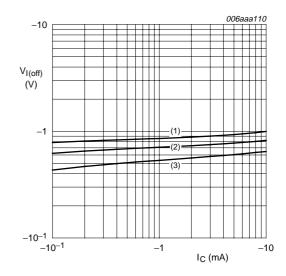
$$V_{CE} = -0.3 \text{ V}$$

(1) 
$$T_{amb} = -40 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig 3. On-state input voltage as a function of collector current; typical values



$$V_{CE} = -5 \text{ V}$$

(1) 
$$T_{amb} = -40 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig 4. Off-state input voltage as a function of collector current; typical values

### 8. Package outline

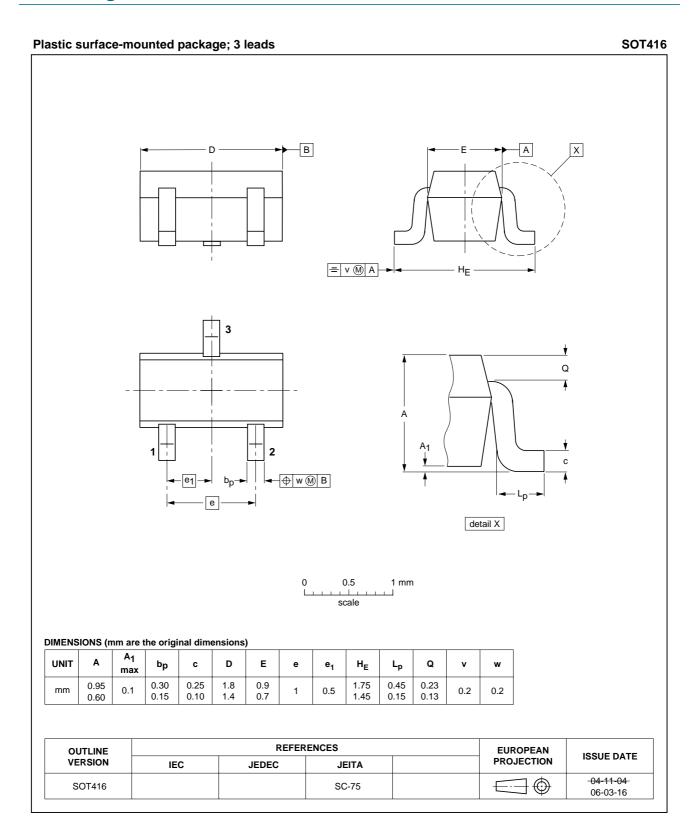


Fig 5. Package outline SOT416 (SC-75)

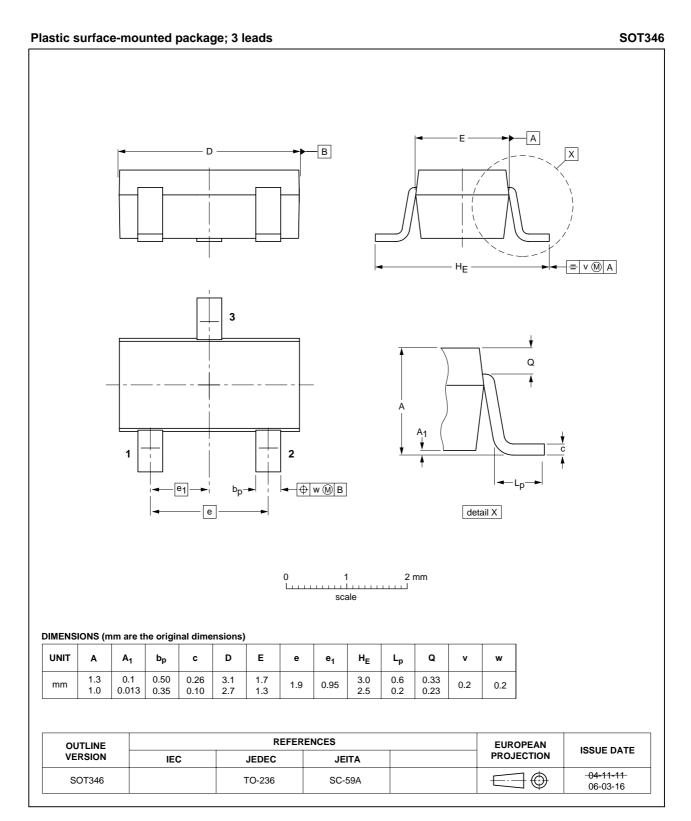


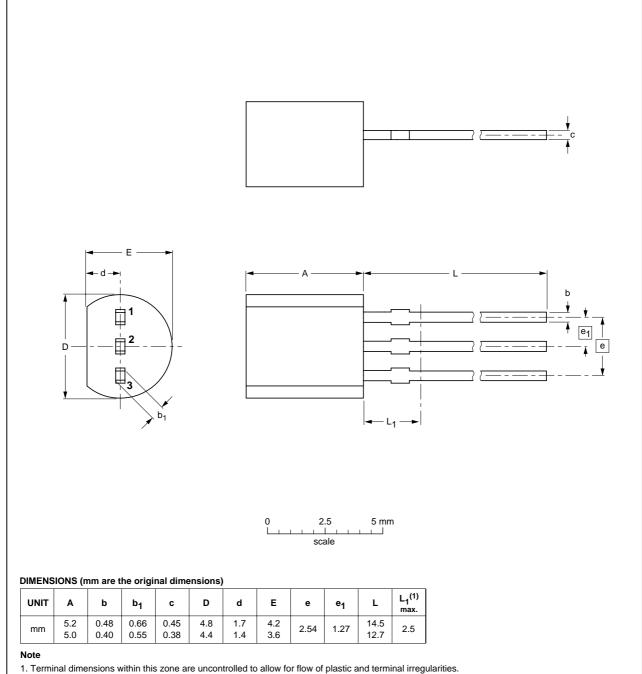
Fig 6. Package outline SOT346 (SC-59/TO-236)

### Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm **SOT883** e<sub>1</sub> 0.5 | 1 mm **DIMENSIONS (mm are the original dimensions)** A<sub>1</sub> max. A<sup>(1)</sup> UNIT b $b_1$ D Ε e<sub>1</sub> L $L_{1}$ 0.30 0.55 0.30 0.50 0.20 0.62 1.02 mm 0.03 0.35 0.46 0.12 0.47 0.55 0.95 0.22 0.22 1. Including plating thickness REFERENCES OUTLINE **EUROPEAN** ISSUE DATE VERSION **PROJECTION JEDEC** 03-02-05 $\bigcirc$ SOT883 SC-101 03-04-03

Fig 7. Package outline SOT883 (SC-101)

### Plastic single-ended leaded (through hole) package; 3 leads

SOT54



	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT54		TO-92	SC-43A		$\qquad \qquad \bigoplus$	<del>-04-06-28-</del> 04-11-16

Fig 8. Package outline SOT54 (SC-43A/TO-92)

### Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)

SOT54A

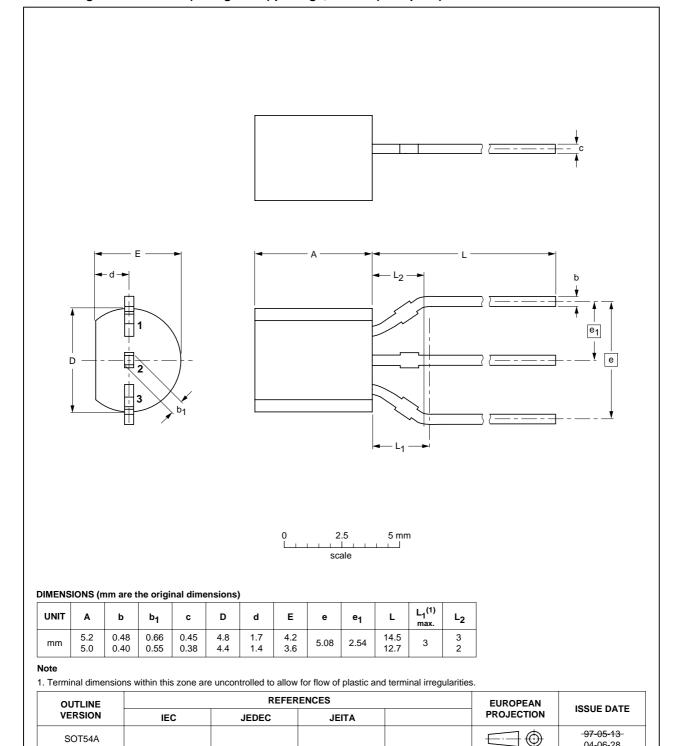


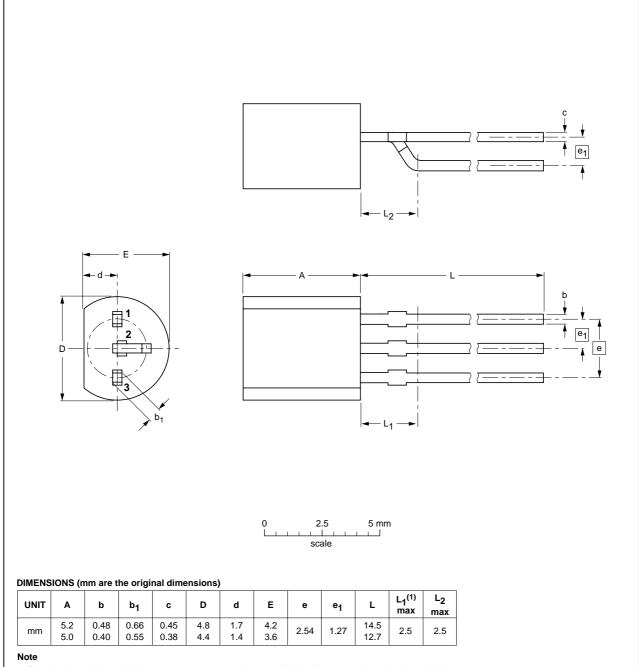
Fig 9. Package outline SOT54A

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04-06-28

### Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT54 variant						<del>-04-06-28</del> 05-01-10

Fig 10. Package outline SOT54 variant

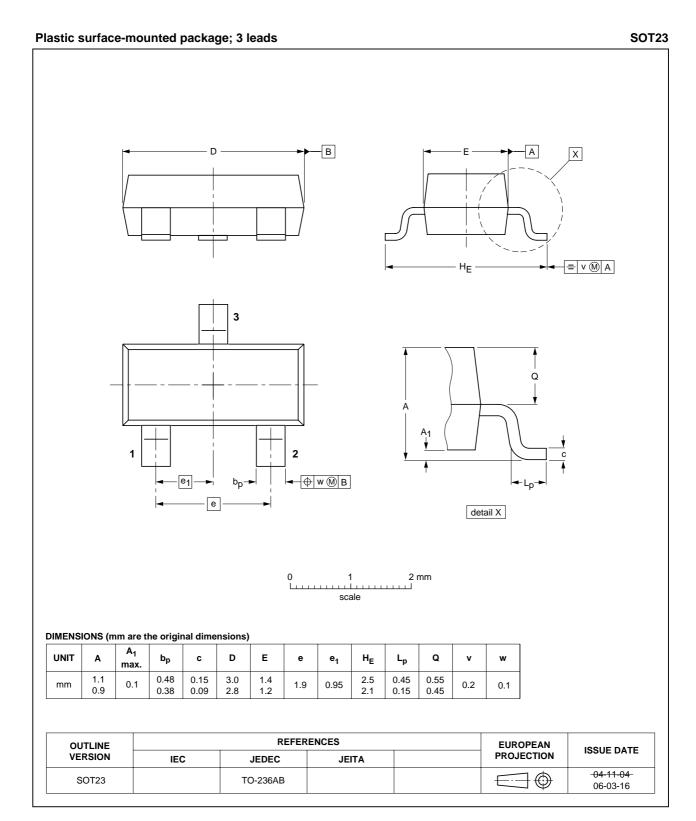


Fig 11. Package outline SOT23 (TO-236AB)

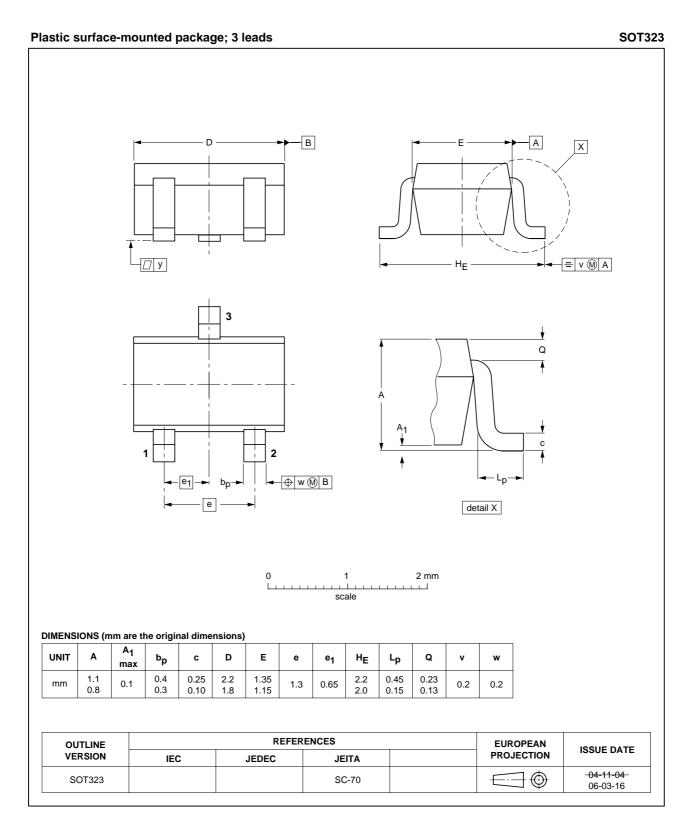


Fig 12. Package outline SOT323 (SC-70)

### 9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA113ZE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113ZK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113ZM	SOT883	2 mm pitch, 8 mm tape and reel	•	-	-315
PDTA113ZS	SOT54	bulk, straight leads	•	-412	-
	SOT54A	tape and reel, wide pitch	•	-	-116
	SOT54A	tape ammopack, wide patch	•	-	-126
	SOT54 variant	bulk, delta pinning	•	-112	-
PDTA113ZT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA113ZU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

<sup>[1]</sup> For further information and the availability of packing methods, see Section 12.

# 10. Revision history

### Table 10. Revision history

	•						
Document ID	Release date	Data sheet status	Change notice	Supersedes			
PDTA113Z_SER_4	20090902	Product data sheet	-	PDTA113Z_SER_3			
Modifications:	<ul> <li>This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li> </ul>						
	<ul> <li>Figure 5 "Package outline SOT416 (SC-75)": updated</li> </ul>						
	<ul> <li>Figure 6 "Package outline SOT346 (SC-59/TO-236)": updated</li> </ul>						
	<ul> <li>Figure 11 "Package outline SOT23 (TO-236AB)". updated</li> </ul>						
	<ul> <li><u>Figure 12 "Package outline SOT323 (SC-70)"</u>: updated</li> </ul>						
PDTA113Z_SER_3	20050407	Product data sheet	-	PDTA113ZT_2			
PDTA113ZT_2	20040518	Objective data sheet	-	PDTA113ZT_1			
PDTA113ZT_1	20040325	Objective data sheet	-	-			

### 11. Legal information

#### 11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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### 12. Contact information

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For sales office addresses, please send an email to: salesaddresses@nxp.com

# PDTA113Z series

PNP resistor-equipped transistors; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

### 13. Contents

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

