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## Trusted Platform Module LPC Interface

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### SUMMARY DATASHEET

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#### Features

- Fully compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) version 1.2 specification
- Compliant with TCG PC client-specific TPM Interface Specification (TIS) version 1.2
- Single-chip, turnkey solution
- Hardware asymmetric crypto engine
- Atmel® AVR® RISC microprocessor
- Internal EEPROM storage for RSA keys
- 33MHz Low Pin Count (LPC) bus for easy PC interface
- Secure hardware and firmware design and chip layout
- Internal, high-quality Random Number Generator (RNG) – FIPS 140-2 compliant
- NV storage space for 1756 bytes of user defined data
- 3.3V supply voltage
- 28-lead thin TSSOP, 28-lead wide TSSOP, or 40-pad QFN packages
- Offered in both commercial (0 to 70°C) and industrial (-40 to +85°C) temperature ranges

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#### Description

The Atmel AT97SC3204 is a fully integrated security module designed to be integrated into personal computers and other embedded systems. It implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

The chip communicates with the PC through the LPC interface. The TPM supports SIRQ (for interrupts) and CLKRUN to permit clock stopping for power savings in mobile computers.

**This is a summary document.  
The complete document is  
available under NDA. For more  
information, please contact  
your local Atmel sales office.**

# 1. Pin Configurations and Pinouts

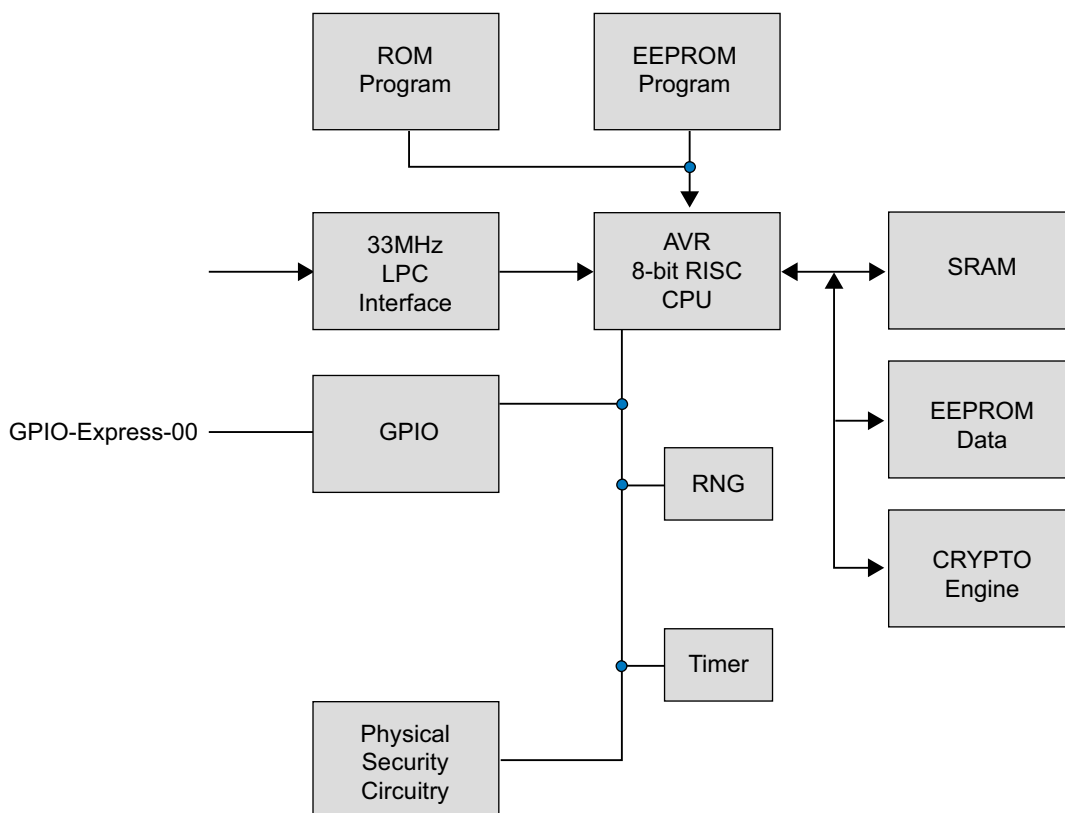
**Table 1-1. Pin Configurations**

Pin name	Function
V <sub>CC</sub>	3.3V Supply Voltage
SB3V	Standby 3.3V Supply Voltage
GND	Ground
LRESET#	PCI Reset Input Active Low
LAD0	LPC Command, Address, Data Line Input/Output
LAD1	LPC Command, Address, Data Line Input/Output
LAD2	LPC Command, Address, Data Line Input/Output
LAD3	LPC Command, Address, Data Line Input/Output
LCLK	33MHz PCI Clock Input
LFRAME#	LPC FRAME Input
CLKRUN#	PCI Clock Run Input/Output
LPCPD#	LPC Power-Down Input
SERIRQ	Serialized Interrupt Request Input/Output
GPIO-Express-00	GPIO assigned to TPM_NV_INDEX_GPIO_00
TestI	Test Input (Disabled)
TestBI	Test Input (Disabled)
ATest	Atmel Test Pin
NC	No Connect
NBO	Not Bounded Out

**Table 1-2. Pinouts**



## 2. Block Diagram



The TPM includes a hardware random number generator, including a FIPS-approved Pseudo Random Number Generator that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

The chip uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM\_FlushSpecific, TPM\_Loadkey2), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM and ODM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary device driver software for integration into certain operating systems, along with BIOS drivers. Atmel will also provide manufacturing support software for use by OEMs and ODMs during initialization and verification of the TPM during board assembly.

Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 to 3, on the TCG Web site located at <https://www.trustedcomputinggroup.org>. TPM features specific to PC Client platforms are specified in the “TCG PC Client Specific TPM Interface Specification, Version 1.2”, also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the “TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2”, also available on the TCG website.

### 3. Ordering Information

Atmel Ordering Code	Package		Operating Range
AT97SC3204 <sup>(1)</sup>	28X1 (28-pin thin TSSOP)	Lead-free, RoHS	Commercial (0°C to 70°C)
AT97SC3204 <sup>(1)</sup>	40ML1 (40-pin QFN)		Industrial (-40°C to 85°C)

Note: 1. Please see the AT97SC3204 datasheet addendum for the complete catalog number ordering code.

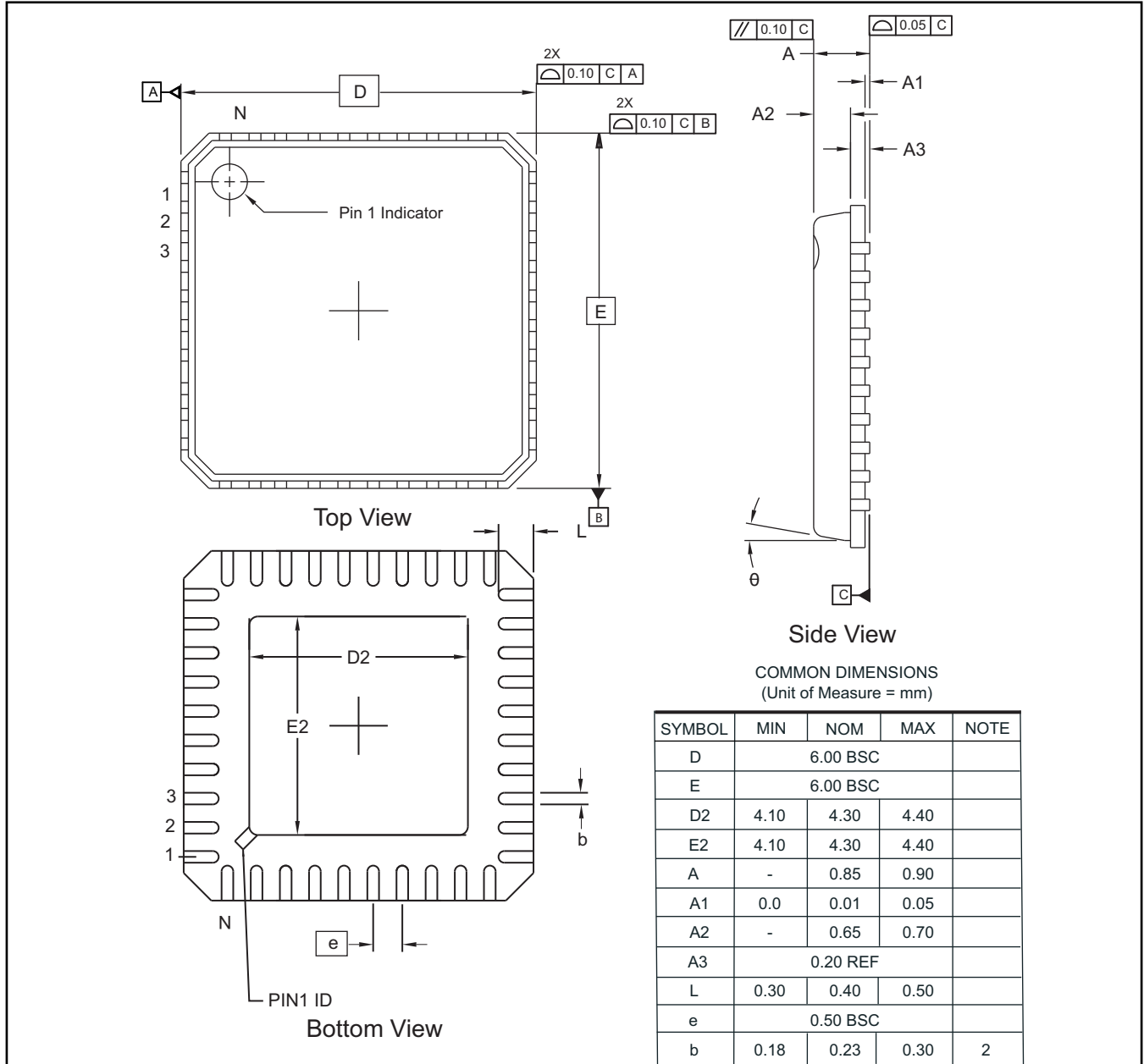
Package Type	
<b>28X1</b>	28-lead, 4.4mm body width, Plastic Thin Shrink Small Outline (thin TSSOP)
<b>40ML1</b>	40-pad 6.0 x 6.0x0.9mm body, 0.50mm pitch, Very-thin Quad Flat No Lead (VQFN)

## 4. Package Drawings

### 4.1 28X1 — 28-lead Thin TSSOP



## 4.2 40ML1 — 40-pad VQFN



- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation WJJD-2, for proper dimensions, tolerances, datums, etc.
  2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

09/23/11

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**

40ML1, 40-pad 6.0 x 6.0x0.9 mm Body, 0.50 mm pitch, Very-Thin Quad Flat No Lead Package (VQFN) Punched

**GPC**

ZJI

**DRAWING NO.**

40ML1

**REV.**

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## 5. Revision History

Doc. Rev.	Date	Comments
5295ES	03/2013	Removed bullet from features: 2048-bit RSA® sign in 200ms. Updated footers and disclaimer page.
5295DS	12/2012	Changed GPIO6 to GPIO-Express-00. Updated package drawings 28A3 and 40ML1. Updated package drawing 28A1 to 28X1. Updated template and Atmel logos.
5295CS	03/2011	Corrected header and footers.
5295BS	10/2010	Added Industrial Grade support detail.
5295AS	01/2008	Initial document release.



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