9 GHz to 10 GHz, X-Band, GaAs, MMIC, Low Noise Converter

Data Sheet **HMC8108**

FEATURES

- Conversion gain: 13 dB typical
- Image rejection: 20 dBc typical
- Noise figure: 2 dB typical
- Input power for 1 dB compression: −4 dBm typical
- Input third-order intercept: 6 dBm typical
- Output saturated power: 10 dBm typical
- LO leakage at the IF port: −20 dBm typical
- LO leakage at the RF port: −37 dBm typical
- 32-terminal, 5 mm × 5 mm, ceramic leadless chip carrier (LCC)

APPLICATIONS

- Point to point and point to multipoint radios
- Military radar
- Satellite communications

FUNCTIONAL BLOCK DIAGRAM

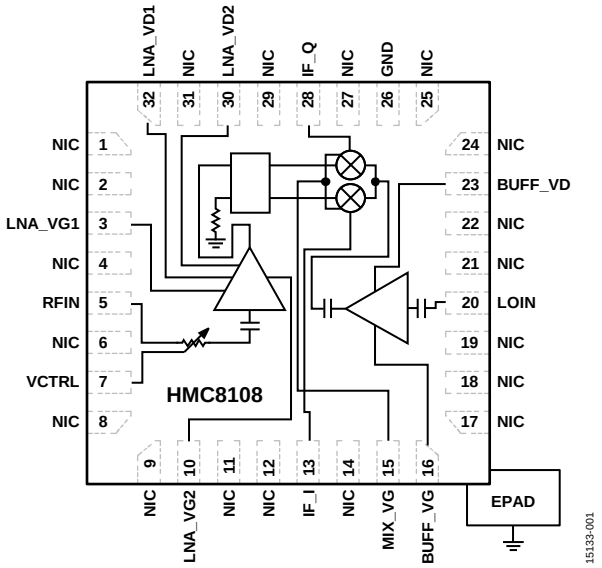

Figure 1.

GENERAL DESCRIPTION

The HMC8108 is a compact, X-band, gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC) in-phase/quadrature (I/Q), low noise converter in a ceramic, leadless chip carrier, RoHS compliant package. The HMC8108 converts radio frequency (RF) input signals ranging from 9 GHz to 10 GHz to a typical single-ended intermediate frequency (IF) signal of 60 MHz at its output. This device provides a small signal conversion gain of 13 dB with a noise figure of 2 dB and image rejection of 20 dBc.

The HMC8108 uses a low noise amplifier followed by an image reject mixer that is driven by an active LO buffer amplifier. The image reject mixer eliminates the need for a filter following the low noise amplifier and removes thermal noise at the image frequency. I/Q mixer outputs are provided, and an external 90° hybrid is needed to select the required sideband. The HMC8108 is a much smaller alternative to hybrid style, image reject mixer, downconverter assemblies and is compatible with surface-mount manufacturing techniques.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

2/2017—Revision 0: Initial Version

SPECIFICATIONS

T_A = −25°C, IF = 60 MHz, LNA_VD1/LNA_VD2 = +3 V, BUFF_VD = +3 V, VCTRL = −1 V, MIX_VG = −1.4 V, LO power= −5 dBm, downconverter mode with lower side selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range					
Radio Frequency	RF	9		10	GHz
Local Oscillator	LO	9		10	GHz
Intermediate Frequency	IF	0.02		1	GHz
LO Input Level		−10		0	dBm
PERFORMANCE					
Conversion Gain		10	13		dB
Gain Variation Range		10	15		dB
Noise Figure	NF		2	2.5	dB
Image Rejection		15	20		dBc
Input Power for 1 dB Compression	P1dB		−4		dBm
Input Third-Order Intercept	IP3	2	6		dBm
Input Second-Order Intercept	IP2		12		dBm
Output Saturated Power	P_{SAT}		10		dBm
LO Leakage at the IF Port[1]			−20		dBm
LO Leakage at the RF Port			−37	−25	dBm
RF Leakage at the IF Port[1]			−27		dBm
Amplitude Balance[1]			3		dB
Phase Balance[1]			4		Degree
Return Loss					
RF Port			15		dB
LO Port			9		dB
IF Port[1]			20		dB
POWER SUPPLY					
LNA_VD1			20		mA
LNA_VD2			30		mA
BUFF_VD			40		mA

[1] Measurements performed without external 90° hybrid at the IF ports.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	
LNA_VD1	5.8 V
LNA_VD2	4.8 V
BUFF_VD	4.2 V
Gate Bias Voltage	
LNA_VG1	−2 V to + 0.15 V
LNA_VG2	−2 V to + 0.15 V
MIX_VG	−2 V to + 0.15 V
BUFF_VG	−2 V to + 0.15 V
VCTRL	−2 V to + 0.15 V
RF Input Power	20 dBm
LO Input Power	24 dBm
Maximum Peak Reflow Temperature (MSL3)[1]	260°C
Maximum Junction Temperature	165°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to 150°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 0 (150 V)
Field Induced Charged Device Model (FICDM)	Class C3 (250 V)

[1] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
E-32-1[1]	93	119.47	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (PCB with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

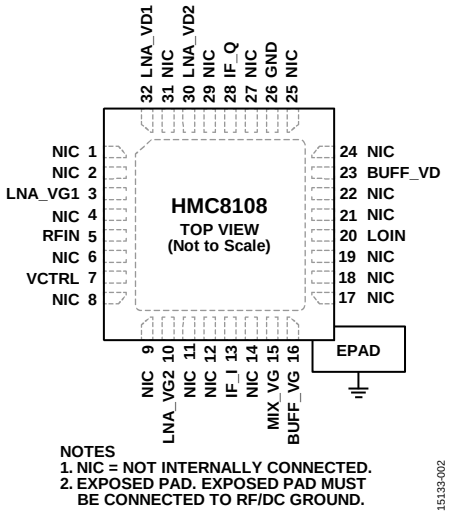

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 6, 8, 9, 11, 12, 14, 17 to 19, 21, 22, 24, 25, 27, 29, 31	NIC	No Internal Connection. These pins are not connected internally.
3	LNA_VG1	Gate Bias Voltage for the First Low Noise Amplifier. See Figure 3 for the interface schematic.
5	RFIN	Radio Frequency Input. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
7	VCTRL	Voltage Control. Gate bias attenuation control for the low noise amplifier. See Figure 5 for the interface schematic.
10	LNA_VG2	Gate Bias Voltage for the Second Low Noise Amplifier. See Figure 6 for the interface schematic.
13, 28	IF_I, IF_Q	In-Phase and Quadrature Intermediate Frequency Output Pins. See Figure 7 for the interface schematic.
15	MIX_VG	Gate Bias Voltage for FET Mixer. See Figure 8 for the interface schematic.
16	BUFF_VG	Gate Bias Voltage for the Local Oscillator Buffer. See Figure 9 for the interface schematic.
20	LOIN	Local Oscillator Input. This pin is ac-coupled and matched to 50 Ω. See Figure 10 for the interface schematic.
23	BUFF_VD	Drain Bias Voltage for the Local Oscillator Buffer. See Figure 11 for the interface schematic.
26	GND	Ground Connect. This pin must be connected to RF/dc ground. See Figure 12 for the interface schematic.
30	LNA_VD2	Drain Bias Voltage for the Second Low Noise Amplifier. See Figure 13 for the interface schematic.
32	LNA_VD1	Drain Bias Voltage for the First Low Noise Amplifier. See Figure 14 for the interface schematic.
	EPAD	Exposed Pad. Connect the exposed pad to RF/dc ground. See Figure 12 for the interface schematic.

INTERFACE SCHEMATICS

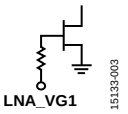

Figure 3. LNA_VG1 Interface Schematic

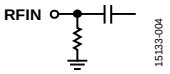

Figure 4. RFIN Interface Schematic

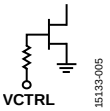

Figure 5. VCTRL Interface Schematic

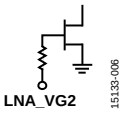

Figure 6. LNA_VG2 Interface Schematic

Figure 7. IF_I and IF_Q Interface Schematic

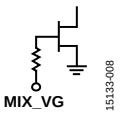

Figure 8. MIX_VG Interface Schematic

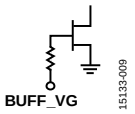

Figure 9. BUFF_VG Interface Schematic

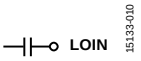

Figure 10. LOIN Interface Schematic

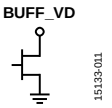

Figure 11. BUFF_VD Interface Schematic

Figure 12. GND and EPAD Interface Schematic

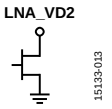

Figure 13. LNA_VD2 Interface

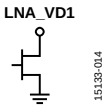

Figure 14. LNA_VD1 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

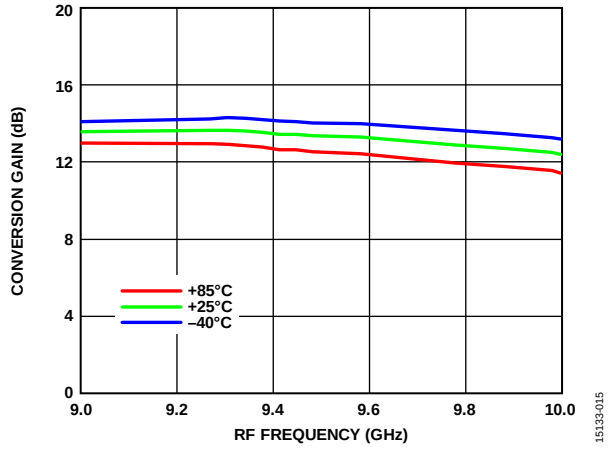

Figure 15. Conversion Gain vs. RF Frequency over Temperature

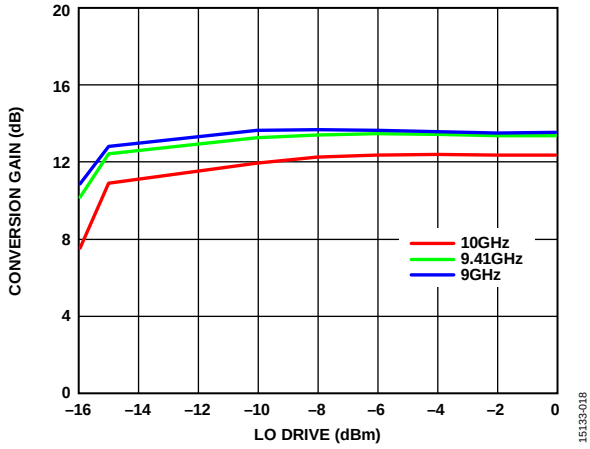

Figure 18. Conversion Gain vs. LO Drive at Various RF Frequencies

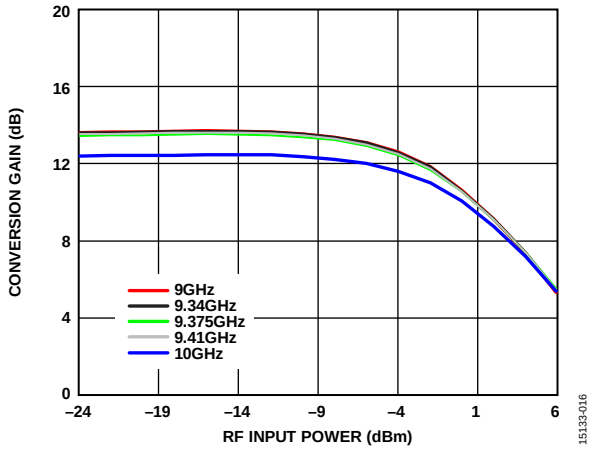

Figure 16. Conversion Gain vs. RF Input Power at Various RF Frequencies

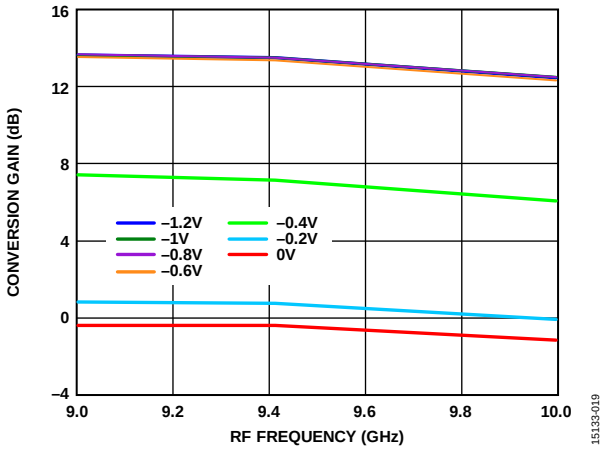

Figure 19. Conversion Gain vs. RF Frequency at Various Control Voltages

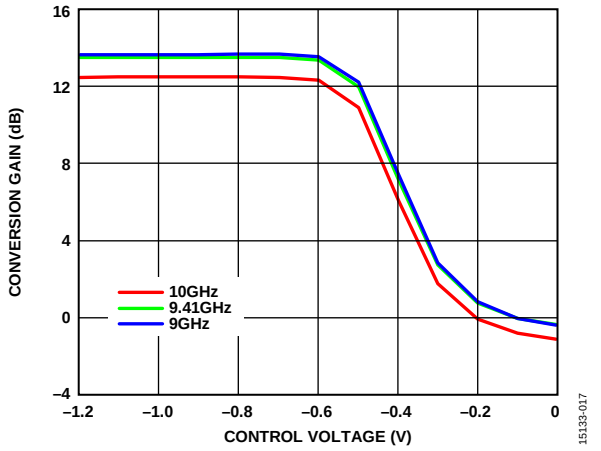

Figure 17. Conversion Gain vs. Control Voltage at Various RF Frequencies

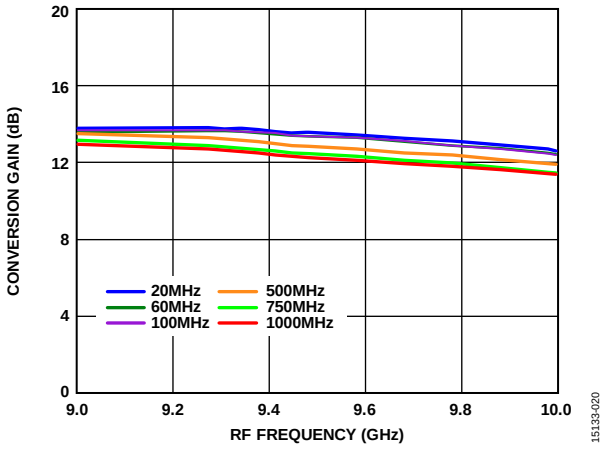

Figure 20. Conversion Gain vs. RF Frequency at Various IF Frequencies

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

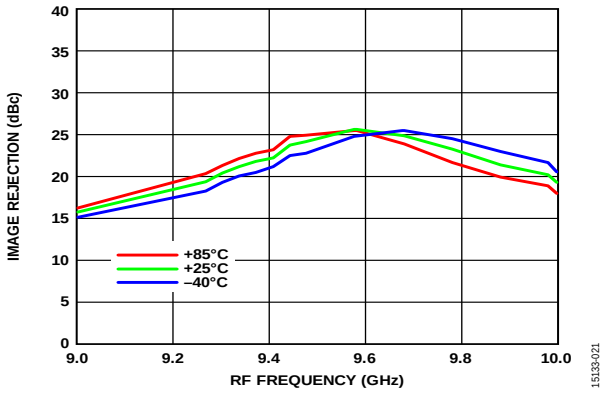

Figure 21. Image Rejection vs. RF Frequency over Temperature

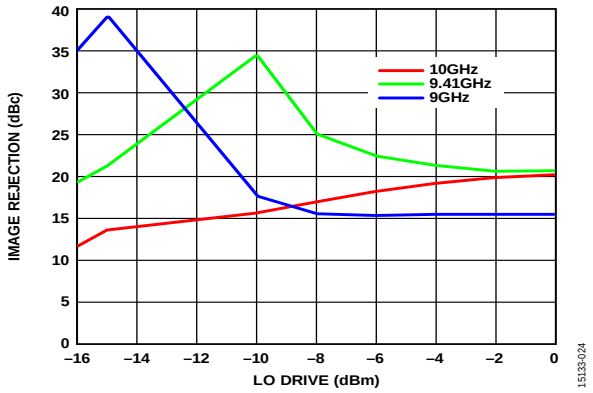

Figure 24. Image Rejection vs. LO Drive at Various RF Frequencies

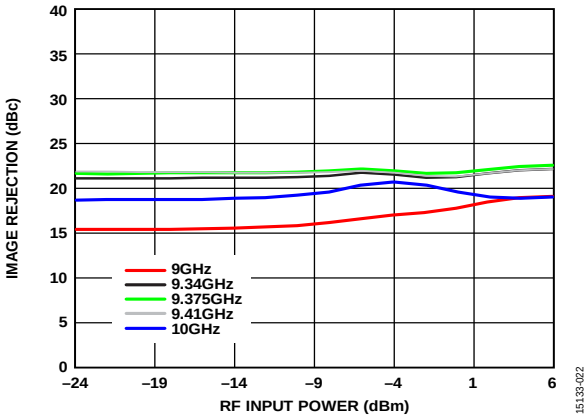

Figure 22. Image Rejection vs. RF Input Power at Various RF Frequencies

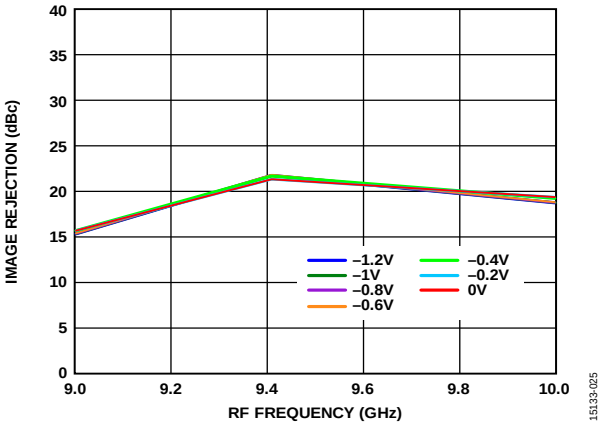

Figure 25. Image Rejection vs. RF Frequency at Various Control Voltages

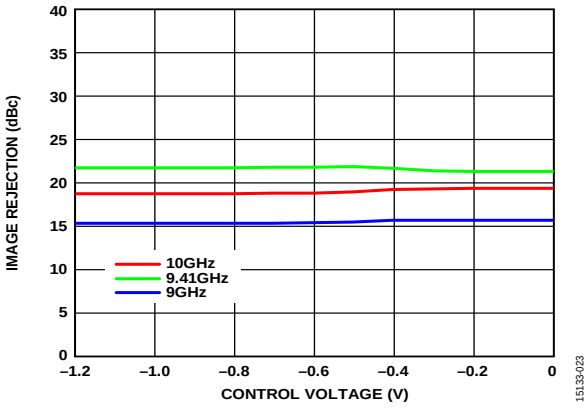

Figure 23. Image Rejection vs. Control Voltage at Various RF Frequencies

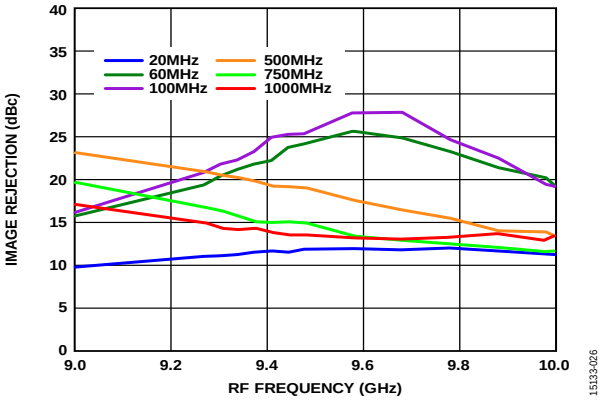

Figure 26. Image Rejection vs. RF Frequency at Various IF Frequencies

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

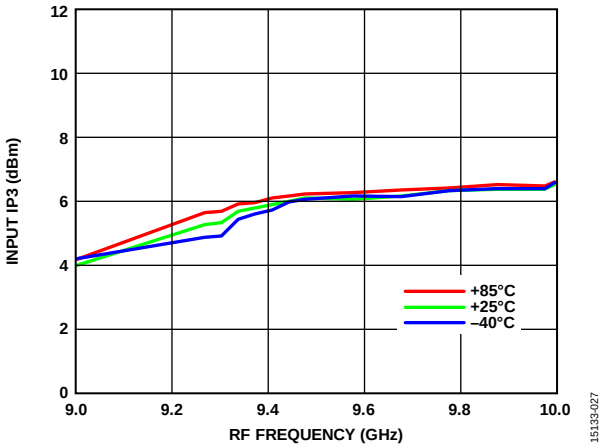

Figure 27. Input Third-Order Intercept (IP3) vs. RF Frequency over Temperature

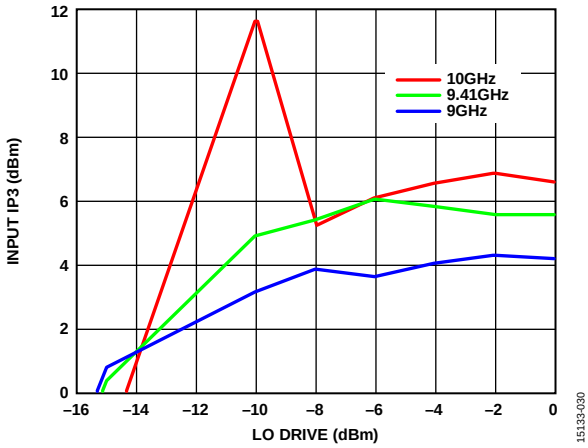

Figure 30. Input Third-Order Intercept (IP3) vs. LO Drive at Various RF Frequencies

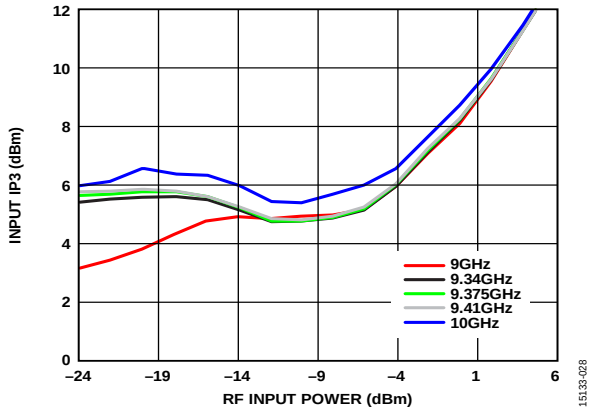

Figure 28. Input Third-Order Intercept (IP3) vs. RF Input Power at Various RF Frequencies

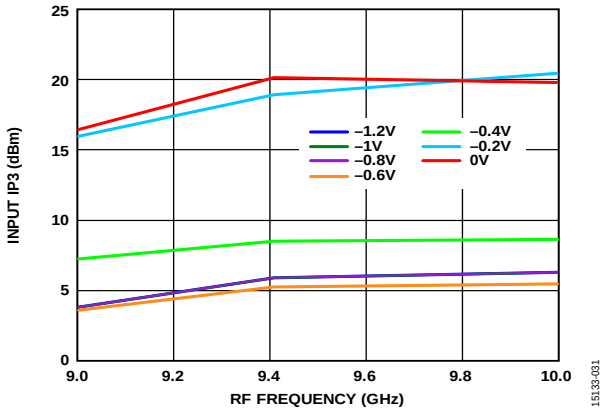

Figure 31. Input Third-Order Intercept (IP3) vs. RF Frequency at Various Control Voltages

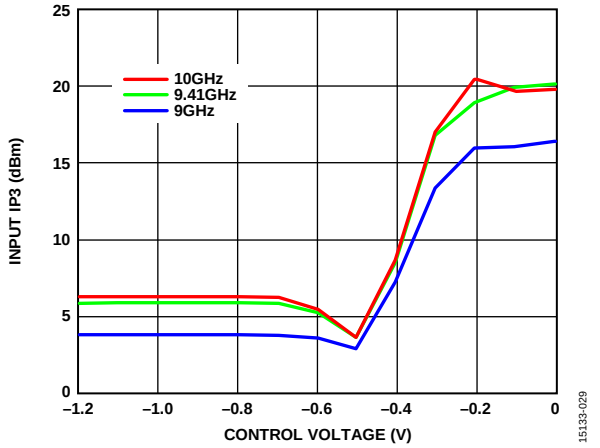

Figure 29. Input Third-Order Intercept (IP3) vs. Control Voltage at Various RF Frequencies

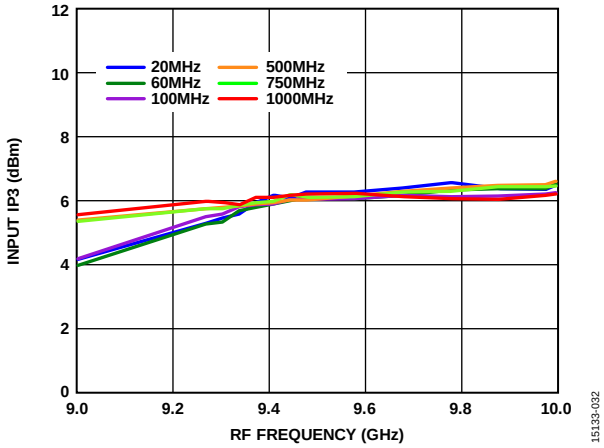

Figure 32. Input Third-Order Intercept (IP3) vs. RF Frequency at Various IF Frequencies

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

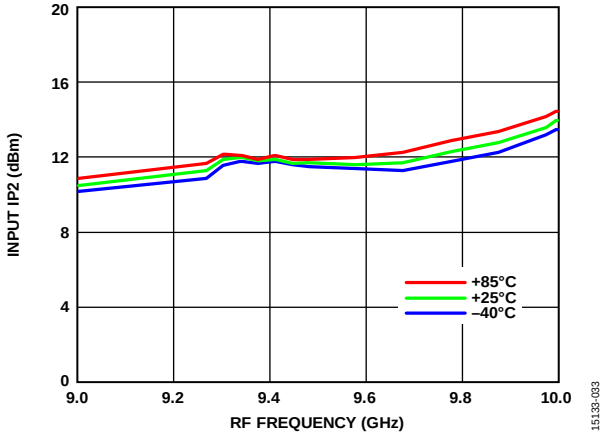

Figure 33. Input Second-Order Intercept (IP2) vs. RF Frequency over Temperature

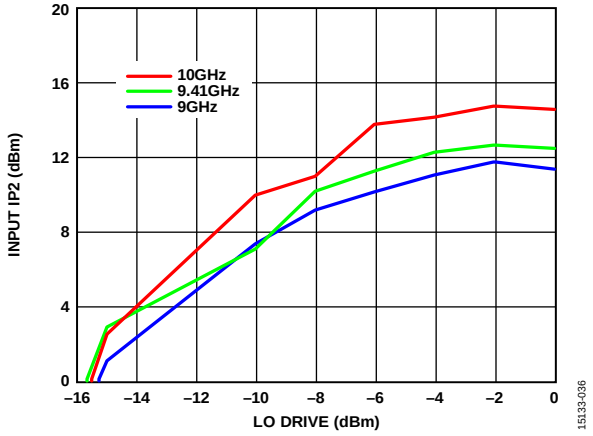

Figure 36. Input Second-Order Intercept (IP2) vs. LO Drive at Various RF Frequencies

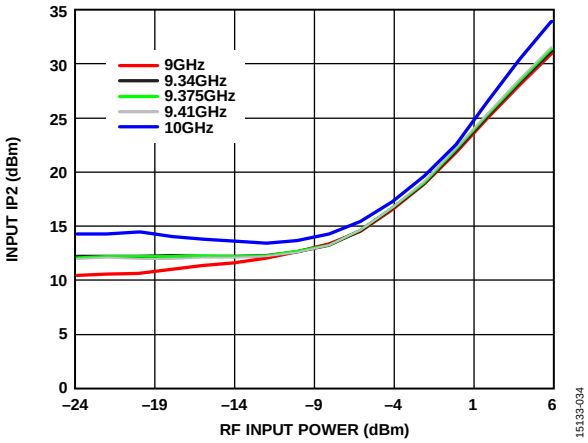

Figure 34. Input Second-Order Intercept (IP2) vs. RF Input Power at Various RF Frequencies

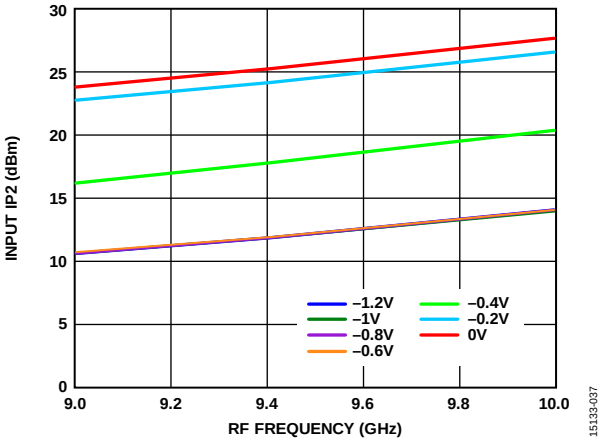

Figure 37. Input Second-Order Intercept (IP2) vs. RF Frequency at Various Control Voltages

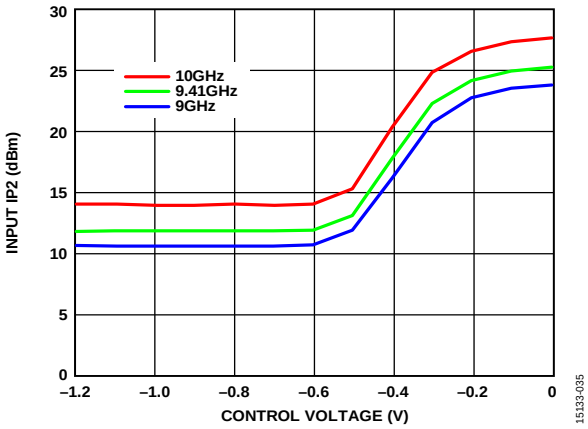

Figure 35. Input Second-Order Intercept (IP2) vs. Control Voltage at Various RF Frequencies

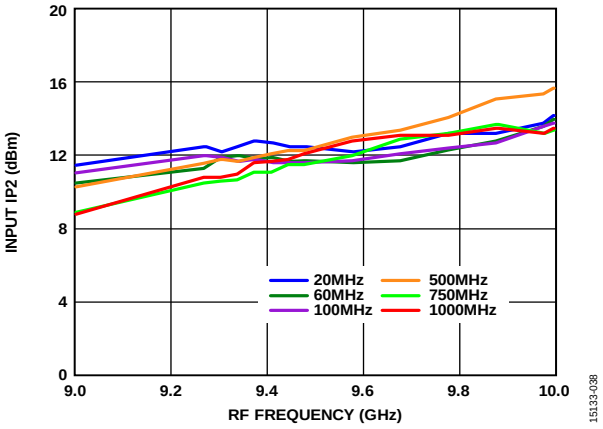

Figure 38. Input Second-Order Intercept (IP2) vs. RF Frequency at Various IF Frequencies

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

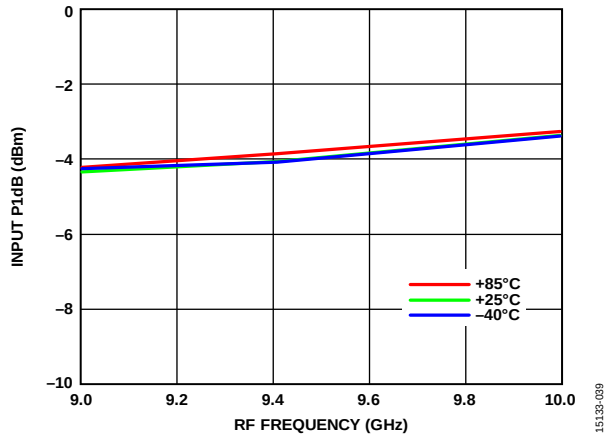

Figure 39. Input Power for 1 dB Compression (P1dB) vs. RF Frequency over Temperature

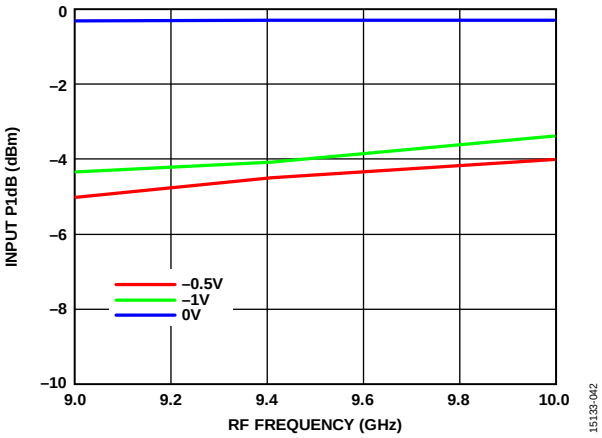

Figure 42. Input Power for 1 dB Compression (P1dB) vs. RF Frequency at Various Control Voltages

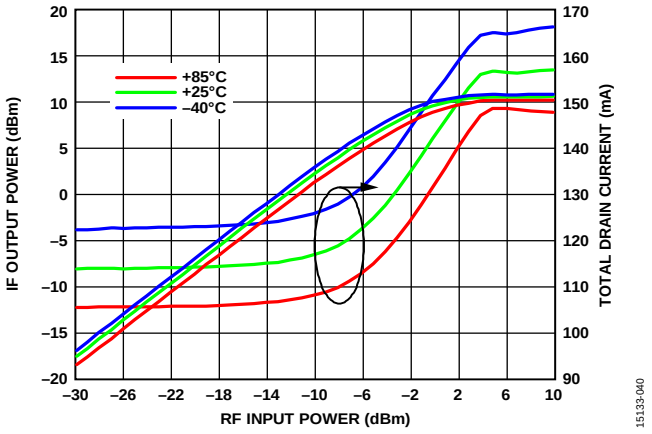

Figure 40. IF Output Power and Total Drain Current vs. RF Input Power over Temperature

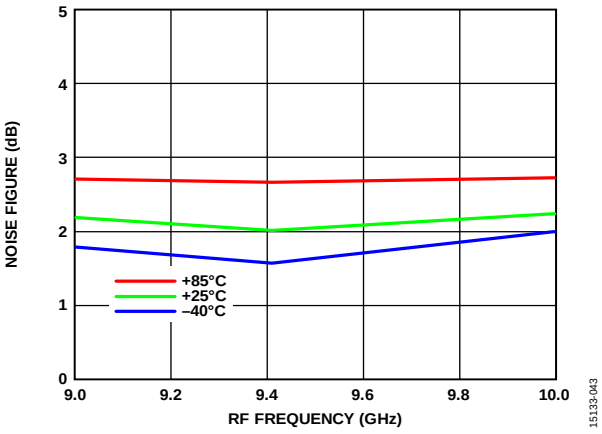

Figure 43. Noise Figure vs. RF Frequency over Temperature

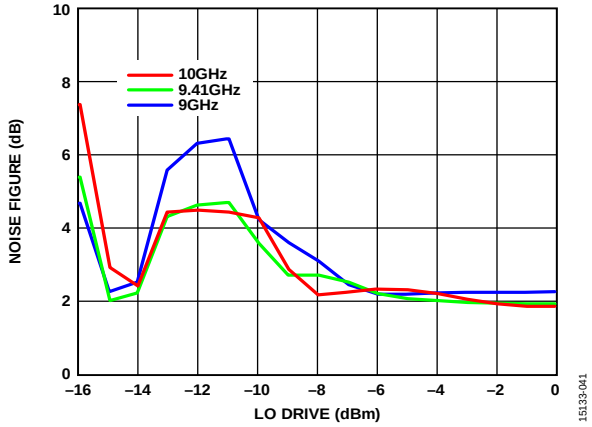

Figure 41. Noise Figure vs. LO Drive at Various RF Frequencies

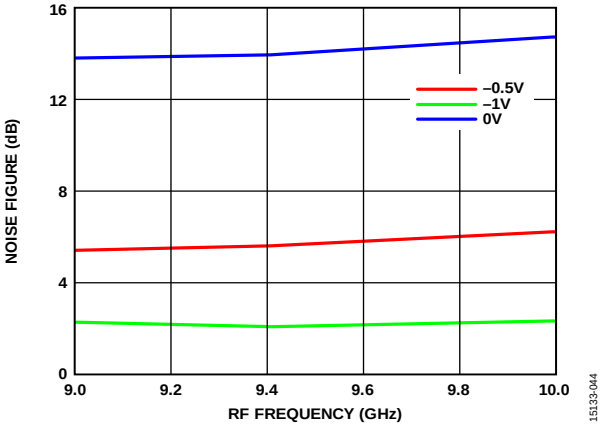

Figure 44. Noise Figure vs. RF Frequency at Various Control Voltages

Measurements performed as image reject mixer with lower sideband selected, external 90° hybrid at the IF ports, IF = 60 MHz, LO drive = −5 dBm, and T_A = −25°C, unless otherwise noted.

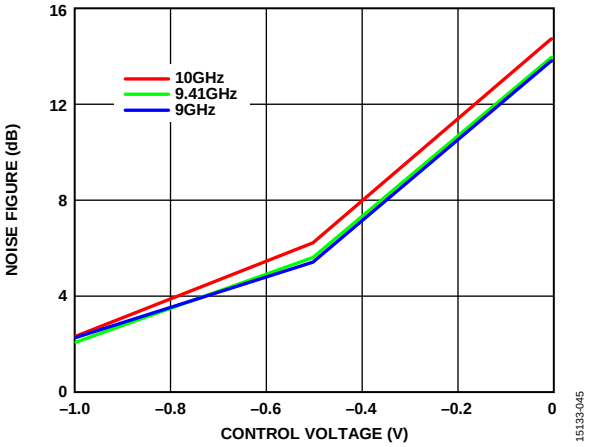

Figure 45. Noise Figure vs. Control Voltage at Various RF Frequencies

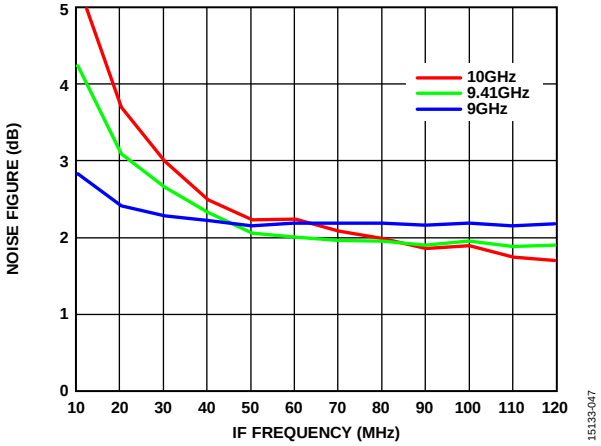

Figure 47. Noise Figure vs. IF Frequency at Various RF Frequencies

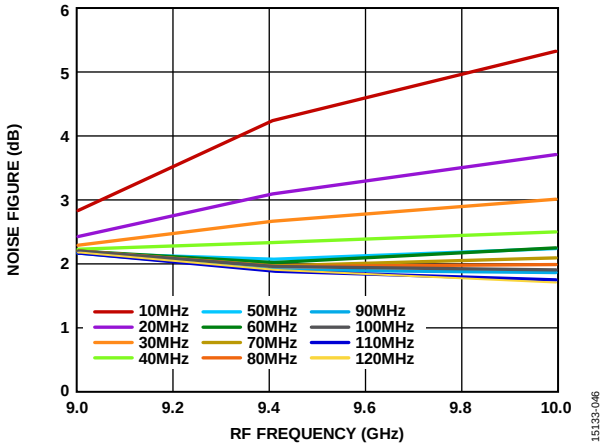

Figure 46. Noise Figure vs. RF Frequency at Various IF Frequencies

Measurements performed without external 90° hybrid at the IF ports and T_A = −25°C, unless otherwise noted.

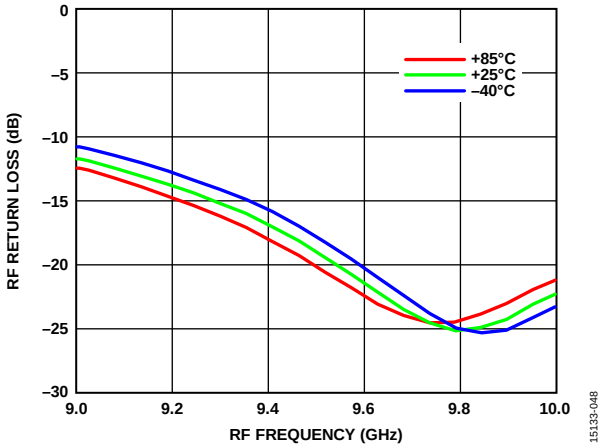

Figure 48. RF Return Loss vs. RF Frequency over Temperature

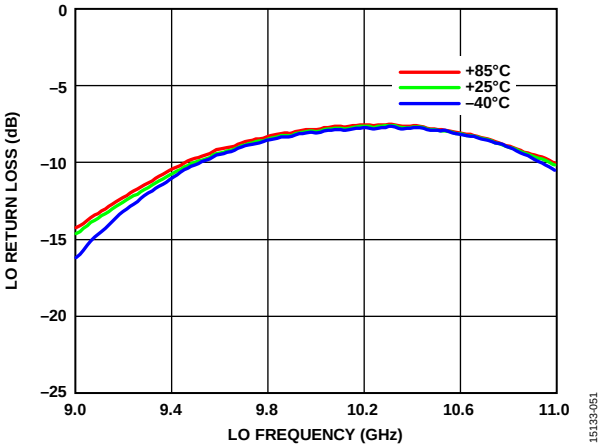

Figure 51. LO Return Loss vs. LO Frequency over Temperature

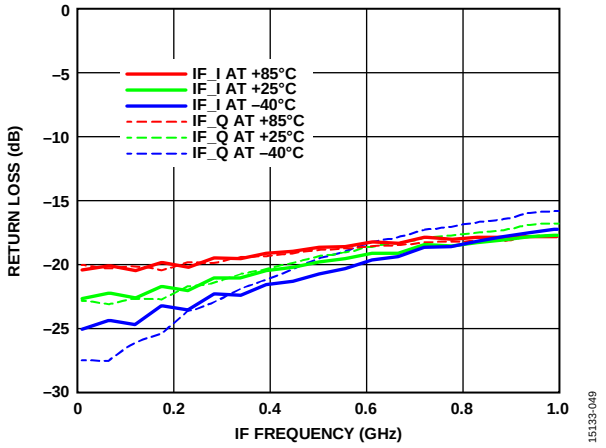

Figure 49. In-Phase and Quadrature IF Output Return Loss vs. IF Frequency over Temperature

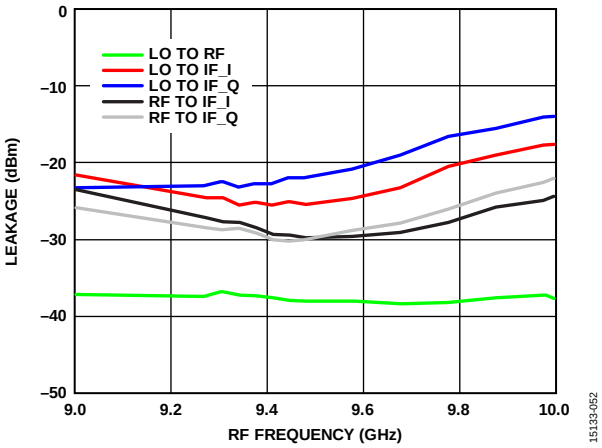

Figure 52. Leakage vs. RF Frequency

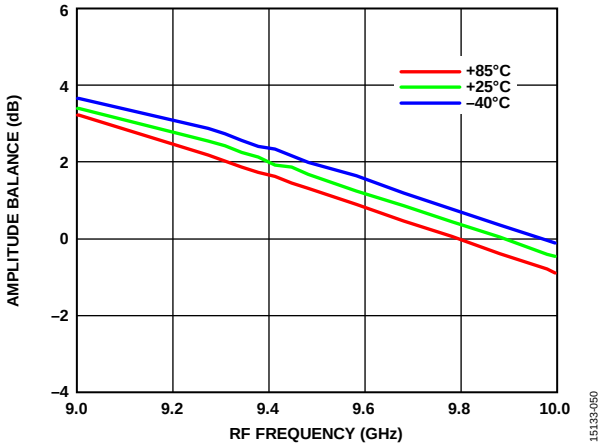

Figure 50. Amplitude Balance vs. RF Frequency over Temperature

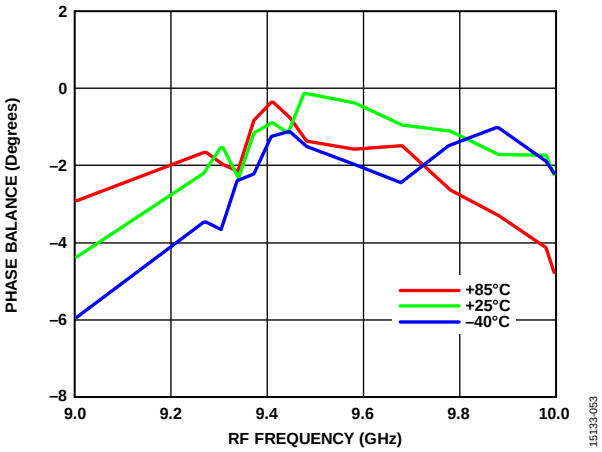

Figure 53. Phase Balance vs. RF Frequency over Temperature

THEORY OF OPERATION

The HMC8108 is a X-band, low noise converter with integrated LO buffers that converts RF input signals ranging from 9 GHz to 10 GHz down to a typical single-ended IF signal of 60 MHz at its output. See Figure 54 for a functional block diagram of the circuit architecture of the HMC8108.

The RF input signal passes through two stages of low noise amplification. The preamplified RF input signal then splits through an internal hybrid to feed two singly balanced passive mixers. A power divider followed by three LO buffer amplifiers drives the two I and Q mixer cores to convert the amplified RF input frequencies to a 60 MHz typical single-ended IF. A variable attenuator allows gain control ranging from 10 dB to 30 dB.

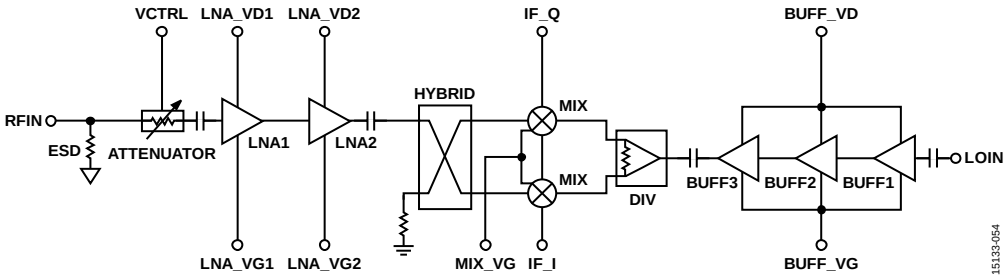

Figure 54. Functional Block Diagram of the Circuit Architecture

APPLICATIONS INFORMATION

A typical lower sideband application circuit is shown in Figure 57. The IF_Q output signal of the HMC8108 is connected to the 90° port of the hybrid coupler followed by a low-pass filter to produce a lower sideband IF output signal. The LO input signal passes through a voltage control oscillator (VCO) followed by an optional buffer amplifier, a 2× frequency multiplier, and an optional band-pass filter before entering the LO port of the device. Band-pass filter and LO buffer are optional and depend on the VCO specification and the LO input power requirement. External capacitors of 0.6 pF, 1 nF, 10 nF, and 100 nF, and 5.6 nH inductors are connected to the input voltage pin of the device. The IF_I and IF_Q pins are dc-coupled and must not source or sink more than 3 mA of current or device malfunction or possible device failure may result. For applications not requiring operation to dc, use an off chip dc blocking capacitor.

BIASING SEQUENCE

The HMC8108 uses amplifier and LO buffer stages. These active stages use depletion mode, pseudomorphic high electron mobility transfer (pHEMT) transistors.

To avoid transistor damage, follow these power-up bias sequence steps:

1. Set the LNA_VG1, LNA_VG2, and BUFF_VG power supplies to −2 V and the MIX_VG power supply to +1.4 V. Do not turn on the power supplies.
2. Set the LNA_VD1, LNA_VD2, and BUFF_VD power supplies to 3 V. Do not turn on the power supplies.
3. Set the VCTRL power supply to −1 V. Do not turn on the power supply.
4. Turn on the power supplies in Step 1, Step 2, and Step 3 in order.
5. Adjust the LNA_VG1, LNA_VG2, and BUFF_VG power supplies between −2 V and 0 V to achieve an quiescent current LNA_ID1, LNA_ID2, and BUFF_ID = 20 mA, 30 mA, and 40 mA, respectively.
6. Connect the signal generator to the RF and LO input.
7. Connect the 90° hybrid to the IF_I and IF_Q output. Note that IF_Q is connected to the 90° port of the hybrid. Under this condition, the lower sideband is selected.
8. Turn on the LO and RF input to see the output on the spectrum analyzer.

To turn off the HMC8108, take the following steps:

1. Turn off the LO and RF signal source.
2. Turn off the LNA_VD1, LNA_VD2, and BUFF_VD power supplies.
3. Turn off the LNA_VG1, LNA_VG2, BUFF_VG, MIX_VG, and VCTRL power supplies. Refer to Figure 55 for the HMC8108 lab bench setup.

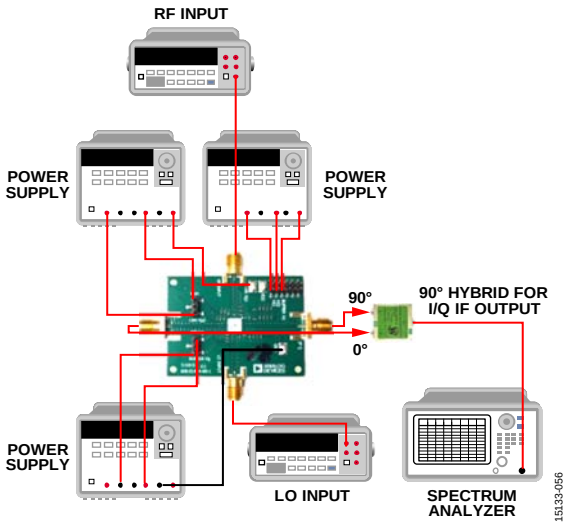

Figure 55. HMC8108 Lab Bench Setup

RESULTS

Figure 56 shows the expected results when testing the HMC8108 with the following operating conditions:

- RF = −15 dBm at 9.44 GHz
- LO = −5 dBm at 9.5 GHz
- The on board IF_Q port is connected to the 90° port of the hybrid.
- The lower sideband is selected.

Note that hybrid, cable, and board loss were not deembedded.

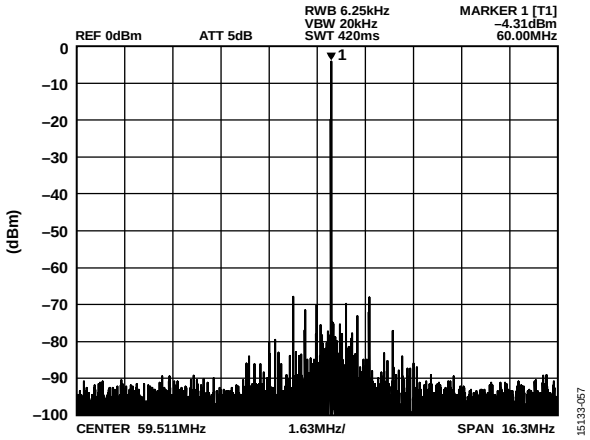

Figure 56. Test Results at IF = 60 MHz

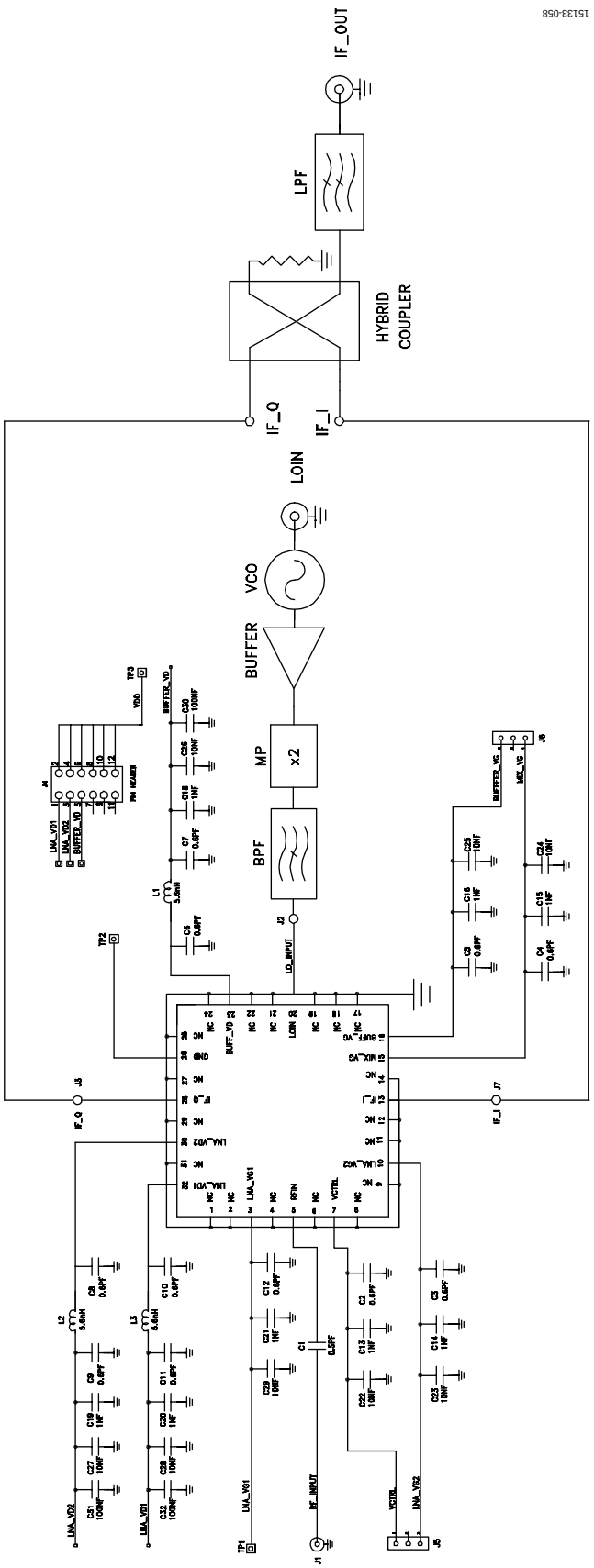

Figure 57. Typical Application Circuit

EVALUATION BOARD INFORMATION

RF circuit design techniques were implemented for the evaluation board PCB shown in Figure 58. Signal lines have 50 Ω impedance, and the package ground leads and exposed pad are connected directly to the ground plane. A sufficient number of via holes connect the top and bottom ground planes. The full evaluation circuit board shown in Figure 58 is available from Analog Devices, Inc., upon request.

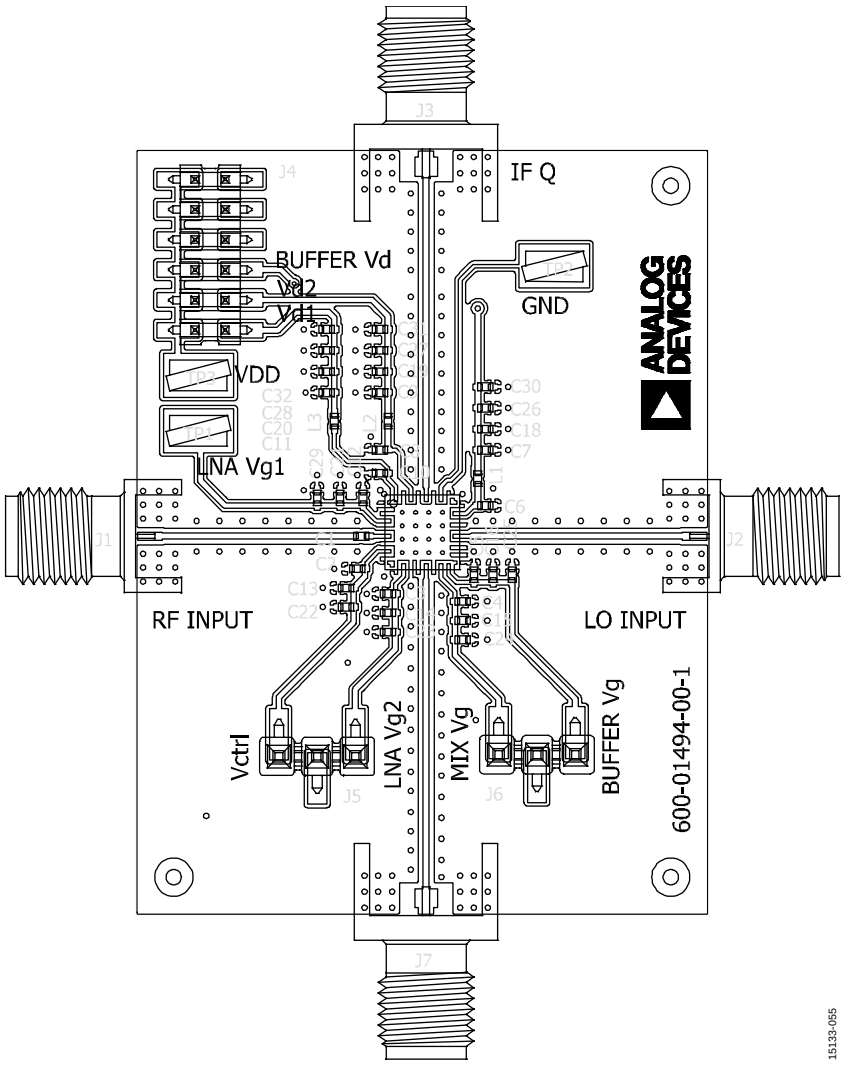

Figure 58. EV1HMC8108LC5 Evaluation PCB Top Layer

Table 5. Bill of Material for the EV1HMC8108LC5 Evaluation PCB

Reference Designator	Quantity	Description
600-01494-00-1	1	Evaluation board PCB; circuit board material: Rogers 4350 or Arlon 25FR
J1, J2	2	SMA connectors, SRI
J3, J7	2	SMA connectors, Johnson
J4	1	Connector header, 2 mm ,12-position vertical, SMT
J5, J6	2	Terminal strips, single row, 3-pin, SMT
C1	1	Ceramic capacitor, 0.5 pF, 50 V, C0G, 0402
C2 to C12	11	Ceramic capacitors, 0.6 pF, ±0.1 pF, 50 V, C0G, 0402
C13 to C16, C18 to C21	8	Ceramic capacitors, 1 nF, 50 V, X7R, 0402
C22 to C29	8	Ceramic capacitors, 10 nF, 50 V, 10%, X7R, 0402
C30 to C32	3	Ceramic capacitors, 100 nF, 16 V, 10%, X7R, 0402
L1 to L3	3	Inductors, 5.6 nH, 0402, ±5%, 760 mA
TP1 to TP3	3	Test points, PC compact, SMT
U1	1	Device under test (DUT), HMC8108LC5

OUTLINE DIMENSIONS

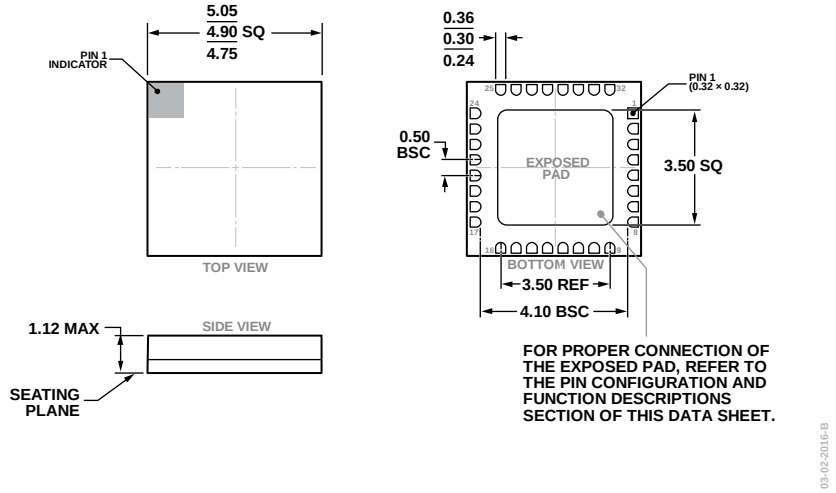

Figure 59. 32-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Body Material	Lead Finish	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC8108LC5	−40°C to +85°C	Alumina Ceramic	Gold over Nickel	MSL3	32-Terminal LCC	E-32-1	H8108 XXXX
HMC8108LC5TR	−40°C to +85°C	Alumina Ceramic	Gold over Nickel	MSL3	32-Terminal LCC	E-32-1	H8108 XXXX
HMC8108LC5TR-R5	−40°C to +85°C	Alumina Ceramic	Gold over Nickel	MSL3	32-Terminal LCC	E-32-1	H8108 XXXX
EV1HMC8108LC5	−40°C to +85°C	Alumina Ceramic			Evaluation Board		

[1] The HMC8108LC5, the HMC8108LC5TR, and the HMC8108LC5TR-R5 are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section.
[3] The HMC8108LC5, the HMC8108LC5TR, and the HMC8108LC5TR-R5 four-digit lot numbers are XXXX.