MIC2582/MIC2583

Single Channel Hot Swap Controllers

General Description

The MIC2582 and MIC2583 are single channel positive voltage hot swap controllers designed to allow the safe insertion of boards into live system backplanes. The MIC2582 and MIC2583 are available in 8-pin SOIC and 16-pin QSOP packages, respectively. Using a few external components and by controlling the gate drive of an external N-Channel MOSFET device, the MIC2582/83 provide inrush current limiting and output voltage slew rate control in harsh, critical power supply environments. Additionally, a circuit breaker function will latch the output MOSFET off if the current limit threshold is exceeded for a determined period. The MIC2583R option includes an auto-restart function upon detecting an over current condition.

Datasheets and support documentation can be found on Micrel's web site at www.micrel.com.

Features

- MIC2582:
  Pin-for-pin functional equivalent to the LTC1422
- 2.3V to 13.2V supply voltage operation
- Surge voltage protection up to 20V
- Current regulation limits inrush current regardless of load capacitance
- Programmable inrush current limiting
- Electronic circuit breaker
- Optional dual-level overcurrent threshold detects excessive load faults
- Fast response to short circuit conditions (<1µs)
- Programmable output under-voltage detection
- Under-voltage Lockout (UVLO) protection
- Auto-restart function (MIC2583R)
- Power-On Reset and Power-Good status outputs (Power-Good for the MIC2583 and MIC2583R only)
- /FAULT status output (MIC2583 and MIC2583R)

Applications

- RAID systems
- Base stations
- PC board hot swap insertion and removal
- +12V backplanes
- Network switches

Typical Applications

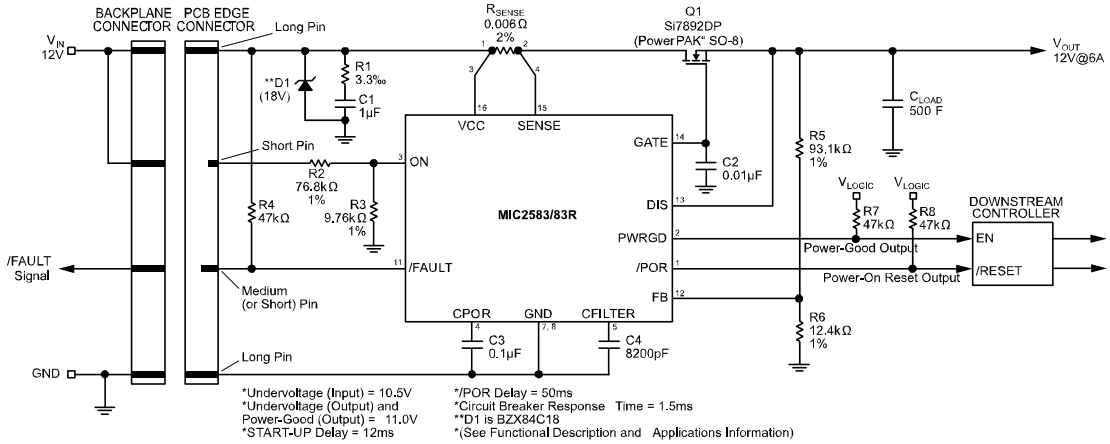


Figure 1. MIC2583/83R Typical Application Circuit

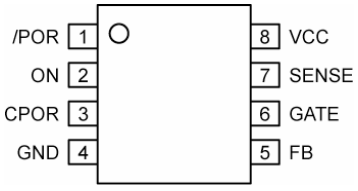
Ordering Information

Part Number		Fast Circuit Breaker Threshold	Circuit Breaker	Package
Standard	**Pb-Free**			
MIC2582-JBM	MIC2582-xYM	x = J, 100mV x = J1, Off x = M, Off	Latched off	8-Pin SOIC
MIC2583-xBQS	MIC2583-xYQS	x = J, 100mV x = K*, 150mV x = L*, 200mV x = M*, Off	Latched off	16-pin QSOP
MIC2583R-xBQS	MIC2583R-xYQS	x = J, 100mV x = K*, 150mV x = L*, 200mV x = M*, Off	Auto-retry	16-pin QSOP

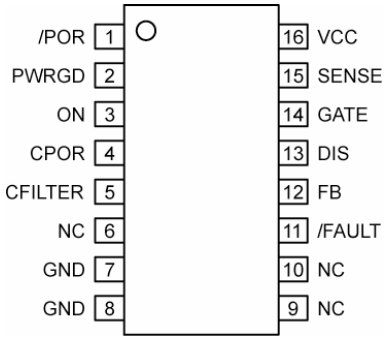
Note:

* Contact factory for availability.

Pin Configuration



8-Pin SOIC (M)



16-Pin QSOP (QS)

Pin Description

Pin Number 8-Pin SOIC	Pin Number 16-Pin QSOP	Pin Name	Pin Name
1	1	/POR	Power-On Reset Output: Open drain N-channel device, Active Low. This pin remains asserted during start-up until a time period (t_{POR}) after the FB pin voltage rises above the power-good threshold (VFB). The timing capacitor C_{POR} determines t_{POR}. When the output voltage monitored at the FB pin falls below V_{FB}, /POR is asserted for a minimum of one timing cycle (t_{POR}). The /POR pin requires a pull-up resistor (10kΩ minimum) to VCC.
2	3	ON	ON Input: Active High. The ON pin, an input to a Schmitt-triggered comparator used to enable/disable the controller, is compared to a 1.24V reference with 50mV of hysteresis. When a logic high is applied to the ON pin (V_{ON} > 1.24V), a start-up sequence begins when the GATE pin starts ramping up towards its final operating voltage. When the ON pin receives a logic low signal (V_{ON} < 1.19V), the GATE pin is grounded and /FAULT remains high if VCC is above the UVLO threshold. ON must be low for 20µs in order to initiate a start-up sequence. Additionally, toggling the ON pin LOW to HIGH resets the circuit breaker.
3	4	CPOR	Power-On Reset Timer: A capacitor connected between this pin and ground sets the supply contact start-up delay (t_{START}) and the power-on reset interval (t_{POR}). When VCC rises above the UVLO threshold, the capacitor connected to C_{POR} begins to charge. When the voltage at CPOR crosses 0.3V, the start-up threshold (V_{START}), a start cycle is initiated if ON is asserted while capacitor C_{POR} is immediately discharged to ground. When the voltage at FB rises above V_{FB}, capacitor C_{POR} begins to charge again. When the voltage at CPOR rises above the power-on reset delay threshold (V_{TH}), the timer resets by pulling CPOR to ground, and /POR is de-asserted. If C_{POR} is left open, then t_{START} defaults to 20µs.
4	7, 8	GND	Ground Connection: Tie to analog ground.
5	12	FB	Power-Good Threshold Input (Under-voltage Detect): This input is internally compared to a 1.24V reference with 30mV of hysteresis. An external resistive divider may be used to set the voltage at this pin. If this input momentarily goes below 1.24V, then /POR is activated for one timing cycle, t_{POR}, indicating an output under-voltage condition. The /POR signal de-asserts one timing cycle after the FB pin exceeds the power-good threshold by 30mV. A 5µs filter on this pin prevents glitches from inadvertently activating this signal.
6	14	GATE	Gate Drive Output: Connects to the gate of an external N-channel MOSFET. An internal clamp ensures that no more than 9V is applied between the GATE pin and the source of the external MOSFET. The GATE pin is immediately brought low when either the circuit breaker trips or an under-voltage lockout condition occurs.
7	15	SENSE	Circuit Breaker Sense Input: A resistor between this pin and VCC sets the current limit threshold. Whenever the voltage across the sense resistor exceeds the slow trip current limit threshold ($V_{TRIPSLOW}$), the GATE voltage is adjusted to ensure a constant load current. If $V_{TRIPSLOW}$ (50mV) is exceeded for longer than time period t_{OCSLOW}, then the circuit breaker is tripped and the GATE pin is immediately pulled low. If the voltage across the sense resistor exceeds the fast trip circuit breaker threshold, $V_{TRIPFAST}$, at any point due to fast, high amplitude power supply faults, then the GATE pin is immediately brought low without delay. To disable the circuit breaker, the SENSE and VCC pins can be tied together. The default $V_{TRIPFAST}$ for either device is 100mV. Other fast trip thresholds are available: 150mV, 200mV, or OFF ($V_{TRIPFAST}$ disabled). Please contact factory for availability of other options.
8	16	VCC	Positive Supply Input: 2.3V to 13.2V. The GATE pin is held low by an internal under-voltage lockout circuit until VCC exceeds a threshold of 2.2V. If VCC exceeds 13.2V, an internal shunt regulator protects the chip from transient voltages up to 20V at the VCC and SENSE pins.

Pin Number 8-Pin SOIC	Pin Number 16-Pin QSOP	Pin Name	Pin Name
n/a	2	PWRGD	Power-Good Output: Open drain N-channel device, Active High. When the voltage at the FB pin is lower than 1.24V, PWRGD output is held low. When the voltage at the FB pin exceeds 1.24V, then PWRGD is asserted immediately. The PWRGD pin requires a pull-up resistor (10kΩ minimum) to VCC.
n/a	5	CFILTER	Current Limit Response Timer: A capacitor connected to this pin defines the period of time (t_{OCSLOW}) in which an over current event must last to signal a fault condition and trip the circuit breaker. If no capacitor is connected, then t_{OCSLOW} defaults to 5µs.
n/a	11	/FAULT	Circuit Breaker Fault Status Output: Open drain N-channel device, Active Low. The /FAULT pin is asserted when the circuit breaker trips due to an over current condition or when an under-voltage lockout condition exists. The/FAULT pin requires a pull-up resistor (10kΩ minimum) to VCC.
n/a	13	DIS	Discharge Output: When the MIC2583/83R is turned off, a 500Ω internal resistor at this output allows the discharging of any load capacitance to ground.
n/a	6, 9, 10	NC	No internal connection.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.3V to 20V
/POR, /FAULT, PWRGD pins..... –0.3V to 15V
SENSE pin ..... –0.3V to V_{CC}+0.3V
ON pin ..... –0.3V to V_{CC}+0.3V
GATE pin ..... –0.3V to 20V
FB Input pins ..... –0.3V to 6V
Junction Temperature ..... +125°C
Lead Temperature
Standard Package (-JBM and –xBQS)
(IR Reflow, Peak Temperature) ..240°C + 0°C/-5°C
Pb-Free Package (-xYM or –xYQS)
(IR Reflow, Peak Temperature) ..260°C + 0°C/-5°C
EDS Rating
Human body model..... 2kV
Machine model 100V

Operating Ratings[2]

Supply Voltage (V_{CC})..... +2.3V to +13.2V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
SOIC (θ_{JA})..... 163°C/W
QSOP (θ_{JA}) ..... 112°C/W

Electrical Characteristics[3]

V_{CC} = 5.0V, T_A = 25°C unless noted. **Bold** values indicate –40°C ≤ T_A ≤ +85°C.

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			**2.3**		**13.2**	V
I_{CC}	Supply Current	V_{ON} = 2V			1.5	**2.5**	mA
V_{TRIP}	Circuit Breaker Trip Voltage (Current Limit Threshold)	$V_{TRIP} = V_{CC} - V_{SENSE}$	$V_{TRIPSLOW}$	**42**	50	**59**	
			$V_{TRIPFAST}$ (MIC2582-Jxx)		100		mV
			$V_{TRIPFAST}$ (MIC2583/83R) X = J X = K X = L	**85** **130** **175**	100 150 200	**110** **170** **225**	mV mV mV
V_{GS}	External Gate Drive	$V_{GATE} - V_{CC}$	V_{CC} > 3V	**7**	8	**9**	V
			V_{CC} = 2.3V	**3.5**	4.8	**6.5**	V
I_{GATE}	GATE Pin Pull-Up Current	Start Cycle, V_{GATE} = 0V, V_{CC} = 13.2V		**−30**	17	**−8**	µA
		V_{CC} = 2.3V		**−26**	17	**−8**	µA
$I_{GATEOFF}$	GATE Pink Sink Current	V_{GATE} > 1V	V_{CC} = 13.2V, Note 4		100		µA
			V_{CC} = 2.3V, Note 4		50		µA
		/FAULT = 0 (MIC2583/83R only)	Turn Off		110		µA
I_{TIMER}	Current Limit/Overcurrent Timer (CFILTER) Current (MIC2583/83R)	$V_{CC} - V_{SENSE} > V_{TRIPSLOW}$ (timer on)		**−8.5**	−6.5	**−4.5**	µA
		$V_{CC} - V_{SENSE} > V_{TRIPSLOW}$ (timer off)		**4.5**	6.5	**8.5**	µA
I_{CPOR}	Power-On-Reset Timer Current	Timer on		**−3.5**	2.5	**−1.5**	µA
		Timer off		**0.5**	1.3		mA
V_{TH}	POR Delay and Overcurrent Timer (CFILTER) Threshold	V_{CPOR} rising $V_{CFILTER}$ rising (MIC2583/83R only)		**1.19**	1.245	**1.30**	V
V_{UV}	Undervoltage Lockout Threshold	V_{CC} rising		**2.1**	2.2	**2.3**	V
		V_{CC} falling		**1.90**	2.05	**2.20**	V
V_{UVHYS}	Undervoltage Lockout Hysteresis				150		mV
V_{ON}	ON Pin Threshold Voltage	2.3V ≤ V_{CC} ≤ 13.2V	ON rising	**1.19**	1.24	**1.29**	V
			ON falling	**1.14**	1.19	**1.24**	V
V_{ONHYS}	ON Pin Hysteresis				50		mV

Symbol	Parameter	Condition		Min	Typ	Max	Units
ΔV_{ON}	ON Pin Threshold Line Regulation	2.3V ≤ V_{CC} ≤ 13.2V			2		mV
I_{ON}	ON Pin Input Current	V_{ON} = V_{CC}				−0.5	µA
V_{START}	Start-Up Delay Timer Threshold	V_{CPOR} rising		**0.26**	0.31	**0.36**	V
V_{AUTO}	Auto-Restart Threshold Voltage (MIC2583R only)	Upper threshold		**0.19**	1.24	**1.30**	V
		Lower threshold		**0.26**	0.31	**0.36**	V
I_{AUTO}	Auto-Restart Current (MIC2583R only)	Charge current		**10**	13	**16**	µA
		Discharge current			1.4	**2**	µA
V_{FB}	Power-Good Threshold Voltage	2.3V = V_{CC} = 13.2V	FB rising	**1.19**	1.24	**1.29**	V
			FB falling	**1.15**	1.20	**1.25**	V
V_{FBHYS}	FB Hysteresis				40		mV
I_{FBLKG}	FB Pin Leakage Current	2.3V = V_{CC} = 13.2V, V_{FB} = 1.3V				**1.5**	µA
V_{OL}	/POR, /FAULT, PWRGD Output Voltage (/FAULT, PWRGD MIC2583/83R only)	I_{OUT} = 1mA				**0.4**	V
R_{DIS}	Output Discharge Resistance (MIC2583/83R only)				500	**1000**	Ω
AC Parameters[4]							
t_{OCFAST}	Fast Overcurrent SENSE to GATE Low Trip Time	V_{CC} = 5V, V_{CC} − V_{SENSE} = 100mV C_{GATE} = 10nF, Figure 2			1		µs
t_{OCSLOW}	Slow Overcurrent SENSE to GATE Low Trip Time	V_{CC} = 5V, V_{CC} − V_{SENSE} = 50mV C_{FILTER} = 0, Figure 2			5		µs
t_{ONDLY}	ON Delay Filter				20		µs
t_{FBDLY}	FB Delay Filter				20		µs

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Specification for packaged product only.
4. Not a tested parameter, guaranteed by design.

Timing Diagrams

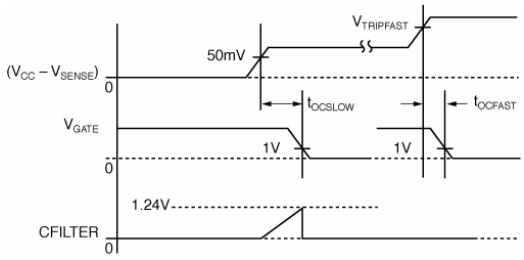


Figure 2. Current-Limit Response

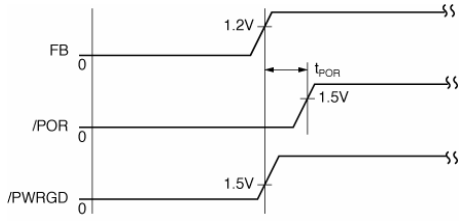


Figure 3. Power-On Reset Response

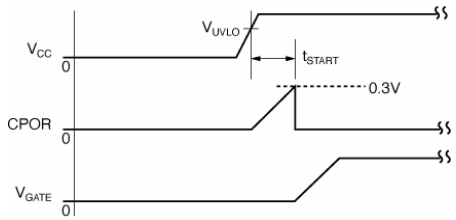


Figure 4. Power-On Start-Up Delay Timing

Test Circuit

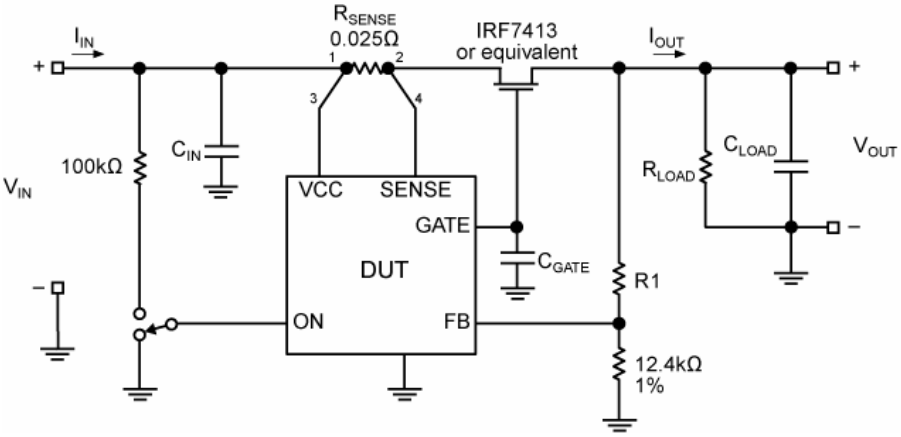
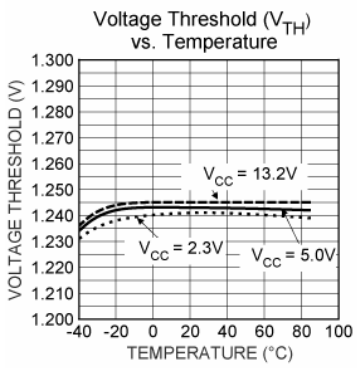
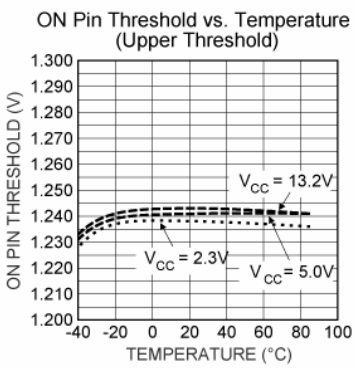
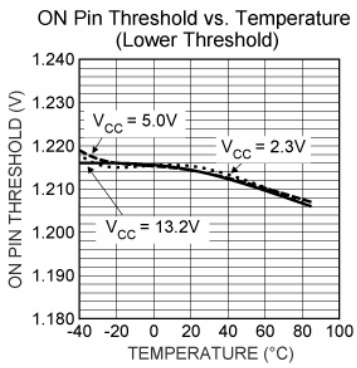


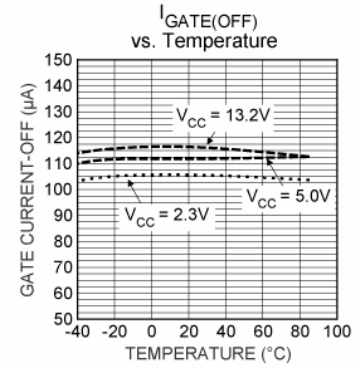
Figure 5. Applications Test Circuit
(not all pins shown for simplicity)

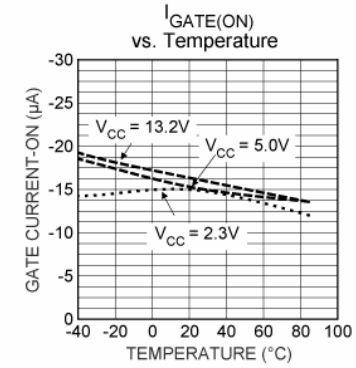
Typical Characteristics

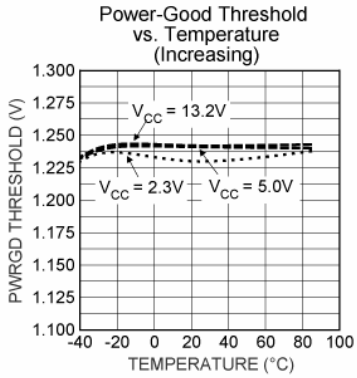


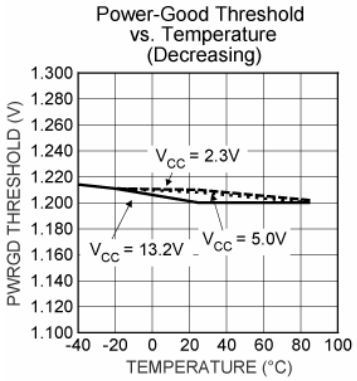


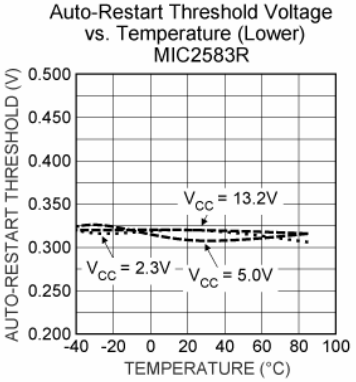


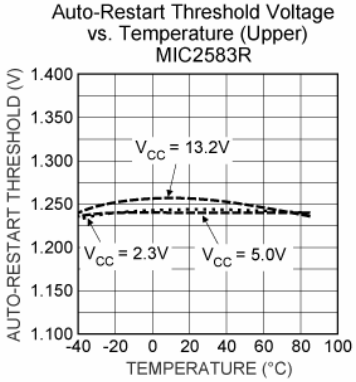


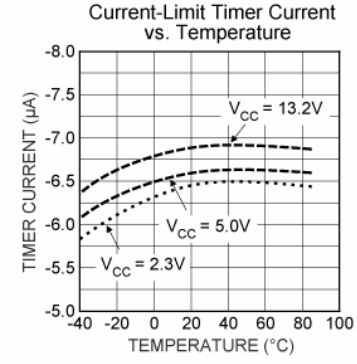


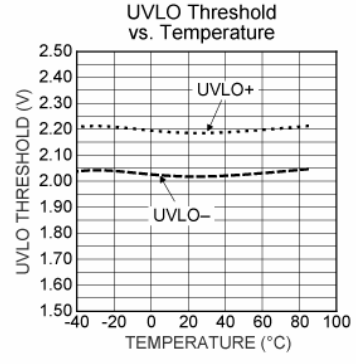


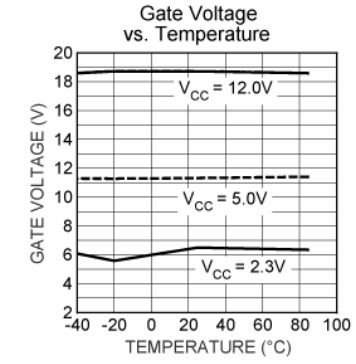


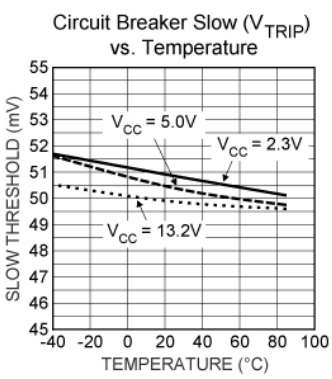


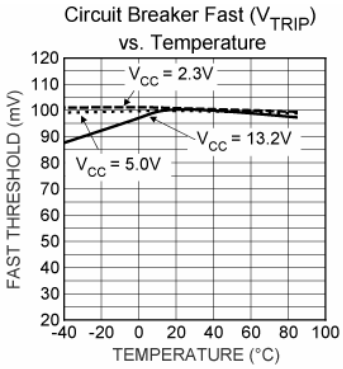


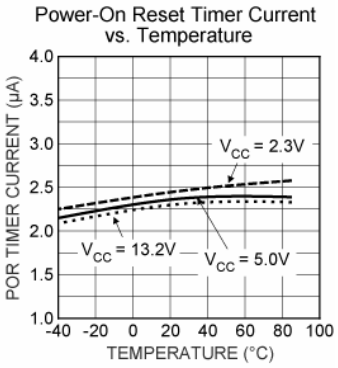


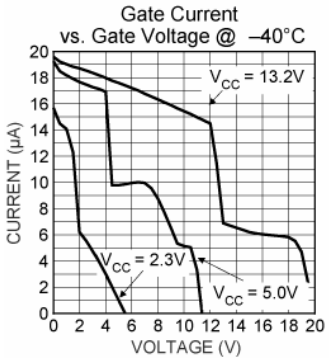


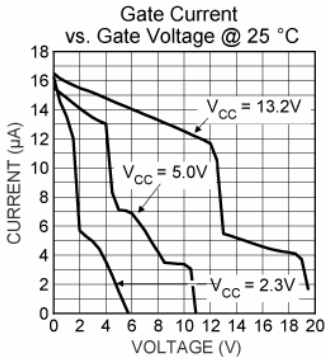


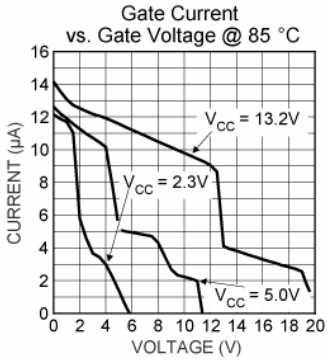

Circuit Breaker Slow (V_{TRIP}) vs. Temperature
SLOW THRESHOLD (mV)
TEMPERATURE (°C)
V_{CC} = 5.0V
V_{CC} = 2.3V
V_{CC} = 13.2V


Circuit Breaker Fast (V_{TRIP}) vs. Temperature
FAST THRESHOLD (mV)
TEMPERATURE (°C)
V_{CC} = 2.3V
V_{CC} = 13.2V
V_{CC} = 5.0V


Power-On Reset Timer Current vs. Temperature
POR TIMER CURRENT (µA)
TEMPERATURE (°C)
V_{CC} = 2.3V
V_{CC} = 13.2V
V_{CC} = 5.0V

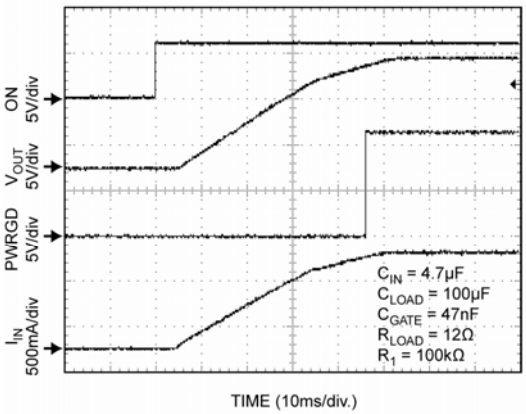

Gate Current vs. Gate Voltage @ –40°C
CURRENT (µA)
VOLTAGE (V)
V_{CC} = 13.2V
V_{CC} = 2.3V
V_{CC} = 5.0V


Gate Current vs. Gate Voltage @ 25 °C
CURRENT (µA)
VOLTAGE (V)
V_{CC} = 13.2V
V_{CC} = 5.0V
V_{CC} = 2.3V

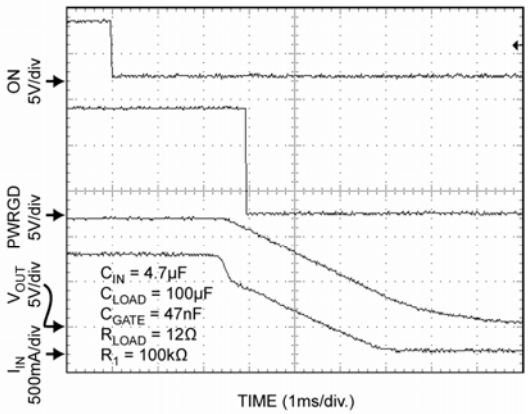

Gate Current vs. Gate Voltage @ 85 °C
CURRENT (µA)
VOLTAGE (V)
V_{CC} = 13.2V
V_{CC} = 2.3V
V_{CC} = 5.0V

Functional Characteristics (See Figure 5, Applications Test Circuit)

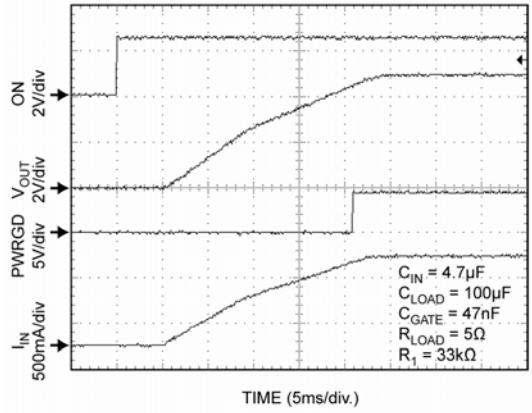
Turn On - V_{OUT} = 12V



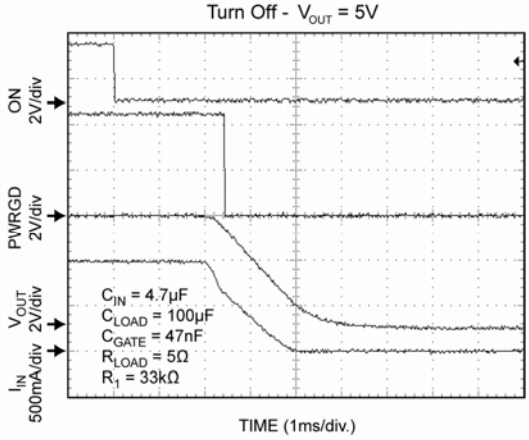
Turn Off - V_{OUT} = 12V



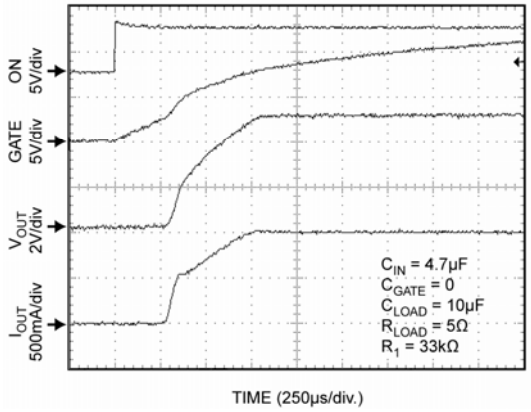
Turn On - V_{OUT} = 5V



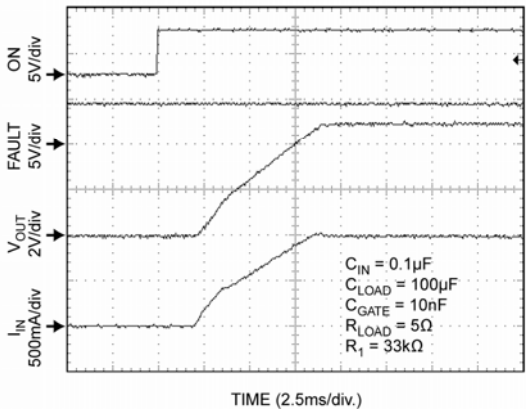
Turn Off - V_{OUT} = 5V



Turn On (C_{GATE} = 0) - V_{OUT} = 5V (MIC2583)

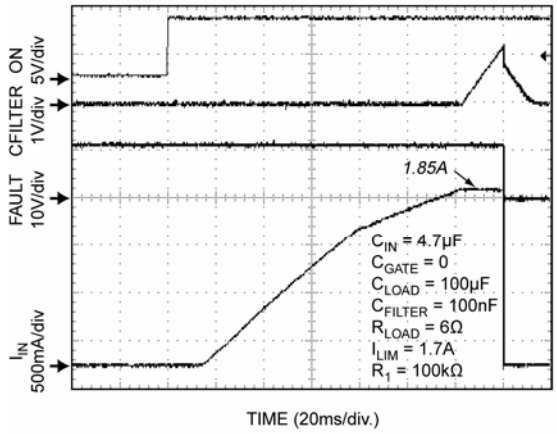


Inrush Current Response - V_{OUT} = 5V

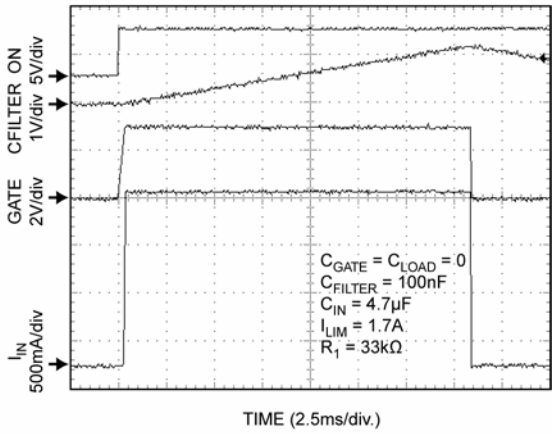


Functional Characteristics (See Figure 5, Applications Test Circuit)

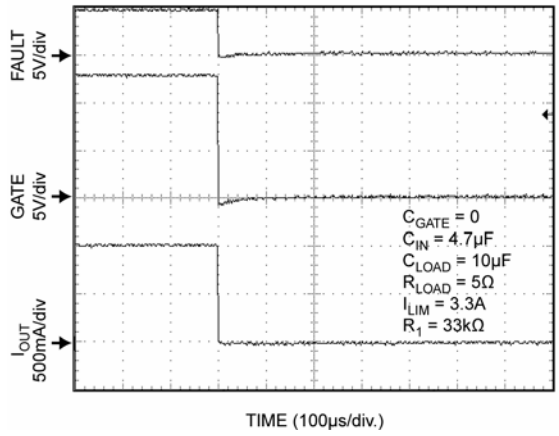
Turn On Into Heavy Load - V_{OUT} = 12V



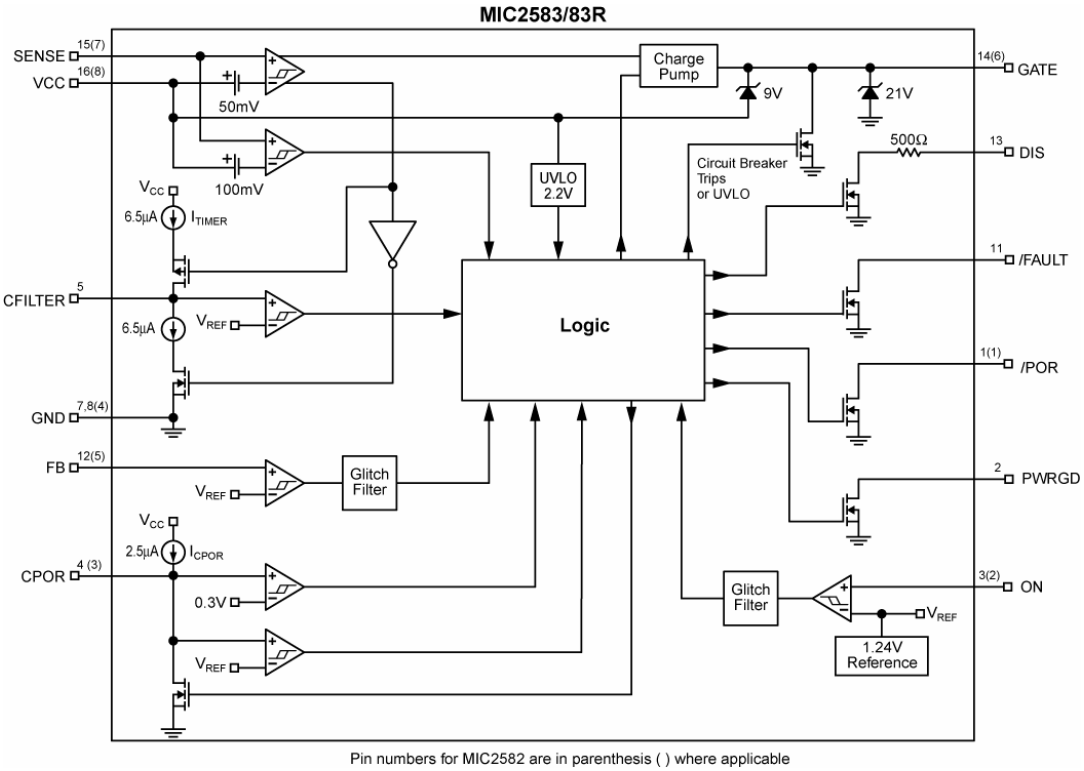
Turn On Into Short Circuit - V_{OUT} = 5V



Shutdown by Short Circuit - V_{OUT} = 5V
(MIC2583)



Functional Diagram



Functional Description

Hot Swap Insertion

When circuit boards are inserted into live system backplanes and supply voltages, high inrush currents can result due to the charging of bulk capacitance that resides across the supply pins of the circuit board. This inrush current, although transient in nature, may be high enough to cause permanent damage to on board components or may cause the system's supply voltages to go out of regulation during the transient period which may result in system failures. The MIC2582 and MIC2583 act as a controller for external N-Channel MOSFET devices in which the gate drive is controlled to provide inrush current limiting and output voltage slew rate control during hot plug insertions.

Power Supply

VCC is the supply input to the MIC2582/83 controller with a voltage range of 2.3V to 13.2V. The VCC input can withstand transient spikes up to 20V. In order to ensure stability of the supply voltage, a minimum 0.47µF capacitor from VCC to ground is recommended. Alternatively, a low pass filter, shown in the typical application circuit (see Figure 1), can be used to eliminate high frequency oscillations as well as help suppress transient spikes.

Also, due to the existence of an undetermined amount of parasitic inductance in the absence of bulk capacitance along the supply path, placing a Zener diode at the VCC of the controller to ground in order to provide external supply transient protection is strongly recommended for relatively high current applications (≥3A). See Figure 1.

Start-Up Cycle

Supply Contact Delay

During a hot insert of a PC board into a backplane or when the supply (VCC) is powered up, as the voltage at the ON pin rises above its threshold (1.24V typical), the MIC2582/83 first checks that both supply voltages are above their respective UVLO thresholds. If so, the device is enabled and an internal 2.5µA current source begins charging capacitor C_{POR} to 0.3V to initiate a start-up sequence. Once the start-up delay (t_{START}) elapses, the CPOR pin is pulled immediately to ground and a 17µA current source begins charging the GATE output to drive the external MOSFET that switches V_{IN} to V_{OUT}. The programmed contact start-up delay is calculated using the following equation:

$$t_{START} = C_{POR}\left[\frac{V_{START}}{I_{CPOR}}\right] \cong 0.12\,x\,C_{POR}\,(\mu F) \qquad (1)$$

Where the start-up delay timer threshold (V_{START}) is 0.3V, and the Power-On Reset timer current (I_{CPOR}) is 2.5µA. See Table 2 for some typical supply contact start-up delays using several standard value capacitors. As the GATE voltage continues ramping toward its final value (V_{CC} + V_{GS}) at a defined slew rate (See Load Capacitance/Gate Capacitance Dominated Startup sections), a second CPOR timing cycle begins if: 1)/FAULT is high and 2)CFILTER is low (i.e., not an overvoltage, undervoltage lockout, or overcurrent state). This second timing cycle (t_{POR}) begins when the voltage at the FB pin exceeds its threshold (V_{FB}). This condition indicates that the output voltage is valid. See Figure 3 in the Timing Diagrams. When the power supply is already present (i.e., not a "hot swapping" condition) and the MIC2582/83 device is enabled by applying a logic high signal at the ON pin, the GATE output begins ramping immediately as the first CPOR timing cycle is bypassed. Active current regulation is employed to limit the inrush current transient response during start-up by regulating the load current at the programmed current limit value (See Current Limiting and Dual-Level Circuit Breaker section). The following equation is used to determine the nominal current limit value:

$$I_{LIM} = \frac{V_{TRIPSLOW}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}} \qquad (2)$$

where $V_{TRIPSLOW}$ is the current limit slow trip threshold found in the electrical table and R_{SENSE} is the selected value that will set the desired current limit. There are two basic start-up modes for the MIC2582/83: 1) Start-up dominated by load capacitance and 2) start-up dominated by total gate capacitance. The magnitude of the inrush current delivered to the load will determine the dominant mode. If the inrush current is greater than the programmed current limit (I_{LIM}), then load capacitance is dominant. Otherwise, gate capacitance is dominant. The expected inrush current may be calculated using the following equation:

$$INRUSH \cong I_{GATE}\,x\,\frac{C_{LOAD}}{C_{GATE}} = 17\mu A\,x\,\frac{C_{LOAD}}{C_{GATE}} \qquad (3)$$

where I_{GATE} is the GATE pin pull-up current, C_{LOAD} is the load capacitance, and C_{GATE} is the total GATE capacitance (C_{ISS} of the external MOSFET and any external capacitor connected from the MIC2582/83 GATE pin to ground).

Load Capacitance Dominated Start-Up

In this case, the load capacitance (C_{LOAD}) is large enough to cause the inrush current to exceed the programmed current limit but is less than the fast-trip threshold (or the fast-trip threshold is disabled, 'M' option). During start-up under this condition, the load current is regulated at the programmed current limit value (I_{LIM}) and held constant until the output voltage rises to its final value. The output slew rate and equivalent GATE voltage slew rate is computed by the

following equation:

$$\text{Output Voltage Slew Rate, } dV_{OUT}/dt = \frac{I_{LIM}}{C_{LOAD}} \quad (4)$$

where I_{LIM} is the programmed current limit value. Consequently, the value of C_{FILTER} must be selected to ensure that the overcurrent response time, t_{OCSLOW}, exceeds the time needed for the output to reach its final value. For example, given a MOSFET with an input capacitance C_{ISS} = C_{GATE} = 4700pF, C_{LOAD} is 2200µF, and I_{LIM} is set to 6A with a 12V input, then the load capacitance dominates as determined by the calculated INRUSH > I_{LIM}. Therefore, the output voltage slew rate determined from Equation 4 is:

$$\text{Output Voltage Slew Rate, } dV_{OUT}/dt = \frac{6A}{2200\mu F} = 2.73\frac{V}{ms}$$

and the resulting t_{OCSLOW} needed to achieve a 12V output is approximately 4.5ms. (See Power-On Reset and Overcurrent Timer Delays section to calculate t_{OCSLOW}).

GATE Capacitance Dominated Start-Up

In this case, the value of the load capacitance relative to the GATE capacitance is small enough such that the load current during start-up never exceeds the current limit threshold as determined by Equation 3. The minimum value of C_{GATE} that will ensure that the current limit is never exceeded is given by the equation below:

$$C_{GATE}(\text{min}) = \frac{I_{GATE}}{I_{LIM}} \times C_{LOAD} \quad (5)$$

where C_{GATE} is the summation of the MOSFET input capacitance (C_{ISS}) and the value of the external capacitor connected to the GATE pin of the MIC2582/83 to ground. Once C_{GATE} is determined, use the following equation to determine the output slew rate for gate capacitance dominated start-up.

$$dV_{OUT}/dt = \frac{I_{GATE}}{C_{GATE}} \quad (6)$$

Table 1 depicts the output slew rate for various values of C_{GATE}.

I_{GATE} = 17µA	
C_{GATE}	**dV_{OUT}/dt**
0.001µF	17V/ms
0.01µF	1.7V/ms
0.1µF	0.17V/ms
1µF	0.017V/ms

Table 1. Output Slew Rate Selection for GATE Capacitance Dominated Start-Up

Current Limiting and Dual-Level Circuit Breaker

Many applications will require that the inrush and steady state supply current be limited at a specific value in order to protect critical components within the system. Connecting a sense resistor between the VCC and SENSE pins sets the nominal current limit value of the MIC2582/83 and the current limit is calculated using Equation 2.

The MIC2582/83 also features a dual-level circuit breaker triggered via 50mV and 100mV current-limit thresholds sensed across the VCC and SENSE pins. The first level of the circuit breaker functions as follows. For the MIC2583/83R, once the voltage sensed across these two pins exceeds 50mV, the overcurrent timer, its duration set by capacitor C_{FILTER}, starts to ramp the voltage at C_{FILTER} using a 6.5µA constant current source. If the voltage at C_{FILTER} reaches the overcurrent timer threshold (V_{TH}) of 1.24V, then C_{FILTER} immediately returns to ground as the circuit breaker trips and the GATE output is immediately shut down. The default overcurrent time period for the MIC2582/83 is 5µs. For the second level, if the voltage sensed across VCC and SENSE exceeds 100mV at any time, the circuit breaker trips and the GATE shuts down immediately, bypassing the overcurrent time period. The MIC2582-MYM option is equipped with only a single circuit breaker threshold (50mV). To disable current limit and circuit breaker operation, tie the SENSE and VCC pins together and the C_{FILTER} (MIC2583/83R) pin to ground.

Output Undervoltage Detection

The MIC2582/83 employ output undervoltage detection by monitoring the output voltage through a resistive divider connected at the FB pin. During turn on, while the voltage at the FB pin is below the threshold (V_{FB}), the /POR pin is asserted low.

Once the FB pin voltage crosses V_{FB}, a 2.5µA current source charges capacitor C_{POR}. Once the CPOR pin voltage reaches 1.24V, the time period t_{POR} elapses as the CPOR pin is pulled to ground and the /POR pin goes HIGH. If the voltage at FB drops below V_{FB} for more than 10µs, the /POR pin resets for at least one timing cycle defined by t_{POR} (See Applications Information for an example).

Power-On Reset and Overcurrent Timer Delays

The Power-On Reset delay, t_{POR}, is the time period for the /POR pin to go HIGH once the voltage at the FB pin exceeds the power-good threshold (V_{FB}). A capacitor connected to CPOR sets the interval and is determined by using Equation 1 with V_{TH} substituted for V_{START}. The resulting equation becomes:

$$t_{POR} = C_{POR} \times \frac{V_{TH}}{I_{CPOR}} \cong 0.5 \times C_{POR}\,(\mu F) \quad (7)$$

where the Power-On Reset threshold (V_{TH}) and timer

current (I_{CPOR}) are typically 1.24V and 2.5µA, respectively.

For the MIC2583/83R, a capacitor connected to CFILTER is used to set the timer which activates the circuit breaker during overcurrent conditions. When the voltage across the sense resistor exceeds the slow trip current limit threshold of 50mV, the overcurrent timer begins to charge for a time period (t_{OCSLOW}), determined by C_{FILTER}. When no capacitor is connected to CFILTER and for the MIC2582, t_{OCSLOW} defaults to 5µs. If t_{OCSLOW} elapses, then the circuit breaker is activated and the GATE output is immediately pulled to ground. For the MIC2583/83R, the following equation is used to determine the overcurrent timer period, t_{OCSLOW}.

$$t_{OCSLOW} = C_{FILTER} \times \frac{V_{TH}}{I_{TIMER}} \cong 0.19 \times C_{FILTER}\ (\mu F) \quad (8)$$

where V_{TH}, the CFILTER timer threshold, is 1.24V and I_{TIMER}, the overcurrent timer current, is 6.5µA. Tables 2 and 3 provide a quick reference for several timer calculations using select standard value capacitors.

C_{POR}	t_{START}	t_{POR}
0.01µF	1.2ms	5ms
0.02µF	2.4ms	10ms
0.033µF	4ms	16.5ms
0.05µF	6ms	25ms
0.1µF	12ms	50ms
0.33µF	40ms	165ms
0.47µF	56ms	235ms
1µF	120ms	500ms

Table 2. Selected Power-On Reset and Start-Up Delays

C_{FILTER}	t_{OCSLOW}
680pF	130µs
2200pF	420µs
4700pF	900µs
8200pF	1.5ms
0.033µF	6ms
0.1µF	19ms
0.22µF	42ms
0.47µF	90ms

Table 3. Selected Overcurrent Timer Delays

Application Information

Design Consideration for Output Undervoltage Detection

For output undervoltage detection, the first consideration is to establish the output voltage level that indicates "power is good." For this example, the output value for which a 12V supply will signal "good" is 11V. Next, consider the tolerances of the input supply and FB threshold (V_{FB}). For this example, the 12V supply varies ±5%, thus the resulting output voltage may be as low as 11.4V and as high as 12.6V. Additionally, the FB threshold has ±50mV tolerance and may be as low as 1.19V and as high as 1.29V. Thus, to determine the values of the resistive divider network (R5 and R6) at the FB pin, shown in the typical application circuit on page 1, use the following iterative design procedure.

1) Choose R6 to allow 100µA or more in the FB resistive divider branch.

$$R6 = \frac{V_{FB(MAX)}}{100\mu A} = \frac{1.29V}{100\mu A} = 12.9k\Omega$$

R6 is chosen as 12.4kΩ ±1%.

2) Next, determine R5 using the output "good" voltage of 11V and the following equation:

$$V_{OUT(Good)} = V_{FB}\left[\frac{(R5 + R6)}{R6}\right] \quad (9)$$

Using some basic algebra and simplifying Equation 9 to isolate R5, yields:

$$R5 = R6\left[\left(\frac{V_{OUT(Good)}}{V_{FB(MAX)}}\right) - 1\right] \quad (9.1)$$

where $V_{FB(MAX)}$ = 1.29V, $V_{OUT(Good)}$ = 11V, and R6 is 12.4kΩ. Substituting these values into Equation 9.1 now yields R5 = 93.33kΩ. A standard 93.1kΩ ±1% is selected.

Now, consider the 11.4V minimum output voltage, the lower tolerance for R6 and higher tolerance for R5, 12.28kΩ and 94.03kΩ, respectively. With only 11.4V available, the voltage sensed at the FB pin exceeds $V_{FB(MAX)}$, thus the /POR and PWRGD (MIC2583/83R) signals will transition from LOW to HIGH, indicating "power is good" given the worse case tolerances of this example. Lastly, in giving consideration to the leakage current associated with the FB input, it is recommended to either: 1) provide ample design margin (20mV to 30mV) to allow for loss in the potential (ΔV) at the FB pin, or 2) allow >>100µA to flow in the FB resistor network.

PCB Connection Sense

There are several configuration options for the MIC2582/83's ON pin to detect if the PCB has been fully seated in the backplane before initiating a start-up cycle. In the typical applications circuit, the MIC2582/83 is mounted on the PCB with a resistive divider network connected to the ON pin. R2 is connected to a short pin on the PCB edge connector. Until the connectors mate, the ON pin is held low which keeps the GATE output charge pump off. Once the connectors mate, the resistor network is pulled up to the input supply,

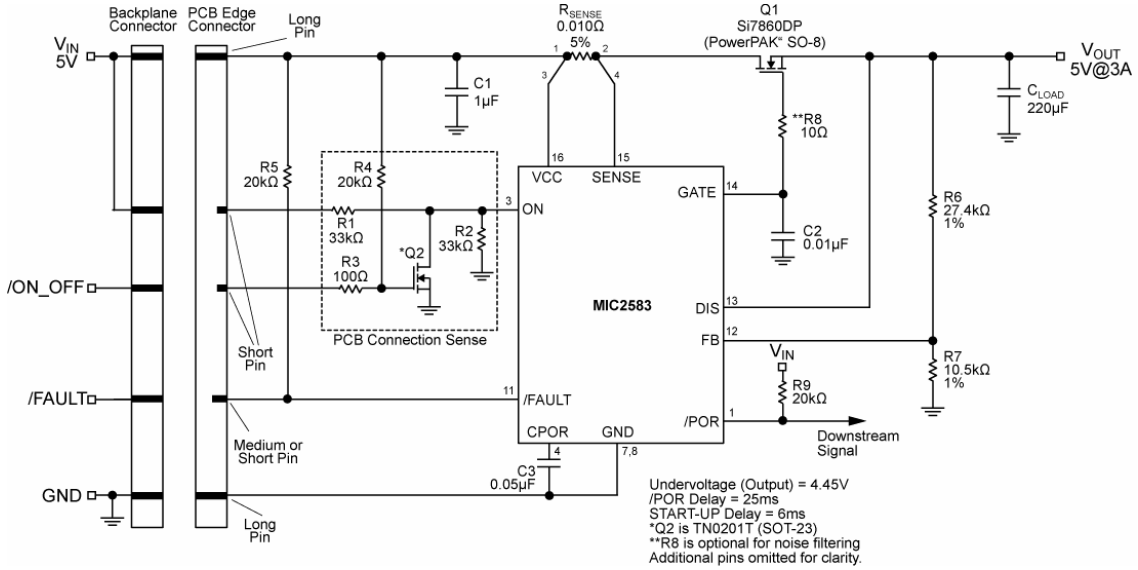


Figure 6. PCB Connection Sense with ON/OFF Control

12V in this example, and the ON pin voltage exceeds its threshold (VON) of 1.24V and the MIC2582/83 initiates a start-up cycle. In Figure 6, the connection sense consisting of a discrete logic-level MOSFET and a few resistors allows for interrupt control from the processor or other signal controller to shut off the output of the MIC2582/83. R4 pulls the GATE of Q2 to V_{IN} and the ON pin is held low until the connectors are fully mated.

Once the connectors fully mate, a logic LOW at the /ON_OFF signal turns Q2 off and allows the ON pin to pull up above its threshold and initiate a start-up cycle. Applying a logic HIGH at the /ON_OFF signal will turn Q2 on and short the ON pin of the MIC2582/83 to ground which turns off the GATE output charge pump.

Higher UVLO Setting

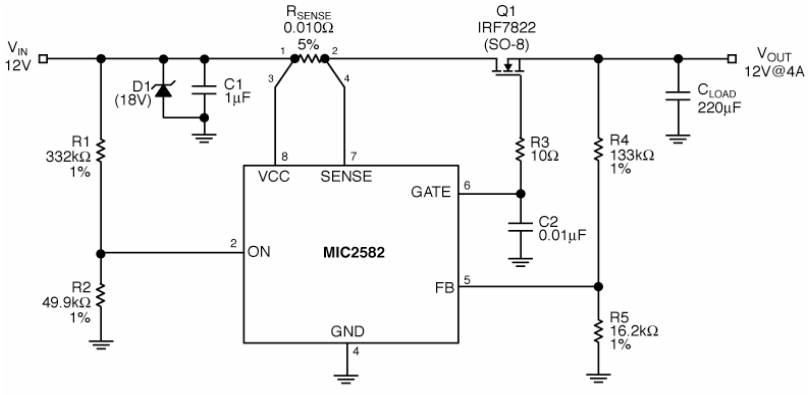
Once a PCB is inserted into a backplane (power supply), the internal UVLO circuit of the MIC2582/83 holds the GATE output charge pump off until VCC exceeds 2.2V. If VCC falls below 2.1V, the UVLO circuit pulls the GATE output to ground and clears the overvoltage and/or current limit faults. A typical 12V application, for example, should implement a higher UVLO than the internal 2.1V threshold of MIC2582 to avoid delivering power to downstream modules/loads while the input is below tolerance. For a higher UVLO threshold, the circuit in Figure 7 can be used to delay the output MOSFET from switching on until the desired input voltage is achieved. The circuit allows the charge pump to remain off until V_{IN} exceeds $\left(1+\frac{R1}{R2}\right)\times 1.24V$. The GATE drive output will be shut down when V_{IN} falls below $\left(1+\frac{R1}{R2}\right)\times 1.19V$. In the example circuit (Figure 7), the rising UVLO threshold is set at approximately 9.5V and the falling UVLO threshold is established as 9.1V. The circuit consists of an external resistor divider at the ON pin that keeps the GATE output charge pump off until the voltage at the ON pin exceeds its threshold (V_{ON}) and after the start-up timer elapses.

5V Switch with 3.3V Supply Generation

The MIC2582/83 can be configured to switch a primary supply while generating a secondary regulated voltage rail. The circuit in Figure 8 enables the MIC2582 to switch a 5V supply while also providing a 3.3V low dropout regulated supply with only a few added external components. Upon enabling the MIC2582, the GATE output voltage increases and thus the 3.3V supply also begins to ramp. As the 3.3V output supply crosses 3.3V, the FB pin threshold is also exceeded which triggers the power-on reset comparator. The /POR pin goes HIGH, turning on transistor Q3 which lowers the voltage on the gate of MOSFET Q2. The result is a regulated 3.3V supply with the gate feedback loop of Q2 compensated by capacitor C3 and resistors R4 and R5. For MOSFET Q2, special consideration must be given to the power dissipation capability of the selected MOSFET as 1.5V to 2V will drop across the device during normal operation in this application. Therefore, the device is susceptible to overheating dependent upon the current requirements for the regulated output. In this example, the power dissipated by Q2 is approximately = 1W. However, a substantial amount of power will be generated with higher current requirements and/or conditions. As a general guideline, expect the ambient temperature within the power supply box to exceed the maximum operating ambient temperature of the system environment by approximately 20ºC. Given the MOSFET's $R_{\theta(JA)}$ and the expected power dissipated by the MOSFET, an approximation for the junction temperature at which the device will operate is obtained as follows:

$$T_J = (P_D \times R_{\theta(JA)}) + T_A \qquad (10)$$

where $T_A = T_{A\ (MAX\ OPERATING)} + 20ºC$. As a precaution, the implementation of additional copper heat sinking is highly recommended for the area under/around the MOSFET.



Undervoltage Lockout Threshold (rising) = 9.5V
Undervoltage Lockout Threshold (falling) = 9.1V
Undervoltage (Output) = 11.4V
Additional pins omitted for clarity.

Figure 7. Higher UVLO Setting

For additional information on MOSFET thermal considerations, please see MOSFET Selection text and subsequent sections.

Auto-Restart - MIC2583R

The MIC2583R provides an auto-restart function. Upon an overcurrent fault condition such as a short circuit, the MIC2583R initially shuts off the GATE output. The MIC2583R attempts to restart with a 12µA charge current at a preset 10% duty cycle until the fault condition is removed. The interval between auto-retry attempts is set by capacitor C_{FILTER}.

Sense Resistor Selection

The MIC2582 and MIC2583 use a low-value sense resistor to measure the current flowing through the MOSFET switch (and therefore the load). This sense resistor is nominally set at 50mV/$I_{LOAD(CONT)}$. To accommodate worst-case tolerances for both the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (i.e., the "trip point") for the MIC2582/83 may be as low as 42mV, which would equate to a sense resistor value of 42mV/$I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields:

$$R_{SENSE(MAX)} = \frac{42mV}{(1.03)(I_{LOAD(CONT)})} = \frac{40.8mV}{I_{LOAD(CONT)}} \quad (11)$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance buildup in the opposite direction. Here, the worst-case maximum current is found using a 59mV trip voltage and a sense resistor that is 3% low in value. The resulting equation is:

$$I_{LOAD(CONT,MAX)} = \frac{59mV}{(0.97)(R_{SENSE(NOM)})} = \frac{60.8mV}{R_{SENSE(NOM)}} \quad (12)$$

As an example, if an output must carry a continuous 2A without nuisance trips occurring, Equation 11 yields: $R_{SENSE(MAX)} = \frac{40.8mV}{2A} = 20.4m\Omega$. The next lowest standard value is 20mΩ. At the other set of tolerance extremes for the output in question,

$I_{LOAD(CONT,MAX)} = \frac{60.8mV}{20.0m\Omega} = 3.04A$, approximately 3A.

Knowing this final data, we can determine the necessary wattage of the sense resistor using $P = I^2R$, where I will be $I_{LOAD(CONT, MAX)}$, and R will be $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following: $P_{MAX} = (3A)^2 (19.4m\Omega) = 0.175W$.
In this example, a ¼W sense resistor is sufficient.

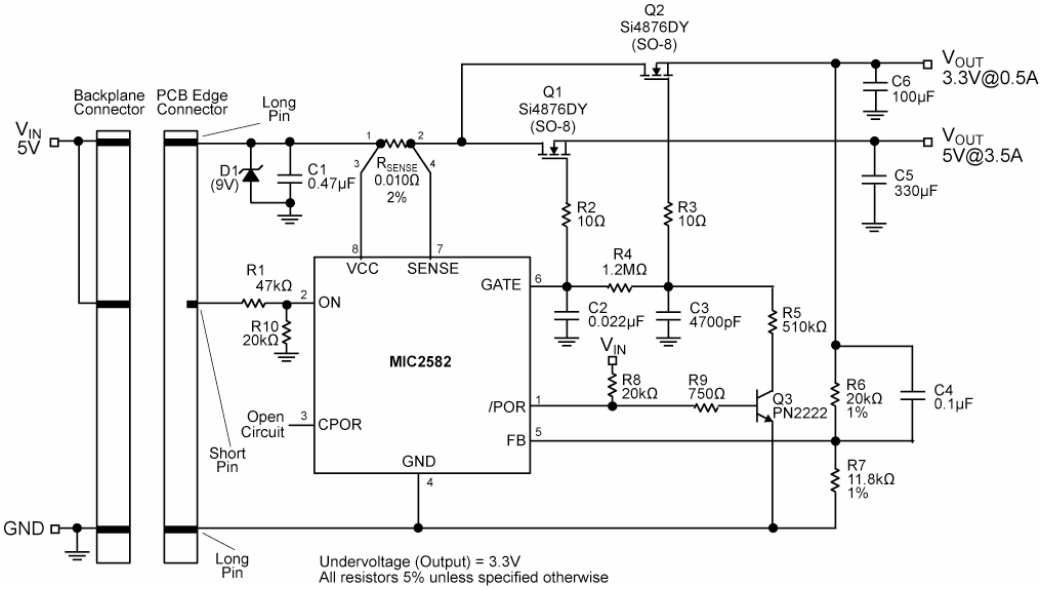


Figure 8. 5V Switch/3.3V LDO Application

MOSFET Selection

Selecting the proper external MOSFET for use with the MIC2582/83 involves three straightforward tasks:

- Choice of a MOSFET which meets minimum voltage requirements.
- Selection of a device to handle the maximum continuous current (steady-state thermal issues).
- Verify the selected part's ability to withstand any peak currents (transient thermal issues).

MOSFET Voltage Requirements

The first voltage requirement for the MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$. For instance, a 12V input may reasonably be expected to see high-frequency transients as high as 18V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 19V. For ample safety margin and standard availability, the closest value will be 20V.

The second breakdown voltage criterion that must be met is a bit subtler than simple drain-source breakdown voltage, but is not hard to meet. In MIC2582/83 applications, the gate of the external MOSFET is driven up to approximately 19.5V by the internal output MOSFET (again, assuming 12V operation).

At the same time, if the output of the external MOSFET (its source) is suddenly subjected to a short, the gate-source voltage will go to (19.5V – 0V) = 19.5V. This means that the external MOSFET must be chosen to have a gate-source breakdown voltage of 20V or more, which is an available standard maximum value. However, if operation is at or above 13V, the 20V gate-source maximum will likely be exceeded. As a result, an external Zener diode clamp should be used to prevent breakdown of the external MOSFET when operating at voltages above 8V. A Zener diode with 10V rating is recommended as shown in Figure 9. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher.

As a general tip, choose surface-mount devices with a drain-source rating of 30V as a starting point.

Finally, the external gate drive of the MIC2582/83 requires a low-voltage logic level MOSFET when operating at voltages lower than 3V. There are 2.5V logic level MOSFETs available. Please see Table 4 "MOSFET and Sense Resistor Vendors" for suggested manufacturers.

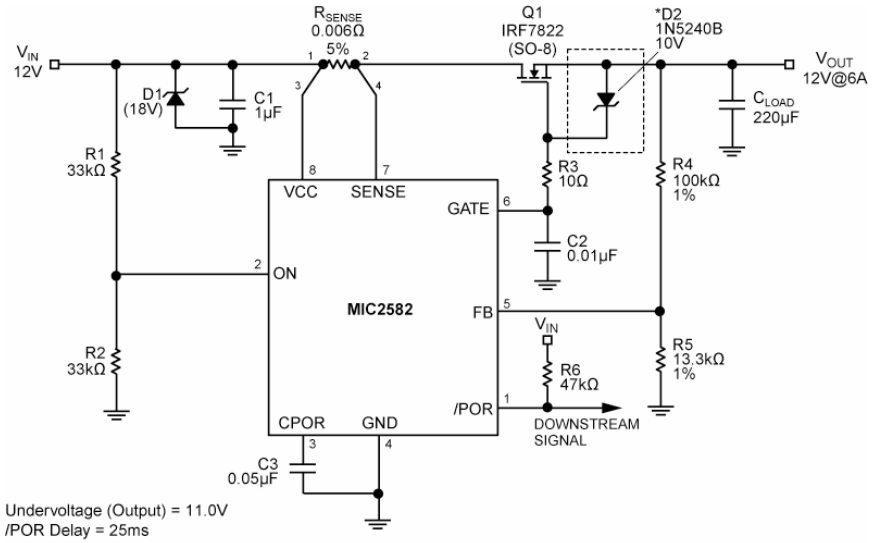


Figure 9. Zener Clamped MOSFET Gate

MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT,\ MAX.)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., can heat be dissipated into the ground plane or power plane, if using a surface-mount part? Is any airflow available?).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on-resistance of the part with 8V of enhancement.

Call this value R_{ON}. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady-state power dissipation is to calculate I^2R.

The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per ºC rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10mΩ at a T_J = 25ºC, and the actual junction temperature ends up at 110ºC, a good first cut at the operating value for R_{ON} would be:

$$R_{ON} \cong 10m\Omega\left[1+(110-25)(0.005)\right] \cong 14.3m\Omega \qquad (13)$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in ºC/W) as that with which the MOSFETs performance was specified by the manufacturer. Here are a few practical tips:

1. The heat from a surface-mount device such as an SOIC-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
2. Airflow works. Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially.

   If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.
3. The best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFETs temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and the worse case continuous I^2R power dissipation which it will see, it remains only to verify the MOSFETs ability to handle short-term overload power dissipation without overheating. A MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance," or $Z_{\theta(JA)}$. Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the following case: V_{IN} = 12V, t_{OCSLOW} has been set to 100msec, $I_{LOAD(CONT.\ MAX)}$ is 2.5A, the slow-trip threshold is 50mV nominal, and the fast-trip threshold is 100mV. If the output is accidentally connected to a 3Ω load, the output current from the MOSFET will be regulated to 2.5A for 100ms (t_{OCSLOW}) before the part trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I;\ E_{MOSFET} = [12V-(2.5A)(3\Omega)] = 4.5V$$

$$P_{MOSFET} = (4.5V \times 2.5A) = 11.25W \text{ for } 100msec.$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal impedance curves become very useful. Figure 10 shows the curve for the Vishay (Siliconix) Si4410DY, a commonly used SOIC-8 power MOSFET.

Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time– 10 minutes or more– before the fault is isolated and the channel is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1sec (=100msec), we see that the $Z_{\theta(JA)}$ of this MOSFET to a highly infrequent event of this duration is only 8% of its continuous $R_{\theta(JA)}$.

This particular part is specified as having an $R_{\theta(JA)}$ of 50°C/W for intervals of 10 seconds or less.

Thus:

Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from our previous approximation hint, the part has an R_{ON} of (0.0335/2) = 17mΩ at 25°C.

Assume it has been carrying just about 2.5A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting temperature, and find the operating junction temperature increase (ΔT_J) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and ΔT_J. Since this is not a closed-form equation, getting a close approximation may take one or two iterations, and the calculation tends to converge quickly.

Then the starting (steady-state) T_J is:

$$T_J \cong T_{A(MAX)} + \Delta T_J$$

$$\cong T_{A(MAX)} + [R_{ON} + T_{A(MAX)} - T_A)(0.005/^oC)(R_{ON})] \times I^2 \times R_{\theta(JA)}$$

$$T_J \cong 55^oC + [17m\Omega + (55^oC\text{-}25^oC)(0.005)(17m\Omega)] \times (2.5A)^2 \times (50^oC/W)$$

$$T_J \cong (55^oC + (0.122W)(50^oC/W)$$

$$\cong 61.1^oC$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with T_J equal to the already calculated value of 61.1°C:

$$T_J \cong T_A + [17m\Omega + (61.1^oC\text{-}25^oC)(0.005)(17m\Omega)] \times (2.5A)^2 \times (50^oC/W)$$

$$T_J \cong (55^oC + (0.125W)(50^oC/W) \cong 61.27^oC$$

So our original approximation of 61.1ºC was very close to the correct value. We will use T_J = 61ºC.

Finally, add the temperature increase due to the maximum power dissipation calculated from a “single event”, (11.25W)(50ºC/W)(0.08) = 45ºC to the steady-state T_J to get $T_{J(TRANSIENT\ MAX.)}$ = 106ºC. This is an acceptable maximum junction temperature for this part.

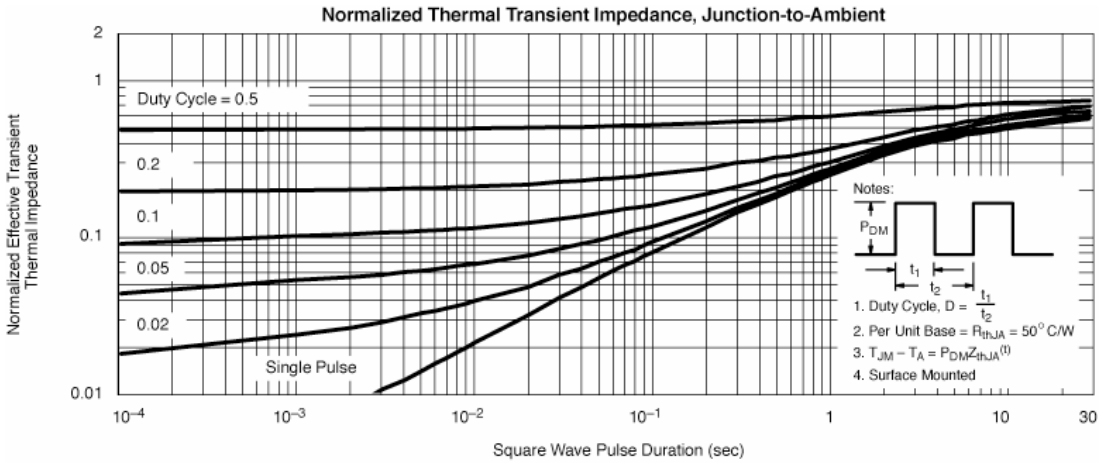


Figure 10. Transient Thermal Impedance

PCB Layout Considerations

Because of the low values of the sense resistors used with the MIC2582/83 controllers, special attention to the layout must be used in order for the device's circuit breaker function to operate properly. Specifically, the use of a 4-wire Kelvin connection to accurately measure the voltage across R_{SENSE} is highly recommended. Kelvin sensing is simply a means of making sure that any voltage drops in the power traces connecting to the resistors does not get picked up by the traces themselves. Additionally, these Kelvin connections should be isolated from all other signal traces to avoid introducing noise onto these sensitive nodes. Figure 11 illustrates a recommended, single layer layout for the R_{SENSE}, Power MOSFET, timer(s), and feedback network connections. The feedback network resistor values are selected for a 12V application. Many hot swap applications will require load currents of several amperes. Therefore, the power (V_{CC} and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1oz. or 2oz.) is kept to a maximum of 10ºC~25ºC. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load.

Finally, the use of plated-through vias will be needed to make circuit connections to power and ground planes when utilizing multi-layer PC boards.

MOSFET and Sense Resistor Vendors

Device types and manufacturer contact information for power MOSFETs and sense resistors are provided in Table 4. Some of the recommended MOSFETs include a metal heat sink on the bottom side of the package. The recommended trace for the MOSFET Gate of Figure 11 must be redirected when using MOSFETs packaged in this style. Contact the device manufacturer for package information.

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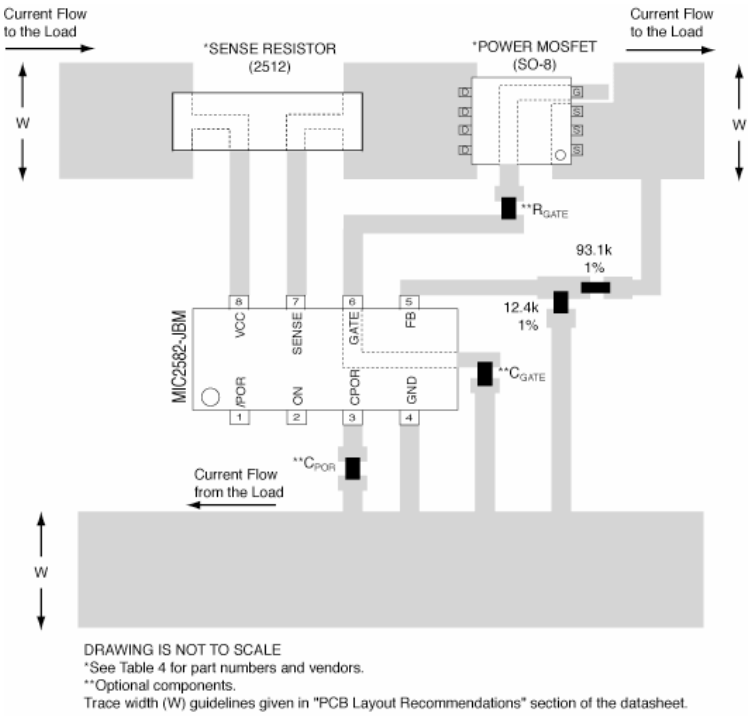


Figure 11. Recommended PCB Layout for Sense Resistor, Power MOSFET, and Feedback Network

MOSFET Vendor	Key MOSFET Type(s)	Applications[1]	Contact Information
Vishay (Siliconix)	Si4420DY (SOIC-8) package Si4442DY (SOIC-8) package Si4876DY (SOIC-8) package Si7892DY (PowerPAK™ SOIC-8)	$I_{OUT} \leq 10A$ I_{OUT} = 10-15A, $V_{CC} < 3V$ $I_{OUT} \leq 5A$, $V_{CC} \leq 5V$ $I_{OUT} \leq 15A$	www.siliconix.com (203) 452-5664
International Rectifier	IRF7413 (SOIC-8 package) IRF7457 (SOIC-8 package) IRF7601 (SOIC-8 package)	$I_{OUT} \leq 10A$ I_{OUT} = 10-15A $I_{OUT} \leq 5A$, $V_{CC} \leq 3V$	www.irf.com (310) 322-3331
Fairchild Semiconductor	FDS6680A (SOIC-8 package)	$I_{OUT} \leq 10A$	www.fairchildsemi.com (207) 775-8100
Philips	PH3230 (SOT669-LFPAK)	$I_{OUT} \geq 20A$	www.philips.com
Hitachi	HAT2099H (LFPAK)	$I_{OUT} \geq 20A$	www.halsp.hitachi.com (408) 433-1990

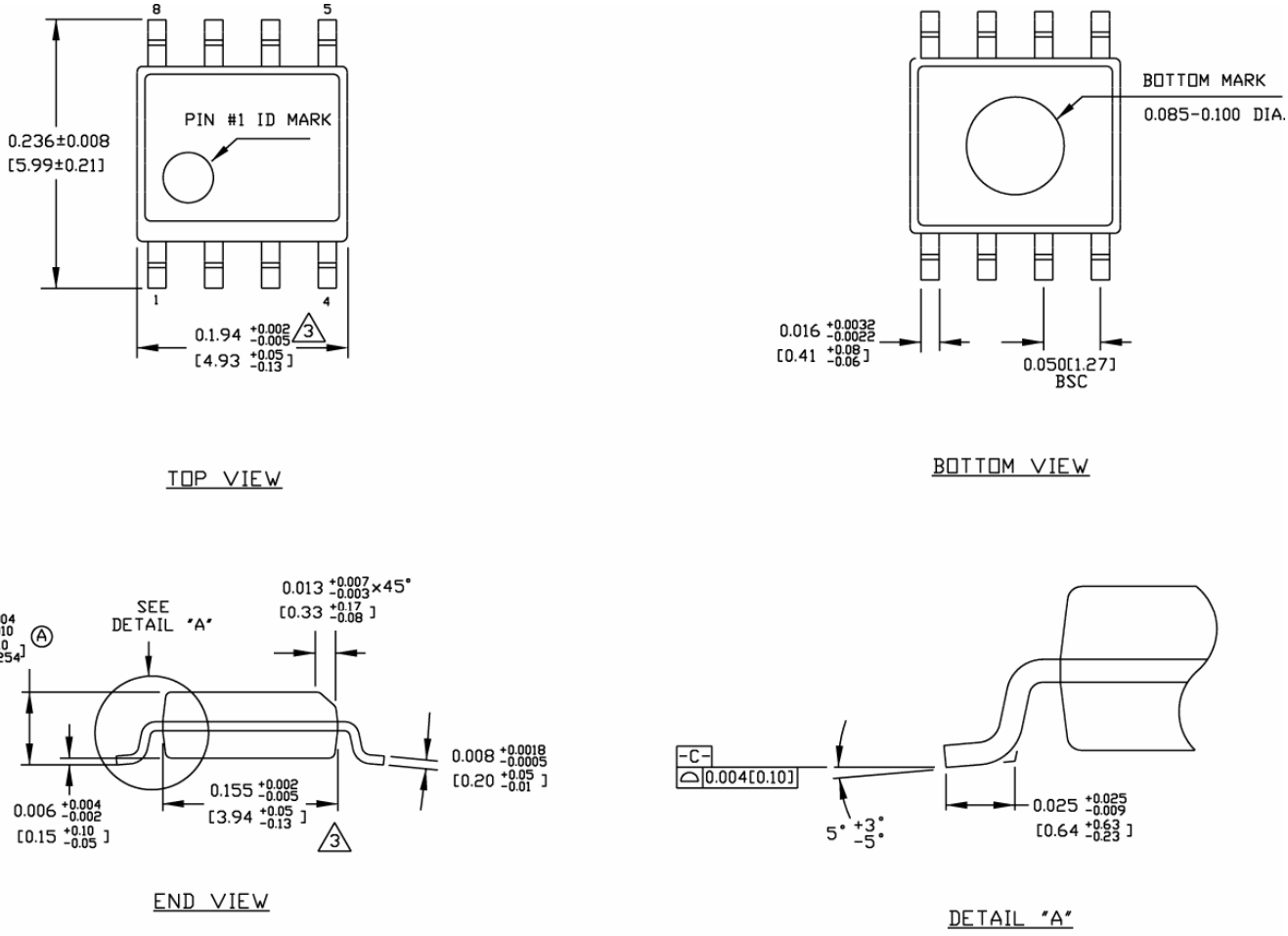
Note:

1. These devices are not limited to these conditions in many cases, but these conditions are provided as a helpful reference for customer applications.

Resistor Vendors	Sense Resistors	Contact Information
Vishay (Dale)	“WSL” Series	www.vishay.com/docswsl_30100.pdf (203) 452-5664
IRC	“OARS” Series ”LR” Series (second source to “WSL”)	www.irctt.com/pdf_files/OARS.pdf www.irctt.com/pdf_files/LRC.pdf (828) 264-8861

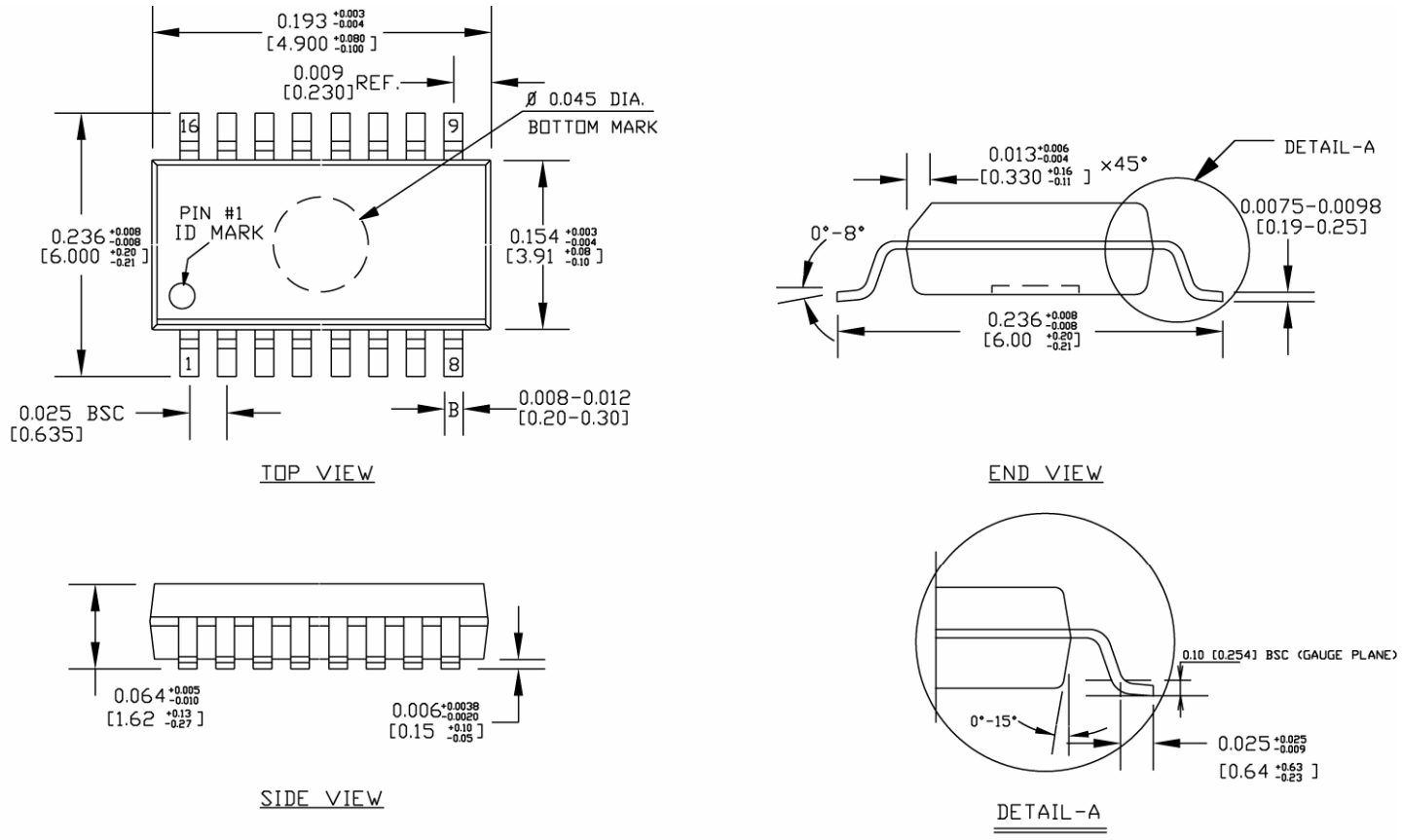
Table 4. MOSFET and Sense Resistor Vendors

Package Information



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)



NOTE:

1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

16-Pin QSOP (QS)

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