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## LCD MODULE SPECIFICATION FOR CUSTOMER'S APPROVAL

CUSTOMER : Standard

MODULE TYPE : MTC-S40400XRYHS

APPROVED BY: (FOR CUSTOMER USE ONLY)

Approved By	Checked By	Prepared By	MT File No	Date Issued

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# FEATURES of LIQUID CRYSTAL DISPLAY MODULE

**MODEL NO. : MTC-S40400XRYHS**

Character Type Dot Matrix LCD Module

Easy interface of 4-bit or 8-bit

Display character pattern : 5 × 7 font with cursor(208 kinds)

The special character pattern can be programmable by Character Generator RAM directly.

A customer character pattern can be programmable by mask option.

Automatically power on reset.

Internal Memory:

- Character Generator ROM (CGROM) : 10,080 bits (204 characters × 5 × 8 dot)

- Character Generator RAM (CGRAM) : 64 × 8 bits (8 characters × 5 × 8 dot)

Low power operation:

- Power supply voltage range : 2.7 ~ 5.5 V ( $V_{DD}$ )

- LCD drive voltage range : 3.0 ~ 13.0 V ( $V_{DD} - V_o$ )

Low power consumption

CMOS process

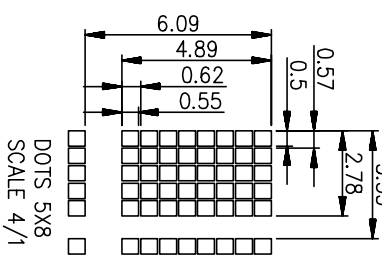
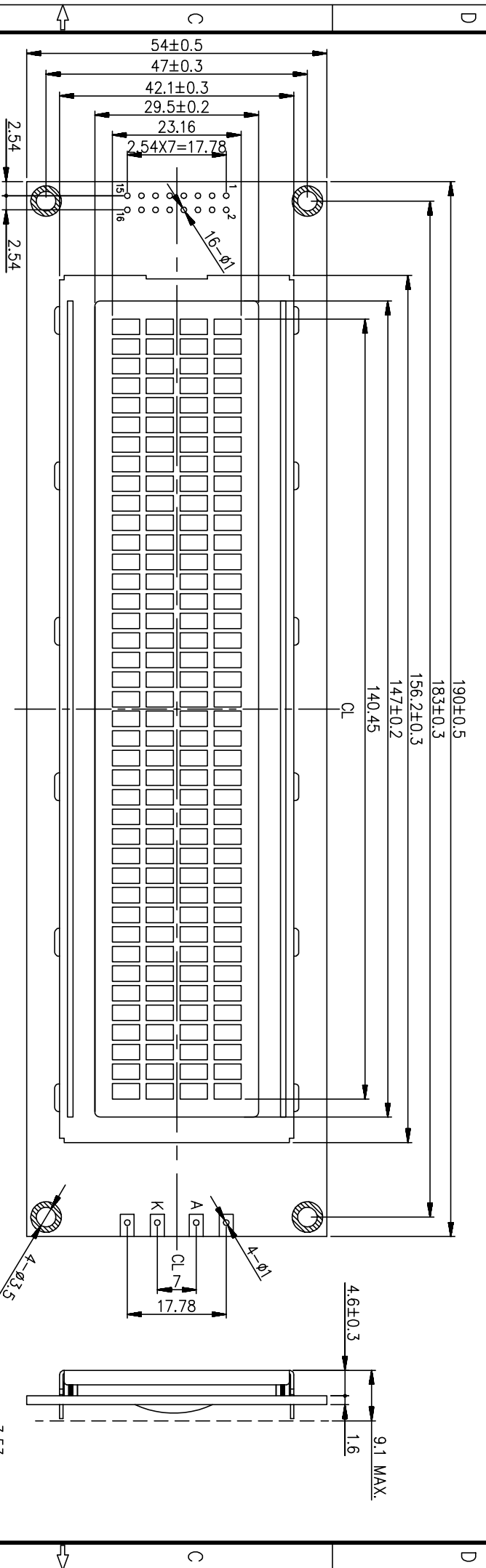
Duty-cycle : 1/16

View Direction	<input checked="" type="checkbox"/> 6 O'clock		<input type="checkbox"/> 12 O'clock		
LCD Type	<input type="checkbox"/> FSTN Positive		<input type="checkbox"/> FSTN Negative		
	<input type="checkbox"/> STN Gray	<input checked="" type="checkbox"/> STN Yellow Green		<input type="checkbox"/> STN Blue	
Rear Polarizer	<input checked="" type="checkbox"/> Reflective		<input type="checkbox"/> Transflective		<input type="checkbox"/> Transmissive
Backlight Type	<input type="checkbox"/> LED	<input type="checkbox"/> Internal Power		<input type="checkbox"/> EL	
		<input type="checkbox"/> External Power		<input type="checkbox"/> CCFL	
Backlight Color	<input type="checkbox"/> White	<input type="checkbox"/> Amber	<input type="checkbox"/> Blue Green	<input checked="" type="checkbox"/> Yellow Green	<input type="checkbox"/> Other
	<input type="checkbox"/> Normal		<input checked="" type="checkbox"/> Wide		<input type="checkbox"/> Super Wide
CCFL Inverter	<input type="checkbox"/> Build-in		<input checked="" type="checkbox"/> Not Build-in		
EL Driver IC	<input type="checkbox"/> Build-in		<input checked="" type="checkbox"/> Not Build-in		
Touch Screen	<input type="checkbox"/> With		<input checked="" type="checkbox"/> Without		

## TO BE VERY CAREFUL !

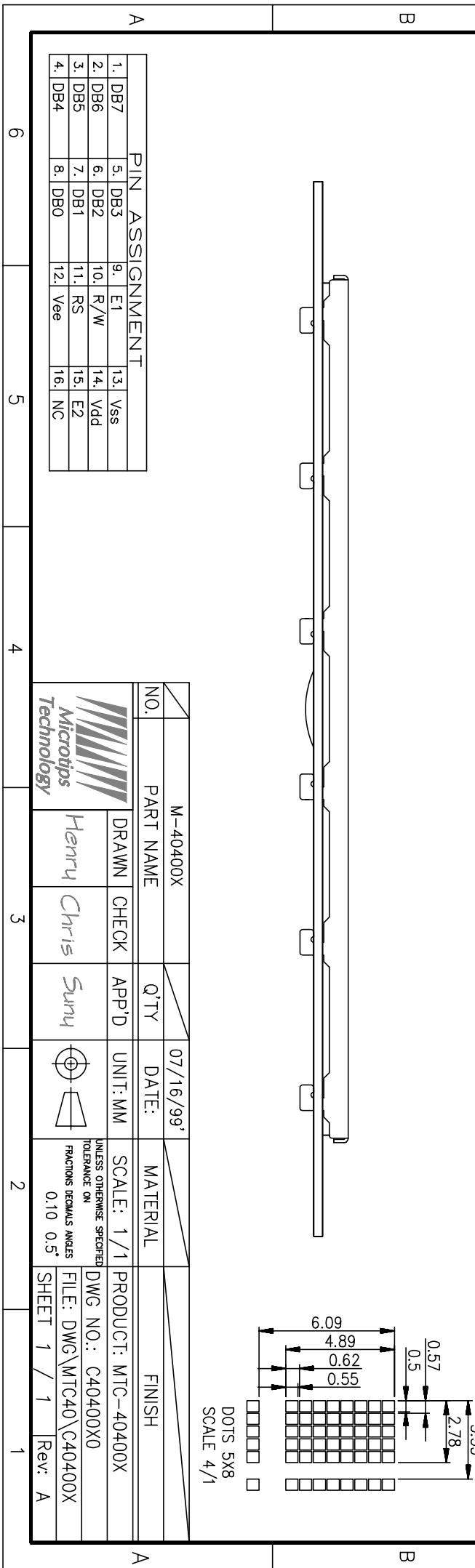
The LCD driver ICs are made of CMOS process, which is very easy to be damaged by static charge, make sure the user is grounded when handling the LCM.

REV.	DESCRIPTION	DRAWN	CHECK	APP'D	DATE



PIN ASSIGNMENT											
1.	DB7	5.	DB3	9.	E1	13.	VSS	17.	DB7	21.	E1
2.	DB6	6.	DB2	10.	R/W	14.	VDD	18.	DB6	22.	R/W
3.	DB5	7.	DB1	11.	RS	15.	E2	19.	DB5	23.	RS
4.	DB4	8.	DB0	12.	Vee	16.	NC	20.	DB4	24.	Vee

NO.	M-40400X		Q'TY	DATE:	MATERIAL		FINISH
PART NAME	DRAWN		APP'D	UNIT:MM	SCALE: 1/1		PRODUCT: MTC-40400X
		Henry	Chris		<small>UNLESS OTHERWISE SPECIFIED TOLERANCE ON FRACTIONS DECIMALS ANGLES</small> 0.10 0.5°		DWG NO.: C40400X0
		Sunny		07/16/99'	<small>UNLESS OTHERWISE SPECIFIED TOLERANCE ON FRACTIONS DECIMALS ANGLES</small> 0.10 0.5°		FILE: DWG\MTC40\C40400X
		Henry	Chris		<small>UNLESS OTHERWISE SPECIFIED TOLERANCE ON FRACTIONS DECIMALS ANGLES</small> 0.10 0.5°		SHEET 1 / 1
		Sunny		07/16/99'	<small>UNLESS OTHERWISE SPECIFIED TOLERANCE ON FRACTIONS DECIMALS ANGLES</small> 0.10 0.5°		Rev: A



## GENERAL SPECIFICATION

Item	Content
Display Resolution	40 Characters× 4 lines
Dimensional Outline(mm)	190.0(W)× 54.0(H)× 9.1 max(D)
Display mode	Reflective/ Positive Type
Circuit	Controller IC, Segment-driver IC
Interface	Data (DB0~DB7), RS, R/W, E1, E2

## ABSOLUTE MAXIMUM RATING

### (1) Electrical Absolute Ratings

Item	Symbol	Min.	Max.	Unit	Note
Power Supply for Logic	$V_{DD}-V_{SS}$	-0.3	7.0	Volt	
Power Supply for LCD	$V_{DD}-V_O$	0	15.0	Volt	
Input Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	Volt	

Note: Operator should be grounded during handling LCM.

### (2) Environmental Absolute Maximum Ratings

Item	Normal Temperature				Wide Temperature			
	Operating		Storage		Operating		Storage	
	Max,	Min.	Max,	Min.	Max,	Min.	Max,	Min.
Ambient Temperature	0°C	+50°C	-20°C	+70°C	-20°C	+60°C	-30°C	+70°C
Humidity(without condensation)	Note 2,4		Note 3,5		Note 4,5		Note 4,6	

Note 2  $T_a \leq 50^\circ\text{C}$ : 80% RH max

$T_a > 50^\circ\text{C}$ : Absolute humidity must be lower than the humidity of 85%RH at 50°C

Note 3  $T_a$  at  $-20^\circ\text{C}$  will be <48hrs at  $70^\circ\text{C}$  will be <120hrs when humidity is higher than 70%.

Note 4 Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 5  $T_a \leq 70^\circ\text{C}$ : 75RH max

$T_a > 70^\circ\text{C}$ : absolute humidity must be lower than the humidity of 75%RH at 70°C

Note 6  $T_a$  at  $-30^\circ\text{C}$  will be <48hrs, at  $80^\circ\text{C}$  will be <120hrs when humidity is higher than 70%.

## ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	note
Power Supply for Logic	$V_{DD}-V_{SS}$	-	2.7	4.5	5.5	Volt	
Input Voltage	$V_{IL}$	L level	$V_{SS}$	$0.2 V_{DD}$	-	Volt	
	$V_{IH}$	H level	$0.8 V_{DD}$	$V_{DD}$	-	Volt	
LCM Recommend LCD Module Driving Voltage	$V_{DD}=5.0V$	Ta=-20°C	-	-	-	Volt	
		Ta=0°C	-	-	-		
		Ta=25°C	3.8	4.05	4.3		
		Ta=50°C	-	-	-		
Power Supply Current for LCM	$I_{DD}$ (B/L OFF)	$V_{DD}=5.0V$ $V_{DD}-V_o=4.05V$ Ta=25°C	-	2.8	4.0	mA	
	$I_{LED}$	$V_{LED}=4.2V$	-	140	200		

## OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Viewing angle range	$\Phi f$ (12 o'clock)	When Cr $\geq 2$	-	40	-	Degree	9,10
	$\Phi b$ (6 o'clock)		-	50	-		
	$\Phi l$ (9 o'clock)		-	40	-		
	$\Phi r$ (3 o'clock)		-	40	-		
Rise Time	$T_r$	$V_{DD}-V_o=4.05V$ Ta=25°C		67	80	mS	
Fall Time	$T_f$			150	200		
Contrast	Cr		-	6.32	-		

## MECHANICAL SPECIFICATION

Product No.		MTC-S40400XRYHS
Module Size		190.0(W)mm× 54.0(H)mm× 9.1(D)mm Max
Display Format		40 characters× 4 lines
Character Size		2.78 mm× 4.89 mm
Character Pitch		3.53 mm× 6.09 mm
Dot Size		0.50(W)mm× 0.55(H)mm
Dot Pitch		0.57(W)mm× 0.62(H)mm
Duty Ratio		1/16 Duty
Character Font Table		<input checked="" type="checkbox"/> English <input type="checkbox"/> European <input type="checkbox"/> Other_____
LCD Display Mode	STN	<input type="checkbox"/> Gray Mode <input checked="" type="checkbox"/> Yellow Mode <input type="checkbox"/> Blue Mode
	FSTN	<input type="checkbox"/> Black & White(Normally White/Positive Image) <input type="checkbox"/> Black & White(Normally White/Negative Image)
	Rear Polarizer:	<input checked="" type="checkbox"/> Reflective <input type="checkbox"/> Transflective <input type="checkbox"/> Transmissive
Viewing Direction		<input checked="" type="checkbox"/> 6 O'clock <input type="checkbox"/> 12 O'clock <input type="checkbox"/> 3 O'clock <input type="checkbox"/> 9 O'clock
Backlight		<input checked="" type="checkbox"/> Without <input type="checkbox"/> CCFL <input type="checkbox"/> EL <input type="checkbox"/> LED
Controller		KS0066 or compatible
DC/DC Converter		Without
CCFL Inverter		Without
EL Driver		Without

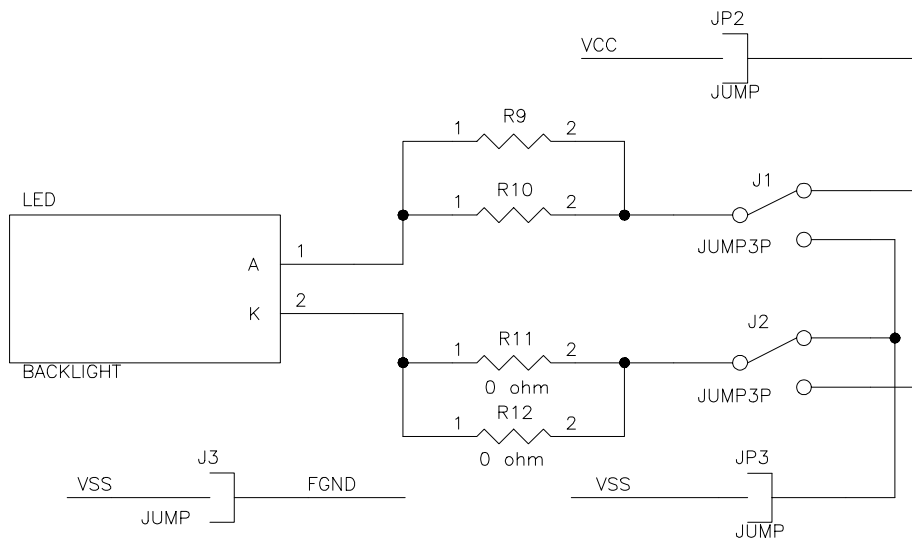
## INTERFACE PIN ASSIGNMENT

PIN NO.	PIN OUT	DESCRIPTION
1   8	DB7   DB0	3-State I/O Data Bus
9	E1	Enable Signal for upper 2 lines
10	R/W	Read/ Write Select
11	RS	Data/ Instruction Register Select
12	V <sub>O</sub>	Power Supply For LCD Panel
13	V <sub>SS</sub>	Ground
14	V <sub>DD</sub>	Logic Circuit Power Supply
15	E2	Enable signal for lower 2 lines
16	NC	No Connection

### JUMPER EXPLANATION

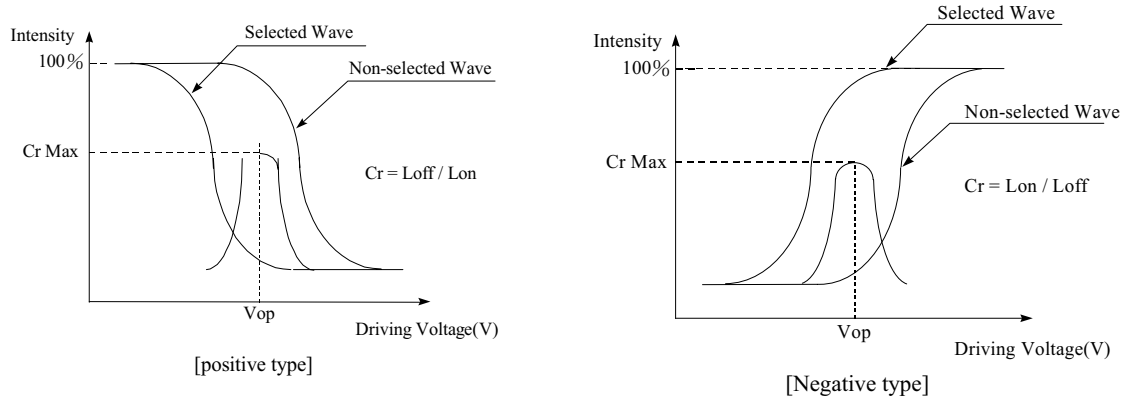
1. JP2 and JP3 are both short: Backlight powered up via V<sub>DD</sub> (pin14) and V<sub>SS</sub> (pin13). Customer can not supply power to A and K. A and K are the terminals of the LED backlight.
2. JP2 short and JP3 open: A is connected to V<sub>DD</sub> with 6-ohm current-limiting resistors in serial and K is NOT short with V<sub>SS</sub>. Backlight is powered with V<sub>DD</sub> (same as logic circuit), customer should keep A floating and could control the backlight independently ON or OFF with K L or H.
3. JP2 open and JP3 short: A is NOT short with V<sub>DD</sub> and K is short with V<sub>SS</sub>. Backlight is common V<sub>SS</sub> with logic and customer should keep K floating or connected to GND (V<sub>SS</sub>) and could control the backlight ON or OFF with A H or L.
4. JP2 and JP3 are both open: The backlight is fully independent with the logic, control the backlight via A and K.
5. J3 short: Bezel and screw holes connected to GND. J3 open: Bezel and screw holes floating
6. Never change the J1 and J2, it may burn off your system.

Note: J3, JP2 and JP3 are #0805 0 ohm resistors on the rear side of the PCB. A and K are the terminals of the LED backlight.

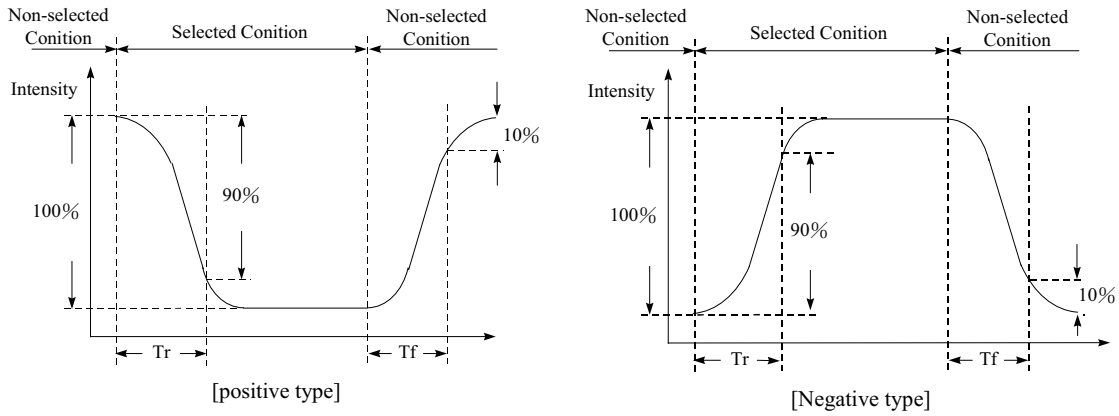




**[Note 7] Definition of Operation Voltage (Vop)**



**[Note 8] Definition of Response Time (Tr, Tf)**



**Conditions:**

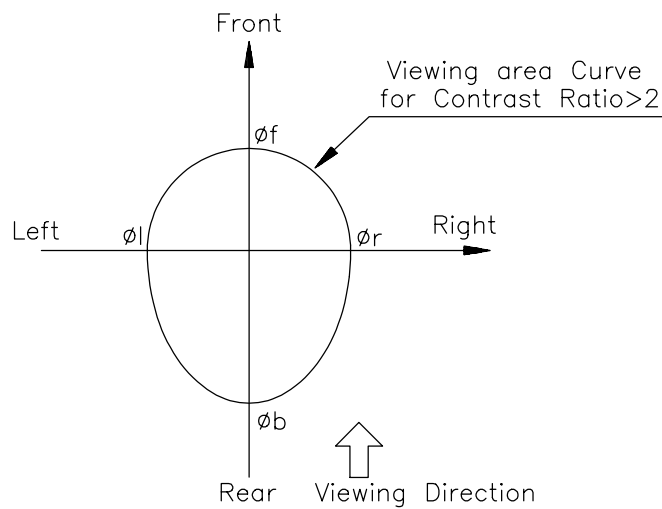
**Operating Voltage : Vop**

**Frame Frequency : 64 Hz**

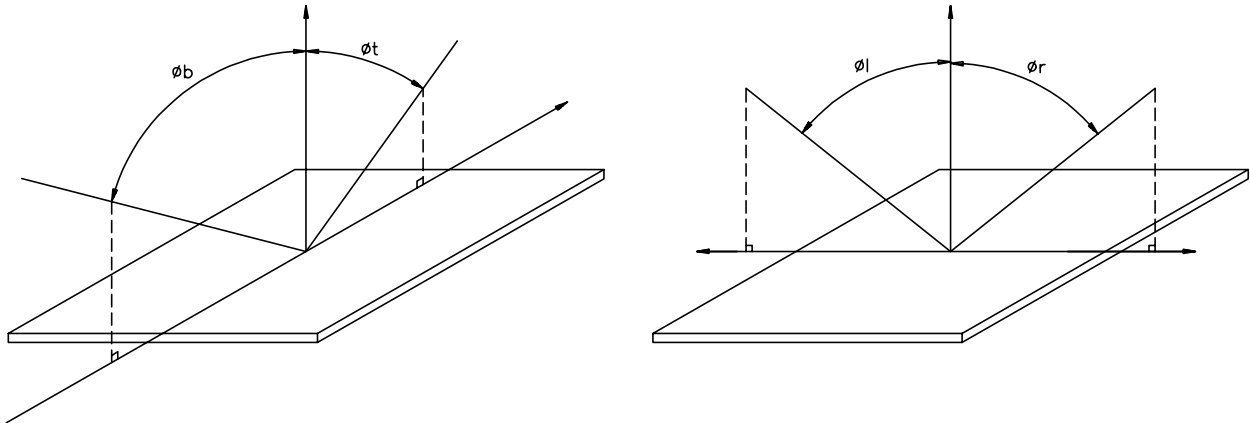
**Viewing Angle( $\theta$ ,  $\varphi$ ):  $0^\circ$ ,  $0^\circ$**

**Driving Wave form : 1/N duty, 1/a bias**

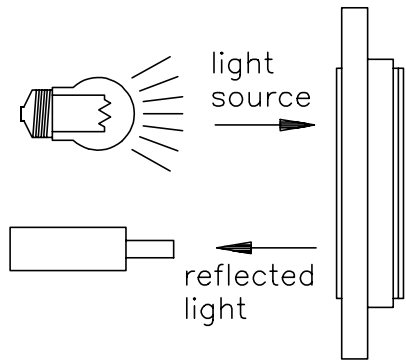
**[Note 9] Definition of Viewing Direction**



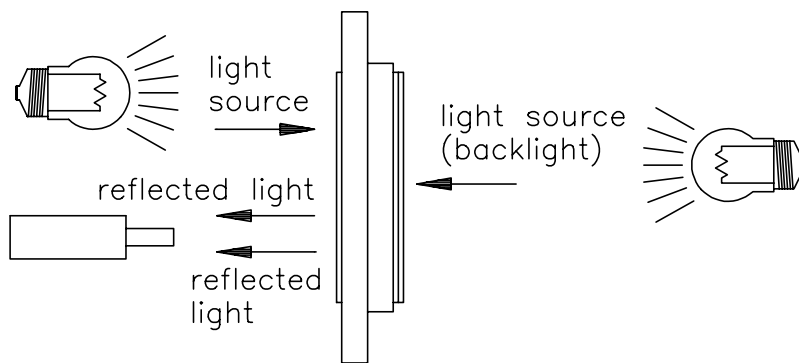
**[Note 10] Definition of viewing angle**



**[Note 11] Description of Measuring Equipment**

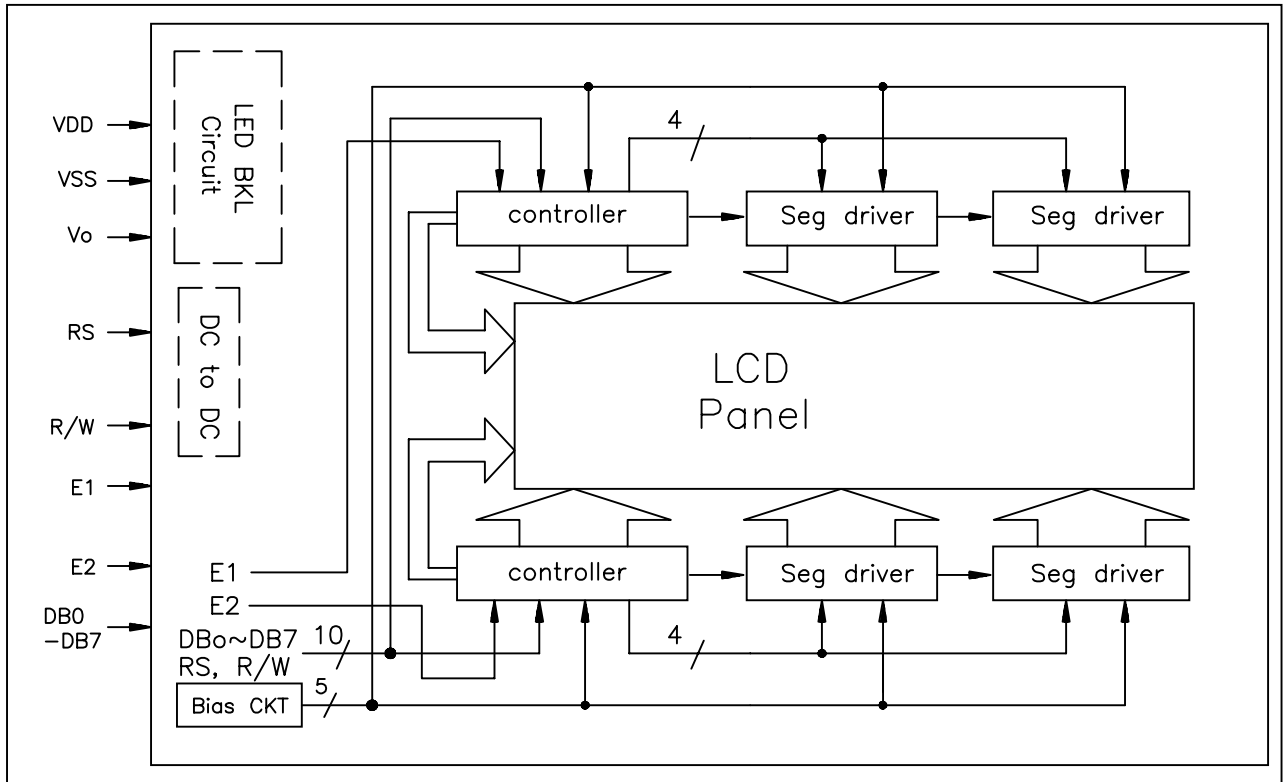


Reflective type

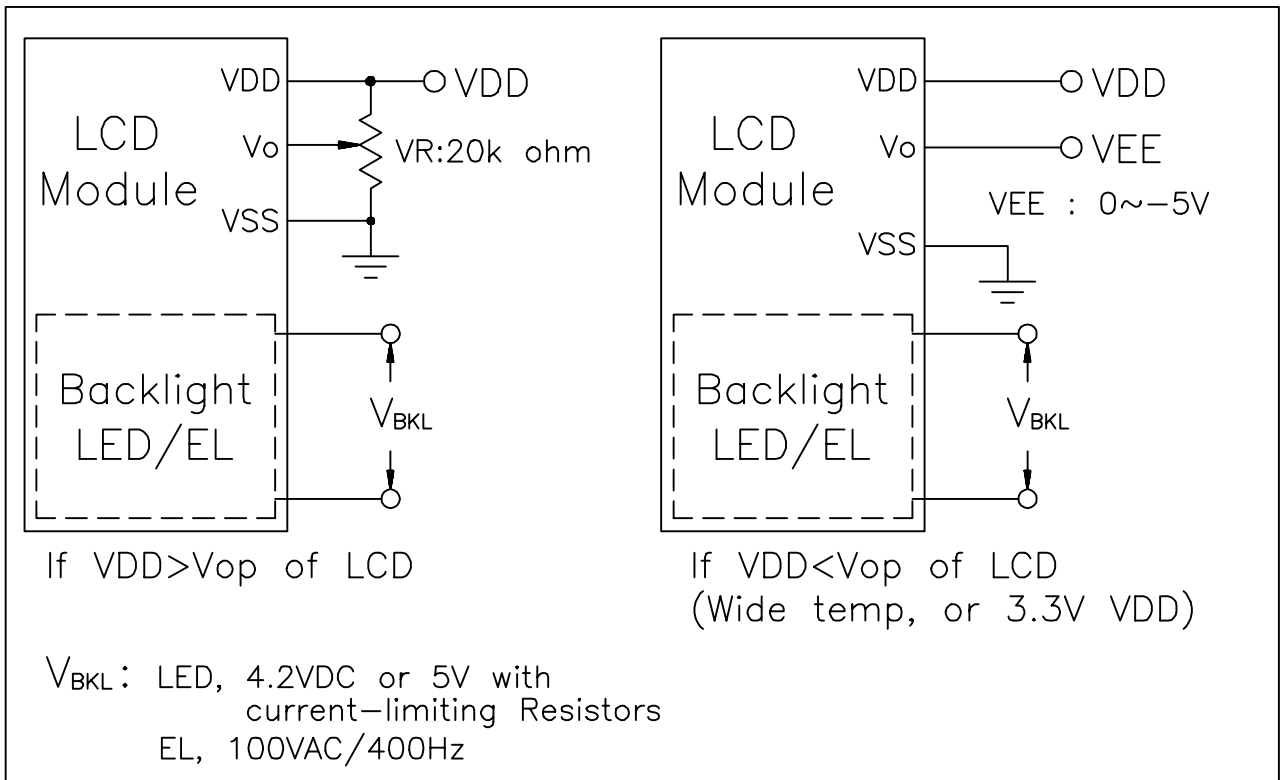


Transflective type  
Transmissive Type

# BLOCK DIAGRAM



# POWER SUPPLY



## TIMING CHARACTERISTICS

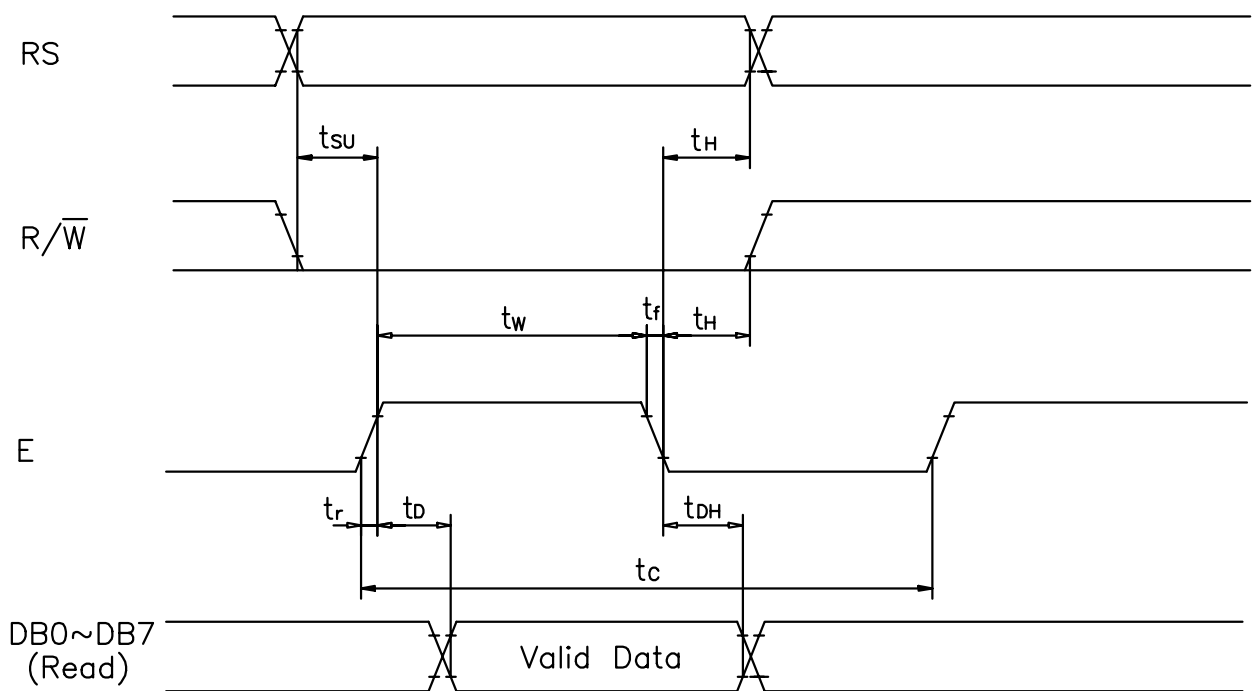
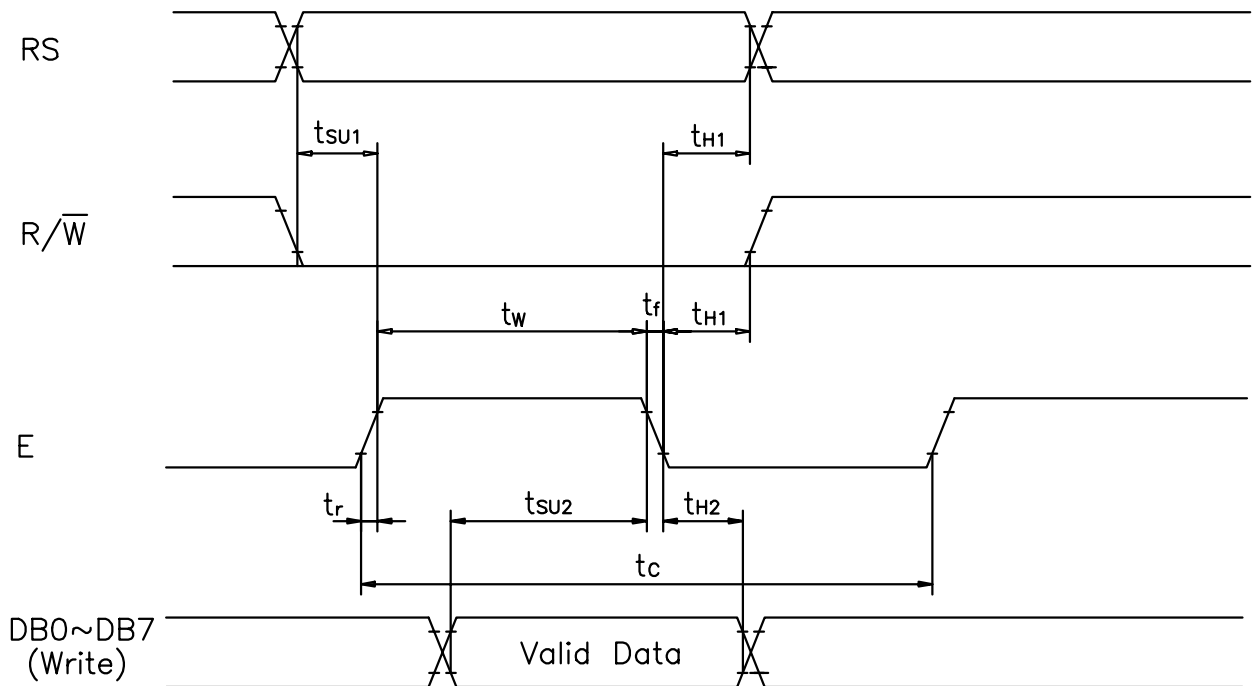
AC Characteristics ( $V_{SS}=0V$ ,  $V_{DD}=4.5V$  to  $5.0V$ ,  $T_a=0$  to  $50^{\circ}C$ )

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	$t_C$	500	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	20	ns
	E Pulse Width(High, Low)	$t_W$	230	-	-	ns
	R/W And RS Setup Time	$t_{SU1}$	40	-	-	ns
	R/W And RS Hold Time	$t_{H1}$	10	-	-	ns
	Data Setup Time	$t_{SU2}$	80	-	-	ns
	Data Hold Time	$t_{H2}$	10	-	-	ns
Read Mode	E Cycle Time	$t_C$	500	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	20	ns
	E Pulse Width(High, Low)	$t_W$	230	-	-	ns
	R/W And RS Setup Time	$t_{SU}$	40	-	-	ns
	R/W And RS Hold Time	$t_H$	10	-	-	ns
	Data Setup Time	$t_D$	-	-	120	ns
	Data Hold Time	$t_{DH}$	5	-	-	ns

AC Characteristics ( $V_{SS}=0V$ ,  $V_{DD}=2.7V$  to  $4.5V$ ,  $T_a=0$  to  $50^{\circ}C$ )

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	$t_C$	1000	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	25	ns
	E Pulse Width(High, Low)	$t_W$	450	-	-	ns
	R/W And RS Setup Time	$t_{SU1}$	60	-	-	ns
	R/W And RS Hold Time	$t_{H1}$	20	-	-	ns
	Data Setup Time	$t_{SU2}$	195	-	-	ns
	Data Hold Time	$t_{H2}$	10	-	-	ns
Read Mode	E Cycle Time	$t_C$	1000	-	-	ns
	E Rise/Fall Time	$t_R, t_F$	-	-	25	ns
	E Pulse Width(High, Low)	$t_W$	450	-	-	ns
	R/W And RS Setup Time	$t_{SU}$	60	-	-	ns
	R/W And RS Hold Time	$t_H$	20	-	-	ns
	Data Setup Time	$t_D$	-	-	360	ns
	Data Hold Time	$t_{DH}$	5	-	-	ns

# Read/Write Timing Chart



## Commands

Instruction	Instruction Code										Description	Execution time( $f_{osc}$ is 270kHz)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.53mS
Return Home	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53mS
Entry Mode	0	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	39 $\mu$ S
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39 $\mu$ S
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	39 $\mu$ S
Function Set	0	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F : 5 X 8 dots/ 5 X 11 dots)	39 $\mu$ S
Set CG RAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter.	39 $\mu$ S
Set DD RAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter.	39 $\mu$ S
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 $\mu$ S
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM).	43 $\mu$ S
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM).	43 $\mu$ S

\* means don't care

## COMMANDS DESCRIPTION

### Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status. namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

### Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Content of DDRAM is not changed.

### Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

#### **I/D : Increment / decrement of DDRAM address (cursor or blink)**

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

\* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

#### **SH: Shift of entire display**

When DDRAM read (CGRAM read/write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" , shift left, I/D = "0" : shift right).

### Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

#### D : Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

#### C : Cursor ON/OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

#### B : Cursor Blink ON/OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = "Low", blink is off.

### Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	*	*

Without writing or reading of display data, shift right/left cursor position or display.

This instruction is used to correct or search display data. (Refer to Table 4)

During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.

Note that display shift is performed simultaneously in all the line.

When displayed data is shifted repeatedly, each line shifted individually.

When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1.
0	1	Shift cursor to the right, AC is increased by 1.
1	0	Shift all of the display to the left, cursor moves according to the display.
1	1	Shift all of the display to the right, cursor moves according to the display.



### Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00	0	0	0	1	DL	N	F	*	*

#### DL : Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data by two times.

#### N : Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

#### F : Display font type control bit

When F = "Low", it means 5 X 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

### Set CG RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

### Set DD RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

### Read Busy Flag and Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

### Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

### Read Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfers RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

## DD RAM ADDRESSING

### For 16×1 or 8×1 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

### For 16×2 or 8×2 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

### For 16×4 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

### For 20×2 Display

Character	1	2	3	4	5	6	7	8	9	10	...	...	17	18	19	20
DD RAM Address	00	01	02	03	04	05	06	07	08	09	...	...	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	...	...	50	51	52	53

### For 20×4 Display

Character	1	2	3	4	5	6	7	8	9	10	...	...	17	18	19	20
DD RAM Address	00	01	02	03	04	05	06	07	08	09	...	...	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	...	...	50	51	52	53
	14	15	16	17	18	19	1A	1B	1C	1D	...	...	24	25	26	27
	54	55	56	57	58	59	5A	5B	5C	5D	...	...	64	65	66	67

### For 40×2 Display

Character	1	2	3	4	5	6	7	8	9	10	...	...	37	38	39	40
DD RAM Address	00	01	02	03	04	05	06	07	08	09	...	...	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	...	...	64	65	66	67

### For 40×4 Display

Character	E	1	2	3	4	5	6	7	8	9	10	...	...	37	38	39	40
DD RAM Address	E1	00	01	02	03	04	05	06	07	08	09	...	...	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	...	...	64	65	66	67
	E2	00	01	02	03	04	05	06	07	08	09	...	...	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	...	...	64	65	66	67

# CG RAM MAPPING

Character Code (DD RAM data)								CG RAM Address						Character Patterns (CG RAM data)																																																										
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																																			
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# CHARACTER FONT TABLE

Upper 4 bits Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)			0	o	P	'	P				—	3	E	o	P
0001	CG RAM (2)		!	l	A	Q	a	9			n	7	+	4	ä	9
0010	CG RAM (3)		"	2	B	R	b	r			r	4	W	x	P	o
0011	CG RAM (4)		#	3	C	S	c	s			l	o	T	E	e	∞
0100	CG RAM (5)		\$	4	D	T	d	t			\	1	h	h	W	a
0101	CG RAM (6)		%	5	E	U	e	u			.	o	*	1	o	ü
0110	CG RAM (7)		&	6	F	V	f	v			9	h	c	a	P	Z
0111	CG RAM (8)		'	7	G	W	g	w			7	+	7	9	9	π
1000	CG RAM (1)		(	8	H	X	h	x			4	o	*	1	o	×
1001	CG RAM (2)		)	9	I	Y	i	y			o	T	h	h	'	y
1010	CG RAM (3)		*	#	J	Z	j	z			z	o	n	v	j	7
1011	CG RAM (4)		+	#	K	K	k	l			*	o	o	o	*	7
1100	CG RAM (5)		,	<	L	+	l	l			h	o	o	o	o	7
1101	CG RAM (6)		—	=	M	M	m	)			z	z	z	z	*	÷
1110	CG RAM (7)		.	>	N	n	n	+			z	o	o	'	n	
1111	CG RAM (8)		/	?	O	o	o	+			W	W	W	W	o	■

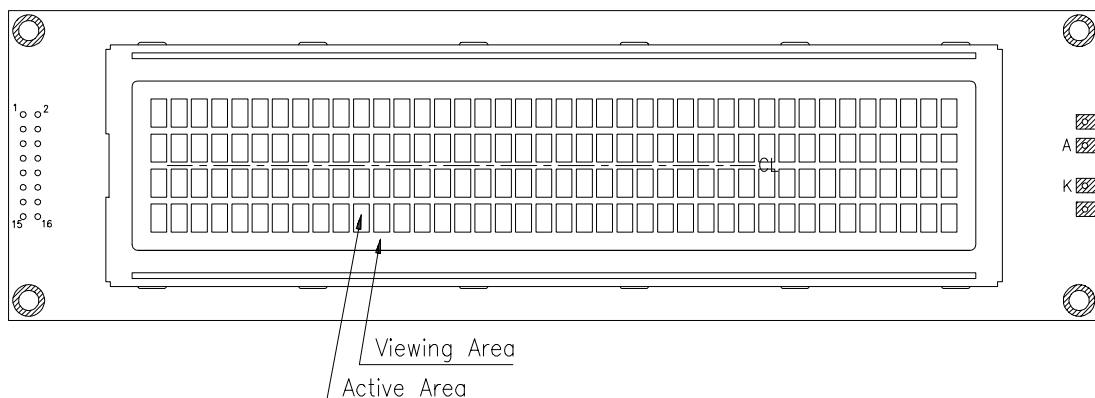
## RELIABILITY TEST

No	Item	Conditions		Note
1	High Temp. Operation	70°C	240 HR	
2	High Temp. Storage	80°C	240 HR	
3	Low Temp. Operation	-20°C	240 HR	
4	Low Temp. Storage	-30°C	240 HR	
5	High Temp./Humid Storage	60°C 90%RH	240 HR	
6	Thermal Shock	-20°C ,30min +60°C ,30min	10 cycles	
7	Vibration Test ( IEC-68-2-6 )	Frequency : 10~55 Hz Duration : 20 times, 6 min/time Amplitude : 0.75 mm	-	
8	Shock ( IEC 68-2-27)	Duration : 11 mS Acceleration : 100g	-	X, Y, Z direction

## APPEARANCE CHECK

CONDIITON OF APPEARANCE CHECK:

- (1) Specimen shall be checked by eyes in distance of 30cm under 40w-fluorescence lamp.
- (2) Checking direction shall be in 45 degree from perpendicular line op specimen surface.



## HANDLING PRECAUTIONS

- (1) Treat polarizer very carefully since it is easy to be damaged.
- (2) When cleaning the display surface, use soft cloth (e.g. gauss) with a solvent (recommended below) and wipe lightly.

- ◆ ethyl alcohol
- ◆ iso-procolol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvents:

- ◆ water
- ◆ ketone
- ◆ aromatics

- (3) Direct current causes electro-chemical reaction with remarkable degradation of the display quality. Give careful consideration to prevent direct current at ON/OFF timing and during operation.
- (4) Avoid strong shock and drop from the height.
- (5) To prevent LCD panels from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.
- (6) Give careful consideration to avoid electrical static discharge with causes uneven contrast.
- (7) Even a small condensation on the contact pads (terminals) causes electro-chemical reaction which makes missing row and column. Give careful attention to avoid condensation. When assembling with zebra connector, clean the surface of the pads with alcohol and keep the air very clean.

# LCD PRODUCT QUALITY STANDARD

## DISPLAY APPEARANCE

No	Item	Criteria
1	inclusions (black spot, white spot, dust)	(1)round type diameter mm(a*)      no of defect* $a \leq 0.20$ neglect $0.20 < a \leq 0.35$ 5max $0.35 < a$ none (2)linear type length mm(l)      width mm(W)      no. of defect na $W \leq 0.03$ neglect $1 \leq 3$ $0.03 < W \leq 0.08$ 6 $3 < l$ $0.08 < W$ none
2	scratch	1. scratch on protective film is permitted. 2. scratch on polarizer shall be as follow: (1)round type diameter mm(a*)      no of defect $a \leq 0.15$ neglect $0.15 < a \leq 0.20$ 2 max $0.20 < a$ none (2)linear type be judged bye 1.-(2) linear type
3	dent	diameter < 1.5mm
4	bubble	not exceeding 0.5mm average diameter is acceptable between glass and polarizing film
5	pin hole	$(a+b)/2 \leq 0.15$ mm maximum number: ignored $0.15 < (a+b)/2 \leq 0.20$ mm maximum number: 10
6	dot defect	$(a+b)/2 \leq 0.20$ mm maximum number: ignored $0.20 < (a+b)/2 \leq 0.30$ mm maximum number: 5 x=width
7	contrast irregularity(spot)	diameter spec      no of defect $a \leq 0.50$ mm                  neglect $0.50 < a \leq 0.75$ 5 $0.75 < a \leq 1.00$ 3 $1.00 < a$ none
8	dot width	design width $\pm 15\%$
9	color tone and uniformity	obvious uneven color is not permitted



## **REVISION HISTORY**

Revision Content	Page	Date
Update the pin assignment	8	Sep. 1, 00