



Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

General Description

The MAX5188 is a dual 8-bit, alternate-phase-update, current-output digital-to-analog converter (DAC) designed for superior performance in systems requiring analog signal reconstruction with low distortion and low-power operation. The MAX5191 provides equal specifications, with on-chip output resistors for voltage-output operation. Both devices are designed for 10pVs glitch operation to reduce distortion and minimize unwanted spurious signal components at the output. An on-board +1.2V bandgap circuit provides a well-regulated, low-noise reference that may be disabled for external reference operation.

The MAX5188/MAX5191 are designed to provide a high level of signal integrity for the least amount of power dissipation. Both DACs operate from a +2.7V to +3.3V single supply. Additionally, these DACs have three modes of operation: normal, low-power standby, and full shutdown. A full shutdown provides the lowest possible power dissipation with a maximum shutdown current of 1 μ A. A fast wake-up time (0.5 μ s) from standby mode to full DAC operation allows for power conservation by activating the DACs only when required.

The MAX5188/MAX5191 are available in a 28-pin QSOP package and are specified for the extended (-40°C to +85°C) temperature range. For pin-compatible 10-bit versions, refer to the MAX5182/MAX5185 data sheet.

Applications

Signal Reconstruction Applications
Digital Signal Processing
Arbitrary Waveform Generators
Imaging Applications

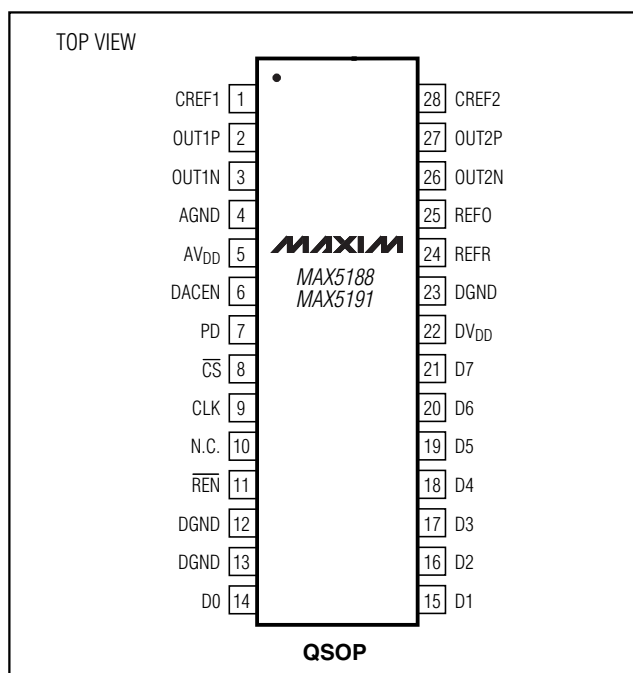
Features

- ◆ +2.7V to +3.3V Single-Supply Operation
- ◆ Wide Spurious-Free Dynamic Range: 70dB at $f_{OUT} = 2.2\text{MHz}$
- ◆ Fully Differential Outputs for Each DAC
- ◆ $\pm 0.5\%$ FSR Gain Mismatch Between DAC Outputs
- ◆ Low-Current Standby or Full Shutdown Modes
- ◆ Internal +1.2V Low-Noise Bandgap Reference
- ◆ Small 28-Pin QSOP Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5188BEEI	-40°C to +85°C	28 QSOP
MAX5191BEEI	-40°C to +85°C	28 QSOP

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD to AGND, DGND-0.3V to +6V
 Digital Inputs to DGND-0.3V to +6V
 OUT1P, OUT1N, OUT2P, OUT2N, CREF1,
 CREF2 to AGND-0.3V to +6V
 VREF to AGND-0.3V to +6V
 AVDD to DVDD±3.3V
 AGND to DGND-0.3V to +0.3V
 Maximum Current into Any Pin50mA

Continuous Power Dissipation (TA = +70°C)
 28-Pin QSOP (derate 9.00mW/°C above +70°C)725mW
 Operating Temperature Ranges
 MAX5188/MAX5191BEEI-40°C to +85°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AVDD = DVDD = +3V ±10%, AGND = DGND = 0, fCLK = 40MHz, IFS = 1mA, 400Ω differential output, CL = 5pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
STATIC PERFORMANCE								
Resolution	N			8			Bits	
Integral Nonlinearity	INL			-1	±0.25	+1	LSB	
Differential Nonlinearity	DNL	Guaranteed monotonic		-1	±0.25	+1	LSB	
Zero-Scale Error		MAX5188		-1			+1	LSB
		MAX5191		-4			+4	LSB
Full-Scale Error		(Note 1)		-20	±4	+20	LSB	
DYNAMIC PERFORMANCE								
Output Settling Time		To ±0.5LSB error band		25			ns	
Glitch Impulse				10			pVs	
Spurious-Free Dynamic Range to Nyquist	SFDR	f _{CLK} = 40MHz	f _{OUT} = 500kHz	72			dBc	
			f _{OUT} = 2.2MHz, T _A = +25°C	57	70			
Total Harmonic Distortion to Nyquist	THD	f _{CLK} = 40MHz	f _{OUT} = 500kHz	-70			dB	
			f _{OUT} = 2.2MHz, T _A = +25°C	-68	-63			
Signal-to-Noise Ratio to Nyquist	SNR	f _{CLK} = 40MHz	f _{OUT} = 500kHz	52			dB	
			f _{OUT} = 2.2MHz, T _A = +25°C	46	52			
DAC-to-DAC Output Isolation		f _{OUT} = 2.2MHz		-60			dB	
Clock and Data Feedthrough		All 0s to all 1s		50			nVs	
Output Noise				10			pA/√Hz	
Gain Mismatch Between DAC Outputs		f _{OUT} = 2.2MHz, T _A = +25°C		±0.5			±1	LSB
ANALOG OUTPUT								
Full-Scale Output Voltage	V _{FS}			400			mV	
Voltage Compliance of Output				-0.3	0.8		V	
Output Leakage Current		DACEN = 0, MAX5188 only		-1	1		µA	
Full-Scale Output Current	I _{FS}	MAX5188 only		0.5	1	1.5	mA	
DAC External Output Resistor Load		MAX5188 only		400			Ω	

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ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD} = DV_{DD} = +3V \pm 10\%$, $AGND = DGND = 0$, $f_{CLK} = 40MHz$, $I_{FS} = 1mA$, 400Ω differential output, $C_L = 5pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

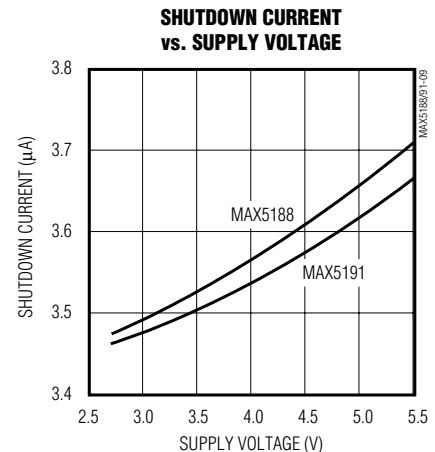
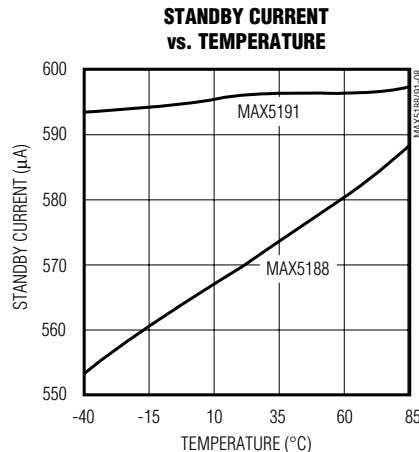
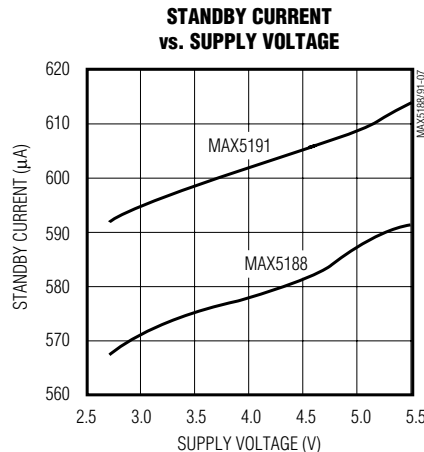
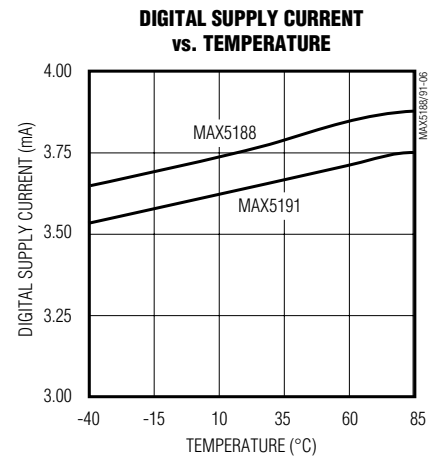
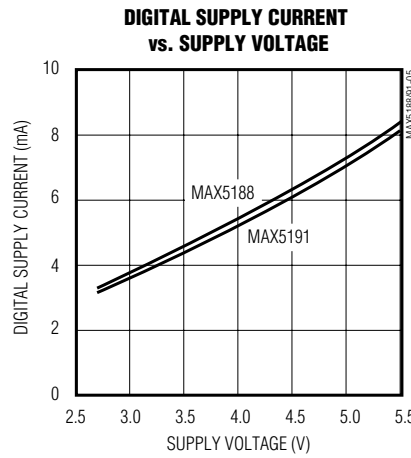
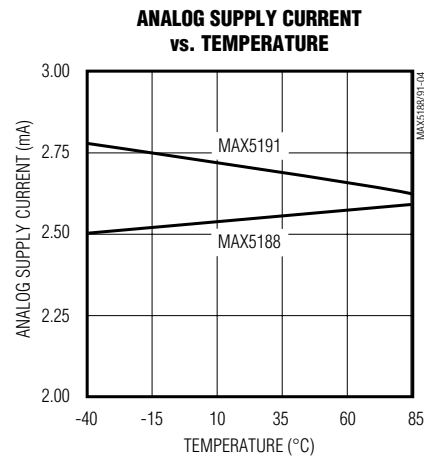
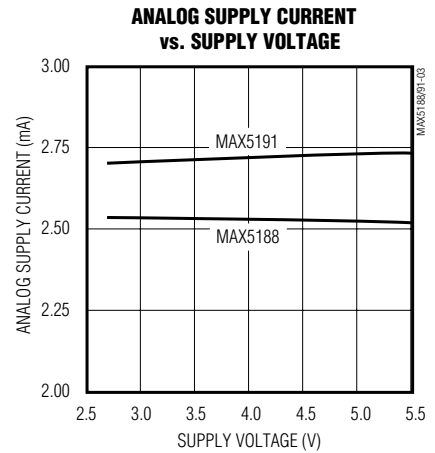
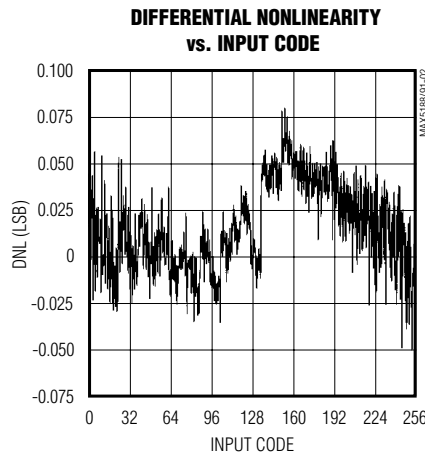
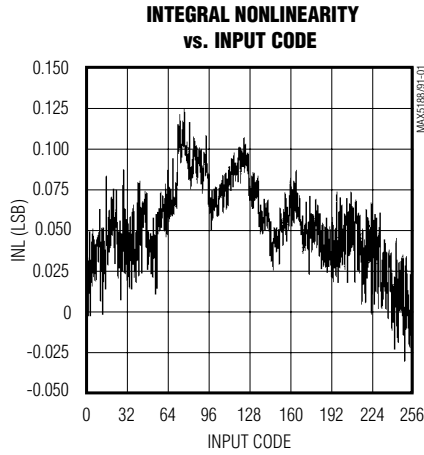
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage Range	V_{REF}		1.12	1.2	1.28	V
Output Voltage Temperature Drift	TCV_{REF}			50		ppm/ $^\circ C$
Reference Output Drive Capability	I_{REFOUT}			10		μA
Reference Supply Rejection				0.5		mV/V
Current Gain (I_{FS} / I_{REF})				8		mA/mA
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AV_{DD}		2.7		3.3	V
Analog Supply Current	I_{AVDD}	PD = 0, DACEN = 1, digital inputs at 0 or DV_{DD}		2.7	5	mA
Digital Power-Supply Voltage	DV_{DD}		2.7		3.3	V
Digital Supply Current	I_{DVDD}	PD = 0, DACEN = 1, digital inputs at 0 or DV_{DD}		4.2	5	mA
Standby Current	$I_{STANDBY}$	PD = 0, DACEN = 0, digital inputs at 0 or DV_{DD}		1	1.5	mA
Shutdown Current	I_{SHDN}	PD = 1, DACEN = X, digital inputs at 0 or DV_{DD} (X = don't care)		0.5	1	μA
LOGIC INPUTS AND OUTPUTS						
Digital Input High Voltage	V_{IH}		2			V
Digital Input Low Voltage	V_{IL}				0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0$ or DV_{DD}			± 1	μA
Digital Input Capacitance	C_{IN}			10		pF
TIMING CHARACTERISTICS						
DAC1 DATA to CLK Rise Setup Time	t_{DS1}		10			ns
DAC2 DATA to CLK Fall Setup Time	t_{DS2}		10			ns
DAC1 CLK Rise to DATA Hold Time	t_{DH1}		0			ns
DAC2 CLK Fall to DATA Hold Time	t_{DH2}		0			ns
$\overline{CS}$ Fall to CLK Rise Time				5		ns
$\overline{CS}$ Fall to CLK Fall Time				5		ns
DACEN Rise Time to V_{OUT}				0.5		μs
PD Fall Time to V_{OUT}				50		μs
Clock Period	t_{CLK}		25			ns
Clock High Time	t_{CH}		10			ns
Clock Low Time	t_{CL}		10			ns

Note 1: Excludes reference and reference resistor (MAX5191) tolerance.

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Typical Operating Characteristics

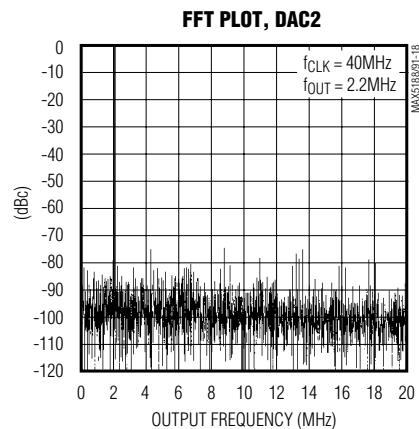
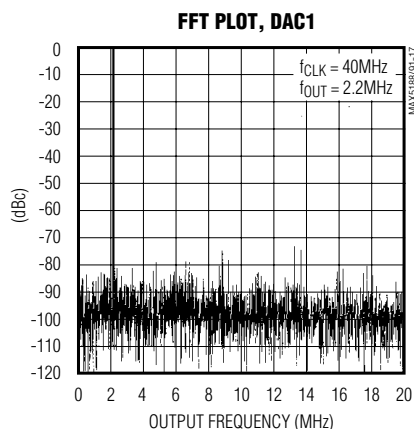
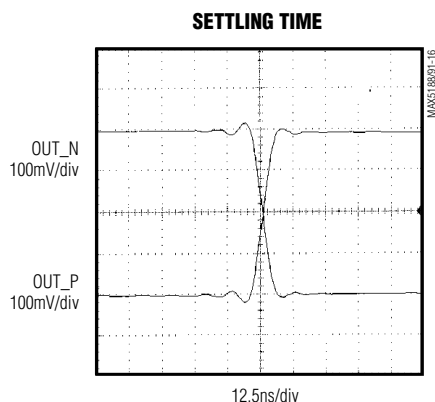
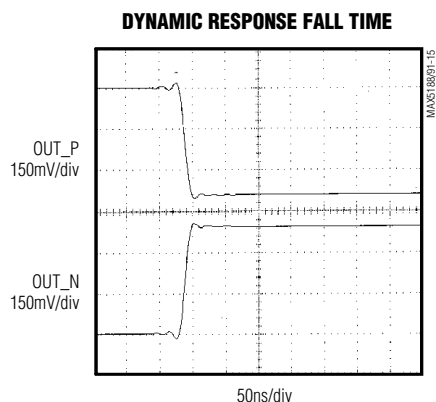
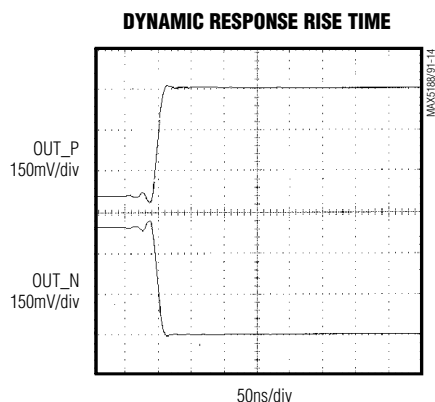
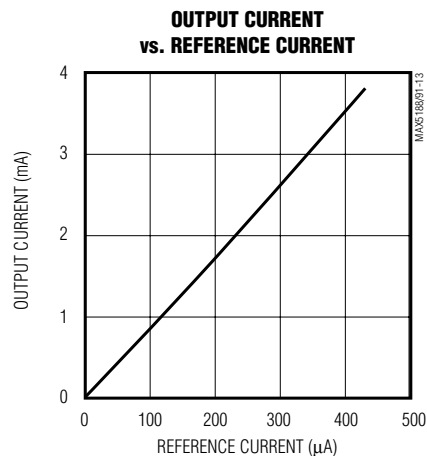
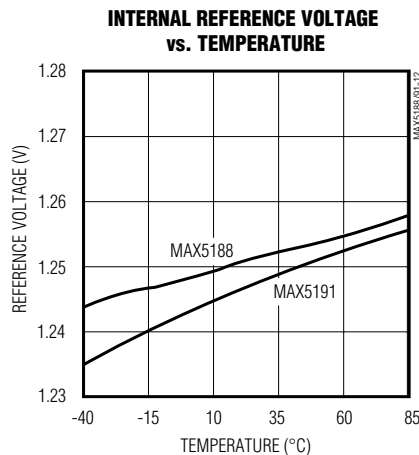
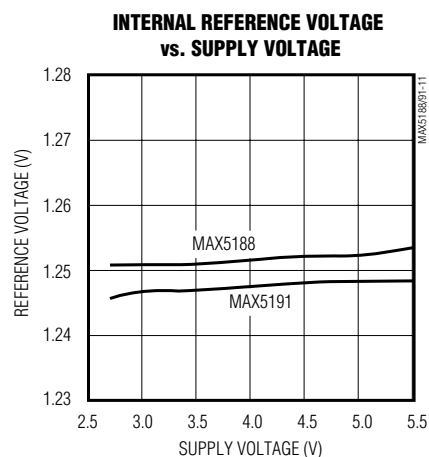
($V_{DD} = DV_{DD} = +3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

Typical Operating Characteristics (continued)

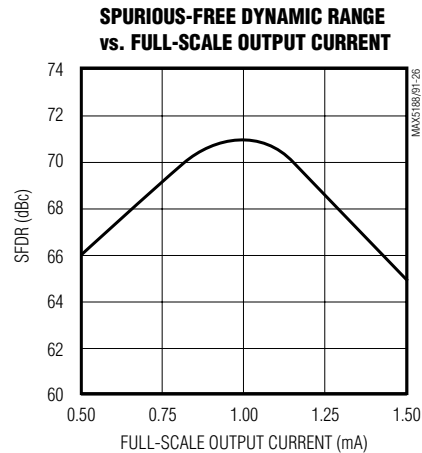
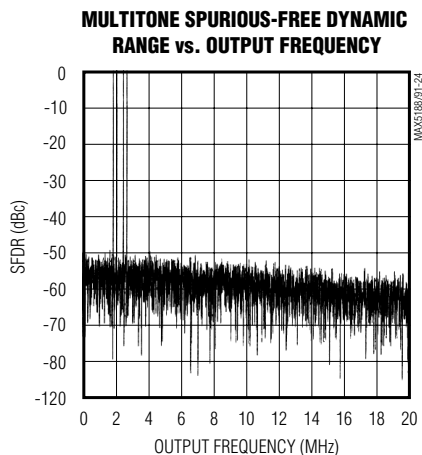
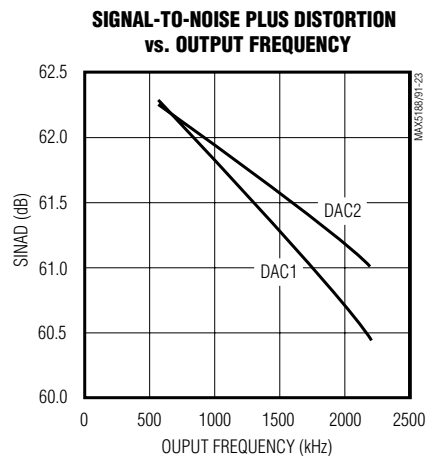
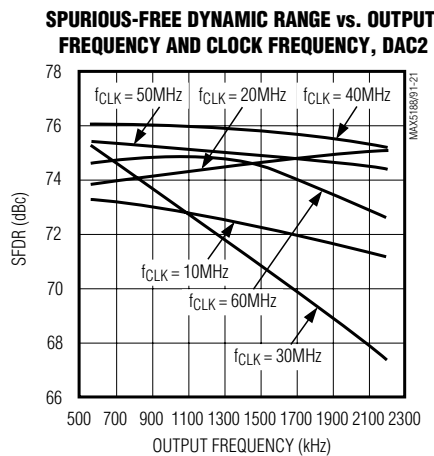
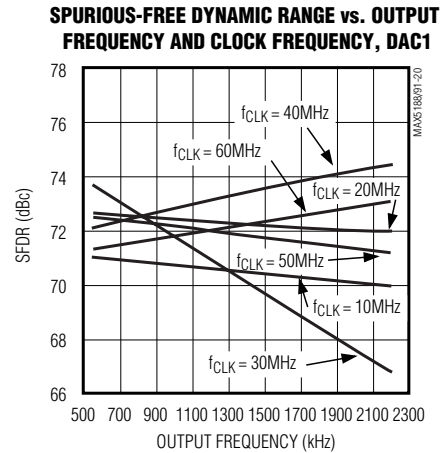
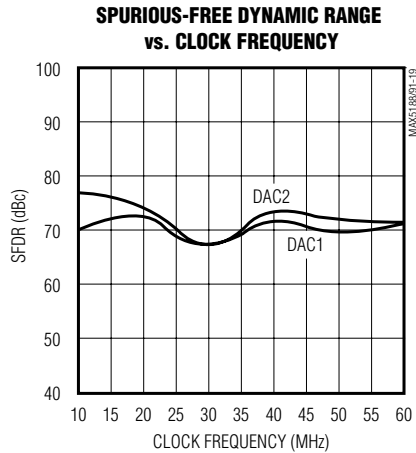
($V_{DD} = DV_{DD} = +3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = +3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

MAX5188/MAX5191

PIN	NAME	FUNCTION
1	CREF1	Reference Bias Bypass, DAC1
2	OUT1P	Positive Analog Output, DAC1. Current output for the MAX5188; voltage output for the MAX5191.
3	OUT1N	Negative Analog Output, DAC1. Current output for the MAX5188; voltage output for the MAX5191.
4	AGND	Analog Ground
5	AVDD	Analog Positive Supply, +2.7V to +3.3V
6	DACEN	DAC Enable, Digital Input 0: Enter DAC standby mode with PD = DGND 1: Power-up DAC with PD = DGND X: Enter shutdown mode with PD = DVDD (X = don't care)
7	PD	Power-Down Select 0: Enter DAC standby mode (DACEN = DGND) or power-up DAC (DACEN = DVDD) 1: Enter shutdown mode
8	$\overline{CS}$	Active-Low Chip Select
9	CLK	Clock Input
10	N.C.	Not Connected. Do not connect to this pin.
11	$\overline{REN}$	Active-Low Reference Enable. Connect to DGND to activate on-chip +1.2V reference.
12, 13, 23	DGND	Digital Ground
14	D0	Data Bit D0 (LSB)
15–20	D1–D6	Data Bits D1–D6
21	D7	Data Bit D7 (MSB)
22	DVDD	Digital Supply, +2.7V to +3.3V
24	REFR	Reference Input
25	REFO	Reference Output
26	OUT2N	Negative Analog Output, DAC2. Current output for the MAX5188; voltage output for the MAX5191.
27	OUT2P	Positive Analog Output, DAC2. Current output for the MAX5188; voltage output for the MAX5191.
28	CREF2	Reference Bias Bypass, DAC2

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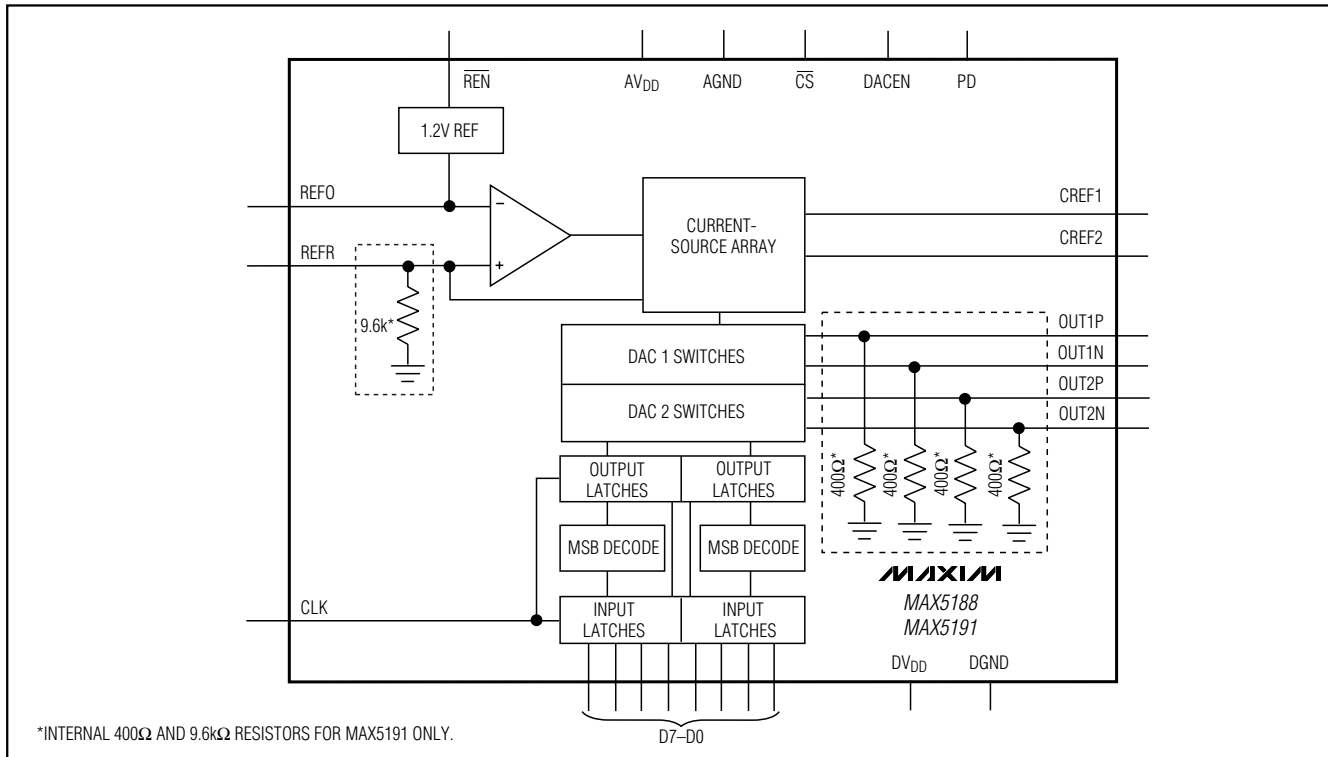


Figure 1. Functional Diagram

Detailed Description

The MAX5188/MAX5191 are dual 8-bit digital-to-analog converters (DACs) capable of operating with clock speeds up to 40MHz. Each of these dual converters consists of separate input and DAC registers, followed by a current-source array capable of generating up to 1.5mA full-scale output current (Figure 1). An integrated +1.2V voltage reference and control amplifier determine the data converters' full-scale output currents/voltages. Careful reference design ensures close gain matching and excellent drift characteristics. The MAX5191's voltage output operation features matched 400Ω on-chip resistors that convert the current from the current array into a voltage.

Internal Reference and Control Amplifier

The MAX5188/MAX5191 provide an integrated 50ppm/°C, +1.2V, low-noise bandgap reference that can be disabled and overridden by an external reference voltage. REFO serves either as an input for an external reference or as an output for the integrated reference. If REN is connected to DGND, the internal reference is selected and REFO provides a +1.2V output.

Due to its limited 10μA output drive capability, the REFO pin must be buffered with an external amplifier if heavier loading is required.

The MAX5188/MAX5191 also employ a control amplifier, designed to simultaneously regulate the full-scale output current I_{FS} for both MAX5188/MAX5191 outputs. The output current is calculated as follows:

$$I_{FS} = 8 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFO} / R_{SET}$) and I_{FS} is the full-scale output current. R_{SET} is the reference resistor that determines the amplifier's output current (Figure 2) on the MAX5188. This current is mirrored into the current-source array, where it is equally distributed between matched current segments and summed to valid output current readings for the DACs.

Inside the MAX5191, each output current (DAC1 and DAC2) is converted to an output voltage (V_{OUT1}, V_{OUT2}) with two internal, ground-referenced, 400Ω load resistors. Using the internal +1.2V reference voltage, the integrated reference output current resistor of the MAX5191 (R_{SET} = 9.6kΩ) sets I_{REF} to 125μA and I_{FS} to 1mA.

Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

MAX5188/MAX5191

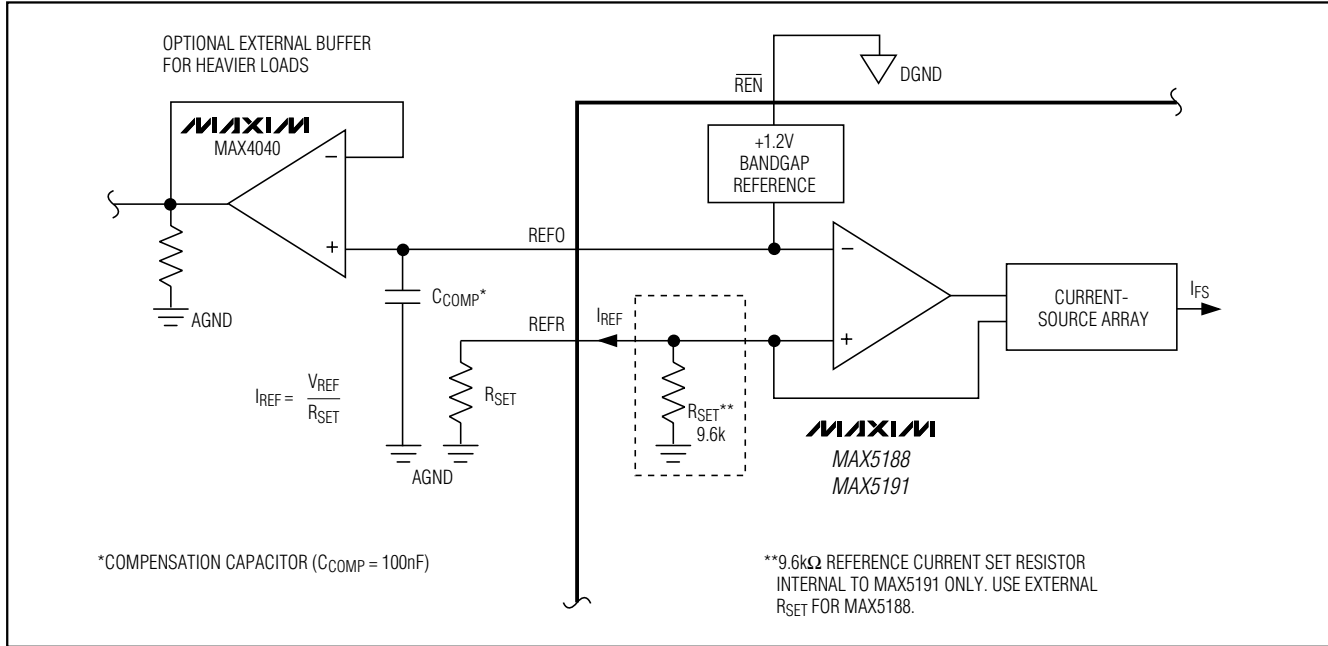


Figure 2. Setting I_{FS} with the Internal +1.2V Reference and Control Amplifier

External Reference

To disable the MAX5188/MAX5191's internal reference, connect $\overline{REN}$ to DV_{DD} . A temperature-stable external reference may now be applied to drive the REFO pin (Figure 3) to set the full-scale output. Choose a reference that can supply at least 150μA to drive the bias circuit that generates the cascode current for the current array. For improved accuracy and drift performance, choose a fixed output voltage reference such as the +1.2V, 25ppm/°C MAX6520 bandgap reference.

Standby Mode

To enter the lower-power standby mode, connect digital inputs PD and DACEN to DGND. In standby, both the reference and the control amplifier are active with the current array inactive. To exit this condition, DACEN

must be pulled high with PD held at DGND. The MAX5188/MAX5191 typically require 50μs to wake up and allow both the outputs and the reference to settle.

Shutdown Mode

For lowest power consumption, the MAX5188/MAX5191 provide a power-down mode in which the reference, control amplifier, and current array are inactive and the DAC's supply current is reduced to 1μA. To enter this mode, connect PD to DV_{DD} . To return to active mode, connect PD to DGND and DACEN to DV_{DD} . About 50μs are required for the devices to leave shutdown mode and settle their outputs to the values prior to shutdown. Table 1 lists the power-down mode selection.

Table 1. Power-Down Mode Selection

PD (POWER-DOWN SELECT)	DACEN (DAC ENABLE)	POWER-DOWN MODE	OUTPUT STATE	
0	0	Standby	MAX5188	High-Z
			MAX5191	AGND
0	1	Wake-Up	Last state prior to standby mode	
1	X	Shutdown	MAX5188	High-Z
			MAX5191	AGND

X = Don't care

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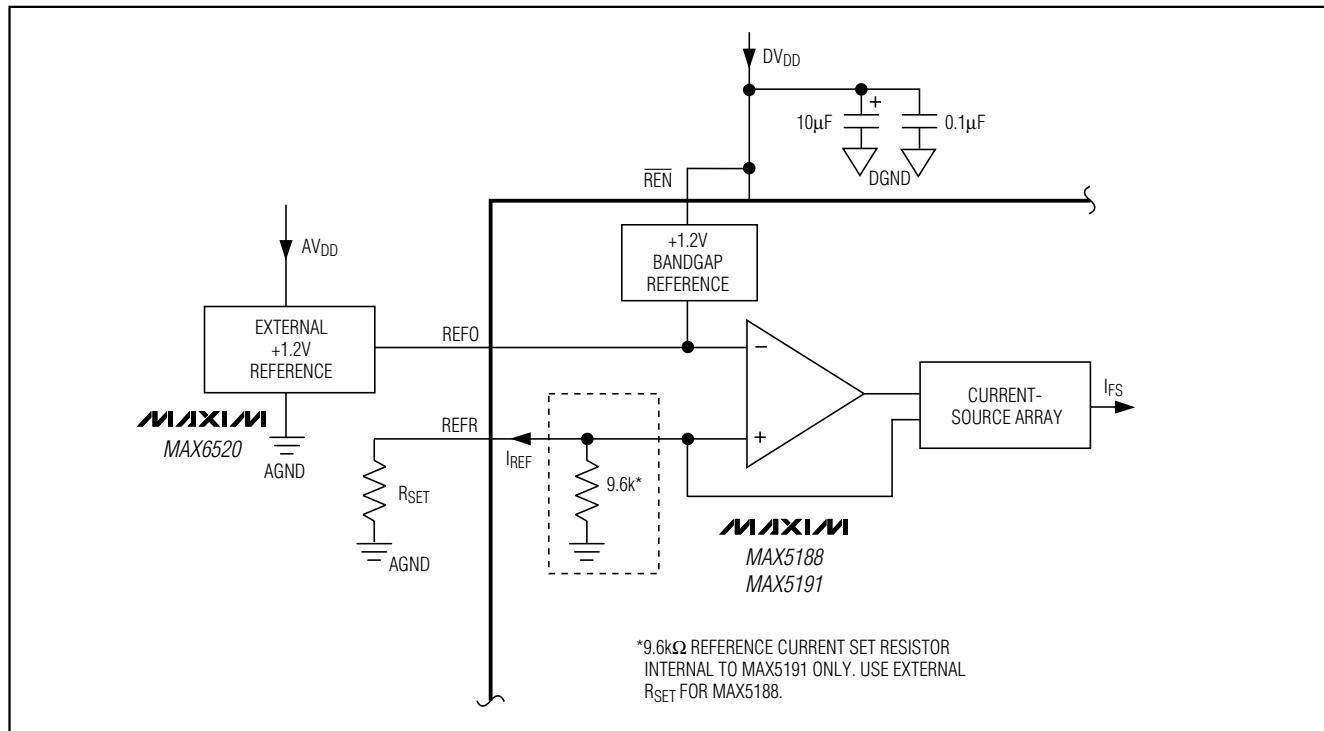


Figure 3. MAX5188/MAX5191 Using an External Reference

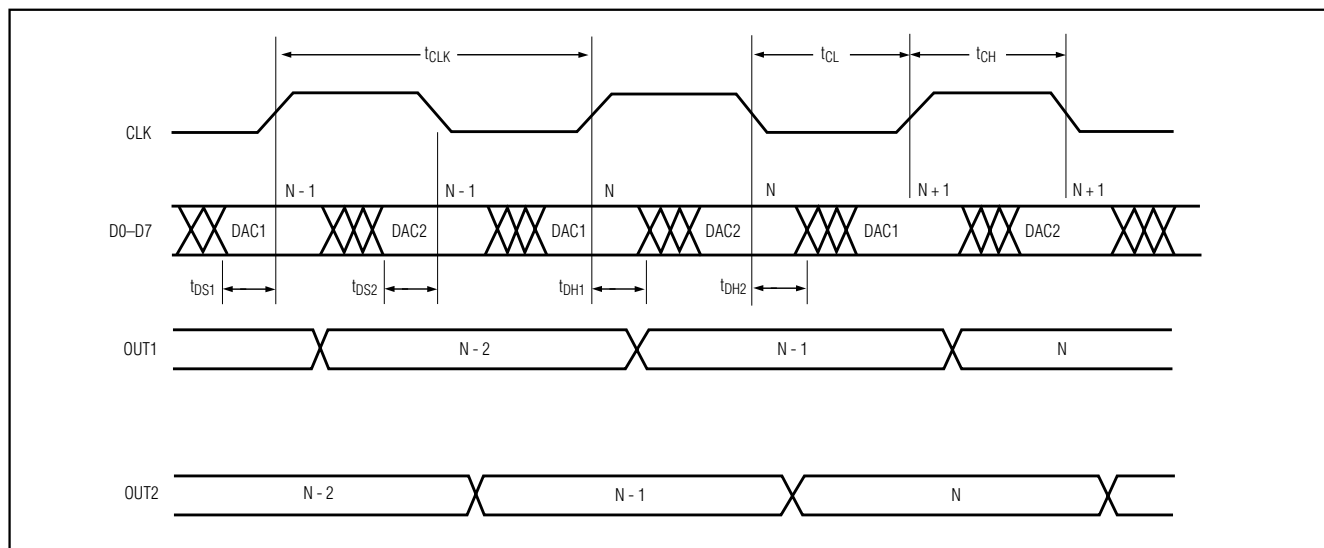


Figure 4. Timing Diagram

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Timing Information

Both internal DAC cells write to their outputs in alternate phase (Figure 4). The input latch of the first DAC (DAC1) is loaded after the clock signal transitions high. When the clock signal transitions low, the input latch of the second DAC (DAC2) is loaded. The contents of the first input latch are shifted into the DAC1 register on the rising edge of the clock; the contents of the second input latch are shifted into the input register of DAC2 on the falling edge of the clock. Both outputs are updated on alternate phases of the clock.

Outputs

The MAX5188 outputs are designed to supply 1mA full-scale output currents into 400Ω loads in parallel with a capacitive load of 5pF. The MAX5191 features integrat-

ed 400Ω resistors that restore the array currents into proportional, differential voltages of 400mV. These differential output voltages can then be used to drive a balun transformer or a low-distortion, high-speed operational amplifier to convert the differential voltage into a single-ended voltage.

Applications Information

Static and Dynamic Performance Definitions

Integral Nonlinearity

Integral nonlinearity (INL) (Figure 5a) is the deviation of the values on an actual transfer function from either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints

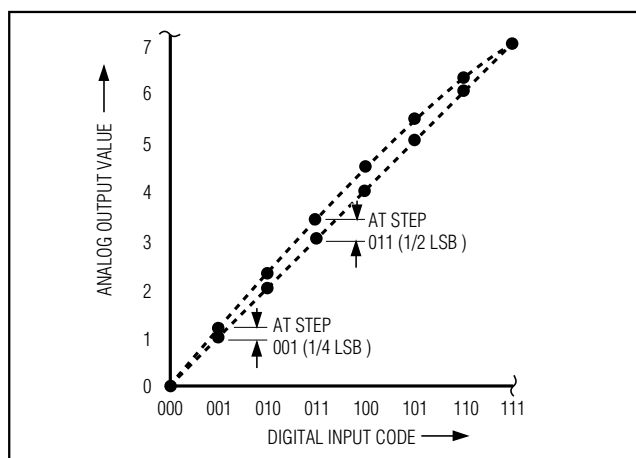


Figure 5a. Integral Nonlinearity

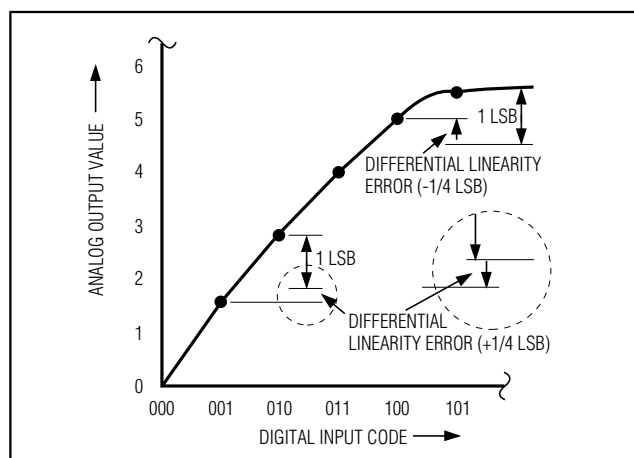


Figure 5b. Differential Nonlinearity

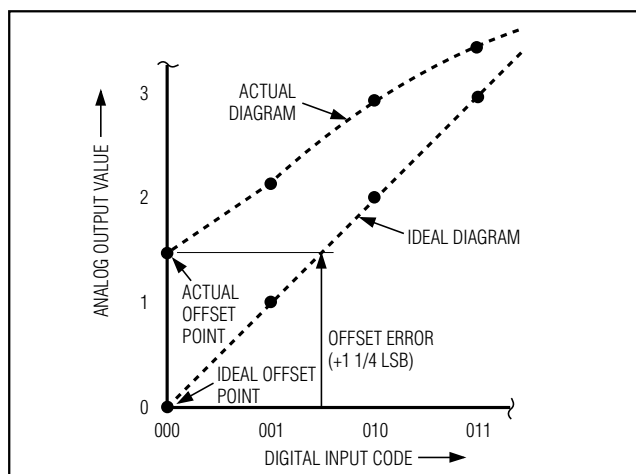


Figure 5c. Offset Error

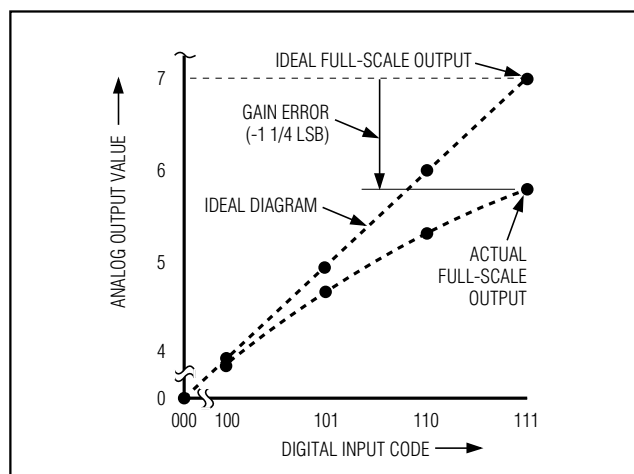


Figure 5d. Gain Error

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of the transfer function once offset and gain errors have been nullified. For a DAC, the deviations are measured at every single step.

Differential Nonlinearity

Differential nonlinearity (DNL) (Figure 5b) is the difference between an actual step height and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error (Figure 5c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated by trimming.

Gain Error

Gain error (Figure 5d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the noise generated on a DAC's output when any digital input transitions. Proper board layout and grounding will significantly reduce this noise, but there will always be some feedthrough caused by the DAC itself.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first four harmonics to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Differential to Single-Ended Conversion

The MAX4108 low-distortion, high input-bandwidth amplifier may be used to generate a voltage from the MAX5188's current-array output. The differential voltage across OUT1P (or OUT2P) and OUT1N (or OUT2N) is converted into a single-ended voltage by designing an appropriate operational amplifier configuration as shown in Figure 6.

Grounding and Power-Supply Decoupling

Grounding and power-supply decoupling strongly influence the performance of the MAX5188/MAX5191. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, which may affect dynamic specifications like SNR or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5188/MAX5191. Therefore, grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed.

First, a multilayer PC board with separate ground and power-supply planes is recommended. High-speed signals should run on controlled impedance lines directly above the ground plane. Since the MAX5188/MAX5191 have separate analog and digital ground buses (AGND and DGND, respectively), the PC board should also have separate analog and digital ground sections with only one point connecting the two. Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane.

Both devices have two power-supply inputs: analog V_{DD} (AV_{DD}) and digital V_{DD} (DV_{DD}). Each AV_{DD} input should be decoupled with parallel 10 μ F and 0.1 μ F ceramic-chip capacitors as close to the pin as possible. Their opposite ends should have the shortest possible connection to the ground plane. The DV_{DD} pins should also have separate 10 μ F and 0.1 μ F capacitors, again adjacent to their respective pins. Try to minimize the analog load capacitance for proper operation. For best performance, bypass CREF1 and CREF2 with low-ESR, 0.1 μ F capacitors to AV_{DD} .

The power-supply voltages should also be decoupled with large tantalum or electrolytic capacitors at the point they enter the PC board. Ferrite beads with additional decoupling capacitors forming a pi network could also improve performance.

Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

MAX518/MAX5191

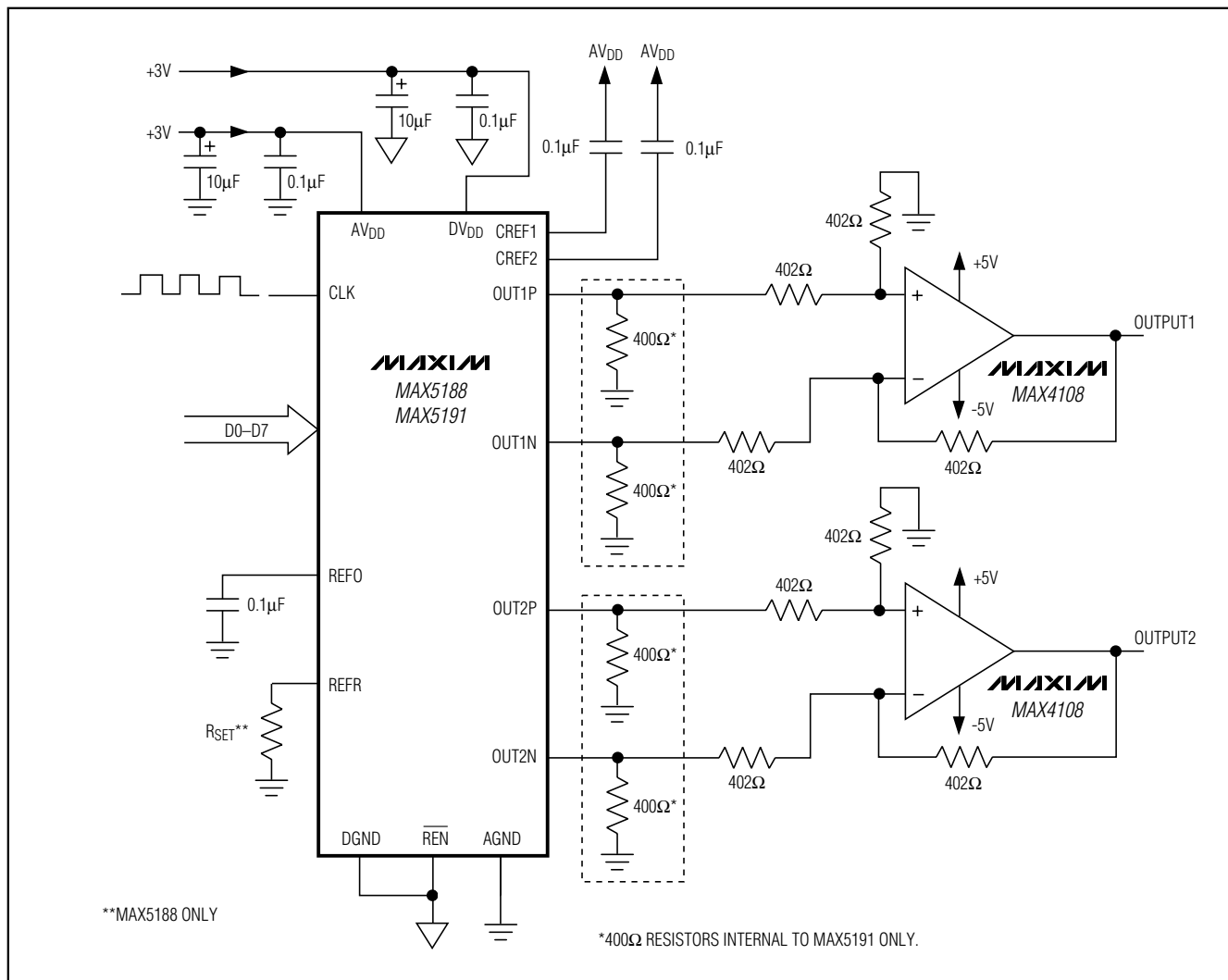


Figure 6. Differential to Single-Ended Conversion Using the MAX4108 Low-Distortion Amplifier

Chip Information

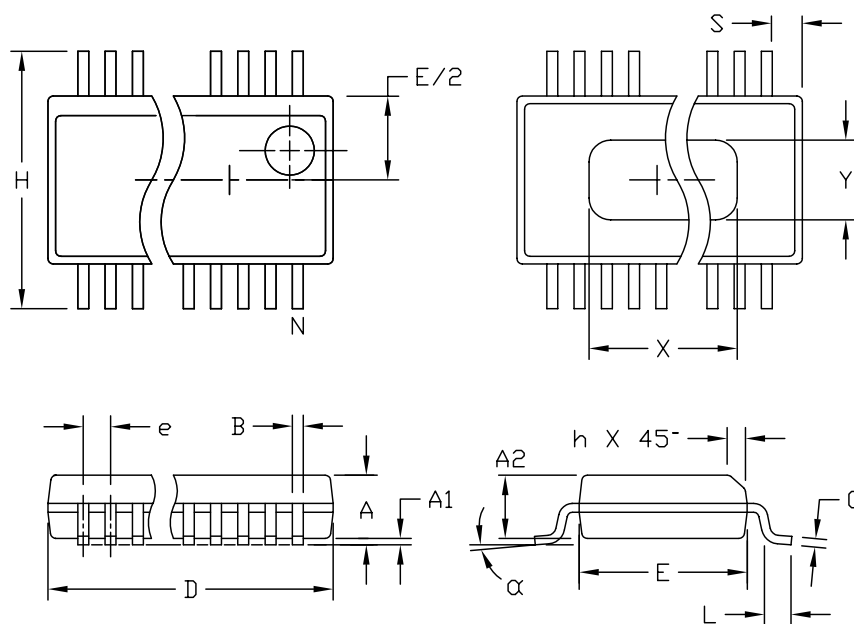
TRANSISTOR COUNT: 9464

SUBSTRATE CONNECTED TO GND

Dual, 8-Bit, 40MHz, Current/Voltage, Alternate-Phase Output DACs

Package Information

QSOP-EPS



NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
D	.189	.196	4.80	4.98	16 AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20 AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

MAXIM	
PROPRIETARY INFORMATION	
TITLE:	
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH	
APPROVAL	DOCUMENT CONTROL NO.
	21-0055
REV	1/1

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