Hi-performance Regulator IC Series for PCs

Termination Regulator for DDR-SDRAMs

BD35390FJ

No.09030EAT25

●Description

BD35390FJ is a termination regulator compatible with JEDEC DDR1/2/3-SDRAM, which functions as a linear power supply incorporating an N-channel MOSFET and provides a sink/source current capability up to 1A respectively. A built-in high-speed OP-AMP specially designed offers an excellent transient response. Requires 3.3 volts or 5.0 volts as a bias power supply to drive the N-channel MOSFET. Has an independent reference voltage input pin (VDDQ) and an independent feedback pin (VTTS) to maintain the accuracy in voltage required by JEDEC, and offers an excellent output voltage accuracy and load regulation.

●Features

1) Incorporates a push-pull power supply for termination (VTT)
2) Incorporates an enabler
3) Incorporates an under voltage lockout (UVLO)
4) Employs SOP-J8 package : 3.9×4.9×1.375(mm)
5) Incorporates a thermal shutdown protector (TSD)
6) Operates with input voltage from 2.7 to 5.5 volts
7) Compatible with Dual Channel (DDR1, DDR2, DDR3)
8) Incorporates PGOOD function

●Use

Power supply for DDR1/2/3 SDRAM

●Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Input Voltage	VCC	7 *1*2	V
Enable Input Voltage	VEN	7 *1*2	V
Termination Input Voltage	VTT_IN	7 *1*2	V
VDDQ Reference Voltage	VDDQ	7 *1*2	V
Output Current (when pulse is active*3)	ITT	1 *1	A
Power Dissipation1	Pd1	563 *4	mW
Power Dissipation2	Pd2	675 *5	mW
Operating Temperature Range	Topr	-30～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Voltage under less than 10u sec.
*4 Reduced by 4.50℃/W for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*5 Reduced by 5.40℃/W for each increase in Ta of 1℃ over 25℃ (when mounted on a 70mm×70mm×1.6mm glass epoxy board)

●Operating Conditions(Ta=25℃)

Parameter	Symbol	Limit		Unit
		MIN	MAX	
Input Voltage	VCC	2.7	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
VDDQ Reference Voltage	VDDQ	1.0	2.75	V
Enable Input Voltage	VEN	-0.3	5.5	V

●**Electrical Characteristics(Unless otherwise noted, Ta=25℃, VCC=3.3V, VEN=3V, VDDQ=1.8V, VTT_IN=1.8V)**

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	0.5	1.0	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	VEN=3V
[Enable]						
High Level Enable Input Voltage	VENHIGH	2.3	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	
Enable Pin Input Current	IEN	-	7	10	μA	VEN=3V
[Termination]						
Termination Output Voltage (DDR2)	VTT2	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	ITT=-1.0A to 1.0A Ta=0℃ to 100℃
Termination Output Voltage (DDR1)	VTT1	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	VCC = 5.3V, VDDQ = 2.5V VTT_IN = 2.5V ITT=-1.0A to 1.0A Ta=0℃ to 100℃
Termination Output Voltage (DDR3)	VTT3	1/2×VDDQ -15m	1/2×VDDQ	1/2×VDDQ +15m	V	VCC = 3.3V, VDDQ =1.5V VTT_IN =1.5V ITT=-1.0A to 1.0A Ta=0℃ to 100℃
Source current	ITT+	1.0	-	-	A	
Sink current	ITT-	-	-	-1.0	A	
Load Regulation	⊿VTT	-	-	50	mV	ITT=-1.0A to 1.0A
Upper Side ON Resistance	HRON	-	0.35	0.65	Ω	
Lower Side ON Resistance	LRON	-	0.35	0.65	Ω	
[VREF]						
Input Impedance	ZVDDQ	140	200	260	kΩ	
[PGOOD]						
VTT PGOOD Low Threshold voltage	PGDLow	-	1/2×VDDQ -30m	-	V	
VTT PGOOD High Threshold Voltage	PGDHigh	-	1/2×VDDQ +30m	-	V	
PGOOD output ON resistor	PGDRon	-	10	20	Ω	
PGOOD output leakage current	PGDleak	-	-	1	μA	PGOOD=6V
PGOOD delay time	PGDdelay	1	2	4	Ms	
[UVLO]						
Threshold Voltage	VUVLO	2.35	2.50	2.65	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	120	180	240	mV	VCC : sweep down

●Reference Data

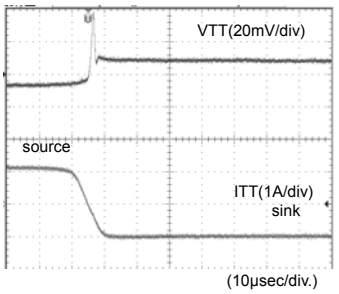


Fig.1 DDR3 (1A→-1A)

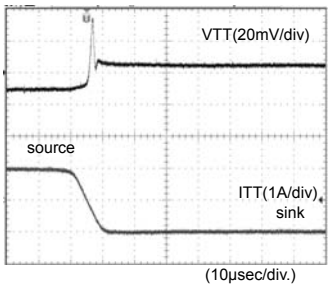


Fig.2 DDR2 (1A→-1A)

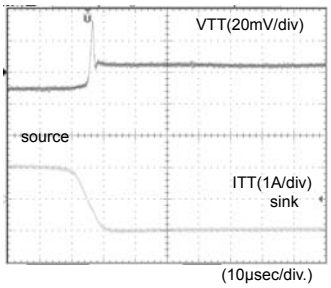


Fig.3 DDR1(1A→-1A)

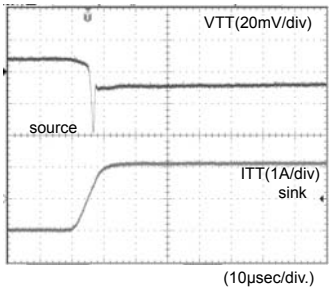


Fig.4 DDR3 (-1A→1A)

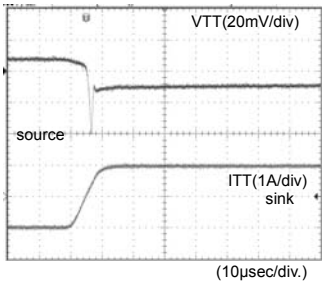


Fig.5 DDR2 (-1A→1A)

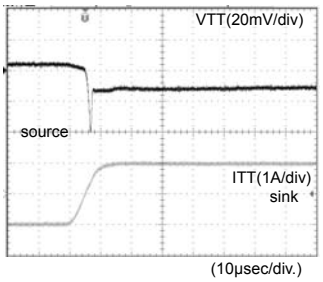


Fig.6 DDR1 (-1A→1A)

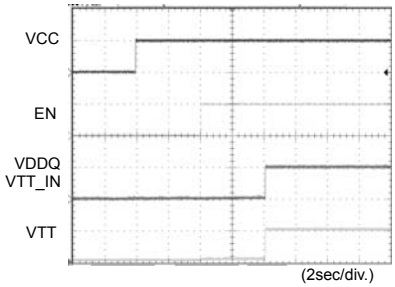


Fig.7 Input sequence1

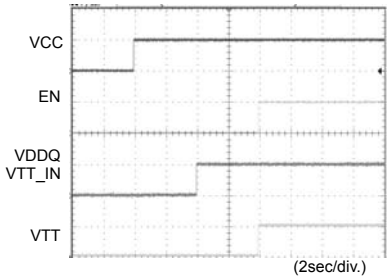


Fig.8 Input sequence2

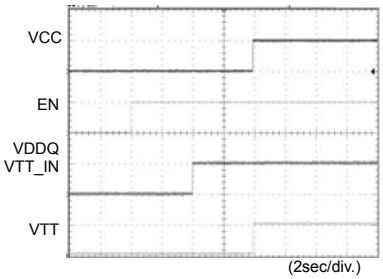


Fig.9 Input sequence3

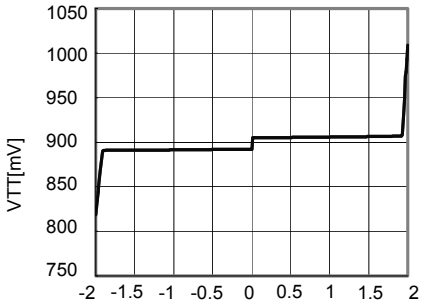


Fig.10 ITT-VTT(DDR2)

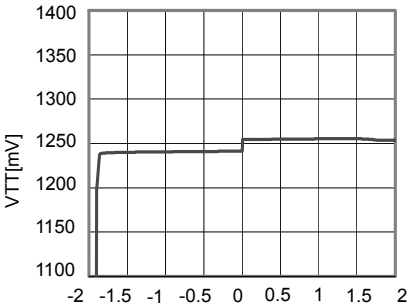


Fig.11 ITT-VTT(DDR1)

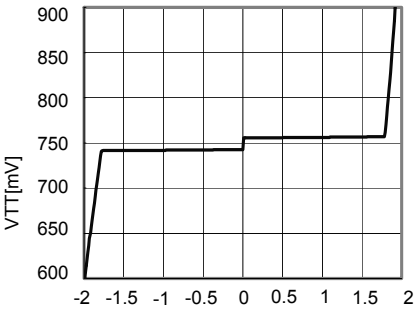


Fig.12 ITT-VTT(DDR3)

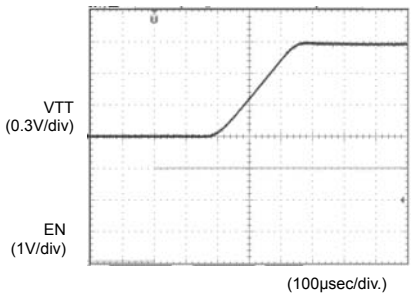


Fig.13 EN soft start
(DDR2)

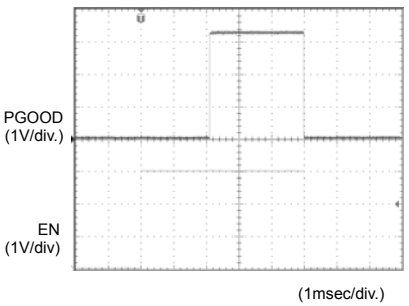


Fig.14 PGOOD Delay
(Start up-Shut down)

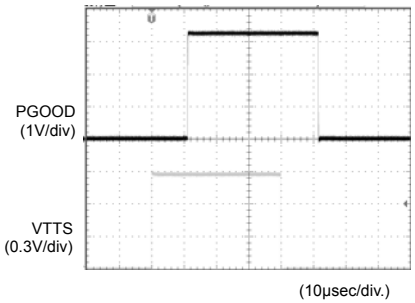
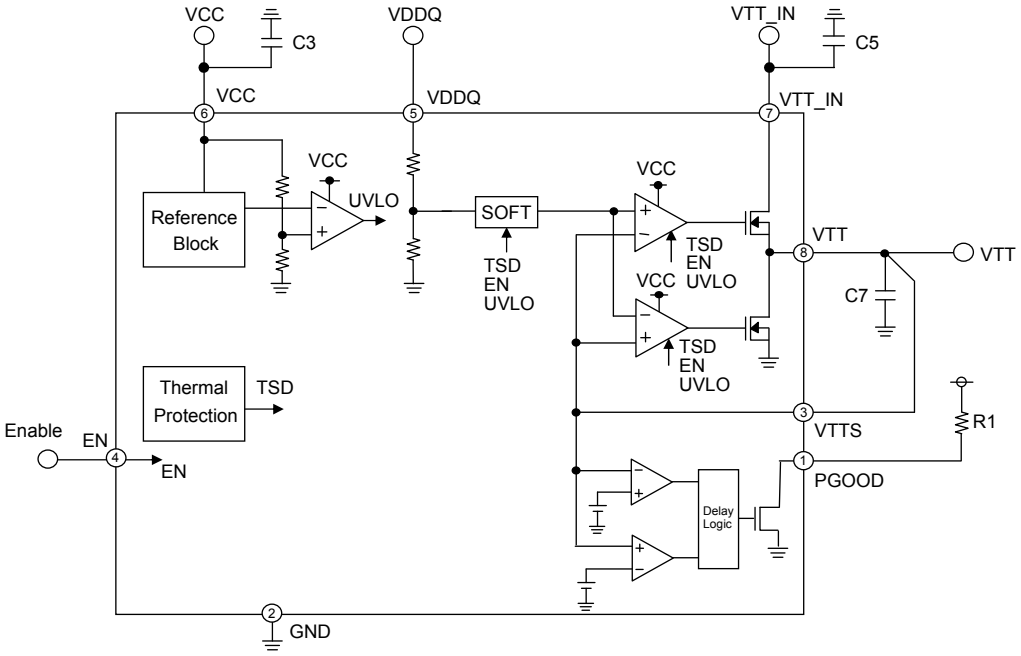
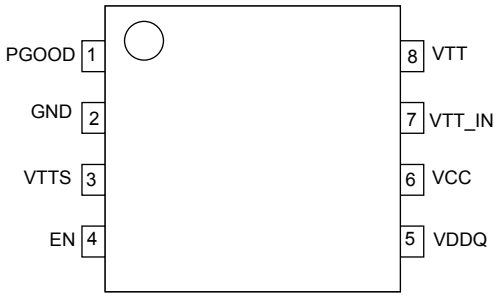


Fig.15 PGOOD Delay
(TSD OFF-TSD ON)

●Block Diagram



●Pin Configration



●Pin Function

PIN No.	PIN NAME	PIN FUNCTION
1	PGOOD	PGOOD output pin
2	GND	GND
3	VTTS	Detector Pin for Termination Voltage
4	EN	ENABLE input pin
5	VDDQ	Reference Voltage Input Pin
6	VCC	VCC Pin
7	VTT_IN	Termination power supply Pin
8	VTT	Termination Output Pin

●Description of operations

・VCC

In BD35390FJ, an independent power input pin is provided for an internal circuit operation of the IC. This is used to drive the amplifier circuit of the IC, and its maximum current rating is 4mA. The power supply voltage is 2.7 to 5.5 volts. It is recommended to connect a bypass capacitor of 1μF or so to VCC.

・VDDQ

Reference input pin for the output voltage that may be used to satisfy the JEDEC requirement for DDR1/2/3-SDRAM (VTT = 1/2VDDQ) by dividing the voltage inside the IC with two 100kΩ voltage-divider resistors.
For BD35390FJ, care must be taken to an input noise to VDDQ pin because this IC also cuts such noise input into half and provides it with the voltage output divided in half. Such noise may be reduced with an RC filter consisting of such resistance and capacitance (220Ω and 2.2μF, for instance) that may not give significant effect to voltage dividing inside the IC.

・VTT_IN

VTT_IN is a power supply input pin for VTT output. Voltage in the range between 1.0 and 5.5 volts may be supplied to this VTT_IN terminal, but care must be taken to the current limitation due to on-resistance of the IC and the change in allowable loss due to input/output voltage difference.
Generally, the following voltages are supplied:

- ・DDR1 VTT_IN=2.5V
- ・DDR2 VTT_IN=1.8V
- ・DDR3 VTT_IN=1.5V

Higher impedance of the voltage input at VTT_IN may result in oscillation or degradation in ripple rejection, which must be noted. To VTT_IN terminal, it is recommended to use a 10μF capacitor characterized with less change in capacitance. But it may depend on the characteristics of the power supply input and the impedance of the pc board wiring, which must be carefully checked before use.

・PGOOD

PGOOD pin is power good output pin. This is the open drain pin, so pull up resistor is connected via other power supply If VTT voltage becomes over 1/2 ×VDDQ+30mV,or under 1/2 ×VDDQ+30mV, it outputs High voltage.

・VTTS

An isolated pin provided to improve load regulation of VTT output. In case that longer wiring is needed to the load at VTT output, connecting VTTS from the load side may improve the load regulation.

・VTT

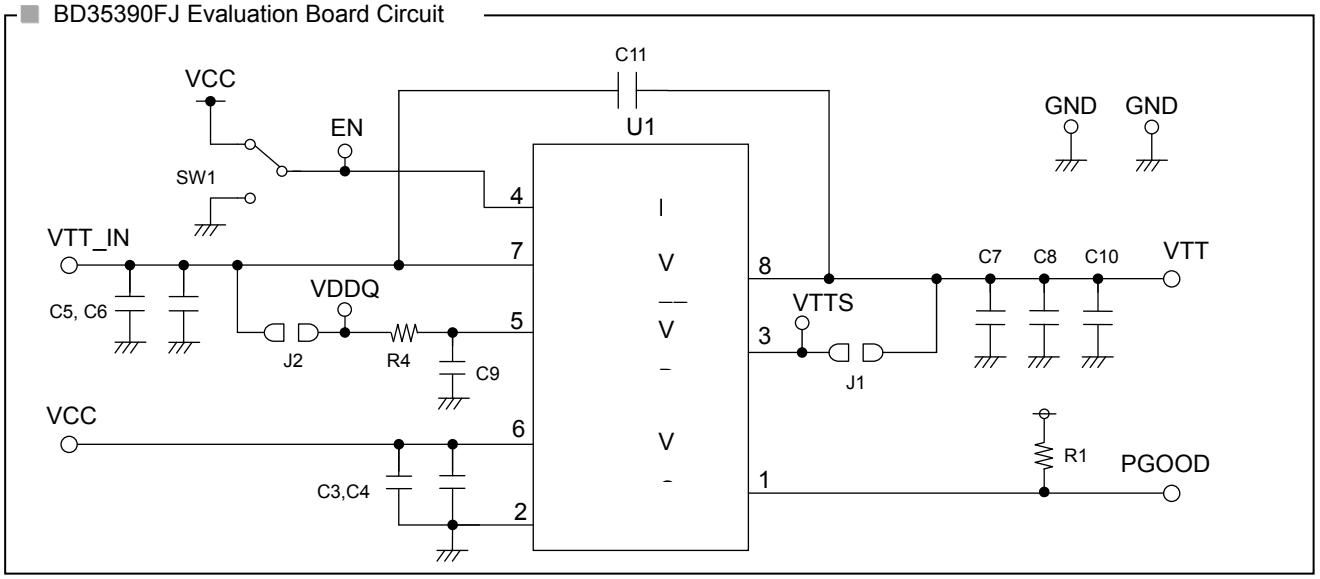
A DDR memory termination output pin. BD35390FJ has a sink/source current capability of ±1.0A respectively. The output voltage tracks the voltage divided in half at VDDQ pin. VTT output is turned to OFF when VCC UVLO or thermal shutdown protector is activated with EN pin level turned to “Low”. Do not fail to connect a capacitor to VTT output pin for a loop gain phase compensation and a reduction in output voltage variation in the event of sudden change in load. Insufficient capacitance may cause an oscillation. High ESR (Equivalent Series Resistance) of the capacitor may result in increase in output voltage variation in the event of sudden change in load. It is recommended to use a 10μF or so ceramic capacitor, though it depends on ambient temperature and other conditions.

・EN

With an input of 2.3 volts or higher, the level at EN pin turns to “High” to provide VTT output. If the input is lowered to 0.8 volts or less, the level at EN pin turns to “Low” and VTT status turns to Hi-Z.

●Evaluation Board

■ BD35390FJ Evaluation Board Circuit



■ BD35390FJ Evaluation Board Application Components

Designation	Value	Company	Part No.
U1	-	ROHM	BD35390FJ
R1	10kΩ	ROHM	MCR031002
R4	220Ω	ROHM	MCR032200
J1	0Ω	-	-
J2	0Ω	-	-
C3	1μF	KYOCERA	CM105B105K06A
C4	-	-	-

Designation	Value	Company	Part No.
C5	10μF	KYOCERA	CM21B106M06A
C6	-	-	-
C7	10μF	KYOCERA	CM21B106M06A
C8	-	-	-
C9	2.2μF	KYOCERA	CM105B225K06A
C10	-	-	-
C11	-	-	-

●Heat loss

Thermal design must be conducted with the operation under the conditions listed below (which are the guaranteed temperature range requiring consideration on appropriate margins etc);

1: Ambient temperature Ta: 100℃ or lower

2:Chip junction temperature Tj: 150℃ or lower

The chip junction temperature Tj can be considered as follows:

Most of heat loss in BD35390FJ occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between VIN and Vo by the output current. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

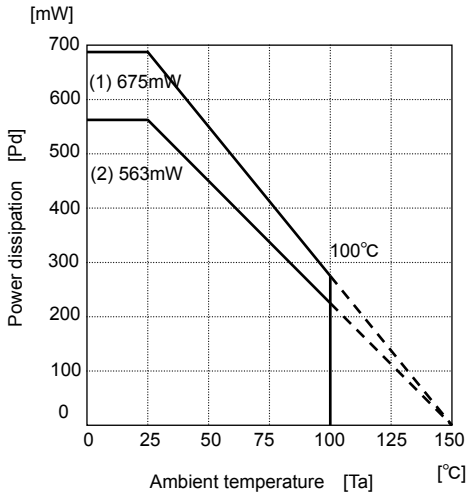
Power consumption (W) = Input voltage (V_{TT_IN})-Output voltage (V_{TT}≒1/2VDDQ) × Io(Ave)

Example) Where V_{TT_IN} =1.8V, VDDQ=1.8V, Io(Ave)= 0.5A

Power consumption(W) = $\{1.8(V)-0.9(V)\}$ × 0.5(A)

= 0.45(W)

●Heat dissipation characteristics



(1) mounted on 70mm × 70mm × 1.6mm glass-epoxy board
θj-c=185.2℃/W
(2) With no heat sink
θj-a=222.2℃/W

●Note for Use

1.Absolute maximum ratings

For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

2.GND potential

Bring the GND terminal potential to the minimum potential in any operating condition.

3.Thermal design

Consider allowable loss (Pd) under actual working condition and carry out thermal design with sufficient margin provided.

4.Terminal-to-terminal short-circuit and erroneous mounting

When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.

5.Operation in strong electromagnetic field

The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.

6.Built-in thermal shutdown protection circuit

The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15°C (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.

7.Capacitor across output and GND

In the event a large capacitor is connected across output and GND, when Vcc and VIN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000 μF between output and GND.

8.Inspection by set substrate

In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.

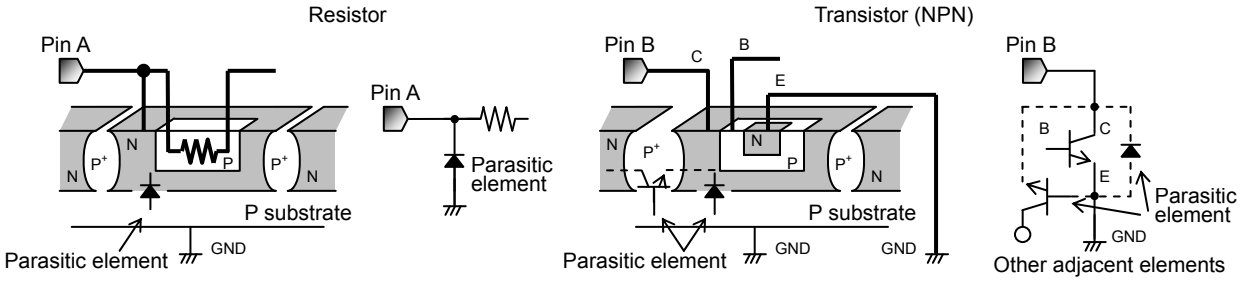
9. Inputs to IC terminals

This device is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a PN junction which works as:

・a diode if the electric potentials at the terminals satisfy the following relationship; GND>Terminal A>Terminal B, or

・a parasitic transistor if the electric potentials at the terminals satisfy the following relationship; Terminal B>GND Terminal A.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.



10. GND wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

11. Output capacitor (C7)
Do not fail to connect a capacitor to VTT output pin for stabilization of output voltage. This output capacitor works as a loop gain phase compensator and an output voltage variation reducer in the event of sudden change in load. Insufficient capacitance may cause an oscillation. And if the equivalent series resistance (ESR) of this capacitor is high, the variation in output voltage increases in the event of sudden change in load. It is recommended to use a 10μF or so ceramic capacitor, though it depends on ambient temperature and load conditions. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

12. Input capacitors setting (C3 and C5)
These input capacitors are used to reduce the output impedance of power supply to be connected to the input terminals (VCC and VTT_IN). Increase in the power supply output impedance may result in oscillation or degradation in ripple rejecting characteristics. It is recommended to use a low temperature coefficient 1μF (for VCC) and 10μF (for VTT_IN) capacitor, but it depends on the characteristics of the power supply input, and the capacitance and impedance of the pc board wiring pattern. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

13. Input terminals (VCC, VDDQ, VTT_IN and EN)
VCC, VDDQ, VTT_IN and EN terminals of this IC are made up independent one another. To VCC terminal, the UVLO function is provided for malfunction protection. Irrespective of the input order of the inputs terminals, VTT output is activated to provide the output voltage when UXLO and EN voltages reach the threshold voltage while VREF output is activated when UXLO voltage reaches the threshold. If VDDQ and VTT_IN terminals have equal potential and common impedance, any change in current at VTT_IN terminal may result in variation of VTT_IN voltage, which affects VDDQ terminal and may cause variation in the output voltage. It is therefore required to perform wiring in such manner that VDDQ and VTT_IN terminals may not have common impedance. If impossible, take appropriate corrective measures including suitable CR filter to be inserted between VDDQ and VTT_IN terminals.

14. VTTS terminal
A terminal used to improve load regulation of VTT output. Connection with VTT terminal must be done not to have common impedance with high current line, which may offer better load regulation of VTT output.

15. Operating range
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

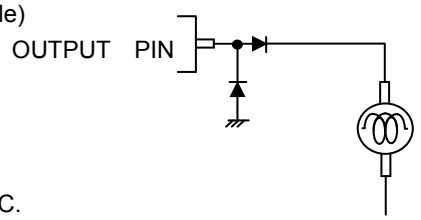
16. Allowable loss Pd
For the allowable loss, the thermal derating characteristics are shown in the Exhibit, which should be used as a guide. Any uses that exceed the allowable loss may result in degradation in the functions inherent to IC including a decrease in current capability due to chip temperature increase. Use within the allowable loss.

17. Thermal shut down circuits
This IC incorporates a built-in-thermal shutdown circuit, to prevent the IC from thermal breaking down. In thermal shut down circuit operation, VTT output turns to be OFF. The thermal shut down circuit is originally designed to protect he incorporated IC, so that thermal design needs to be designed below the temperature, which enables to run the thermal shut down circuits.

18. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.
In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

19. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)



20. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC.
In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.

●Ordering part number

B	D	3	5	3	9	0	F	J	-	E	2

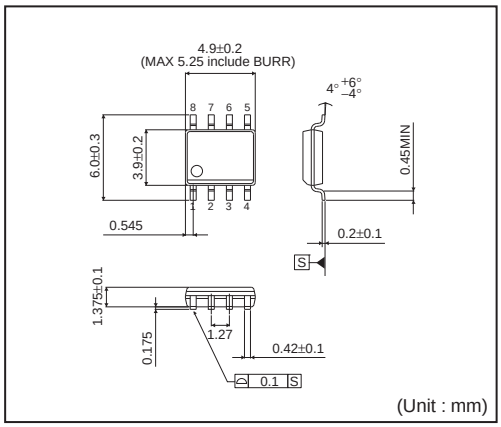
Part No.

Part No.
35390

Package
FJ : SOP-J8

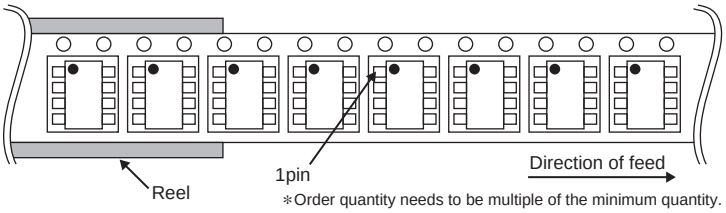
Packaging and forming specification
E2: Embossed tape and reel

SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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