

VSC8530-05 Datasheet
Single Port Industrial Grade Fast Ethernet Copper PHY
with RGMII/RMII Interfaces



a  MICROCHIP company

Contents

| | | |
|----------|--|----------|
| 1 | Revision History | 1 |
| 1.1 | Revision 4.0 | 1 |
| 2 | Overview | 2 |
| 2.1 | Key Features | 2 |
| 2.1.1 | Superior PHY and Interface Technology | 2 |
| 2.1.2 | Fast Link Up/Link Drop Modes | 2 |
| 2.1.3 | Best-in-Class Power Consumption | 2 |
| 2.1.4 | Key Specifications | 2 |
| 2.2 | Block Diagram | 3 |
| 3 | Functional Descriptions | 4 |
| 3.1 | Operating Modes | 4 |
| 3.2 | MAC Interface | 4 |
| 3.2.1 | RGMII MAC Interface Mode | 4 |
| 3.2.2 | RMII Mode | 5 |
| 3.2.3 | MAC Interface Edge Rate Control | 7 |
| 3.3 | Hardware Mode Strapping and PHY Addressing | 8 |
| 3.3.1 | CLKOUT Signal Configuration | 8 |
| 3.3.2 | Managed Mode | 8 |
| 3.3.3 | Unmanaged Mode | 9 |
| 3.4 | Cat5 Twisted Pair Media Interface | 10 |
| 3.4.1 | Voltage Mode Line Driver | 10 |
| 3.4.2 | Cat5 Auto-Negotiation and Parallel Detection | 10 |
| 3.4.3 | Automatic Crossover and Polarity Detection | 10 |
| 3.4.4 | Manual MDI/MDIX Setting | 11 |
| 3.4.5 | Energy-Efficient Ethernet | 11 |
| 3.5 | Reference Clock | 12 |
| 3.6 | Ethernet Inline-Powered Devices | 13 |
| 3.7 | IEEE 802.3af Power-over-Ethernet Support | 14 |
| 3.8 | ActiPHY Power Management | 14 |
| 3.8.1 | Low Power State | 15 |
| 3.8.2 | Link Partner Wake-Up State | 15 |
| 3.8.3 | Normal Operating State | 15 |
| 3.9 | Serial Management Interface | 15 |
| 3.9.1 | SMI Frames | 16 |
| 3.9.2 | SMI Interrupt | 16 |
| 3.10 | LED Interface | 17 |
| 3.10.1 | LED Modes | 17 |
| 3.10.2 | Basic Serial LED Mode | 18 |
| 3.10.3 | Extended LED Modes | 19 |
| 3.10.4 | LED Behavior | 19 |
| 3.11 | Wake-On-LAN and SecureOn | 20 |
| 3.12 | Fast Link Failure Indication | 20 |
| 3.13 | Forced Speed Mode Link-Up Timing | 21 |
| 3.14 | Testing Features | 21 |
| 3.14.1 | Ethernet Packet Generator | 21 |
| 3.14.2 | Far-End Loopback | 21 |
| 3.14.3 | Near-End Loopback | 22 |
| 3.14.4 | Connector Loopback | 22 |

| | | |
|----------|---|-----------|
| 3.14.5 | VeriPHY Cable Diagnostics | 22 |
| 3.15 | Configuration | 23 |
| 3.15.1 | Managed Applications | 23 |
| 3.15.2 | Unmanaged Applications | 23 |
| 4 | Registers | 24 |
| 4.1 | Register and Bit Conventions | 24 |
| 4.2 | IEEE 802.3 and Main Registers | 25 |
| 4.2.1 | Mode Control | 26 |
| 4.2.2 | Mode Status | 27 |
| 4.2.3 | Device Identification | 27 |
| 4.2.4 | Auto-Negotiation Advertisement | 28 |
| 4.2.5 | Link Partner Auto-Negotiation Capability | 28 |
| 4.2.6 | Auto-Negotiation Expansion | 29 |
| 4.2.7 | Transmit Auto-Negotiation Next Page | 29 |
| 4.2.8 | Auto-Negotiation Link Partner Next Page Receive | 29 |
| 4.2.9 | MMD Access Control Register | 30 |
| 4.2.10 | MMD Address or Data Register | 30 |
| 4.2.11 | 100BASE-TX Status Extension | 30 |
| 4.2.12 | Bypass Control | 31 |
| 4.2.13 | Error Counter 1 | 31 |
| 4.2.14 | Error Counter 2 | 31 |
| 4.2.15 | Error Counter 3 | 32 |
| 4.2.16 | Extended Control and Status | 32 |
| 4.2.17 | Extended PHY Control 1 | 33 |
| 4.2.18 | Extended PHY Control 2 | 33 |
| 4.2.19 | Interrupt Mask | 34 |
| 4.2.20 | Interrupt Status | 35 |
| 4.2.21 | Device Auxiliary Control and Status | 35 |
| 4.2.22 | LED Mode Select | 36 |
| 4.2.23 | LED Behavior | 37 |
| 4.2.24 | Extended Page Access | 37 |
| 4.3 | Extended Page 1 Registers | 38 |
| 4.3.1 | VeriPHY Status 1 | 38 |
| 4.3.2 | Cu Media CRC Good Counter | 38 |
| 4.3.3 | Extended Mode Control | 39 |
| 4.3.4 | ActiPHY Control | 39 |
| 4.3.5 | PoE and Miscellaneous Functionality | 40 |
| 4.3.6 | VeriPHY Control 1 | 40 |
| 4.3.7 | VeriPHY Control 2 | 41 |
| 4.3.8 | VeriPHY Control 3 | 41 |
| 4.3.9 | Ethernet Packet Generator (EPG) Control 1 | 42 |
| 4.3.10 | Ethernet Packet Generator Control 2 | 42 |
| 4.4 | Extended Page 2 Registers | 43 |
| 4.4.1 | Cu PMD Transmit Control | 43 |
| 4.4.2 | EEE Control | 45 |
| 4.4.3 | RGMIIC Control | 46 |
| 4.4.4 | Wake-on-LAN MAC Address [15:0] | 47 |
| 4.4.5 | Wake-on-LAN MAC Address [31:16] | 47 |
| 4.4.6 | Wake-on-LAN MAC Address [47:32] | 47 |
| 4.4.7 | Secure-On Password [15:0] | 47 |
| 4.4.8 | Secure-On Password [31:16] | 48 |
| 4.4.9 | Secure-On Password [47:32] | 48 |
| 4.4.10 | Wake-on-LAN and MAC Interface Control | 48 |
| 4.4.11 | Extended Interrupt Mask | 49 |
| 4.4.12 | Extended Interrupt Status | 49 |
| 4.5 | General Purpose Registers | 50 |

| | | |
|----------|--|-----------|
| 4.5.1 | CLKOUT Control | 50 |
| 4.5.2 | GPIO Control 2 | 50 |
| 4.5.3 | Enhanced LED Control | 51 |
| 4.6 | Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf | 51 |
| 4.6.1 | PMA/PMD Status 1 | 52 |
| 4.6.2 | PCS Status 1 | 52 |
| 4.6.3 | EEE Capability | 52 |
| 4.6.4 | EEE Wake Error Counter | 52 |
| 4.6.5 | EEE Advertisement | 53 |
| 4.6.6 | EEE Link Partner Advertisement | 53 |
| 4.6.7 | 802.3bf Registers | 53 |
| 5 | Electrical Specifications | 54 |
| 5.1 | DC Characteristics | 54 |
| 5.1.1 | VDDMAC, VDDIO, and VDDMDIO (2.5 V) | 54 |
| 5.1.2 | VDDMAC, VDDIO, and VDDMDIO (3.3 V) | 54 |
| 5.1.3 | VDDMAC and VDDMDIO (1.5 V) | 55 |
| 5.1.4 | VDDMAC and VDDMDIO (1.8 V) | 55 |
| 5.1.5 | VDDMDIO (1.2 V) | 55 |
| 5.1.6 | XTAL1 | 56 |
| 5.1.7 | LED | 56 |
| 5.1.8 | Internal Pull-Up or Pull-Down Resistors | 56 |
| 5.1.9 | Current Consumption | 56 |
| 5.2 | AC Characteristics | 57 |
| 5.2.1 | Reference Clock | 57 |
| 5.2.2 | CLKOUT | 58 |
| 5.2.3 | RMII_CLKOUT | 59 |
| 5.2.4 | Basic Serial LEDs | 59 |
| 5.2.5 | RMII AC Characteristics | 60 |
| 5.2.6 | Uncompensated RGMII | 60 |
| 5.2.7 | Compensated RGMII | 61 |
| 5.2.8 | Serial Management Interface | 62 |
| 5.2.9 | Reset Timing | 63 |
| 5.3 | Operating Conditions | 63 |
| 5.4 | Stress Ratings | 64 |
| 6 | Pin Descriptions | 65 |
| 6.1 | Pin Identifications | 65 |
| 6.2 | Pin Diagram | 65 |
| 6.3 | Pins by Function | 66 |
| 7 | Package Information | 70 |
| 7.1 | Package Drawing | 70 |
| 7.2 | Thermal Specifications | 71 |
| 7.3 | Moisture Sensitivity | 72 |
| 8 | Design Considerations | 73 |
| 8.1 | 10BASE-T signal amplitude | 73 |
| 8.2 | Receive error counter only clears when NRESET applied in RMII mode | 73 |
| 8.3 | Anomalous PCS error indications in Energy Efficient Ethernet mode | 73 |
| 9 | Ordering Information | 74 |

Figures

| | | |
|-----------|--|----|
| Figure 1 | Application Diagram | 2 |
| Figure 2 | Block Diagram | 3 |
| Figure 3 | RGMII MAC Interface | 5 |
| Figure 4 | RMII MAC Interface | 5 |
| Figure 5 | Mode 1 | 6 |
| Figure 6 | Mode 2 | 7 |
| Figure 7 | Cat5 Media Interface | 10 |
| Figure 8 | Low Power Idle Operation | 11 |
| Figure 9 | XTAL Reference Clock | 12 |
| Figure 10 | External 3.3 V Reference Clock | 12 |
| Figure 11 | Inline-Powered Ethernet Switch Diagram | 13 |
| Figure 12 | ActiPHY State Diagram | 15 |
| Figure 13 | SMI Read Frame | 16 |
| Figure 14 | SMI Write Frame | 16 |
| Figure 15 | MDINT Configured as an Open-Drain (Active-Low) Pin | 17 |
| Figure 16 | Wake-on-LAN Functionality | 20 |
| Figure 17 | Far-End Loopback Diagram | 22 |
| Figure 18 | Near-End Loopback Diagram | 22 |
| Figure 19 | Connector Loopback Diagram | 22 |
| Figure 20 | Register Space Diagram | 24 |
| Figure 21 | Test Circuit for Clock Output Signal | 58 |
| Figure 22 | Basic Serial LED Timing | 60 |
| Figure 23 | Uncompensated RGMII Timing | 61 |
| Figure 24 | Compensated Input RGMII Timing | 62 |
| Figure 25 | Compensated Output RGMII Timing | 62 |
| Figure 26 | Serial Management Interface Timing | 63 |
| Figure 27 | Pin Diagram | 66 |
| Figure 28 | Package Drawing | 71 |

Tables

| | | |
|----------|---|----|
| Table 1 | Operating Modes | 4 |
| Table 2 | Recommended Values for R_S ($\pm 5\%$) | 4 |
| Table 3 | RMII Pin Allocation | 5 |
| Table 4 | Recommended Edge Rate Settings | 7 |
| Table 5 | MAC Interface Edge Rate Control | 7 |
| Table 6 | Hardware Mode Strapping and PHY Addressing | 8 |
| Table 7 | Managed Mode | 8 |
| Table 8 | Signals A and B | 9 |
| Table 9 | Signals C and D | 9 |
| Table 10 | Supported MDI Pair Combinations | 11 |
| Table 11 | REFCLK Frequency Selection | 12 |
| Table 12 | LED Drive State | 17 |
| Table 13 | LED Mode and Function Summary | 17 |
| Table 14 | LED Serial Bitstream Order | 18 |
| Table 15 | Extended LED Mode and Function Summary | 19 |
| Table 16 | Forced Speed Mode Link-Up Timing | 21 |
| Table 17 | IEEE 802.3 Registers | 25 |
| Table 18 | Main Registers | 25 |
| Table 19 | Mode Control, Address 0 (0x00) | 26 |
| Table 20 | Mode Status, Address 1 (0x01) | 27 |
| Table 21 | Identifier 1, Address 2 (0x02) | 27 |
| Table 22 | Identifier 2, Address 3 (0x03) | 27 |
| Table 23 | Device Auto-Negotiation Advertisement, Address 4 (0x04) | 28 |
| Table 24 | Auto-Negotiation Link Partner Ability, Address 5 (0x05) | 28 |
| Table 25 | Auto-Negotiation Expansion, Address 6 (0x06) | 29 |
| Table 26 | Auto-Negotiation Next Page Transmit, Address 7 (0x07) | 29 |
| Table 27 | Auto-Negotiation LP Next Page Receive, Address 8 (0x08) | 29 |
| Table 28 | MMD EEE Access, Address 13 (0x0D) | 30 |
| Table 29 | MMD Address or Data Register, Address 14 (0x0E) | 30 |
| Table 30 | 100BASE-TX Status Extension, Address 16 (0x10) | 30 |
| Table 31 | Bypass Control, Address 18 (0x12) | 31 |
| Table 32 | Extended Control and Status, Address 19 (0x13) | 31 |
| Table 33 | Extended Control and Status, Address 20 (0x14) | 31 |
| Table 34 | Extended Control and Status, Address 21 (0x15) | 32 |
| Table 35 | Extended Control and Status, Address 22 (0x16) | 32 |
| Table 36 | Extended PHY Control 1, Address 23 (0x17) | 33 |
| Table 37 | Extended PHY Control 2, Address 24 (0x18) | 33 |
| Table 38 | Interrupt Mask, Address 25 (0x19) | 34 |
| Table 39 | Interrupt Status, Address 26 (0x1A) | 35 |
| Table 40 | Auxiliary Control and Status, Address 28 (0x1C) | 35 |
| Table 41 | LED Mode Select, Address 29 (0x1D) | 36 |
| Table 42 | LED Behavior, Address 30 (0x1E) | 37 |
| Table 43 | Extended/GPIO Register Page Access, Address 31 (0x1F) | 37 |
| Table 44 | Extended Registers Page 1 Space | 38 |
| Table 45 | VeriPHY Status Register 1, Address 16E1 (0x10) | 38 |
| Table 46 | Cu Media CRC Good Counter, Address 18E1 (0x12) | 38 |
| Table 47 | Extended Mode Control, Address 19E1 (0x13) | 39 |
| Table 48 | Extended PHY Control 3, Address 20E1 (0x14) | 39 |
| Table 49 | Extended PHY Control 4, Address 23E1 (0x17) | 40 |
| Table 50 | VeriPHY Control Register 1, Address 24E1 (0x18) | 40 |
| Table 51 | VeriPHY Control Register 2, Address 25E1 (0x19) | 41 |
| Table 52 | VeriPHY Control Register 3, Address 26E1 (0x1A) | 41 |
| Table 53 | VeriPHY Control Register 3 Fault Codes | 41 |
| Table 54 | EPG Control Register 1, Address 29E1 (0x1D) | 42 |

| | | |
|-----------|--|----|
| Table 55 | EPG Control Register 2, Address 30E1 (0x1E) | 42 |
| Table 56 | Extended Registers Page 2 Space | 43 |
| Table 57 | Cu PMD Transmit Control, Address 16E2 (0x10) | 43 |
| Table 58 | EEE Control, Address 17E2 (0x11) | 45 |
| Table 59 | RGMII Control, Address 20E2 (0x14) | 46 |
| Table 60 | Wake-on-LAN MAC Address, 21E2 (0x15) | 47 |
| Table 61 | Wake-on-LAN MAC Address, 22E2 (0x16) | 47 |
| Table 62 | Wake-on-LAN MAC Address, 23E2 (0x17) | 47 |
| Table 63 | Secure-On Password, 24E2 (0x18) | 47 |
| Table 64 | Secure-On Password, 25E2 (0x19) | 48 |
| Table 65 | Secure-On Password, 26E2 (0x1A) | 48 |
| Table 66 | WoL and MAC Interface Control, Address 27E2 (0x1B) | 48 |
| Table 67 | Extended Interrupt Mask, Address 28E2 (0x1C) | 49 |
| Table 68 | Extended Interrupt Status, Address 29E2 (0x1D) | 49 |
| Table 69 | General Purpose Registers Space | 50 |
| Table 70 | CLKOUT Control, Address 13G (0x0D) | 50 |
| Table 71 | GPIO Control 2, Address 14G (0x0E) | 50 |
| Table 72 | Enhanced LED Control, Address 25G (0x19) | 51 |
| Table 73 | Clause 45 Registers Page Space | 51 |
| Table 74 | PMA/PMD Status 1 | 52 |
| Table 75 | PCS Status 1, Address 3.1 | 52 |
| Table 76 | EEE Capability, Address 3.20 | 52 |
| Table 77 | EEE Wake Error Counter, Address 3.22 | 53 |
| Table 78 | EEE Advertisement, Address 7.60 | 53 |
| Table 79 | EEE Advertisement, Address 7.61 | 53 |
| Table 80 | 802.3bf Registers | 53 |
| Table 81 | VDDMAC, VDDIO, and VDDMDIO (2.5 V) DC Characteristics | 54 |
| Table 82 | VDDMAC, VDDIO, and VDDMDIO (3.3 V) DC Characteristics | 54 |
| Table 83 | VDDMAC and VDDMDIO DC Characteristics (1.5 V) | 55 |
| Table 84 | VDDMAC and VDDMDIO DC Characteristics (1.8 V) | 55 |
| Table 85 | VDDMDIO DC Characteristics | 55 |
| Table 86 | XTAL1 DC Characteristics | 56 |
| Table 87 | LED DC Characteristics | 56 |
| Table 88 | Internal Pull-Up or Pull-Down Resistors (RGMII/RMII Interface) | 56 |
| Table 89 | Internal Pull-Up or Pull-Down Resistors (Other I/Os) | 56 |
| Table 90 | Current Consumption | 57 |
| Table 91 | Current Consumption (VDDMAC) | 57 |
| Table 92 | Power Consumption | 57 |
| Table 93 | RefClk | 57 |
| Table 94 | XTAL RefClk | 58 |
| Table 95 | CLKOUT AC Characteristics | 59 |
| Table 96 | RMII_CLKOUT AC Characteristics | 59 |
| Table 97 | Basic Serial LEDs AC Characteristics | 59 |
| Table 98 | RMII AC Characteristics | 60 |
| Table 99 | Uncompensated RGMII AC Characteristics | 60 |
| Table 100 | PHY Input (GTX_CLK Delay When Register 20E2.[2:0]=011'b) | 61 |
| Table 101 | PHY Output (RX_CLK Delay When Register 20E2.[6:4]=100'b) | 62 |
| Table 102 | Serial Management Interface AC Characteristics | 62 |
| Table 103 | Reset Timing AC Characteristics | 63 |
| Table 104 | Recommended Operating Conditions | 63 |
| Table 105 | Stress Ratings | 64 |
| Table 106 | Pin Type Symbol Definitions | 65 |
| Table 107 | Thermal Resistances | 72 |
| Table 108 | Ordering Information | 74 |

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 of this document was published in November 2018. This was the first publication.

2 Overview

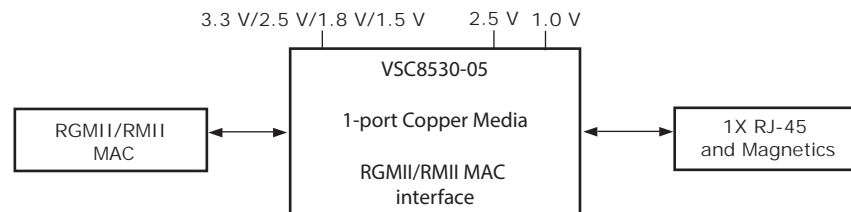
The VSC8530-05 device is designed for space-constrained 10/100BASE-TX applications. It features integrated, line-side termination to conserve board space, lower EMI, and improve system performance. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines.

Microsemi's EcoEthernet™ v2.0 technology supports IEEE 802.3az Energy-Efficient Ethernet (EEE) and power-saving features to reduce power based on link state and cable reach. VSC8530-05 optimizes power consumption in all link operating speeds and features a Wake-on-LAN (WoL) power management mechanism for bringing the PHY out of a low-power state using designated magic packets.

Fast link failure (FLF) indication for high availability networks identifies the onset of a link failure for 100BASE-TX links.

The following illustration shows a high-level, general view of a typical VSC8530-05 application.

Figure 1 • Application Diagram



2.1 Key Features

This section lists the main features and benefits of the VSC8530-05 device.

2.1.1 Superior PHY and Interface Technology

- Integrated 10/100BASE-TX Ethernet copper transceiver with the industry's only non-TDR-based VeriPHY™ cable diagnostics algorithm
- Patented line driver with low EMI voltage mode architecture and integrated line-side termination resistors
- Wake-on-LAN using magic packets
- HP Auto-MDIX and manual MDI/MDIX support
- RGMII/RMII MAC interface
- Jumbo frame support up to 16 kilobytes with programmable synchronization FIFOs

2.1.2 Fast Link Up/Link Drop Modes

- Fast link failure indication

2.1.3 Best-in-Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy-Efficient Ethernet
- Fully optimized power consumption for all link speeds
- Clause 45 registers to support Energy-Efficient Ethernet

2.1.4 Key Specifications

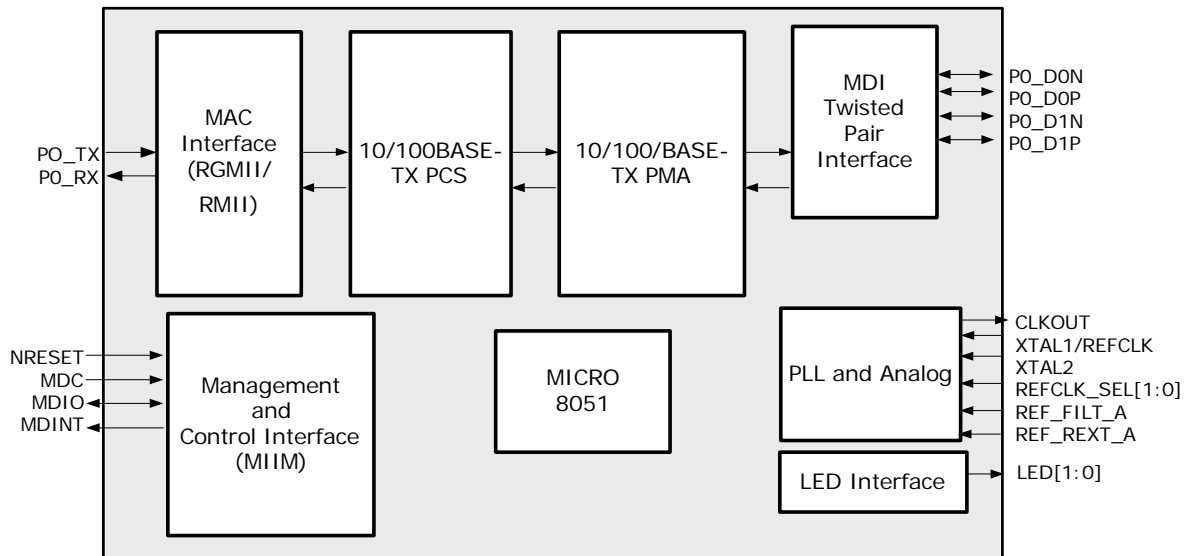
- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX) specifications
- Supports RGMII, RMII
- Supports 1.5 V, 1.8 V, 2.5 V, and 3.3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 50 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz, or 125 MHz, regardless of chosen Xtal or OSC frequencies
- Supports a wide array of stand-alone hardware configuration options

- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors
- Device supports operating temperature of -40 °C ambient to 125 °C junction
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 6 mm x 6 mm, 48-pin QFN package

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8530-05 device.

Figure 2 • Block Diagram



3 Functional Descriptions

This section describes the functional aspects of the VSC8530-05 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

3.1 Operating Modes

The following table lists the operating modes of the VSC8530-05 device.

Table 1 • Operating Modes

| Operating Mode | Supported Media |
|----------------|-----------------|
| RGMII-Cat5 | 10/100BASE-TX |
| RMII-Cat5 | 10/100BASE-TX |

3.2 MAC Interface

The VSC8530-05 device supports RMII version 1.2 and RGMII versions 1.3 and 2.0, and MAC interfaces at 1.5 V, 1.8 V, 2.5 V, and 3.3 V operating voltages. In order to help reduce EMI, the VSC8530-05 device also includes edge rate programmability for the MAC interface signals through register 27E2.7:5.

The recommended values for R_S (as shown in [Figure 3](#), page 5, [Figure 5](#), page 6, and [Figure 6](#), page 7) are listed in the following table.

Table 2 • Recommended Values for R_S ($\pm 5\%$)

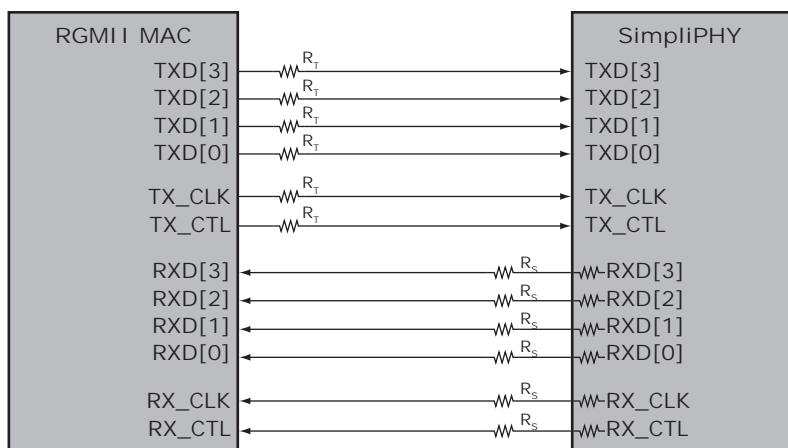
| VDDMAC Value | R_S Value |
|--------------|-------------|
| 1.5 V | 27 Ω |
| 1.8 V | 33 Ω |
| 2.5 V | 39 Ω |
| 3.3 V | 39 Ω |

Refer to the MAC datasheet for the value to use for R_T .

3.2.1 RGMII MAC Interface Mode

The VSC8530-05 device supports RGMII versions 1.3 and 2.0 (without HSTL modes). The RGMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RGMII-compatible MAC. The device is compliant with the RGMII interface specification when VDDMAC is operating at 2.5 V. While the RGMII specification only specifies operation at 2.5 V, the device can also support the RGMII interface at 1.5 V, 1.8 V, and 3.3 V.

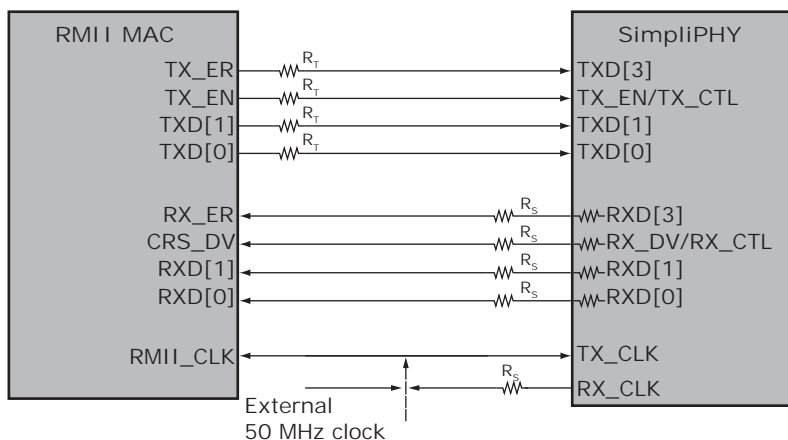
Figure 3 • RGMII MAC Interface



3.2.2 RMII Mode

The RMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RMII-compatible MAC. The device is compliant with the RMII interface specification when VDDMAC is operating at 3.3 V. While the RMII specification only specifies operation at 3.3 V, the device can also support the RMII interface at 1.5 V, 1.8 V, and 2.5 V.

Figure 4 • RMII MAC Interface



3.2.2.1 RMII Pin Allocation

The following table lists the chip pins used for RMII signaling in RMII mode.

Table 3 • RMII Pin Allocation

| Chip Pin | RMII Signal |
|----------|----------------------------|
| TX_CLK | RMII_CLKIN |
| RX_CLK | RMII_CLKOUT |
| TXD3 | TX_ER (to support 802.3az) |
| TXD1 | TXD1 |
| TXD0 | TXD0 |
| TX_CTL | TX_EN |
| RXD1 | RXD1 |

Table 3 • RMI Pin Allocation (continued)

| Chip Pin | RMI Signal |
|----------|------------|
| RXD0 | RXD0 |
| RXD3 | RX_ER |
| RX_CTL | CRS_DV |

Even though the RMI specification does not call for the use of TX_ER signal, it is required in order to support Energy-Efficient Ethernet (802.3az).

3.2.2.2 RMI Clocking Overview

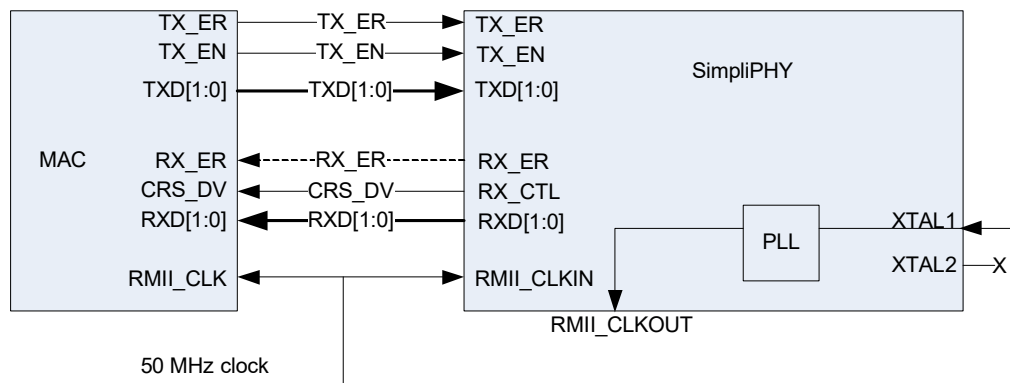
When the device is in RMI mode, the clock inputs to the device need to support the various modes in which RMI devices can operate. There are two basic modes of operation in RMI mode:

- Mode 1—system provides a 50 MHz clock that is used to clock the RMI interface and must be used as the chip reference clock.
- Mode 2—PHY operates from a 25 MHz or 125 MHz reference clock, and sources the 50 MHz clock used for the RMI interface.

These two modes of operation and the clocking schemes are described in the following sections.

3.2.2.2.1 Mode 1

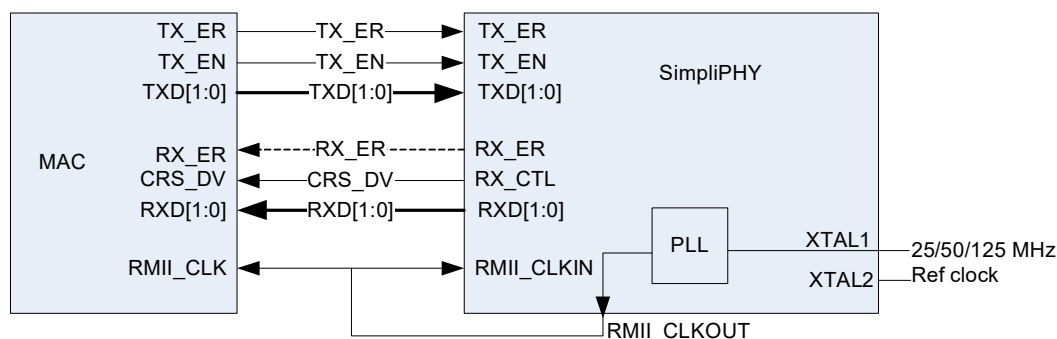
In this mode of operation, an external source is used to provide a 50 MHz clock through the RMI_CLKIN and the XTAL1 pin. This 50 MHz clock is used as the main clock for the RMI interface, and must be used as the reference clock for the PHY connected to the XTAL1 pin. In this mode, the RMI_CLKOUT signal from the PHY is not used. The RMI_CLKOUT is enabled by default and that clock output should be disabled through register 27E2.4. The following figure illustrates RMI signal connections at the system level.

Figure 5 • Mode 1

3.2.2.2.2 Mode 2

In this mode of operation, the PHY operates from a 25 MHz crystal (XTAL1 and XTAL2) or 25 MHz/125 MHz single-ended external clock (XTAL1), and sources the 50 MHz clock required for the RMI interface. This 50 MHz clock is output from the PHY on the RMI_CLKOUT pin and then connected to the MAC and PHY RMI_CLKIN signals. In this mode, the PHY generates a 50 MHz clock for the system and that clock output is enabled. The following figure illustrates RMI signal connections at the system level.

Figure 6 • Mode 2



3.2.3 MAC Interface Edge Rate Control

The VSC8530-05 device includes programmable control of the rise/fall times for the MAC interface signals. The default setting will select the fastest rise/fall times. However, the fast edge rate will result in higher power consumption on the MAC interface and may result in higher EMI.

It is recommended that the user select the appropriate edge rate setting based on the VDDMAC supply voltage, as shown in the following table.

Table 4 • Recommended Edge Rate Settings

| VDDMAC Voltage | Edge Rate Setting |
|----------------|-------------------|
| 3.3 V | 100 |
| 2.5 V | 100 |
| 1.8 V | 111 |
| 1.5 V | 111 |

In order to further reduce power consumption and EMI, the user may elect to choose a slower edge rate than recommended if the end application supports it.

The MAC interface signal rise/fall times can be changed by writing to register bits 27E2.7:5. The typical change in edge rate for each setting at various VDDMAC voltages is shown in the following table.

Table 5 • MAC Interface Edge Rate Control

| Register Setting | Edge Rate Change (VDDMAC) | | | |
|------------------|---------------------------|-----------------------|--------------------------|--------------------------|
| | 3.3 V | 2.5 V | 1.8 V | 1.5 V |
| 111 (fastest) | Default | Default | Default (recommended) | Default (recommended) |
| 110 | -2% | -3% | -5% | -6% |
| 101 | -4% | -6% | -9% | -14% |
| 100 | -7% (recommended) | -10% (recommended) | -16% | -21% |
| 011 | -10% | -14% | -23% | -29% |
| 010 | -17% | -23% | -35% | -42% |
| 001 | -29% | -37% | -52% | -58% |
| 000 (slowest) | -53% | -63% | -76% | -77% |

These values are based on measurements performed on typical silicon at nominal supply and room temperature settings.

3.3 Hardware Mode Strapping and PHY Addressing

The VSC8530-05 device provides hardware-configured modes of operation that are achieved by sampling output pins on the rising edge of reset and externally pulling the pin to a logic HIGH or LOW (based on the desired configuration). These output pins are required by the device as inputs while NRESET is asserted and the logic state of the pin is latched in the device upon de-assertion of NRESET. To ensure correct operation of the hardware strapping function, any other device connected to these pins must not actively drive a signal onto them.

The following table describes the pins used for this purpose and their respective modes.

Table 6 • Hardware Mode Strapping and PHY Addressing

| Pin(s) | Operation Mode |
|--------|------------------------------|
| CLKOUT | Enable/disable CLKOUT signal |
| RX_CLK | Managed or unmanaged mode |
| RXD0 | Signal A |
| RXD1 | Signal B |
| RXD2 | Signal C |
| RXD3 | Signal D |
| RX_CTL | Signal E |

3.3.1 CLKOUT Signal Configuration

When the CLKOUT signal is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the CLKOUT output is disabled and the device will drive a logic low level on that pin after reset de-assertion. When the CLKOUT signal is pulled HIGH externally and the state of that signal is latched to logic 1, the CLKOUT output is enabled. This behavior can also be controlled through register 13G.15.

The CLKOUT signal is frequency-locked to the reference clock signal input through XTAL1/XTAL2 pins. The frequency of CLKOUT can be programmed to the following values through register 13G.14:13:

- 25 MHz
- 50 MHz
- 125 MHz

3.3.2 Managed Mode

When RX_CLK pin is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a managed mode. In managed mode, the remaining 5 signals (A–E) are used to set the PHY address, allowing up to 32 devices to reside on the shared MDIO bus. In this mode, the device can be configured using register access and no additional hardware configurability is provided. The following table lists the assigned PHY address values in managed mode.

Table 7 • Managed Mode

| Signal | PHY Address Values |
|----------|--------------------|
| Signal A | PHY address bit 0 |
| Signal B | PHY address bit 1 |
| Signal C | PHY address bit 2 |
| Signal D | PHY address bit 3 |
| Signal E | PHY address bit 4 |

3.3.3 Unmanaged Mode

When RX_CLK is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in an unmanaged mode. In unmanaged mode, the PHY address of the device is fixed to 5'b00000. The signals A–E are used to set default chip configurations, as described in the following sections.

Note: The default values for the following registers depend on the chosen hardware strapping options.

- 0.13, 0.6—Forced speed selection
- 0.12—Enable autonegotiation
- 0.8—Duplex
- 23.12:11—MAC interface selection
- 19E1.3:2—Force MDI crossover
- 20E2.6:4—RX_CLK delay
- 20E2.2:0—TX_CLK delay

Additionally, the following registers are set to 1 by default in unmanaged mode.

- 28.6—ActiPHY enable

3.3.3.1 Signals A and B

Signals A and B are used to set the RGMII RX_CLK and TX_CLK delay settings (as defined in register 20E2), as per the following table.

Table 8 • Signals A and B

| Signals A, B | RX_CLK and TX_CLK Delay Setting |
|--------------|---------------------------------|
| 0, 0 | 000 - 0.2 ns |
| 0, 1 | 010 - 1.1 ns |
| 1, 0 | 100 - 2.0 ns |
| 1, 1 | 110 - 2.6 ns |

3.3.3.2 Signals C and D

Signals C and D are used to select the link advertisement settings, as defined in the following table.

Table 9 • Signals C and D

| Signals C, D | Link Advertisement |
|--------------|--|
| 0, 0/1 | Default mode of operation, 10/100/ FDX/HDX, autoneg ON |
| 1, 0 | 100BTX, HDX forced mode, autoneg OFF |
| 1, 1 | 10BT, HDX forced mode, autoneg OFF |

3.3.3.3 Signal E

Signal E is used to select between RMII and RGMII MAC interface modes. When the state of Signal E is latched to logic 0 on the rising edge of reset, the device operates in RGMII mode. When the state of Signal E is latched to logic 1 on the rising edge of reset, the device operates in RMII mode.

Note: RMII only supports 10/100 Mbps speeds. When RMII mode is selected, the link advertisement selection must also be changed to either 01, 10, or 11 settings, as defined in [Table 9](#), page 9.

Note: Correct configuration of the device is an end user responsibility, and no attempt is made in the device to disallow incorrect configurations.

Additionally, in unmanaged mode, the following settings are changed from their default values:

- Enable ActiPHY (register 28.6 set to 1)

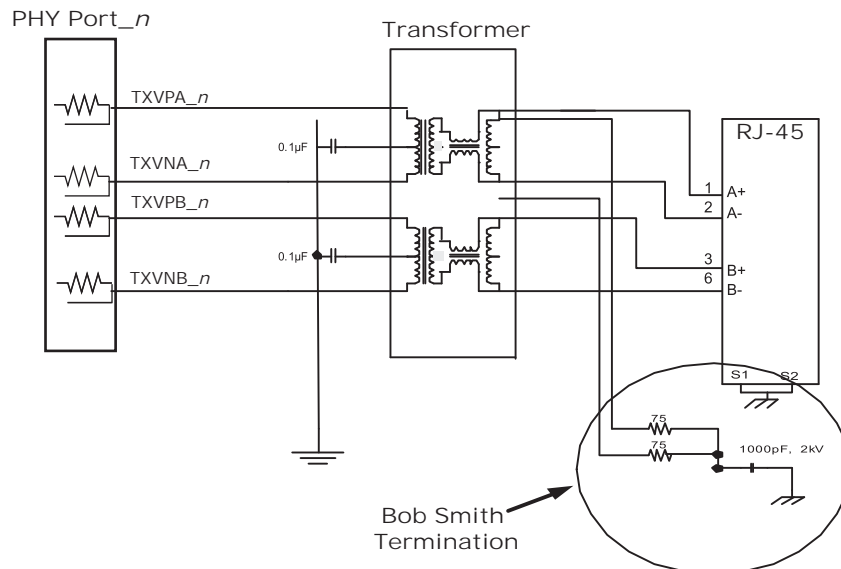
3.4 Cat5 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for Energy-Efficient Ethernet.

3.4.1 Voltage Mode Line Driver

The VSC8530-05 device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors that are required to connect the PHY's Cat5 interface to an external 1:1 transformer. The interface does not require the user to place an external voltage on the center tap of the magnetic. The following figure illustrates the connections.

Figure 7 • Cat5 Media Interface



3.4.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8530-05 device supports twisted pair auto-negotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed and duplex configuration. Auto-negotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8530-05 device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support auto-negotiation, the VSC8530-05 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing register 0, bit 12. When auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

3.4.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8530-05 device includes a robust automatic crossover detection feature for all speeds on the twisted pair interface. Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8530-05 device can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A is connected to the RJ45 connector 1, 2 in normal MDI mode.

Table 10 • Supported MDI Pair Combinations

| RJ45 Connections | | |
|------------------|------|--------------|
| 1, 2 | 3, 6 | Mode |
| A | B | Normal MDI |
| B | A | Normal MDI-X |

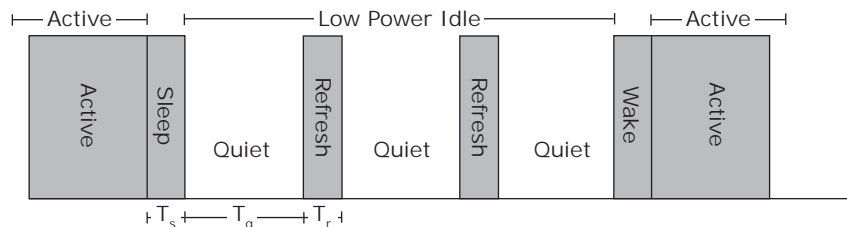
3.4.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

3.4.5 Energy-Efficient Ethernet

The VSC8530-05 device supports the IEEE 802.3az-2010 Energy-Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 8 • Low Power Idle Operation



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The VSC8530-05 device uses LPI to optimize power dissipation in 100BASE-TX mode.

In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T-compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8530-05 device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy-efficient Ethernet features are controlled through Clause 45 registers. For more information, see [Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf](#), page 51.

3.5 Reference Clock

The VSC8530-05 device supports multiple reference clock input options to allow maximum system level flexibility. There are two REFCLK_SEL signals available to allow an end user to select between the various options. The following table shows the functionality and associated reference clock frequency.

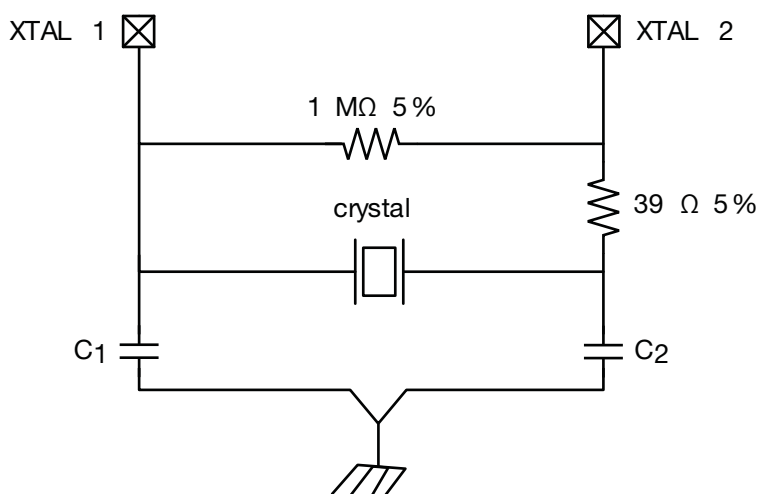
Table 11 • REFCLK Frequency Selection

| REFCLK_SEL [1:0] | Reference Clock Mode |
|------------------|--|
| 00 | 25 MHz, on-chip oscillator ON (XTAL1/2 pins) |
| 01 | 25 MHz, on-chip oscillator OFF (XTAL1 pin) |
| 10 | 50 MHz, on-chip oscillator OFF (XTAL1 pin) |
| 11 | 125 MHz, on-chip oscillator OFF (XTAL1 pin) |

The following figure shows a reference tank circuit for a fundamental mode crystal.

Note: For best performance, traces on PCB should be of similar length and Kelvin-connected to ground.

Figure 9 • XTAL Reference Clock

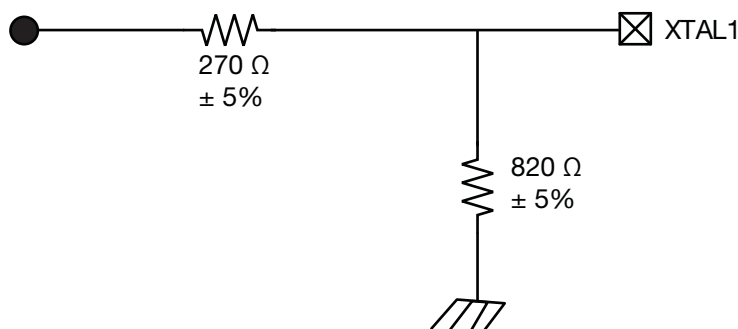


with REFCLK_SEL [1:0] = 00

Note: Routing capacitance less than 1 pF from each XTAL pin to crystal device.

The following figure shows an external 3.3 V reference clock.

Figure 10 • External 3.3 V Reference Clock



Note: Reference clock source less than $\lambda/10$ from XTAL1.

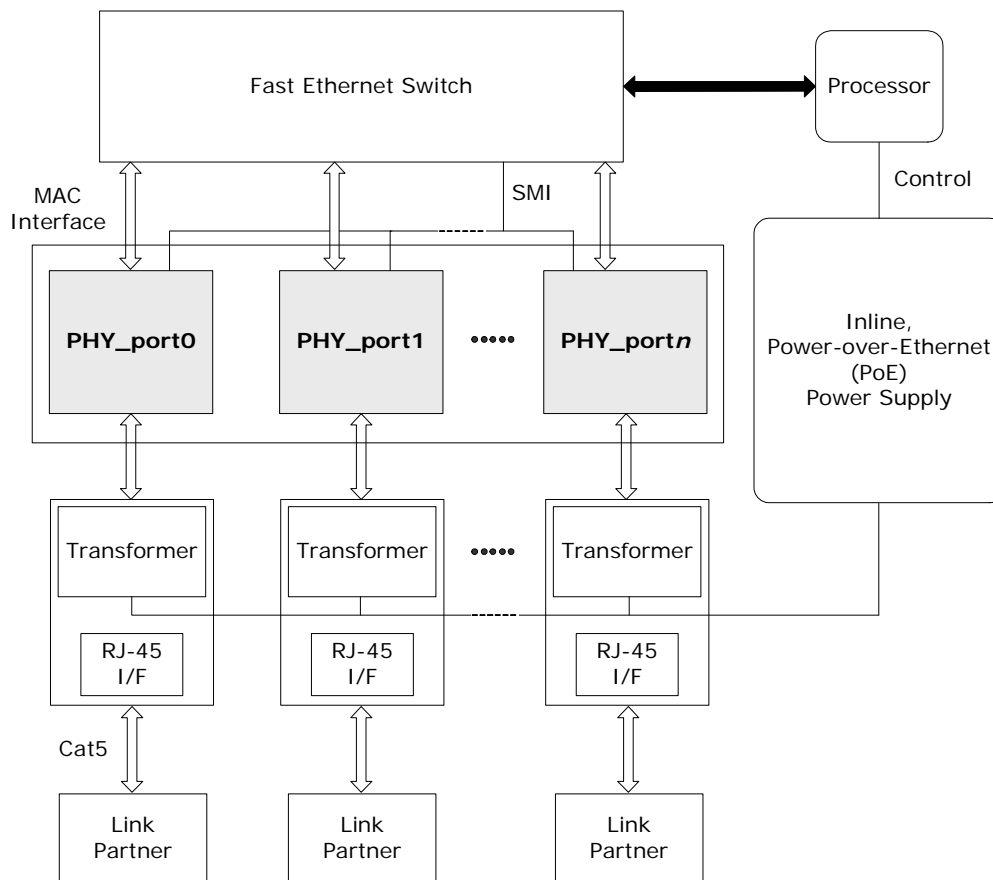
Note: No voltage scaling is required for a 2.5 V external reference.

3.6 Ethernet Inline-Powered Devices

The VSC8530-05 device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptible power source.

For more information about legacy inline-powered device detection, visit the Cisco website at www.cisco.com. The following illustration shows an example of an inline-powered Ethernet switch application.

Figure 11 • Inline-Powered Ethernet Switch Diagram



The following procedure describes the steps that an Ethernet switch must perform to process inline-power requests made by a link partner that is, in turn, capable of receiving inline-power:

1. Enable the inline-powered device detection mode on each VSC8530-05 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the auto-negotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse signal to the link partner. Reading register bit 23E1.9:8 returns 00 during the search for devices that require Power-over-Ethernet (PoE).
3. The VSC8530-05 PHY monitors its inputs for the fast link pulse signal looped back by the link partner. A link partner capable of receiving PoE loops back the fast link pulses when the link partner is in a powered down state. This is reported when register bit 23E1.9:8 reads back 01. It can also be verified as an inline-power detection interrupt by reading register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When a link partner

- device does not loop back the fast link pulse after a specific time, register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8530-05 PHY reports that the link partner requires PoE, the Ethernet switch must enable inline-power on this port, independent of the PHY.
 5. The PHY automatically disables inline-powered device detection when the register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal auto-negotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).
 6. In the event of a link failure (indicated when register bit 1.2 reads 0), it is recommended that the inline-power be disabled to the inline-powered device independent of the PHY. The VSC8530-05 PHY disables its normal auto-negotiation process and re-enables its inline-powered device detection mode.

3.7 IEEE 802.3af Power-over-Ethernet Support

The VSC8530-05 device is compatible with designs intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

3.8 ActiPHY Power Management

In addition to the IEEE-specified power down control bit (device register bit 0.11), the VSC8530-05 device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of fast link pulse over copper media.

The ActiPHY power management mode is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

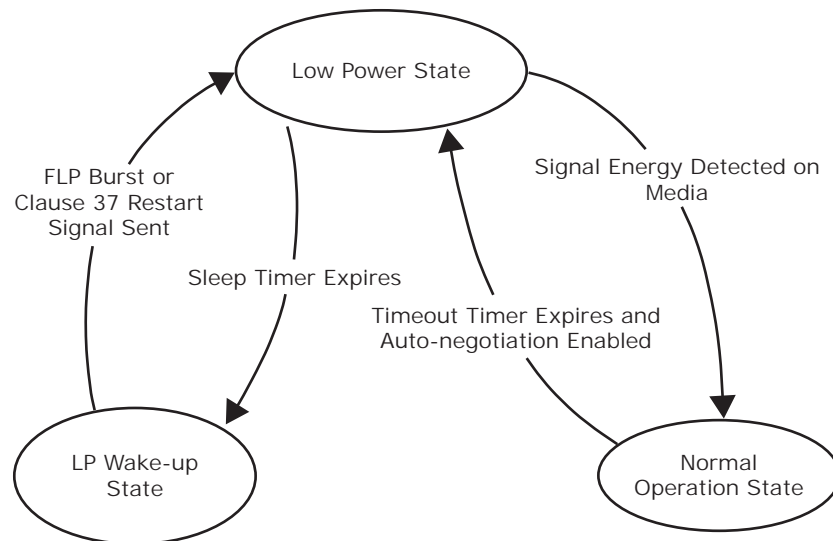
The VSC8530-05 device switches between the low power state and link partner wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described.

When auto-negotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and link partner wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 12 • ActiPHY State Diagram



3.8.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to an auto-negotiation-capable link partner or another PHY in enhanced ActiPHY link partner wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to link partner wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

3.8.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete fast link pulse bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.8.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

3.9 Serial Management Interface

The VSC8530-05 device includes an IEEE 802.3-compliant Serial Management Interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Additional pages of registers are accessible using device register 31.

Energy-efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14.

The SMI is a synchronous serial interface with input data to the VSC8530-05 device on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge

of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2 k Ω pull-up resistor is required on the MDIO pin.

3.9.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 13 • SMI Read Frame

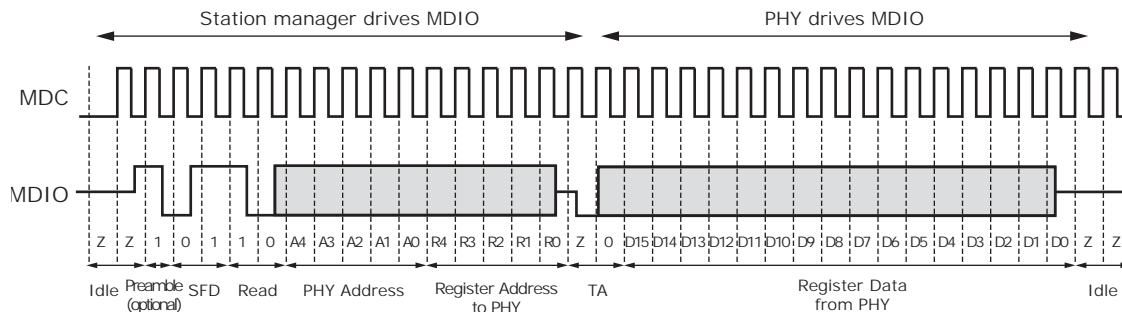
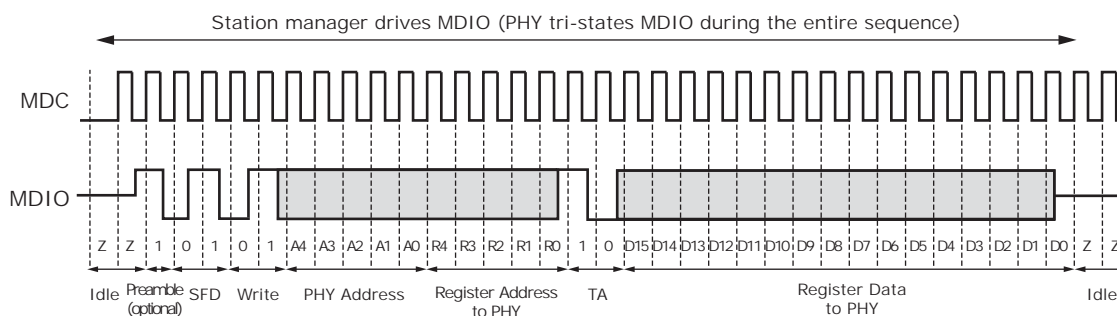


Figure 14 • SMI Write Frame



The following list defines the terms used in the SMI read and write timing diagrams.

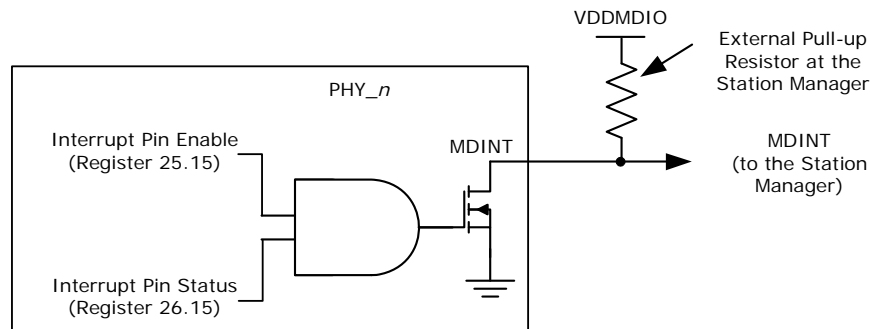
- **Idle**—During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode does not contain any transitions on MDIO, the number of bits is undefined during idle.
- **Preamble**—By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least 1 bit; otherwise, it can be of an arbitrary length.
- **Start of Frame Delimiter (SFD)**—A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.
- **Read or Write Opcode**—A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.
- **PHY Address**—The particular VSC8530-05 device responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).
- **Register Address**—The next five bits are the register address.
- **Turnaround**—The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8530-05 device drives the second TA bit, a logical 0.
- **Data**—The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.
- **Idle**—The sequence is repeated.

3.9.2 SMI Interrupt

The SMI includes an interrupt signal, MDINT, for signaling the station manager when certain events occur in the VSC8530-05 device.

When a PHY generates an interrupt, the MDINT pin is asserted by driving low if the interrupt pin enable bit (register 25.15) is set. The MDINT pin is configured for open-drain (active-low) operation. Tie the pin to a pull-up resistor to VDDMDIO. The following illustration shows the configuration.

Figure 15 • MDINT Configured as an Open-Drain (Active-Low) Pin



3.10 LED Interface

The LED interface supports direct drive and basic serial LED mode configuration. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits 13:10. The default polarity is active low.

Direct drive mode provides two LED signals, LED0 and LED1. The mode and function of each LED signal can be configured independently.

In basic serial LED mode, all signals that can be displayed on LEDs are sent as LED_Data and LED_CLK for external processing.

The following table shows the bit 9 settings for register 14G that are used to control the LED behavior for all the LEDs in the VSC8530-05 device.

Table 12 • LED Drive State

| Setting | Active | Not Active |
|-------------------------------|--------|-----------------|
| 14G.9 = 1 (default) | Ground | Tristate |
| 14G.9 = 0 (alternate setting) | Ground | V _{DD} |

3.10.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The default LED state is active low and can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions. The modes listed are equivalent to the setting used in register 29 to configure each LED pin.

Table 13 • LED Mode and Function Summary

| Mode | Function Name | LED State and Description |
|------|---------------|---|
| 0 | Link/Activity | 1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present. |
| 1 | Reserved | Reserved. |

Table 13 • LED Mode and Function Summary (continued)

| Mode | Function Name | LED State and Description |
|------|-----------------------|---|
| 2 | Link100/Activity | 1: No link in 100BASE-TX. 0: Valid 100BASE-TX. Blink or pulse-stretch = Valid 100BASE-TX link with activity present. |
| 3 | Link10/Activity | 1: No link in 10BASE-T. 0: Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present. |
| 4 | Reserved | Reserved. |
| 5 | Reserved | Reserved. |
| 6 | Link10/100/Activity | 1: No link in 10BASE-T or 100BASE-TX. 0: Valid 10BASE-T or 100BASE-TX link. Blink or pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present. |
| 7 | Reserved | Reserved. |
| 8 | Duplex/Collision | 1: Link established in half-duplex mode, or no link established. 0: Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present. |
| 9 | Collision | 1: No collision detected. Blink or pulse-stretch = Collision detected. |
| 10 | Activity | 1: No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present when register bit 30.14 is set to 1). |
| 11 | Reserved | Reserved. |
| 12 | Autonegotiation Fault | 1: No auto-negotiation fault present. 0: Auto-negotiation fault occurred. |
| 13 | Serial Mode | Serial stream. See Basic Serial LED Mode , page 18. Only relevant on PHY port 0. Reserved in others. |
| 14 | Force LED Off | 1: De-asserts the LED ¹ . |
| 15 | Force LED On | 0: Asserts the LED ¹ . |

1. Setting this mode suppresses LED blinking after reset.

3.10.2 Basic Serial LED Mode

The VSC8530-05 device can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 to serial LED mode in register 29, bits 3:0 to 0xD. When serial LED mode is enabled, the LED0 pin becomes the serial data pin, and the LED1 pin becomes the serial clock pin. The serial LED mode clocks the LED status bits on the rising edge of the serial clock.

The LED behavior settings can also be used in serial LED mode. The LED combine and LED blink or pulse-stretch setting of LED0 is used to control the behavior of each bit of the serial LED stream. To configure LED behavior, set device register 30.

The following table shows the serial output bitstream of each LED signal.

Table 14 • LED Serial Bitstream Order

| Output | |
|---------------|---|
| Link/activity | 1 |
| Reserved | 2 |

Table 14 • LED Serial Bitstream Order (continued)

| Output | |
|-----------------------|----|
| Link100/activity | 3 |
| Link10/activity | 4 |
| Reserved | 5 |
| Duplex/collision | 6 |
| Collision | 7 |
| Activity | 8 |
| Reserved | 9 |
| Tx activity | 10 |
| Rx activity | 11 |
| Autonegotiation fault | 12 |

3.10.3 Extended LED Modes

In addition to the LED modes in register 29, there are also additional LED modes that are enabled on the LED pin whenever the corresponding register 19E1, bits 13 to 12 are set to 1. Each of these bits enable an extended mode shown in the following table. For example, LED0 = mode 22 means that register 19E1 bit 12 = 1 and register 29 bits 3 to 0 = 0110.

The following table provides a summary of the extended LED modes and functions.

Table 15 • Extended LED Mode and Function Summary

| Mode | Function Name | LED State and Description |
|-------------|----------------------|---|
| 16-19 | Reserved | Reserved. |
| 20 | Force LED Off | 1: De-asserts the LED. |
| 21 | Force LED On | 0: Asserts the LED. LED pulsing is disabled in this mode. |
| 22 | Fast Link Fail | Enable fast link fail on the LED pin. |
| 23 | WoL interrupt | Enable WoL interrupt indication on the LED pin. |

3.10.4 LED Behavior

Several LED behaviors can be programmed into the VSC8530-05 device. Use the settings in register 30 and 19E1 to program LED behavior, as described in the following sections.

3.10.4.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 100BASE-TX mode and activity present can be displayed with one LED by configuring an LED pin to Link100/Activity mode. The LED asserts when linked to a 100BASE-TX partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the link partner. When disabled, the combine feature only provides the status of the selected primary function. In this example, only Link100 asserts the LED, and the secondary mode, Activity, does not display when the combine feature is disabled.

3.10.4.2 LED Blink or Pulse-Stretch

This behavior is available for LED mode 9 (collision) and LED mode 10 (activity) indications only, and can be uniquely configured for each LED pin. For more information, see [Table 13](#), page 17. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch ensures that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

3.10.4.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on a LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

3.10.4.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz programmable duty cycle. The pulsing enable is controlled through register 30, bit 12 and the duty cycle through register 25G, bits 15:8.

3.10.4.5 LED Blink After Reset

[Configuration](#), page 23 The LEDs will blink for one second after a software reset is applied. This feature can be enabled by setting register 19E1, bit 11 = 1.

3.10.4.6 Pulse Programmable Control

These bits add the ability to width and frequency of LED pulses. This feature facilitates power reduction options.

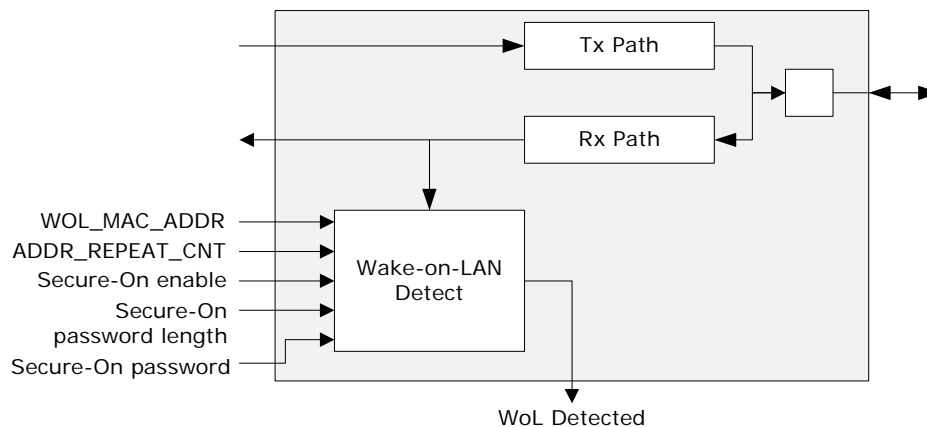
3.10.4.7 Fast Link Failure

For more information about this feature, see [Fast Link Failure Indication](#), page 20.

3.11 Wake-On-LAN and SecureOn

The VSC8530-05 device supports Wake-on-LAN, an Ethernet networking standard to awaken hosts by using a “magic packet” that is decoded to ascertain the source, and then assert an interrupt pin or a LED. The VSC8530-05 device also supports SecureOn to secure Wake-on-LAN against unauthorized access. The following illustration shows an overview of the Wake-on-LAN functionality.

Figure 16 • Wake-on-LAN Functionality



Wake-on-LAN detection is available in 10BASE-T and 100BASE-TX modes. It is enabled by setting the interrupt mask register (25.6) and its status is read in the interrupt status register (26.6). Wake-on-LAN and SecureOn are configured using register 27E2. The MAC address is saved in its local register space (21E2, 22E2, and 23E2).

3.12 Fast Link Failure Indication

For 100BASE-TX links, the link failure is based on a circuit that analyzes the integrity of the link and will assert at the indication of failure (< 3 ms. worst case).

Fast link failure is supported through the MDINT (active low) pin only in 100BASE-TX mode.

Note: A system can later confirm the fast link down indication for system management purposes by actively polling the link status bit to determine if a link has failed.

Note: Fast Link Failure Indication should not be used when EEE is enabled on a link.

3.13 Forced Speed Mode Link-Up Timing

The following table specifies the time the device will take to establish a link when operating in a forced speed mode.

Table 16 • Forced Speed Mode Link-Up Timing

| Forced Mode | Minimum | Maximum | Units |
|-----------------------------------|---------|---------|-------|
| 100Base-TX, HP Auto-MDIX Disabled | 43 | 240 | ms |
| 100Base-TX, HP Auto-MDIX Enabled | 43 | 4000 | ms |

In 100Base-TX mode, HP Auto-MDIX can be disabled by setting register 18 bit 7.

Link-up times are given for previously-configured PHYs on each side of the link— that is, the times do not include configuration time prior to attempting link-up. Both the device and link partner must be configured in forced speed mode to achieve the listed link-up times.

3.14 Testing Features

The VSC8530-05 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

3.14.1 Ethernet Packet Generator

The Ethernet Packet Generator (EPG) can be used at each of the 10/100BASE-TX speed settings for copper Cat5 media to isolate problems between the MAC and the VSC8530-05 device, or between a locally connected PHY and its remote link partner. Enabling the EPG feature disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Note: The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8530-05 device is connected to a live network.

To enable the EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. When it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

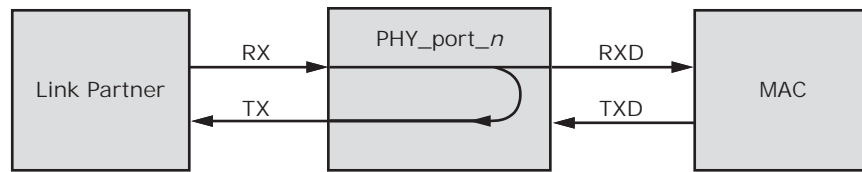
When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Interpacket gap
- FCS state
- Transmit duration
- Payload pattern

When register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

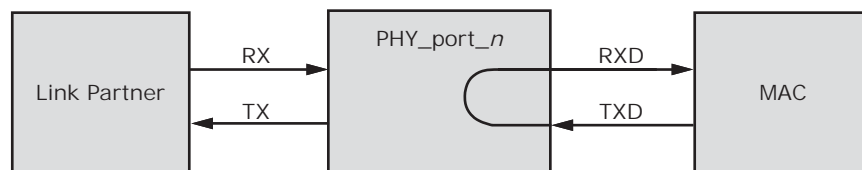
3.14.2 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the media interface into the MAC interface of the PHY where it is retransmitted back to the link partner on the media interface, as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

Figure 17 • Far-End Loopback Diagram

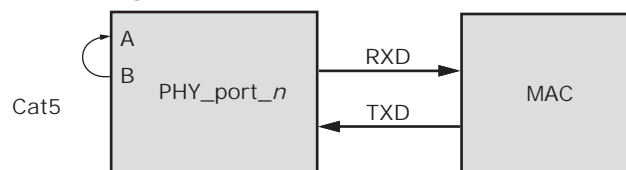
3.14.3 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

Figure 18 • Near-End Loopback Diagram

3.14.4 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Connect pair A to pair B, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 19 • Connector Loopback Diagram

When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0 and 4.

3.14.5 VeriPHY Cable Diagnostics

The VSC8530-05 device includes a comprehensive suite of cable diagnostic functions available using SMI reads and writes. These functions allow a variety of cable operating conditions and statuses to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions, and to isolate a number of common faults that can occur on the Cat5 twisted pair cabling.

Note: When a link is established in 100BASE-TX or 10BASE-T modes, VeriPHY causes the link to drop while the diagnostics are running. After diagnostics are finished, the link is re-established.

The following diagnostic functions are part of the VeriPHY suite.

- Detecting coupling between cable pairs
- Detecting cable pair termination
- Determining cable length

3.14.5.1 Coupling Between Cable Pairs

Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause error conditions, such as anomalous coupling between cable pairs. These conditions can prevent the device from establishing a link in any speed.

3.14.5.2 Cable Pair Termination

Proper termination of a Cat5 cable pair requires a 100 Ω differential impedance between the positive and negative cable terminals. IEEE 802.3 allows for a termination between 85 Ω (minimum) and 115 Ω (maximum). If the termination falls outside of this range, the VeriPHY diagnostics report it as an anomalous termination. The diagnostics can also determine the presence of an open or shorted cable pair.

3.14.5.3 Cable Length

When the Cat5 cable in an installation is properly terminated, VeriPHY reports the approximate cable length (in meters). If there is a cable fault, the distance to the fault is reported. Cable length reporting is reliable for cables between 10 and 100 meters.

3.15 Configuration

The VSC8530-05 device can be configured by setting internal memory registers using the management interface or by using the unmanaged mode as described in [Unmanaged Mode](#), page 9.

3.15.1 Managed Applications

To configure the device using the management interface, perform the following steps:

1. Apply power.
2. Apply RefClk.
3. Release reset, drive high. Power and clock must be high before releasing reset.
4. Wait 15 ms minimum.
5. Apply patch from PHY_API if available (required for production release, optional for board testing).
6. Configure register 23 for MAC interface mode.
 - Read register 23 (to access register 23, register 31 must be 0).
 - Set bits 12:11, MAC configuration, as follows:
10: RGMII
01: RMII
 - Write new register 23.
7. Software reset.
 - Read register 0 (to access register 0, register 31 must be 0).
 - Set bit 15 to 1.
 - Write new register 0.
8. Read register 0 until bit 15 equals to 0.
9. For RGMII mode: Configure register 20E2 (to access register 20E2, register 31 must be set to 2). Set bit 11 to 0 and set RX_CLK delay and TX_CLK delay accordingly through bit [6:4] and/or bit [2:0] respectively.

3.15.2 Unmanaged Applications

To configure the device using unmanaged mode, perform the following steps:

1. Apply power.
2. Apply RefClk.
3. Release reset, drive high. Power and clock must be high before releasing reset.
4. Wait 15 ms minimum.
5. (Optional) For applications that gain register access to the device using the management interface, steps 6–10 can then be performed in order to modify default settings.

4 Registers

This section provides information about how to configure the VSC8530-05 device using its internal memory registers and the management interface. The registers marked reserved and factory test should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

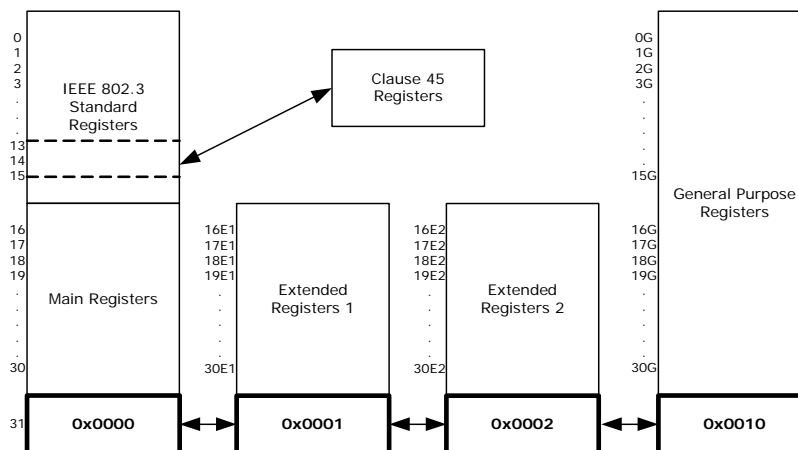
- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- R/W: Read and Write
- RWSC: Read and Write, Self-Clearing

The VSC8530-05 device uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Two pages of extended registers with addresses from 17E1–30E1 and 16E2–30E2
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az-2010 Energy-Efficient Ethernet registers and IEEE 802.3bf-2011 registers

The following illustration shows the relationship between the device registers and their address spaces.

Figure 20 • Register Space Diagram



Reserved Registers

For main registers 16–31, extended registers 17E1–30E1, 16E2–30E2, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.

Reserved Bits

In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (such as 27E1) means it is a register contained within extended register page number 1. A register with a G attached (such as 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

4.2 IEEE 802.3 and Main Registers

In the VSC8530-05 device, the page space of the standard registers consists of the IEEE 802.3 standard registers and the Microsemi standard registers. The following table lists the names of the registers associated with the addresses as specified by IEEE 802.3.

Table 17 • IEEE 802.3 Registers

| Address | Name |
|---------|---|
| 0 | Mode Control |
| 1 | Mode Status |
| 2 | PHY Identifier 1 |
| 3 | PHY Identifier 2 |
| 4 | Auto-negotiation Advertisement |
| 5 | Auto-negotiation Link Partner Ability |
| 6 | Auto-negotiation Expansion |
| 7 | Auto-negotiation Next-Page Transmit |
| 8 | Auto-negotiation Link Partner Next-Page Receive |
| 9–12 | Reserved |
| 13 | MMD EEE Access |
| 14 | MMD Address or Data Register |
| 15 | Reserved |

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 18 • Main Registers

| Address | Name |
|---------|-----------------------------|
| 16 | 100BASE-TX status extension |
| 17 | Reserved |
| 18 | Bypass control |
| 19 | Error Counter 1 |
| 20 | Error Counter 2 |
| 21 | Error Counter 3 |
| 22 | Extended control and status |
| 23 | Extended PHY control 1 |
| 24 | Extended PHY control 2 |
| 25 | Interrupt mask |
| 26 | Interrupt status |
| 27 | Reserved |

Table 18 • Main Registers (continued)

| Address | Name |
|---------|-------------------------------|
| 28 | Auxiliary control and status |
| 29 | LED mode select |
| 30 | LED behavior |
| 31 | Extended register page access |

4.2.1 Mode Control

The device register at memory address 0 controls several aspects of the VSC8530-05 device functionality. The following table shows the available bit settings in this register and what they control.

Table 19 • Mode Control, Address 0 (0x00)

| Bit | Name | Access | Description | Default |
|-----|----------------------------|--------|--|---------|
| 15 | Software reset | R/W | Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait 1 μ s after setting this bit to initiate another SMI register access. | 0 |
| 14 | Loopback | R/W | 1: Loopback enabled. 0: Loopback disabled. When loopback is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register). | 0 |
| 13 | Forced speed selection LSB | R/W | Least significant bit. MSB is bit 6. 00: 10 Mbps 01: 100 Mbps 10: Reserved 11: Reserved | 1 |
| 12 | Autonegotiation enable | R/W | 1: Autonegotiation enabled. 0: Autonegotiation disabled. | 1 |
| 11 | Power-down | R/W | 1: Power down enabled. | 0 |
| 10 | Isolate | R/W | 1: Disable MAC interface outputs and ignore MAC interface inputs. | 0 |
| 9 | Restart autonegotiation | R/W | Self-clearing bit. 1: Restart autonegotiation on media interface. | 0 |
| 8 | Duplex | R/W | 1: Full-duplex. 0: Half-duplex. | 0 |
| 7 | Collision test enable | R/W | 1: Collision test enabled. | 0 |
| 6 | Forced speed selection MSB | R/W | Most significant bit. LSB is bit 13. 00: 10 Mbps 01: 100 Mbps 10: Reserved 11: Reserved | 0 |
| 5:0 | Reserved | RO | Reserved. | |

4.2.2 Mode Status

The register at address 1 in the device main registers space enables reading the currently enabled mode setting. The following table shows possible readouts of this register.

Table 20 • Mode Status, Address 1 (0x01)

| Bit | Name | Access | Description | Default |
|-----|---------------------------------|--------|--|---------|
| 15 | 100BASE-T4 capability | RO | 1: 100BASE-T4 capable. | 0 |
| 14 | 100BASE-TX FDX capability | RO | 1: 100BASE-TX FDX capable. | 1 |
| 13 | 100BASE-TX HDX capability | RO | 1: 100BASE-TX HDX capable. | 1 |
| 12 | 10BASE-T FDX capability | RO | 1: 10BASE-T FDX capable. | 1 |
| 11 | 10BASE-T HDX capability | RO | 1: 10BASE-T HDX capable. | 1 |
| 10 | 100BASE-T2 FDX capability | RO | 1: 100BASE-T2 FDX capable. | 0 |
| 9 | 100BASE-T2 HDX capability | RO | 1: 100BASE-T2 HDX capable. | 0 |
| 8 | Extended status enable | RO | 1: Extended status information present in register 15. | 1 |
| 7 | Reserved | RO | Reserved. | |
| 6 | Preamble suppression capability | RO | 1: MF preamble can be suppressed. 0: MF required. | 1 |
| 5 | Autonegotiation complete | RO | 1: Auto-negotiation complete. | 0 |
| 4 | Remote fault | RO | Latches high. 1: Far-end fault detected. | 0 |
| 3 | Autonegotiation capability | RO | 1: Auto-negotiation capable. | 1 |
| 2 | Link status | RO | Latches low. 1: Link is up. | 0 |
| 1 | Jabber detect | RO | Latches high. 1: Jabber condition detected. | 0 |
| 0 | Extended capability | RO | 1: Extended register capable. | 1 |

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8530-05 device are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 21 • Identifier 1, Address 2 (0x02)

| Bit | Name | Access | Description | Default |
|------|--|--------|----------------------------------|---------|
| 15:0 | Organizationally unique identifier (OUI) | RO | OUI most significant bits (3:18) | 0x0007 |

Table 22 • Identifier 2, Address 3 (0x03)

| Bit | Name | Access | Description | Default |
|-------|------------------------|--------|------------------------------------|---------|
| 15:10 | OUI | RO | OUI least significant bits (19:24) | 000001 |
| 9:4 | Microsemi model number | RO | VSC8530-05 | 010110 |
| 3:0 | Device revision number | RO | Revision C | 0010 |

4.2.4 Auto-Negotiation Advertisement

The bits in address 4 in the main registers space control the ability to notify other devices of the status of its auto-negotiation feature. The following table shows the available settings and readouts.

Table 23 • Device Auto-Negotiation Advertisement, Address 4 (0x04)

| Bit | Name | Access | Description | Default |
|-----|--------------------------------|--------|--------------------------------|---------|
| 15 | Next page transmission request | R/W | 1: Request enabled | 0 |
| 14 | Reserved | RO | Reserved | |
| 13 | Transmit remote fault | R/W | 1: Enabled | 0 |
| 12 | Reserved | RO | Reserved | |
| 11 | Advertise asymmetric pause | R/W | 1: Advertises asymmetric pause | 0 |
| 10 | Advertise symmetric pause | R/W | 1: Advertises symmetric pause | 0 |
| 9 | Advertise100BASE-T4 | R/W | 1: Advertises 100BASE-T4 | 0 |
| 8 | Advertise100BASE-TX FDX | R/W | 1: Advertise 100BASE-TX FDX | 1 |
| 7 | Advertise100BASE-TX HDX | R/W | 1: Advertises 100BASE-TX HDX | 1 |
| 6 | Advertise10BASE-T FDX | R/W | 1: Advertises 10BASE-T FDX | 1 |
| 5 | Advertise10BASE-T HDX | R/W | 1: Advertises 10BASE-T HDX | 1 |
| 4:0 | Advertise selector | R/W | | 00001 |

4.2.5 Link Partner Auto-Negotiation Capability

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8530-05 device is compatible with the auto-negotiation functionality.

Table 24 • Auto-Negotiation Link Partner Ability, Address 5 (0x05)

| Bit | Name | Access | Description | Default |
|-----|-----------------------------------|--------|--------------------------------|---------|
| 15 | LP next page transmission request | RO | 1: Requested | 0 |
| 14 | LP acknowledge | RO | 1: Acknowledge | 0 |
| 13 | LP remote fault | RO | 1: Remote fault | 0 |
| 12 | Reserved | RO | Reserved | |
| 11 | LP advertise asymmetric pause | RO | 1: Capable of asymmetric pause | 0 |
| 10 | LP advertise symmetric pause | RO | 1: Capable of symmetric pause | 0 |
| 9 | LP advertise 100BASE-T4 | RO | 1: Capable of 100BASE-T4 | 0 |
| 8 | LP advertise 100BASE-TX FDX | RO | 1: Capable of 100BASE-TX FDX | 0 |
| 7 | LP advertise 100BASE-TX HDX | RO | 1: Capable of 100BASE-TX HDX | 0 |
| 6 | LP advertise 10BASE-T FDX | RO | 1: Capable of 10BASE-T FDX | 0 |
| 5 | LP advertise 10BASE-T HDX | RO | 1: Capable of 10BASE-T HDX | 0 |
| 4:0 | LP advertise selector | RO | | 00000 |

4.2.6 Auto-Negotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP auto-negotiation functioning. The following table shows the available settings and readouts.

Table 25 • Auto-Negotiation Expansion, Address 6 (0x06)

| Bit | Name | Access | Description | Default |
|------|-------------------------------|--------|--|---------|
| 15:5 | Reserved | RO | Reserved. | |
| 4 | Parallel detection fault | RO | This bit latches high. 1: Parallel detection fault. | 0 |
| 3 | LP next page capable | RO | 1: LP is next page capable. | 0 |
| 2 | Local PHY next page capable | RO | 1: Local PHY is next page capable. | 1 |
| 1 | Page received | RO | This bit latches high. 1: New page is received. | 0 |
| 0 | LP is autonegotiation capable | RO | 1: LP is capable of auto-negotiation. | 0 |

4.2.7 Transmit Auto-Negotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an auto-negotiation sequence. The following table shows the settings available.

Table 26 • Auto-Negotiation Next Page Transmit, Address 7 (0x07)

| Bit | Name | Access | Description | Default |
|------|--------------------------|--------|--|------------|
| 15 | Next page | R/W | 1: More pages follow. | 0 |
| 14 | Reserved | RO | Reserved. | |
| 13 | Message page | R/W | 1: Message page. 0: Unformatted page. | 1 |
| 12 | Acknowledge 2 | R/W | 1: Complies with request. 0: Cannot comply with request. | 0 |
| 11 | Toggle | RO | 1: Previous transmitted LCW = 0. 0: Previous transmitted LCW = 1. | 0 |
| 10:0 | Message/unformatted code | R/W | | 0000000001 |

4.2.8 Auto-Negotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP auto-negotiation. The following table shows the possible readouts.

Table 27 • Auto-Negotiation LP Next Page Receive, Address 8 (0x08)

| Bit | Name | Access | Description | Default |
|------|-----------------------------|--------|--|-----------|
| 15 | LP next page | RO | 1: More pages follow. | 0 |
| 14 | Acknowledge | RO | 1: LP acknowledge. | 0 |
| 13 | LP message page | RO | 1: Message page. 0: Unformatted page. | 0 |
| 12 | LP acknowledge 2 | RO | 1: LP complies with request. | 0 |
| 11 | LP toggle | RO | 1: Previous transmitted LCW = 0. 0: Previous transmitted LCW = 1. | 0 |
| 10:0 | LP message/unformatted code | RO | | All zeros |

4.2.9 MMD Access Control Register

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 28 • MMD EEE Access, Address 13 (0x0D)

| Bit | Name | Access | Description |
|-------|----------|--------|--|
| 15:14 | Function | R/W | 00: Address. 01: Data, no post increment. 10: Data, post increment for read and write. 11: Data, post increment for write only. |
| 13:5 | Reserved | RO | Reserved. |
| 4:0 | DVAD | R/W | Device address as defined in IEEE 802.3az-2010 table 45–1. |

4.2.10 MMD Address or Data Register

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 29 • MMD Address or Data Register, Address 14 (0x0E)

| Bit | Name | Access | Description |
|------|-----------------------|--------|--|
| 15:0 | Register Address/Data | R/W | When register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register. |

4.2.11 100BASE-TX Status Extension

Register 16 in the main registers page space provides additional information about the status of the 100BASE-TX operation.

Table 30 • 100BASE-TX Status Extension, Address 16 (0x10)

| Bit | Name | Access | Description | Default |
|-----|--------------------------------|--------|--|---------|
| 15 | 100BASE-TX Descrambler | RO | 1: Descrambler locked. | 0 |
| 14 | 100BASE-TX lock error | RO | Self-clearing bit. 1: Lock error detected. | 0 |
| 13 | 100BASE-TX disconnect state | RO | Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected. | 0 |
| 12 | 100BASE-TX current link status | RO | 1: PHY 100BASE-TX link active. | 0 |
| 11 | 100BASE-TX receive error | RO | Self-clearing bit. 1: Receive error detected. | 0 |
| 10 | 100BASE-TX transmit error | RO | Self-clearing bit. 1: Transmit error detected. | 0 |
| 9 | 100BASE-TX SSD error | RO | Self-clearing bit. 1: Start-of-stream delimiter error detected. | 0 |
| 8 | 100BASE-TX ESD error | RO | Self-clearing bit. 1: End-of-stream delimiter error detected. | 0 |
| 7:0 | Reserved | RO | Reserved. | |

4.2.12 Bypass Control

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

Table 31 • Bypass Control, Address 18 (0x12)

| Bit | Name | Access | Description | Default |
|-----|--|--------|--|---------|
| 15 | Transmit disable | R/W | 1: PHY transmitter disabled. | 0 |
| 14 | 4B5B encoder/decoder | R/W | 1: Bypass 4B/5B encoder/decoder. | 0 |
| 13 | Scrambler | R/W | 1: Bypass scrambler. | 0 |
| 12 | Descrambler | R/W | 1: Bypass descrambler. | 0 |
| 11 | PCS receive | R/W | 1: Bypass PCS receiver. | 0 |
| 10 | PCS transmit | R/W | 1: Bypass PCS transmit. | 0 |
| 9 | LFI timer | R/W | 1: Bypass Link Fail Inhibit (LFI) timer. | 0 |
| 8 | Reserved | RO | Reserved. | |
| 7 | HP Auto-MDIX at forced 10/100 | R/W | Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds. | 1 |
| 6 | Reserved | R/W | Reserved. | 0 |
| 5 | Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled) | R/W | Sticky bit. 1: Disable the automatic pair swap correction. | 0 |
| 4 | Disable polarity correction | R/W | Sticky bit. 1: Disable polarity inversion correction on each subchannel. | 0 |
| 3 | Parallel detect control | R/W | Sticky bit. 1: Do not ignore advertised ability. 0: Ignore advertised ability. | 1 |
| 20 | Reserved | RO | Reserved. | |

4.2.13 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 32 • Extended Control and Status, Address 19 (0x13)

| Bit | Name | Access | Description | Default |
|------|-----------------------|--------|---|---------|
| 15:8 | Reserved | RO | Reserved. | |
| 7:0 | Receive error counter | RO | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00 |

4.2.14 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 33 • Extended Control and Status, Address 20 (0x14)

| Bit | Name | Access | Description | Default |
|------|-----------------------|--------|---|---------|
| 15:8 | Reserved | RO | Reserved. | |
| 7:0 | False carrier counter | RO | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00 |

4.2.15 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 34 • Extended Control and Status, Address 21 (0x15)

| Bit | Name | Access | Description | Default |
|------|--------------------------------------|--------|---|---------|
| 15:8 | Reserved | RO | Reserved. | |
| 7:0 | Copper media link disconnect counter | RO | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00 |

4.2.16 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 35 • Extended Control and Status, Address 22 (0x16)

| Bit | Name | Access | Description | Default |
|-------|---------------------------|--------|--|---------|
| 15 | Force 10BASE-T link high | R/W | Sticky bit. 1: Bypass link integrity test. 0: Enable link integrity test. | 0 |
| 14 | Jabber detect disable | R/W | Sticky bit. 1: Disable jabber detect. | 0 |
| 13 | Disable 10BASE-T echo | R/W | Sticky bit. 1: Disable 10BASE-T echo. | 1 |
| 12 | Disable SQE mode | R/W | Sticky bit. 1: Disable SQE mode. | 1 |
| 11:10 | 10BASE-T squelch control | R/W | Sticky bit. 00: Normal squelch. 01: Low squelch. 10: High squelch. 11: Reserved. | 00 |
| 9 | Sticky reset enable | R/W | Super-sticky bit. 1: Enabled. | 1 |
| 8 | EOF Error | RO | This bit is self-clearing. 1: EOF error detected. | 0 |
| 7 | 10BASE-T disconnect state | RO | This bit is self-clearing. 1: 10BASE-T link disconnect detected. | 0 |
| 6 | 10BASE-T link status | RO | 1: 10BASE-T link active. | 0 |
| 5:1 | Reserved | RO | Reserved. | |
| 0 | SMI broadcast write | R/W | Sticky bit. 1: Enabled. | 0 |

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.

- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

4.2.17 Extended PHY Control 1

The following table shows the settings available.

Table 36 • Extended PHY Control 1, Address 23 (0x17)

| Bit | Name | Access | Description | Default |
|-------|---------------------------|--------|---|---------|
| 15:14 | Reserved | RO | Reserved. | |
| 13 | MAC supplied clock enable | R/W | MAC interface RX_CLK synchronization. 0: Synchronize RX_CLK to recovered clock. 1: Synchronize RX_CLK to REFCLK. Note: This bit is not applicable to the RMII MAC interface selection. This bit may be changed or written prior to a soft-reset, after which it takes effect. | 0 |
| 12:11 | MAC interface selection | R/W | MAC interface mode. 00: Reserved. 01: RMII. 10: RGMII. 11: Reserved. Note: These bits may be changed or written prior to a soft-reset, after which it takes effect. | 10 |
| 10:4 | Reserved | RO | Reserved. | |
| 3 | Far-end loopback mode | R/W | 1: Enabled. | 0 |
| 2:0 | Reserved | RO | Reserved. | |

Note: After configuring bits 13:11 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. On read, these bits only indicate the actual operating mode and not the pending operating mode setting before a software reset has taken place.

4.2.18 Extended PHY Control 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 37 • Extended PHY Control 2, Address 24 (0x18)

| Bit | Name | Access | Description | Default |
|-------|------------------------------|--------|--|---------|
| 15:13 | 100BASE-TX edge rate control | R/W | Sticky bit. 011: +7 edge rate (slowest). 010: +6 edge rate. 001: +5 edge rate. 000: +4 edge rate. 111: +3 edge rate. 110: +2 edge rate. 101: +1 edge rate. 100: Fastest edge rate. | 000 |

Table 37 • Extended PHY Control 2, Address 24 (0x18) (continued)

| Bit | Name | Access | Description | Default |
|------|-------------------------------|--------|--|---------|
| 12 | PICMG 2.16 reduced power mode | R/W | Sticky bit. 1: Enabled. | 0 |
| 11:6 | Reserved | RO | Reserved. | |
| 5:4 | Jumbo packet mode | R/W | Sticky bit. 00: Normal IEEE 1.5 kB packet length. 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock). 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock). 11: Reserved. | 00 |
| 3:1 | Reserved | RO | Reserved. | |
| 0 | Connector loopback | R/W | 1: Enabled. | 0 |

Note: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

4.2.19 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 38 • Interrupt Mask, Address 25 (0x19)

| Bit | Name | Access | Description | Default |
|-----|---|--------|-------------------------|---------|
| 15 | MDINT interrupt status enable | R/W | Sticky bit. 1: Enabled. | 0 |
| 14 | Speed state change mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 13 | Link state change mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 12 | FDX state change mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 11 | Autonegotiation error mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 10 | Autonegotiation complete mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 9 | Inline-powered device (PoE) detect mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 8 | Symbol error interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 7 | Fast link failure interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 6 | Wake-on-LAN event interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 5 | Extended interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 4 | Reserved | RO | Reserved. | |
| 3 | False carrier interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 2 | Reserved | RO | Reserved. | |
| 1 | Reserved | RO | Reserved. | |
| 0 | RX_ER interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

4.2.20 Interrupt Status

The status of interrupts already written to the device is available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 39 • Interrupt Status, Address 26 (0x1A)

| Bit | Name | Access | Description | Default |
|-----|-------------------------------------|--------|--|---------|
| 15 | Interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 14 | Speed state change status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 13 | Link state change status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 12 | FDX state change status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 11 | Autonegotiation error status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 10 | Autonegotiation complete status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 9 | Inline powered device detect status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 8 | Symbol error status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 7 | Fast link failure detect status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 6 | Wake-on-LAN event status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 5 | Extended interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 4 | Reserved | RO | Reserved. | |
| 3 | False carrier interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 2 | Reserved | RO | Reserved. | |
| 1 | Reserved | RO | Reserved. | |
| 0 | RX_ER interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.
- If bit 5 is set, register 29E2 must be read to determine the source of the interrupt.

4.2.21 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 40 • Auxiliary Control and Status, Address 28 (0x1C)

| Bit | Name | Access | Description | Default |
|-----|-----------------------------------|--------|---|---------|
| 15 | Autonegotiation complete | RO | Duplicate of bit 1.5 when auto-negotiation is enabled, otherwise this is the current link status. | 0 |
| 14 | Autonegotiation disabled | RO | Inverted duplicate of bit 0.12. | 0 |
| 13 | HP Auto-MDIX crossover indication | RO | 1: HP Auto-MDIX crossover performed internally. | 0 |
| 12 | Reserved | RO | Reserved. | |

Table 40 • Auxiliary Control and Status, Address 28 (0x1C) (continued)

| Bit | Name | Access | Description | Default |
|-----|--|--------|--|---------|
| 11 | A polarity inversion | RO | 1: Polarity swap on pair A. | 0 |
| 10 | B polarity inversion | RO | 1: Polarity swap on pair B. | 0 |
| 9:8 | Reserved | RO | Reserved. | |
| 7 | ActiPHY link status time-out control [1] | R/W | Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds. 01: 3.3 seconds. 10: 4.3 seconds. 11: 5.3 seconds. | 0 |
| 6 | ActiPHY mode enable | R/W | Sticky bit. 1: Enabled. | 0 |
| 5 | FDX status | RO | 1: Full-duplex. 0: Half-duplex. | 0 |
| 4:3 | Speed status | RO | 00: Speed is 10BASE-T. 01: Speed is 100BASE-TX. 10: Reserved. 11: Reserved. | 00 |
| 2 | ActiPHY link status time-out control [0] | R/W | Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds. 01: 3.3 seconds. 10: 4.3 seconds. 11: 5.3 seconds. | 1 |
| 1:0 | Media mode status | RO | 00: No media selected. 01: Copper media selected. 10: Reserved. 11: Reserved. | 00 |

4.2.22 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more information about LED modes, see [Table 13](#), page 17. For information about enabling the extended LED mode bits in Register 19E1 bits 13 to 12, see [Table 15](#), page 19.

Table 41 • LED Mode Select, Address 29 (0x1D)

| Bit | Name | Access | Description | Default |
|------|------------------|--------|---|---------|
| 15 | Reserved | RO | Reserved. | |
| 14:8 | Reserved | RO | Reserved. | |
| 7:4 | LED1 mode select | R/W | Sticky bit. Select from LED modes 0–15. | 0101 |
| 3:0 | LED0 mode select | R/W | Sticky bit. Select from LED modes 0–15. | 0100 |

4.2.23 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 42 • LED Behavior, Address 30 (0x1E)

| Bit | Name | Access | Description | Default |
|-------|---------------------------------|--------|---|---------|
| 15:13 | Reserved | RO | Reserved. | |
| 12 | LED pulsing enable | R/W | Sticky bit. 0: Normal operation. 1: LEDs pulse with a 5 kHz, programmable duty cycle when active. | 0 |
| 11:10 | LED blink/pulse-stretch rate | R/W | Sticky bit. 00: 2.5 Hz blink rate/400 ms pulse-stretch. 01: 5 Hz blink rate/200 ms pulse-stretch. 10: 10 Hz blink rate/100 ms pulse-stretch. 11: 20 Hz blink rate/50 ms pulse-stretch. The blink rate selection sets the rate used for all LED pins. | 01 |
| 9:7 | Reserved | RO | Reserved. | |
| 6 | LED1 pulse-stretch/blink select | R/W | Sticky bit. 1: Pulse-stretch. 0: Blink. | 0 |
| 5 | LED0 pulse-stretch/blink select | R/W | Sticky bit. 1: Pulse-stretch. 0: Blink. | 0 |
| 4:2 | Reserved | RO | Reserved. | |
| 1 | LED1 combine feature disable | R/W | Sticky bit. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only). | 0 |
| 0 | LED0 combine feature disable | R/W | Sticky bit. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only). | 0 |

Note: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

4.2.24 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, an extended set of registers provide an additional 15 register spaces.

The register at address 31 controls access to the extended registers. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 43 • Extended/GPIO Register Page Access, Address 31 (0x1F)

| Bit | Name | Access | Description | Default |
|------|------------------------------------|--------|---|---------|
| 15:0 | Extended/GPIO page register access | R/W | 0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Registers 16–30 access extended register space 1. 0x0002: Registers 16–30 access extended register space 2. 0x0010: Registers 0–30 access GPIO register space. | 0x0000 |

4.3 Extended Page 1 Registers

To access the extended page 1 registers (17E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 17E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 44 • Extended Registers Page 1 Space

| Address | Name |
|-----------|--|
| 16E1 | VeriPHY Status Register 1 |
| 17E1 | Reserved |
| 18E1 | Cu Media CRC Good Counter |
| 19E1 | Extended Mode Control |
| 20E1 | Extended PHY Control 3 (ActiPHY) |
| 21E1–22E1 | Reserved |
| 23E1 | Extended PHY Control 4 (PoE and CRC Error Counter) |
| 24E1 | VeriPHY Control 1 |
| 25E1 | VeriPHY Control 2 |
| 26E1 | VeriPHY Control 3 |
| 27E1–28E1 | Reserved |
| 29E1 | Ethernet Packet Generator (EPG) 1 |
| 30E1 | EPG 2 |

4.3.1 VeriPHY Status 1

Register 16E1 in the extended register space provides status of the VeriPHY diagnostics for pairs A and B. These results are valid when bit 24E1.14 is set to 1.

Table 45 • VeriPHY Status Register 1, Address 16E1 (0x10)

| Bit | Name | Access | Description | Default |
|------|------------------------|--------|--|---------|
| 15:8 | Pair B (3, 6) distance | RO | Loop length or distance to anomaly for pair B (3, 6) | 0x00 |
| 7:0 | Pair A (1, 2) distance | RO | Loop length or distance to anomaly for pair A (1, 2) | 0x00 |

Note: The resolution of the 8-bit length field is 1 meter.

4.3.2 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface: the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 46 • Cu Media CRC Good Counter, Address 18E1 (0x12)

| Bit | Name | Access | Description | Default |
|-----|------------------------|--------|---|---------|
| 15 | Packet since last read | RO | Self-clearing bit. 1: Packet received since last read. | 0 |
| 14 | Reserved | RO | Reserved. | |

Table 46 • Cu Media CRC Good Counter, Address 18E1 (0x12) (continued)

| Bit | Name | Access | Description | Default |
|------|------------------------------------|--------|--|---------|
| 13:0 | Cu Media CRC good counter contents | RO | Self-clearing bit. Counter containing the number of packets with valid CRCs modulo 10,000; this counter does not saturate and will roll over to zero on the next good packet received after 9,999. | 0x0000 |

4.3.3 Extended Mode Control

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

Table 47 • Extended Mode Control, Address 19E1 (0x13)

| Bit | Name | Access | Description | Default |
|-------|--------------------------|--------|---|---------|
| 15:14 | Reserved | RO | Reserved. | |
| 13 | LED1 Extended Mode | R/W | Sticky bit. 1: See Basic Serial LED Mode , page 18. | 0 |
| 12 | LED0 Extended Mode | R/W | Sticky bit. 1: See Basic Serial LED Mode , page 18. | 0 |
| 11 | LED Reset Blink Suppress | R/W | Sticky bit. 1: Blink LEDs after Software reset is de-asserted. 0: Suppress LED blink after Software reset is de-asserted. | 0 |
| 10:4 | Reserved | RO | Reserved. | |
| 3:2 | Force MDI crossover | R/W | Sticky bit. 00: Normal HP Auto-MDIX operation. 01: Reserved. 10: Copper media forced to MDI. 11: Copper media forced MDI-X. | 00 |
| 1:0 | Reserved | RO | Reserved. | |

4.3.4 ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer and its wake-up timer. The following table shows the settings available.

Table 48 • Extended PHY Control 3, Address 20E1 (0x14)

| Bit | Name | Access | Description | Default |
|-------|-----------------------|--------|--|---------|
| 15 | Reserved | RO | Reserved. | |
| 14:13 | ActiPHY sleep timer | R/W | Sticky bit. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds. | 01 |
| 12:11 | ActiPHY wake-up timer | R/W | Sticky bit. 00: 160 ms. 01: 400 ms. 10: 800 ms. 11: 2 seconds. | 00 |

Table 48 • Extended PHY Control 3, Address 20E1 (0x14) (continued)

| Bit | Name | Access | Description | Default |
|-----|----------------------------------|--------|--|---------|
| 10 | Slow MDC | R/W | Sticky bit. 1: Indicates that MDC runs at less than 1 MHz (use of this bit is optional and indicated when MDC runs at less than 1 MHz). | 0 |
| 9:8 | Reserved | RO | Reserved. | |
| 7:6 | Media mode status | RO | 00: No media selected. 01: Copper media selected. 10: Reserved. 11: Reserved. | 00 |
| 5 | Enable 10BASE-T no preamble mode | R/W | Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it. | 0 |
| 4:0 | Reserved | RO | Reserved. | |

4.3.5 PoE and Miscellaneous Functionality

The register at address 23E1 controls various aspects of inline-powering and the CRC error counter in the VSC8530-05 device.

Table 49 • Extended PHY Control 4, Address 23E1 (0x17)

| Bit | Name | Access | Description | Default |
|-------|--|--------|---|---------|
| 15:11 | PHY address | RO | Internal PHY address: 0–31. | |
| 10 | Inline powered device detection | R/W | Sticky bit. 1: Enabled. | 0 |
| 9:8 | Inline powered device detection status | RO | Only valid when bit 10 is set. 00: Searching for devices. 01: Device found; requires inline-power. 10: Device found; does not require inline-power. 11: Reserved. | 00 |
| 7:0 | Cu Media CRC error counter | RO | Self-clearing 8-bit error count register. | |

4.3.6 VeriPHY Control 1

Register 24E1 in the extended register space provides control over the device VeriPHY diagnostics features. There are three separate VeriPHY control registers. The following table shows the settings available and describes the expected readouts.

Table 50 • VeriPHY Control Register 1, Address 24E1 (0x18)

| Bit | Name | Access | Description | Default |
|------|------------------------|--------|--|---------|
| 15 | VeriPHY trigger | R/W | Self-clearing bit. 1: Triggers the VeriPHY algorithm and clears when VeriPHY has completed. Settings in registers 24E–26E become valid after this bit clears. | 0 |
| 14 | VeriPHY valid | RO | 1: VeriPHY results in registers 24E–26E are valid. | 0 |
| 13:8 | Pair A (1, 2) distance | RO | Loop length or distance to anomaly for pair A (1, 2). | 0x00 |

Table 50 • VeriPHY Control Register 1, Address 24E1 (0x18) (continued)

| Bit | Name | Access | Description | Default |
|-----|------------------------|--------|---|---------|
| 7:6 | Reserved | RO | Reserved. | |
| 5:0 | Pair B (3, 6) distance | RO | Loop length or distance to anomaly for pair B (3, 6). | 0x00 |

Note: The resolution of the 6-bit length field is 3 meters.

4.3.7 VeriPHY Control 2

The register at address 25E1 consists of the second of the three device registers that provide control over VeriPHY diagnostics features. The following table shows the expected readouts.

Table 51 • VeriPHY Control Register 2, Address 25E1 (0x19)

| Bit | Name | Access | Description | Default |
|------|----------|--------|-------------|---------|
| 15:0 | Reserved | RO | Reserved | |

Note: The resolution of the 6-bit length field is 3 meters.

4.3.8 VeriPHY Control 3

The register at address 26E1 consists of the third of the three device registers that provide control over VeriPHY diagnostics features. Specifically, this register provides information about the termination status (fault condition) for all link partner pairs. The following table shows the expected readouts.

Table 52 • VeriPHY Control Register 3, Address 26E1 (0x1A)

| Bit | Name | Access | Description | Default |
|-------|----------------------------------|--------|-------------------------------------|---------|
| 15:12 | Pair A (1, 2) termination status | RO | Termination fault for pair A (1, 2) | 0x00 |
| 11:8 | Pair B (3, 6) termination status | RO | Termination fault for pair B (3, 4) | 0x00 |
| 7:0 | Reserved | RO | Reserved | |

The following table shows the meanings for the various fault codes.

Table 53 • VeriPHY Control Register 3 Fault Codes

| Code | Denotes |
|------|--|
| 0000 | Correctly terminated pair |
| 0001 | Open pair |
| 0010 | Shorted pair |
| 0100 | Abnormal termination |
| 1000 | Cross-pair short to pair A |
| 1001 | Cross-pair short to pair B |
| 1100 | Abnormal cross-pair coupling with pair A |
| 1101 | Abnormal cross-pair coupling with pair B |

4.3.9 Ethernet Packet Generator (EPG) Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 54 • EPG Control Register 1, Address 29E1 (0x1D)

| Bit | Name | Access | Description | Default |
|-------|---|--------|--|---------|
| 15 | EPG enable ¹ | R/W | 1: Enable EPG. | 0 |
| 14 | EPG run or stop | R/W | 1: Run EPG. | 0 |
| 13 | Transmission duration | R/W | 1: Continuous (sends in 10,000-packet increments). 0: Send 30,000,000 packets and stop. | 0 |
| 12:11 | Packet length | R/W | 00: 125 bytes. 01: 64 bytes. 10: 1518 bytes. 11: 10,000 bytes (jumbo packet). | 00 |
| 10 | Interpacket gap | R/W | 1: 8,192 ns. 0: 96 ns. | 0 |
| 9:6 | Destination address | R/W | Lowest nibble of the 6-byte destination address. | 0001 |
| 5:2 | Source address | R/W | Lowest nibble of the 6-byte destination address. | 0000 |
| 1 | Payload type | R/W | 1: Randomly generated payload pattern. 0: Fixed based on payload pattern. | 0 |
| 0 | Bad frame check sequence (FCS) generation | R/W | 1: Generate packets with bad FCS. 0: Generate packets with good FCS. | 0 |

- To end forced transmission of EEE LPIs from the PHY, clear the force EEE LPI bit (17E2.4) first before clearing the EPG enable bit (29E1.15).

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8530-05 device is connected to a live network.
- Bit 29E1.13 (continuous EPG mode control): when enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF F0 through 0xFF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF F0 through 0xFF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.10 Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 55 • EPG Control Register 2, Address 30E1 (0x1E)

| Bit | Name | Access | Description | Default |
|------|--------------------|--------|--|---------|
| 15:0 | EPG packet payload | R/W | Data pattern repeated in the payload of packets generated by the EPG | 0x0000 |

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see [Table 43](#), page 37.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 56 • Extended Registers Page 2 Space

| Address | Name |
|-----------|---------------------------------------|
| 16E2 | Cu PMD Transmit Control |
| 17E2 | EEE Control |
| 18E2–19E2 | Reserved |
| 20E2 | RGMII Control |
| 21E2 | Wake-on-LAN MAC Address [15:0] |
| 22E2 | Wake-on-LAN MAC Address [31:16] |
| 23E2 | Wake-on-LAN MAC Address [47:32] |
| 24E2 | Secure-On Password [15:0] |
| 25E2 | Secure-On Password [31:16] |
| 26E2 | Secure-On Password [47:32] |
| 27E2 | Wake-on-LAN and MAC Interface Control |
| 28E2 | Extended Interrupt Mask |
| 29E2 | Extended Interrupt Status |
| 30E2 | Reserved |

4.4.1 Cu PMD Transmit Control

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. For help with changing these values, contact your Microsemi representative.

Table 57 • Cu PMD Transmit Control, Address 16E2 (0x10)

| Bit | Name | Access | Description | Default |
|-------|----------|--------|-------------|---------|
| 15:12 | Reserved | RO | Reserved | |

Table 57 • Cu PMD Transmit Control, Address 16E2 (0x10) (continued)

| Bit | Name | Access | Description | Default |
|------|---|--------|--|---------|
| 11:8 | 100BASE-TX signal amplitude trim ¹ | R/W | Sticky bit. 100BASE-TX signal amplitude 0000: 1.8% 0001: 2.7% 0010: 3.6% 0011: 4.5% 0100: 5.4% 0101: 6.3% 0110: 7.2% 0111 8.1% 1000: -8% 1001: -6.2% 1010: -4.4% 1011: -2.7% 1100: -1.8% 1101: -0.9% 1110: 0% 1111: 0.9% | 0010 |
| 7:4 | 10BASE-T signal amplitude trim ² | R/W | Sticky bit. 10BASE-T signal amplitude 0000: 0% 0001: 0.9% 0010: 1.8% 0011: 2.7% 0100: 3.6% 0101: 4.5% 0110: 5.4% 0111: 6.1% 1000: -7.2% 1001: -6.3% 1010: -5.4% 1011: -4.5% 1100: -3.6% 1101: -2.7% 1110: -1.8% 1111: -0.9% | 1000 |

Table 57 • Cu PMD Transmit Control, Address 16E2 (0x10) (continued)

| Bit | Name | Access | Description | Default |
|-----|---------------------------------|--------|---|---------|
| 3:0 | 10BASE-Te signal amplitude trim | R/W | Sticky bit. 10BASE-Te signal amplitude 0000: 0% 0001: 0.65% 0010: 1.3% 0011: 1.95% 0100: 2.6% 0101: 3.25% 0110: 3.9% 0111: 4.55% 1000: -5.2% 1001: -4.55% 1010: -3.9% 1011: -3.25% 1100: -2.6% 1101: -1.95% 1110: -1.3% 1111: -0.65% | 1110 |

1. Adjust 100BASE-TX to specific magnetics.
2. Amplitude is limited by V_{CC} (2.5 V).

4.4.2 EEE Control

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in energy-efficient Ethernet (IEEE 802.3az-2010) mode for debug.

Table 58 • EEE Control, Address 17E2 (0x11)

| Bit | Name | Access | Description | Default |
|-------|---------------------------------|--------|--|---------|
| 15 | Enable 10BASE-Te | R/W | Sticky bit. Enable energy efficient (IEEE 802.3az-2010) 10BASE-Te operating mode. | 0 |
| 14:12 | Reserved | RO | Reserved. | |
| 11:10 | Invert LED polarity | R/W | Sticky bit. Invert polarity of LED signals. Default is to drive an active low signal on the LED pins. For more information, see Extended LED Modes , page 19. | 00 |
| 9 | Reserved | RO | Reserved. | |
| 8 | Link status | RO | 1: Link is up. | 0 |
| 7 | Reserved | RO | Reserved. | |
| 6 | 100BASE-TX EEE enable | RO | 1: EEE is enabled for 100BASE-TX. | 0 |
| 5 | Reserved | RO | Reserved. | |
| 4 | Force transmit LPI ¹ | R/W | Sticky bit. 1: Enable the EPG to transmit LPI on the MDI, ignore data from the MAC interface. 0: Transmit idles being received from the MAC. | 0 |

Table 58 • EEE Control, Address 17E2 (0x11) (continued)

| Bit | Name | Access | Description | Default |
|-----|-------------------------------------|--------|---|---------|
| 3 | Inhibit 100BASE-TX transmit EEE LPI | R/W | Sticky bit. 1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC. | 0 |
| 2 | Inhibit 100BASE-TX receive EEE LPI | R/W | Sticky bit. 1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI. | 0 |
| 1:0 | Reserved | RO | Reserved. | |

1. 17E2 bits 4:0 are for debugging purposes only, not for operational use.

4.4.3 RGMII Control

The following table shows the register settings for the RGMII controls at address 20E2.

Table 59 • RGMII Control, Address 20E2 (0x14)

| Bit | Name | Access | Description | Default |
|-------|------------------------|--------|---|---------|
| 15:12 | Reserved | RO | Reserved. | |
| 11:8 | Reserved | RO | Reserved. | |
| 7 | RGMII RXD bit reversal | R/W | Sticky bit. When set to 1, makes the following reversed mapping internally: RXD3 maps to RXD0 RXD2 maps to RXD1 RXD1 maps to RXD2 RXD0 maps to RXD3 | 0 |
| 6:4 | RX_CLK delay | R/W | Sticky bit. 000: 0.2 ns delay. 001: 0.8 ns delay. 010: 1.1 ns delay. 011: 1.7 ns delay. 100: 2.0 ns delay. 101: 2.3 ns delay. 110: 2.6 ns delay. 111: 3.4 ns delay. | 000 |
| 3 | RGMII TXD bit reversal | R/W | Sticky bit. When set to 1, makes the following reversed mapping internally: TXD3 maps to TXD0 TXD2 maps to TXD1 TXD1 maps to TXD2 TXD0 maps to TXD3 | 0 |

Table 59 • RGMII Control, Address 20E2 (0x14) (continued)

| Bit | Name | Access | Description | Default |
|-----|--------------|--------|---|---------|
| 2:0 | TX_CLK delay | R/W | Sticky bit. 000: 0.2 ns delay. 001: 0.8 ns delay. 010: 1.1 ns delay. 011: 1.7 ns delay. 100: 2.0 ns delay. 101: 2.3 ns delay. 110: 2.6 ns delay. 111: 3.4 ns delay. | 000 |

4.4.4 Wake-on-LAN MAC Address [15:0]

The following table shows the register settings for the Wake-on-LAN MAC address at 21E2.

Table 60 • Wake-on-LAN MAC Address, 21E2 (0x15)

| Bit | Name | Access | Description | Default |
|------|------------------------|--------|---|---------|
| 15:0 | WoL MAC address [15:0] | R/W | Sticky bit. WoL MAC address lower two bytes. | 0x0000 |

4.4.5 Wake-on-LAN MAC Address [31:16]

The following table shows the register settings for the Wake-on-LAN MAC address at 22E2.

Table 61 • Wake-on-LAN MAC Address, 22E2 (0x16)

| Bit | Name | Access | Description | Default |
|------|-------------------------|--------|--|---------|
| 15:0 | WoL MAC address [31:16] | R/W | Sticky bit. WoL MAC address middle two bytes. | 0x0000 |

4.4.6 Wake-on-LAN MAC Address [47:32]

The following table shows the register settings for the Wake-on-LAN MAC address at 23E2.

Table 62 • Wake-on-LAN MAC Address, 23E2 (0x17)

| Bit | Name | Access | Description | Default |
|------|-------------------------|--------|---|---------|
| 15:0 | WoL MAC address [47:32] | R/W | Sticky bit. WoL MAC address upper two bytes. | 0x0000 |

4.4.7 Secure-On Password [15:0]

The following table shows the register settings for the Secure-On password used for WoL at 24E2.

Table 63 • Secure-On Password, 24E2 (0x18)

| Bit | Name | Access | Description | Default |
|------|---------------------------|--------|--|---------|
| 15:0 | Secure-On password [15:0] | R/W | Sticky bit. Secure-On password for WoL lower two bytes. | 0x0000 |

4.4.8 Secure-On Password [31:16]

The following table shows the register settings for the Secure-On password used for WoL at 25E2.

Table 64 • Secure-On Password, 25E2 (0x19)

| Bit | Name | Access | Description | Default |
|------|----------------------------|--------|---|---------|
| 15:0 | Secure-On password [31:16] | R/W | Sticky bit. Secure-On password for WoL middle two bytes. | 0x0000 |

4.4.9 Secure-On Password [47:32]

The following table shows the register settings for the Secure-On password used for WoL at 26E2.

Table 65 • Secure-On Password, 26E2 (0x1A)

| Bit | Name | Access | Description | Default |
|------|----------------------------|--------|--|---------|
| 15:0 | Secure-On password [47:32] | R/W | Sticky bit. Secure-On password for WoL upper two bytes. | 0x0000 |

4.4.10 Wake-on-LAN and MAC Interface Control

The following table shows the register settings for the Wake-on-LAN and MAC interface control at address 27E2.

Table 66 • WoL and MAC Interface Control, Address 27E2 (0x1B)

| Bit | Name | Access | Description | Default |
|-------|--|--------|--|---------|
| 15 | Secure-On enable | R/W | Sticky bit. 0: Disabled. 1: Enabled. | 0 |
| 14 | Secure-On password length | R/W | Sticky bit. 0: 6 byte password. 1: 4 byte password. | 0 |
| 13:12 | Reserved | RO | Reserved. | |
| 11:8 | Address repetition count in Magic packet | R/W | Sticky bit. Count value: 0000: 1 0001: 2 0010: 3 0011: 4 0100: 5 0101: 6 0110: 7 0111: 8 1000: 9 1001: 10 1010: 11 1011: 12 1100: 13 1101: 14 1110: 15 1111: 16 | 1111 |

Table 66 • WoL and MAC Interface Control, Address 27E2 (0x1B) (continued)

| Bit | Name | Access | Description | Default |
|-----|-----------------------|--------|--|---------|
| 7:5 | Pad edge rate control | R/W | Sticky bit. MAC interface edge rate control. 000: Slowest edge rate 001: +1 pad edge rate 010: +2 pad edge rate 011: +3 pad edge rate 100: +4 pad edge rate 101: +5 pad edge rate 110: +6 pad edge rate 111: +7 pad edge rate (fastest) | 111 |
| 4 | RMII CLKOUT enable | R/W | Sticky bit. 0: RMII CLKOUT disabled. 1: RMII CLKOUT enabled. | 1 |
| 3:1 | Reserved | RO | Reserved. | |
| 0 | MDINT CMOS drive | R/W | Sticky bit. 0: Disabled. 1: Enabled. | 0 |

4.4.11 Extended Interrupt Mask

The following table shows the register settings for the extended interrupt mask at address 28E2.

Table 67 • Extended Interrupt Mask, Address 28E2 (0x1C)

| Bit | Name | Access | Description | Default |
|-------|---|--------|-------------------------|---------|
| 15:14 | Reserved | RO | Reserved. | |
| 13 | Rx FIFO overflow/underflow interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 12 | Tx FIFO overflow/underflow interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 11:4 | Reserved | RO | Reserved. | |
| 3 | EEE link fail interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 2 | EEE Rx TQ timer interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 1 | EEE wait quiet/Rx TS timer interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |
| 0 | EEE wake error interrupt mask | R/W | Sticky bit. 1: Enabled. | 0 |

4.4.12 Extended Interrupt Status

The following table shows the register settings for the extended interrupt status at address 29E2.

Table 68 • Extended Interrupt Status, Address 29E2 (0x1D)

| Bit | Name | Access | Description | Default |
|-------|---|--------|---|---------|
| 15:14 | Reserved | RO | Reserved. | |
| 13 | Rx FIFO overflow/underflow interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 12 | Tx FIFO overflow/underflow interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 11:4 | Reserved | RO | Reserved. | |

Table 68 • Extended Interrupt Status, Address 29E2 (0x1D) (continued)

| Bit | Name | Access | Description | Default |
|-----|---|--------|---|---------|
| 3 | EEE link fail interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 2 | EEE Rx TQ timer interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 1 | EEE wait quiet/Rx TS timer interrupt status | RO | Self-clearing bit. 1: Interrupt pending. | 0 |
| 0 | EEE wake error interrupt mask | RO | Self-clearing bit. 1: Interrupt pending. | 0 |

4.5 General Purpose Registers

Accessing the general purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31. All general purpose register bits are super-sticky.

Table 69 • General Purpose Registers Space

| Address | Name |
|---------|----------------------|
| 0G–12G | Reserved |
| 13G | CLKOUT Control |
| 14G | GPIO Control 2 |
| 15G–24G | Reserved |
| 25G | Enhanced LED Control |
| 26G–30G | Reserved |

4.5.1 CLKOUT Control

The CLKOUT control register configures the functionality of the CLKOUT output pin.

Table 70 • CLKOUT Control, Address 13G (0x0D)

| Bit | Name | Access | Description | Default |
|-------|-------------------------|--------|---|---------|
| 15 | CLKOUT enable | R/W | 1: CLKOUT enabled. 0: CLKOUT disabled. | 0 |
| 14:13 | CLKOUT frequency select | R/W | 00: 25 MHz. 01: 50 MHz. 10: 125 MHz. 11: Reserved. | 00 |
| 12:0 | Reserved | RO | Reserved. | |

4.5.2 GPIO Control 2

The GPIO control 2 register configures the functionality of the LED pins.

Table 71 • GPIO Control 2, Address 14G (0x0E)

| Bit | Name | Access | Description | Default |
|-------|----------|--------|-------------|---------|
| 15:10 | Reserved | RO | Reserved. | |

Table 71 • GPIO Control 2, Address 14G (0x0E) (continued)

| Bit | Name | Access | Description | Default |
|-----|---------------------------|--------|--|---------|
| 9 | Tri-state enable for LEDs | R/W | 1: Tri-state LED output signals instead of driving them high. This allows the signals to be pulled above V_{DDIO} using an external pull-up resistor. 0: Drive LED bus output signals to high and low values. | 1 |
| 8:0 | Reserved | RO | Reserved. | |

4.5.3 Enhanced LED Control

Register 25G in the extended register space controls the advanced functionality of the parallel LED signals.

Table 72 • Enhanced LED Control, Address 25G (0x19)

| Bit | Name | Access | Description | Default |
|------|--------------------------------|--------|--|---------|
| 15:8 | LED pulsing duty cycle control | R/W | Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments. | 0x00 |
| 7:0 | Reserved | RO | Reserved. | |

4.6 Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf

This section describes the Clause 45 registers that are required to support energy-efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers).

The following table lists the addresses and register names in the Clause 45 register page space. When the link is down, 0 is the value returned for the x.180x addresses.

Table 73 • Clause 45 Registers Page Space

| Address | Name |
|---------|--------------------------------|
| 1.1 | PMA/PMD status 1 |
| 1.1800 | PMA/PMD time sync capable |
| 1.1801 | PMA/PMD delay Tx max. |
| 1.1803 | PMA/PMD delay Tx min. |
| 1.1805 | PMA/PMD delay Rx max. |
| 1.1807 | PMA/PMD delay Rx min. |
| 3.1 | PCS status 1 |
| 3.20 | EEE capability |
| 3.22 | EEE wake error counter |
| 7.60 | EEE advertisement |
| 7.61 | EEE link partner advertisement |

4.6.1 PMA/PMD Status 1

The following table shows the bit descriptions for the PMA/PMD Status 1 register.

Table 74 • PMA/PMD Status 1

| Bit | Name | Access | Description |
|------|-----------------------------|--------|--|
| 15:3 | Reserved | RO | Reserved. |
| 2 | PMD/PMA receive link status | RO/LL | 1: PMA/PMD receive link up. 0: PMA/PMD receive link down. |
| 1:0 | Reserved | RO | Reserved. |

4.6.2 PCS Status 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

Table 75 • PCS Status 1, Address 3.1

| Bit | Name | Access | Description |
|-------|-------------------------|--------|---|
| 15:12 | Reserved | RO | Reserved. |
| 11 | Tx LPI received | RO/LH | 1: Tx PCS has received LPI. 0: LPI not received. |
| 10 | Rx LPI received | RO/LH | 1: Rx PCS has received LPI. 0: LPI not received. |
| 9 | Tx LPI indication | RO | 1: Tx PCS is currently receiving LPI. 0: PCS is not currently receiving LPI. |
| 8 | Rx LPI indication | RO | 1: Rx PCS is currently receiving LPI. 0: PCS is not currently receiving LPI. |
| 7:3 | Reserved | RO | Reserved. |
| 2 | PCS receive link status | RO/LL | 1: PCS receive link up. 0: PCS receive link down. |
| 1:0 | Reserved | RO | Reserved. |

4.6.3 EEE Capability

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

Table 76 • EEE Capability, Address 3.20

| Bit | Name | Access | Description |
|------|----------------|--------|--|
| 15:2 | Reserved | RO | Reserved. |
| 1 | 100BASE-TX EEE | RO | 1: EEE is supported for 100BASE-TX. 0: EEE is not supported for 100BASE-TX. |
| 0 | Reserved | RO | Reserved. |

4.6.4 EEE Wake Error Counter

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as

defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 77 • EEE Wake Error Counter, Address 3.22

| Bit | Name | Access | Description |
|------|--------------------|--------|-------------------------------------|
| 15:0 | Wake error counter | RO | Count of wake time faults for a PHY |

4.6.5 EEE Advertisement

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

Table 78 • EEE Advertisement, Address 7.60

| Bit | Name | Access | Description | Default |
|------|----------------|--------|---|---------|
| 15:2 | Reserved | RO | Reserved. | |
| 1 | 100BASE-TX EEE | R/W | 1: Advertise that the 100BASE-TX has EEE capability. 0: Do not advertise that the 100BASE-TX has EEE capability. | 0 |
| 0 | Reserved | RO | Reserved. | |

4.6.6 EEE Link Partner Advertisement

All the bits in the EEE LP advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

Table 79 • EEE Advertisement, Address 7.61

| Bit | Name | Access | Description |
|------|----------------|--------|--|
| 15:2 | Reserved | RO | Reserved. |
| 1 | 100BASE-TX EEE | RO | 1: Link partner is advertising EEE capability for 100BASE-TX. 0: Link partner is not advertising EEE capability for 100BASE-TX. |
| 0 | Reserved | RO | Reserved. |

4.6.7 802.3bf Registers

The following table shows the bit assignments for the 802.3bf registers. When the link is down, 0 is the value returned. 1.1801 would be device address of 1 and register address of 1801.

Table 80 • 802.3bf Registers

| Register | Name | Function |
|----------|---------------------------|--|
| 1.1800 | PMA/PMD Time Sync capable | 1: PMA/PMD Time Sync Tx capable. 0: PMA/PMD Time Sync Rx capable. |
| 1.1801 | PMA/PMD delay Tx max | Tx maximum delay through PHY (PMA/PMD/PCS). |
| 1.1803 | PMA/PMD delay Tx min | Tx minimum delay through PHY (PMA/PMD/PCS). |
| 1.1805 | PMA/PMD delay Rx max | Rx maximum delay through PHY (PMA/PMD/PCS). |
| 1.1807 | PMA/PMD delay Rx min | Rx minimum delay through PHY (PMA/PMD/PCS). |

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8530-05 device.

5.1 DC Characteristics

This section contains the DC specifications for the VSC8530-05 device.

5.1.1 VDDMAC, VDDIO, and VDDMDIO (2.5 V)

The following table shows the DC specifications for the pins referenced to VDDMAC, VDDIO, and VDDMDIO when it is set to 2.5 V. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, and VDD25A = 2.5 V.

Table 81 • VDDMAC, VDDIO, and VDDMDIO (2.5 V) DC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|------------------------|-------------|---------|---------|---------|---------|----------------------------|
| Output high voltage | V_{OH} | 2.0 | | | V | $I_{OH} = -1.0$ mA |
| Output low voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 1.0$ mA |
| Input high voltage | V_{IH} | 1.85 | | 3.6 | V | |
| Input high voltage | V_{IH} | 1.85 | | 3.1 | V | SMI pins (MDC, MDIO) |
| Input high voltage | V_{IH} | 1.85 | | 2.75 | V | VDDMAC-referenced pins |
| Input low voltage | V_{IL} | -0.3 | | 0.7 | V | |
| Input leakage current | I_{ILEAK} | -85 | | 85 | μ A | Internal resistor included |
| Output leakage current | I_{OLEAK} | -85 | | 85 | μ A | Internal resistor included |

5.1.2 VDDMAC, VDDIO, and VDDMDIO (3.3 V)

The following table shows the DC specifications for the pins referenced to VDDMAC, VDDIO, and VDDMDIO when it is set to 3.3 V. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, and VDD25A = 2.5 V.

Table 82 • VDDMAC, VDDIO, and VDDMDIO (3.3 V) DC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|------------------------|-------------|---------|---------|---------|---------|----------------------------|
| Output high voltage | V_{OH} | 2.6 | | | V | $I_{OH} = -1.0$ mA |
| Output low voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 1.0$ mA |
| Input high voltage | V_{IH} | 2.25 | | 3.6 | V | |
| Input low voltage | V_{IL} | -0.3 | | 0.8 | V | |
| Input leakage current | I_{ILEAK} | -135 | | 135 | μ A | Internal resistor included |
| Output leakage current | I_{OLEAK} | -135 | | 135 | μ A | Internal resistor included |

5.1.3 VDDMAC and VDDMDIO (1.5 V)

The following table shows the DC specifications for the pins referenced to VDDMAC and VDDMDIO when it is set to 1.5 V. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, VDD25A = 2.5 V, and VDDIO = 2.5 V or 3.3 V.

Table 83 • VDDMAC and VDDMDIO DC Characteristics (1.5 V)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|------------------------|-------------|---------|---------|---------|---------|----------------------------|
| Output high voltage | V_{OH} | 1.2 | | | V | $I_{OH} = -1$ mA |
| Output low voltage | V_{OL} | | | 0.25 | V | $I_{OL} = 1$ mA |
| Input high voltage | V_{IH} | 1.13 | | 1.87 | V | VDDMDIO-referenced pins |
| Input high voltage | V_{IH} | 1.13 | | 1.65 | V | VDDMAC-referenced pins |
| Input low voltage | V_{IL} | -0.375 | | 0.45 | V | |
| Input leakage current | I_{ILEAK} | -40 | | 40 | μ A | Internal resistor included |
| Output leakage current | I_{OLEAK} | -40 | | 40 | μ A | Internal resistor included |

5.1.4 VDDMAC and VDDMDIO (1.8 V)

The following table shows the DC specifications for the pins references to VDDMAC and VDDMDIO when it is set to 1.8 V. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, VDD25A = 2.5 V, and VDDIO = 2.5 V or 3.3 V.

Table 84 • VDDMAC and VDDMDIO DC Characteristics (1.8 V)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|------------------------|-------------|---------|---------|---------|---------|----------------------------|
| Output high voltage | V_{OH} | 1.43 | | | V | $I_{OH} = -1$ mA |
| Output low voltage | V_{OL} | | | 0.3 | V | $I_{OL} = 1$ mA |
| Input high voltage | V_{IH} | 1.35 | | 2.25 | V | VDDMDIO-referenced pins |
| Input high voltage | V_{IH} | 1.35 | | 1.98 | V | VDDMAC-referenced pins |
| Input low voltage | V_{IL} | -0.45 | | 0.54 | V | |
| Input leakage current | I_{ILEAK} | -48 | | 48 | μ A | Internal resistor included |
| Output leakage current | I_{OLEAK} | -48 | | 48 | μ A | Internal resistor included |

5.1.5 VDDMDIO (1.2 V)

The following table shows the DC specifications for the pins referenced to VDDMDIO when it is set to 1.2 V. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, and VDD25A = 2.5 V.

Table 85 • VDDMDIO DC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|------------------------|-------------|---------|---------|---------|---------|----------------------------|
| Output high voltage | V_{OH} | 0.95 | | | V | $I_{OH} = -1$ mA |
| Output low voltage | V_{OL} | | | 0.2 | V | $I_{OL} = 1$ mA |
| Input high voltage | V_{IH} | 0.9 | | 1.5 | V | |
| Input low voltage | V_{IL} | -0.3 | | 0.36 | V | |
| Input leakage current | I_{ILEAK} | -32 | | 32 | μ A | Internal resistor included |
| Output leakage current | I_{OLEAK} | -32 | | 32 | μ A | Internal resistor included |

5.1.6 XTAL1

The following table shows the DC specifications for the XTAL1 pin referenced to VDD25A. The specifications listed in the following table are valid only when VDD1 = 1.0 V, VDD1A = 1.0 V, and the on-chip oscillator is turned off.

Table 86 • XTAL1 DC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|------------------------|-------------|---------|---------|---------|---------|
| Input high voltage | V_{IH} | 1.85 | | 2.75 | V |
| Input low voltage | V_{IL} | -0.3 | | 0.7 | V |
| Input leakage current | I_{LEAK} | -85 | | 85 | μ A |
| Output leakage current | I_{OLEAK} | -85 | | 85 | μ A |

5.1.7 LED

The following table shows the DC specifications for the LED pins.

Table 87 • LED DC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|------------------------------------|----------|---------|---------|---------|------|
| Output high current drive strength | I_{OH} | | | -24 | mA |
| Output low current drive strength | I_{OL} | 24 | | | mA |

5.1.8 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. All internal pull-up resistors are connected to their respective I/O supply.

Table 88 • Internal Pull-Up or Pull-Down Resistors (RGMI/ RMI Interface)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|-----------------------------|----------|---------|---------|---------|------------|-----------|
| Internal pull-down resistor | R_{PD} | 31 | 46 | 72 | k Ω | 3.3 V |
| Internal pull-down resistor | R_{PD} | 38 | 59 | 96 | k Ω | 2.5 V |
| Internal pull-down resistor | R_{PD} | 57 | 91 | 155 | k Ω | 1.8 V |
| Internal pull-down resistor | R_{PD} | 78 | 125 | 220 | k Ω | 1.5 V |

Table 89 • Internal Pull-Up or Pull-Down Resistors (Other I/Os)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|-----------------------------|----------|---------|---------|---------|------------|-----------|
| Internal pull-up resistor | R_{PU} | 26 | 39 | 64 | k Ω | 3.3 V |
| Internal pull-down resistor | R_{PD} | 26 | 45 | 79 | k Ω | 3.3 V |
| Internal pull-up resistor | R_{PU} | 33 | 53 | 93 | k Ω | 2.5 V |
| Internal pull-down resistor | R_{PD} | 34 | 58 | 108 | k Ω | 2.5 V |

5.1.9 Current Consumption

The following table shows the measured current consumption values for each mode of operation. Add values from table for VDDMAC current consumption to calculate total typical current for each power supply. Add significant margin above the values for sizing power supplies.

Note: VDDMAC currents at 1.5 V and 1.8 V are measured with an edge rate setting of 111. Currents at 2.5 V and 3.3 V are measured with an edge rate setting of 100.

Table 90 • Current Consumption

| Mode | Typical (mA) | | | |
|----------------|--------------|-------|--------|---------------|
| | VDD1 | VDD1A | VDD25A | VDDIO/VDDMDIO |
| Reset | 15 | 5 | 5 | 5 |
| Power Down | 20 | 20 | 15 | 5 |
| ActiPHY | 20 | 20 | 20 | 5 |
| No Link | 30 | 20 | 55 | 5 |
| 100BASE-TX | 35 | 20 | 100 | 5 |
| 10BASE-T | 20 | 20 | 65 | 5 |
| 100BASE-TX EEE | 25 | 20 | 60 | 5 |
| 10BASE-Te | 20 | 20 | 60 | 5 |

Table 91 • Current Consumption (VDDMAC)

| Mode | Typical (mA) | | | |
|--------------------|--------------|-------|-------|-------|
| | 1.5 V | 1.8 V | 2.5 V | 3.3 V |
| Reset | 5 | 5 | 5 | 5 |
| Power Down | 10 | 10 | 15 | 20 |
| ActiPHY | 10 | 10 | 15 | 20 |
| No Link | 10 | 10 | 15 | 20 |
| RGMI (100BASE-TX) | 5 | 10 | 10 | 15 |
| RGMI (10BASE-T/Te) | 5 | 5 | 5 | 5 |
| RMII (100BASE-TX) | 10 | 15 | 15 | 20 |
| RMII (10BASE-T/Te) | 10 | 10 | 15 | 15 |

Table 92 • Power Consumption

| Parameter | Symbol | Typical | Maximum | Unit |
|------------------------------|--------|---------|---------|------|
| Worst-case power consumption | P_D | | 580 | mW |

5.2 AC Characteristics

This section provides the AC specifications for the VSC8530-05 device.

5.2.1 Reference Clock

The following table lists the AC specifications for the REFCLK reference clock.

Table 93 • RefClk

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|--|--------|----------|---------|---------|------|-----------|
| REFCLK frequency, REFCLK_SEL[1:0]= 11 | f | -100 ppm | 125 | 100 ppm | MHz | |
| REFCLK frequency, REFCLK_SEL[1:0]= 10 | f | -100 ppm | 50 | 100 ppm | MHz | |

Table 93 • RefClk (continued)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|--|------------|----------|---------|---------|-------------------|---------------------------------|
| REFCLK frequency, REFCLK_SEL[1:0]= 01 | f | -100 ppm | 25 | 100 ppm | MHz | |
| Rise time and fall time | t_R, t_F | | | 1.5 | ns | 20% to 80%, 5.1 pF load |
| Duty cycle | | 45 | | 55 | % | |
| Phase jitter—Gaussian | | | | 4 | ps _{RMS} | Bandwidth from 10 kHz to 10 MHz |
| Total jitter, peak-to-peak | | | | 200 | ps _{PP} | 10K samples. |

5.2.1.1 XTAL Reference Clock

When using the 25 MHz crystal clock input option (REFCLK_SEL[1:0] = 00), the additional specifications listed in the following table are required.

Table 94 • XTAL RefClk

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|-----------------|--------|---------|---------|---------|------|
| CL ¹ | | 8 | | | pF |
| Crystal ESR | | | | 60 | Ω |

$$1. \quad CL = \frac{C1_{EXT} \times C2_{EXT}}{C1_{EXT} + C2_{EXT}}$$

where

$$C1_{EXT} = C1 + C_{IN_{EXT}}$$

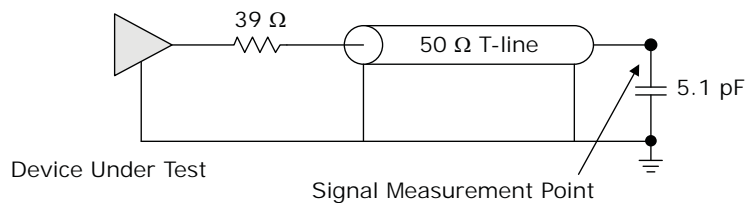
$$C2_{EXT} = C2 + C_{OUT_{EXT}}$$

$C_{IN_{EXT}}$ represents input (XTAL1) I/O, bond pad, package pin, and routing parasitic capacitance

and $C_{OUT_{EXT}}$ represents output (XTAL2) I/O, bond pad, package pin, and routing parasitic capacitance.

For a reference tank circuit, see [Figure 9](#), page 12.

The following illustration shows the test circuit for the CLKOUT, RCVRD_CLK, and RMII_CLKOUT outputs.

Figure 21 • Test Circuit for Clock Output Signal

5.2.2 CLKOUT

This section provides the AC characteristics for the CLKOUT signal.

The following table shows the AC specifications for the CLKOUT output.

Table 95 • CLKOUT AC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|-------------------------------|---------------------------------|---------|---------|---------|------|-------------------------------------|
| CLKOUT frequency | f | | 125 | | MHz | |
| CLKOUT frequency | f | | 50 | | MHz | |
| CLKOUT frequency | f | | 25 | | MHz | |
| CLKOUT cycle time | t_{COCYC} | | 8 | | ns | |
| CLKOUT cycle time | t_{COCYC} | | 20 | | ns | |
| CLKOUT cycle time | t_{COCYC} | | 40 | | ns | |
| Frequency stability | $f_{\text{STABILITY}}$ | | | 5 | ppm | Relative to device REFCLK frequency |
| Duty cycle | DC | 40 | 50 | 60 | % | CLKOUT at 25 MHz and 125 MHz |
| Duty cycle | DC | 35 | 50 | 75 | % | CLKOUT at 50 MHz |
| Clock rise time and fall time | $t_{\text{R}}, t_{\text{F}}$ | | | 1.5 | ns | 20% to 80% |
| Peak-to-peak jitter | $J_{\text{PP}}_{\text{CLKOUT}}$ | | | 700 | ps | 10 k samples |

5.2.3 RMII_CLKOUT

This section provides the AC characteristics for the RMII_CLKOUT signal.

Note: The RMII_CLKOUT signal is provided on the RX_CLK pin (see Table 3, page 5) when the device is operating in RMII mode.

The following table shows the AC specifications for RMII_CLKOUT.

Table 96 • RMII_CLKOUT AC Characteristics

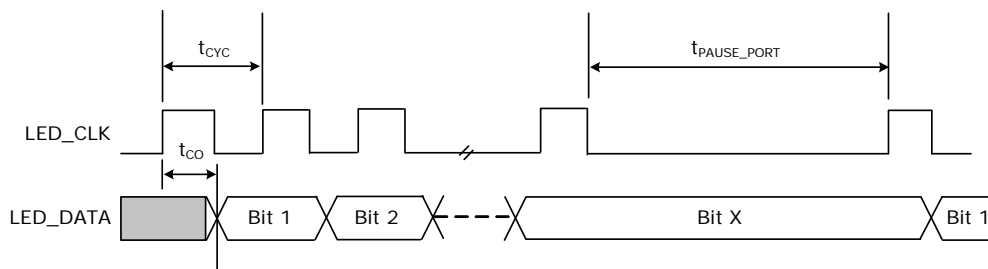
| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|------------------------|----------------|---------|---------|---------|------|
| RMII_CLKOUT frequency | f | | 50 | | MHz |
| RMII_CLKOUT duty cycle | DC | 35 | | 65 | % |
| RMII_CLKOUT rise time | t_{R} | | | 1 | ns |
| RMII_CLKOUT fall time | t_{F} | | | 1 | ns |

5.2.4 Basic Serial LEDs

This section contains the AC specifications for the basic serial LEDs.

Table 97 • Basic Serial LEDs AC Characteristics

| Parameter | Symbol | Typical | Unit |
|----------------------------------|--------------------------|-----------|------|
| LED_CLK cycle time | t_{CYC} | 1024 | ns |
| Pause between LED port sequences | $t_{\text{PAUSE_PORT}}$ | 3072 | ns |
| Pause between LED bit sequences | $t_{\text{PAUSE_BIT}}$ | 25.541632 | ms |
| LED_CLK to LED_DATA | t_{CO} | 1 | ns |

Figure 22 • Basic Serial LED Timing

5.2.5 RMII AC Characteristics

The following table lists the characteristics when using the device in RMII mode.

Table 98 • RMII AC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|------------|---------|---------|---------|------|
| TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER data setup to RMII_CLKIN rising edge | T_{SU} | 4 | | | ns |
| TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER data hold from RMII_CLKIN rising edge | T_{HOLD} | 2 | | | ns |

5.2.6 Uncompensated RGMII

The following table lists the characteristics when using the device in RGMII uncompensated mode. For more information about the RGMII uncompensated timing, see [Figure 23](#), page 61.

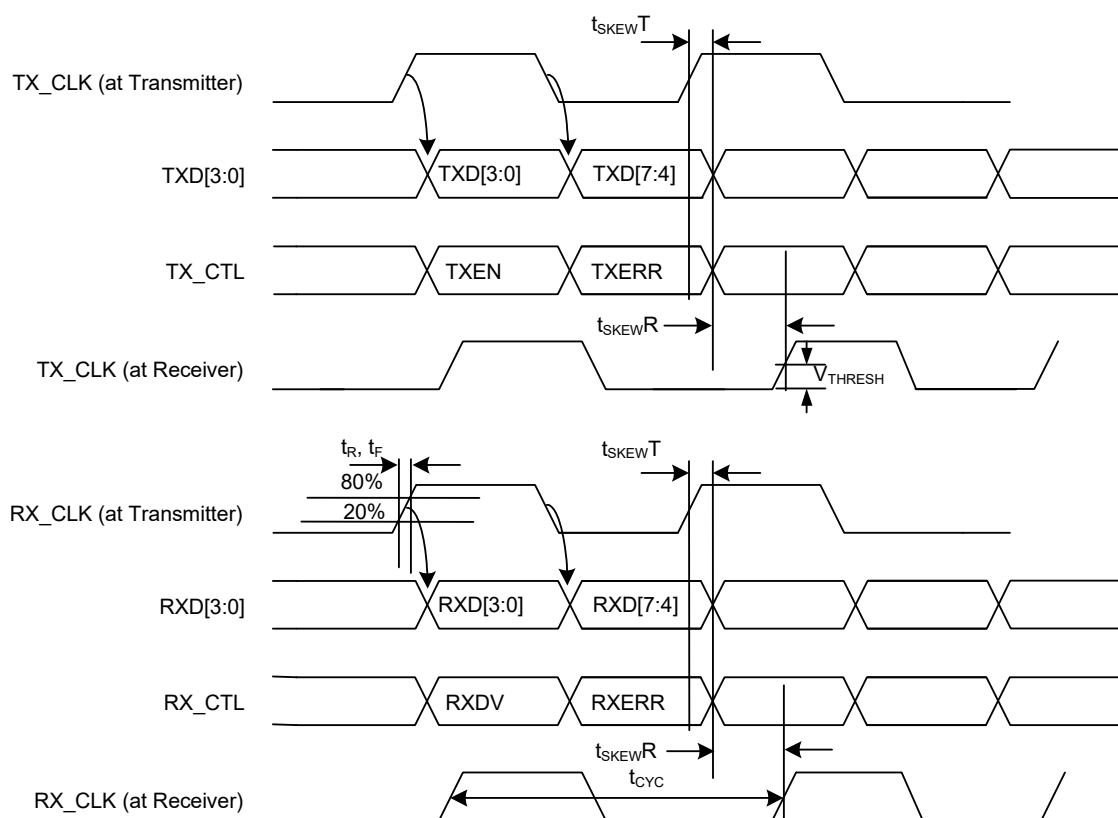
Table 99 • Uncompensated RGMII AC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|--|--------------|---------|------------------------------|---------|------|--|
| Clock frequency | f_{CLK} | | 25 2.5 | | MHz | 100BASE-TX operation 10BASE-T operation |
| Duty cycle | DC | 40 | 50 | 60 | % | |
| Data to clock output skew (at Transmitter) ¹ | t_{SKEWT} | -500 | | 500 | ps | |
| Data to clock output skew (at Receiver) ¹ | t_{SKEWR} | 1 | 1.8 | 2.6 | ns | |
| TX_CLK switching threshold | V_{THRESH} | | 0.75 0.90 1.25 1.65 | | V | VDDMAC = 1.5 V VDDMAC = 1.8 V VDDMAC = 2.5 V VDDMAC = 3.3 V |

Table 99 • Uncompensated RGMII AC Characteristics (continued)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|---------------------------------------|------------|---------|---------|---------|------|-----------------------------------|
| Clock/data output rise and fall times | t_R, t_F | | | 0.75 | ns | VDDMAC = 1.5 V, 27E2.7:5 = 111 |
| | | | | | | VDDMAC = 1.8 V, 27E2.7:5 = 111 |
| | | | | | | VDDMAC = 2.5 V, 27E2.7:5 = 100 |
| | | | | | | VDDMAC = 3.3 V, 27E2.7:5 = 100 |

- When operating in uncompensated mode, the PC board design requires a clock to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

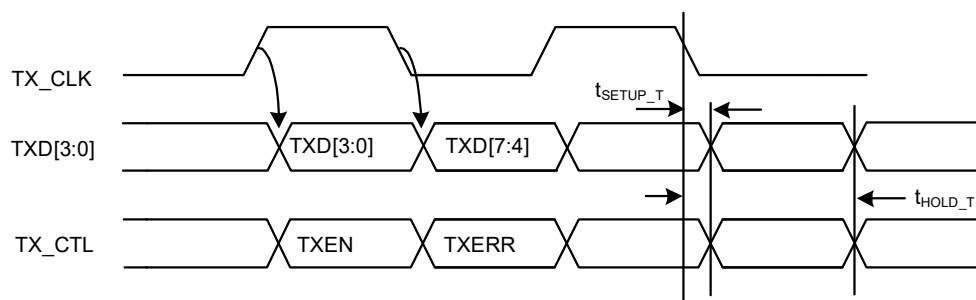
Figure 23 • Uncompensated RGMII Timing

5.2.7 Compensated RGMII

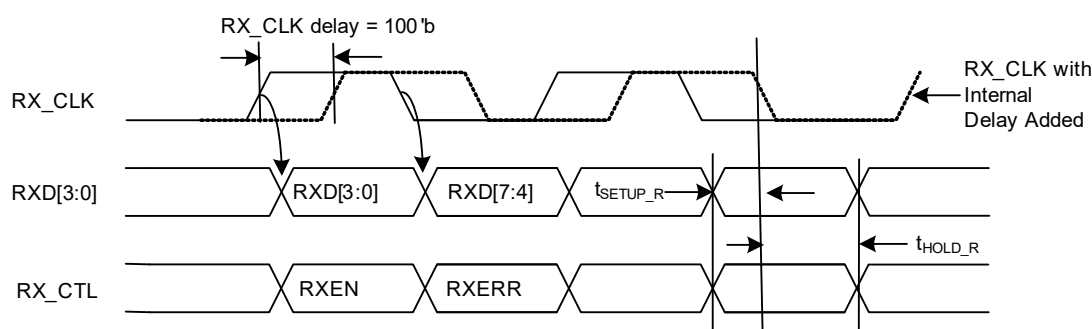
The following table lists the characteristics when using the device in RGMII compensated mode.

Table 100 • PHY Input (GTX_CLK Delay When Register 20E2.[2:0]=011'b)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|---------------|---------|---------|---------|------|
| Data to clock setup (TX_CLK delay = 011'b) | t_{SETUP_T} | -1.0 | | | ns |
| Clock to data hold (TX_CLK delay = 011'b) | t_{HOLD_T} | 2.8 | | | ns |

Figure 24 • Compensated Input RGMII Timing**Table 101 • PHY Output (RX_CLK Delay When Register 20E2.[6:4]=100'b)**

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|----------------------|---------|---------|---------|------|
| Data to clock setup (RX_CLK delay = 100'b) | t_{SETUP_R} | 1.4 | 2.0 | | ns |
| Clock to data hold (RX_CLK delay = 100'b) | t_{HOLD_R} | 1.5 | 2.0 | | ns |

Figure 25 • Compensated Output RGMII Timing

5.2.8 Serial Management Interface

This section contains the AC specifications for the serial management interface (SMI).

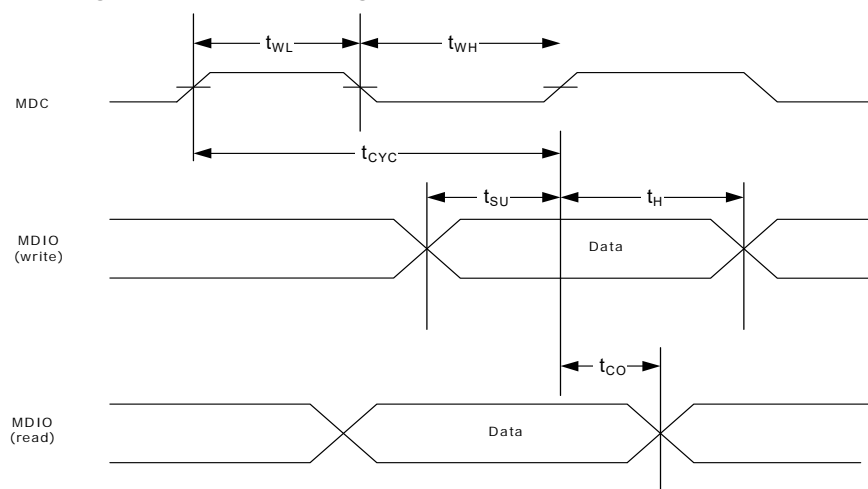
Table 102 • Serial Management Interface AC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|----------------------------|------------------|---------|---------|--------------------------------------|------|---|
| MDC frequency ¹ | f_{CLK} | | 2.5 | 12.5 | MHz | |
| MDC cycle time | t_{CYC} | 80 | 400 | | ns | |
| MDC time high | t_{WH} | 20 | 50 | | ns | |
| MDC time low | t_{WL} | 20 | 50 | | ns | |
| Setup to MDC rising | t_{SU} | 10 | | | ns | |
| Hold from MDC rising | t_{H} | 14 | | | ns | |
| MDC rise time | t_{R} | | | 100 $t_{\text{CYC}} \times 10\%1$ | ns | $f_{\text{CLK}} < 1$ MHz f_{CLK} from 1 MHz to 12.5 MHz |
| MDC fall time | t_{F} | | | 100 $t_{\text{CYC}} \times 10\%1$ | ns | $f_{\text{CLK}} < 1$ MHz f_{CLK} from 1 MHz to 12.5 MHz |

Table 102 • Serial Management Interface AC Characteristics (continued)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|-------------------|----------|---------|---------|---------|------|--|
| MDC to MDIO valid | t_{CO} | | 10 | 300 | ns | Time-dependent on the value of the external pull-up resistor on the MDIO pin |

- For f_{CLK} above 1 MHz, the maximum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the maximum clock rise time and fall time is 50 ns.

Figure 26 • Serial Management Interface Timing

5.2.9 Reset Timing

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

Table 103 • Reset Timing AC Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|-------------|---------|---------|---------|------|
| NRESET assertion time after power supplies and clock stabilize | t_W | 2 | | | ms |
| Recovery time from reset inactive to device fully active | t_{REC} | | 15 | | ms |
| NRESET pulse width | $t_{W(RL)}$ | 100 | | | ns |
| Wait time between NRESET de-assert and access of the SMI interface | t_{WAIT} | 15 | | | ms |

5.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC8530-05 device.

Table 104 • Recommended Operating Conditions

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|-------------|---------|---------|---------|------|
| Power supply voltage for core supply | V_{DD1} | 0.95 | 1.00 | 1.05 | V |
| Power supply voltage for analog circuits | V_{DD1A} | 0.95 | 1.00 | 1.05 | V |
| 2.5 V power supply voltage for analog circuits | V_{DD25A} | 2.38 | 2.5 | 2.62 | V |
| 2.5 V power supply voltage for VDDMAC, VDDIO, and VDDMDIO | V_{25} | 2.38 | 2.5 | 2.62 | V |

Table 104 • Recommended Operating Conditions (continued)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|-----------------|---------|---------|---------|------|
| 3.3 V power supply voltage for VDDMAC, VDDIO, and VDDMDIO | V ₃₃ | 3.135 | 3.3 | 3.465 | V |
| 1.8 V power supply voltage for VDDMAC and VDDMDIO | V ₁₈ | 1.71 | 1.8 | 1.89 | V |
| 1.5 V power supply voltage for VDDMAC and VDDMDIO | V ₁₅ | 1.425 | 1.5 | 1.575 | V |
| 1.2 V power supply voltage for VDDMDIO | V ₁₂ | 1.14 | 1.2 | 1.26 | V |
| VSC8530-05 operating temperature ¹ | T | -40 | | 125 | °C |

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

5.4 Stress Ratings

This section contains the stress ratings for the VSC8530-05 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 105 • Stress Ratings

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|--|-----------------------|---------|------|
| Power supply voltage for core supply | V _{DD1} | -0.3 | 1.10 | V |
| Power supply voltage for analog circuits | V _{DD1A} | -0.3 | 1.10 | V |
| Power supply voltage for analog circuits | V _{DD25A} | -0.3 | 2.75 | V |
| Power supply voltage for digital I/O | V _{DDMAC} , V _{DDIO} , V _{DDMDIO} | -0.3 | 3.6 | V |
| Input voltage for digital I/O (3.3 V) | | | 3.6 | V |
| Input voltage for digital I/O (2.5 V) | | | 3.3 | V |
| Storage temperature | T _S | -55 | 125 | °C |
| Electrostatic discharge voltage, charged device model | V _{ESD_CDM} | -1000 | 1000 | V |
| Electrostatic discharge voltage, human body model | V _{ESD_HBM} | See note ¹ | | V |

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8530-05 device has 48 pins, which are described in this section.



The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

6.1 Pin Identifications

This section contains the pin descriptions for the VSC8530-05 device. The following table provides notations for definitions of the various pin types.

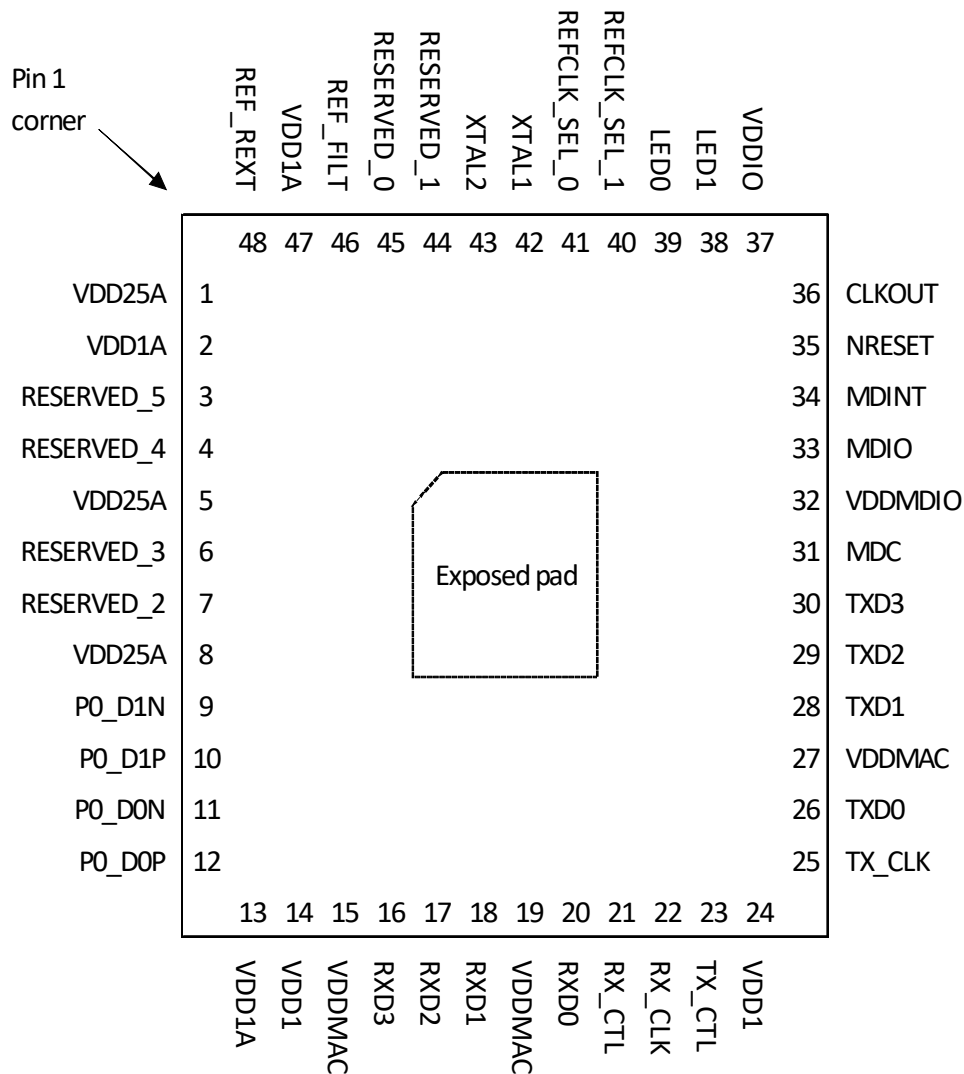
Table 106 • Pin Type Symbol Definitions

| Symbol | Pin Type | Description |
|--------|---------------------|--|
| A | Analog | Analog. |
| ADIFF | Analog differential | Analog differential signal pair. |
| I | Input | Input without on-chip pull-up or pull-down resistor. |
| I/O | Bidirectional | Bidirectional input or output signal. |
| O | Output | Output signal. |
| P | Power | Power. |
| PD | Pull-down | On-chip pull-down resistor present. |
| PU | Pull-up | On-chip pull-up resistor present. |

6.2 Pin Diagram

The following illustration shows the pin diagram for the VSC8530-05 device, as seen looking through the package from the top of it. Note that the exposed pad connects to the package ground.

Figure 27 • Pin Diagram



6.3 Pins by Function

This section contains the functional pin descriptions for the VSC8530-05 device. All power supply pins must be connected to their respective voltage input, even if certain functions are not used for a specific application. No power supply sequencing is required. However, clock and power must be stable before releasing Reset. The SMI pins are referenced to VDDMDIO.

| Functional Group | Name | Number | Type | I/O Domain | Description |
|------------------|--------|--------|-------|------------|---------------------------------|
| Cu PHY Media | P0_D0N | 11 | ADIFF | VDD25A | Tx/Rx channel A negative signal |
| Cu PHY Media | P0_D0P | 12 | ADIFF | VDD25A | Tx/Rx channel A positive signal |
| Cu PHY Media | P0_D1N | 9 | ADIFF | VDD25A | Tx/Rx channel B negative signal |

| | | | | | |
|-------------------|--------------|----|---------|--------|---|
| Cu PHY Media | P0_D1P | 10 | ADIFF | VDD25A | Tx/Rx channel B positive signal |
| Miscellaneous | REF_FILT | 46 | A | VDD25A | Reference filter connects to an external 0.01 uF (20%) capacitor to analog ground |
| Miscellaneous | REF_REXT | 48 | A | VDD25A | Reference connects to an external 2k Ω (1%) resistor to analog ground |
| Miscellaneous | RESERVED_0 | 45 | | VDD25A | Reserved signal, leave unconnected |
| Miscellaneous | RESERVED_1 | 44 | | VDD25A | Reserved signal, leave unconnected |
| Miscellaneous | RESERVED_2 | 7 | ADIFF | VDD25A | Internal test signal. Connect a 100 Ω (5%) resistor across this pin and pin 6. |
| Miscellaneous | RESERVED_3 | 6 | ADIFF | VDD25A | Internal test signal. Connect a 100 Ω (5%) resistor across this pin and pin 7. |
| Miscellaneous | RESERVED_4 | 4 | ADIFF | VDD25A | Internal test signal. Connect a 100 Ω (5%) resistor across this pin and pin 3. |
| Miscellaneous | RESERVED_5 | 3 | ADIFF | VDD25A | Internal test signal. Connect a 100 Ω (5%) resistor across this pin and pin 4. |
| PHY Configuration | CLKOUT | 36 | I/O, PD | VDDIO | Clock output, can be enabled or disabled. Output a clock based on the local reference clock with programmable frequency. This pin is not active when NRESET is asserted and is disabled by default. When disabled, the pin is held low. The logic state on this pin is latched on the rising edge of NRESET to configure CLKOUT output. See "Hardware Mode Strapping and PHY Addressing" for details. |
| PHY Configuration | LED0 | 39 | O | VDDIO | LED direct drive outputs. All LED pins are active low. LED_DATA output in serial LED mode. |
| PHY Configuration | LED1 | 38 | O | VDDIO | LED direct drive outputs. All LED pins are active low. LED_CLK output in serial LED mode. |
| PHY Configuration | NRESET | 35 | I, PD | VDDIO | Device reset. Active low input that powers down the device and sets all register bits to their default state. |
| PHY Configuration | REFCLK_SEL_0 | 41 | I, PU | VDDIO | Reference clock mode/frequency select signal |
| PHY Configuration | REFCLK_SEL_1 | 40 | I, PU | VDDIO | Reference clock mode/frequency select signal |
| PHY Configuration | XTAL1 | 42 | I | VDD25A | Crystal/single ended reference clock input |
| PHY Configuration | XTAL2 | 43 | O | VDD25A | Crystal output, leave unconnected when using single ended reference clock |
| PWR | VDD1 | 14 | P | | 1.0 V digital core power |
| PWR | VDD1 | 24 | P | | 1.0 V digital core power |
| PWR | VDD1A | 2 | P | | 1.0 V analog power requiring additional PCB power supply filtering |

| | | | | |
|------------|---------|----|----------------|--|
| PWR | VDD1A | 13 | P | 1.0 V analog power requiring additional PCB power supply filtering |
| PWR | VDD1A | 47 | P | 1.0 V analog power requiring additional PCB power supply filtering |
| PWR | VDD25A | 1 | P | 2.5 V analog power requiring additional PCB power supply filtering |
| PWR | VDD25A | 5 | P | 2.5 V analog power requiring additional PCB power supply filtering |
| PWR | VDD25A | 8 | P | 2.5 V analog power requiring additional PCB power supply filtering |
| PWR | VDDIO | 37 | P | 2.5 V or 3.3 V general I/O power |
| PWR | VDDMAC | 15 | P | 1.5 V, 1.8 V, 2.5 V, or 3.3 V RGMII/RMII MAC power |
| PWR | VDDMAC | 19 | P | 1.5 V, 1.8 V, 2.5 V, or 3.3 V RGMII/RMII MAC power |
| PWR | VDDMAC | 27 | P | 1.5 V, 1.8 V, 2.5 V, or 3.3 V RGMII/RMII MAC power |
| PWR | VDDMDIO | 32 | P | 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V power for SMI pins |
| RGMII/RMII | RX_CLK | 22 | I/O, PD VDDMAC | RGMII receive clock output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |
| RGMII/RMII | RX_CTL | 21 | I/O, PD VDDMAC | RGMII receive control output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |
| RGMII/RMII | RXD0 | 20 | I/O, PD VDDMAC | RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |
| RGMII/RMII | RXD1 | 18 | I/O, PD VDDMAC | RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |
| RGMII/RMII | RXD2 | 17 | I/O, PD VDDMAC | RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |
| RGMII/RMII | RXD3 | 16 | I/O, PD VDDMAC | RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device. See "Hardware Mode Strapping and PHY Addressing" for details. |

| | | | | | |
|------------|--------|----|-------|---------|--|
| RGMII/RMII | TX_CLK | 25 | I, PD | VDDMAC | RGMII transmit clock input |
| RGMII/RMII | TX_CTL | 23 | I, PD | VDDMAC | RGMII transmit data control input |
| RGMII/RMII | TXD0 | 26 | I, PD | VDDMAC | RGMII data input |
| RGMII/RMII | TXD1 | 28 | I, PD | VDDMAC | RGMII data input |
| RGMII/RMII | TXD2 | 29 | I, PD | VDDMAC | RGMII data input |
| RGMII/RMII | TXD3 | 30 | I, PD | VDDMAC | RGMII data input |
| SMI | MDC | 31 | I | VDDMDIO | Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY. |
| SMI | MDINT | 34 | O, OD | VDDMDIO | Management interrupt signal. These pins can be tied together in a wired-OR configuration with only a single pull-up resistor. |
| SMI | MDIO | 33 | I/O | VDDMDIO | Management data input/output pin. Serial data is written or read from this pin bi-directionally between the PHY and station manager synchronously on the positive edge of MDC. One external pull-up resistor is required at the station manager. |

7 Package Information

The VSC8530XMW-05 package is a lead-free (Pb-free), 48-pin, plastic quad flat no-lead (QFN) package with an exposed pad, 6 mm × 6 mm body size, 0.4 mm pin pitch, and 0.9 mm maximum height.

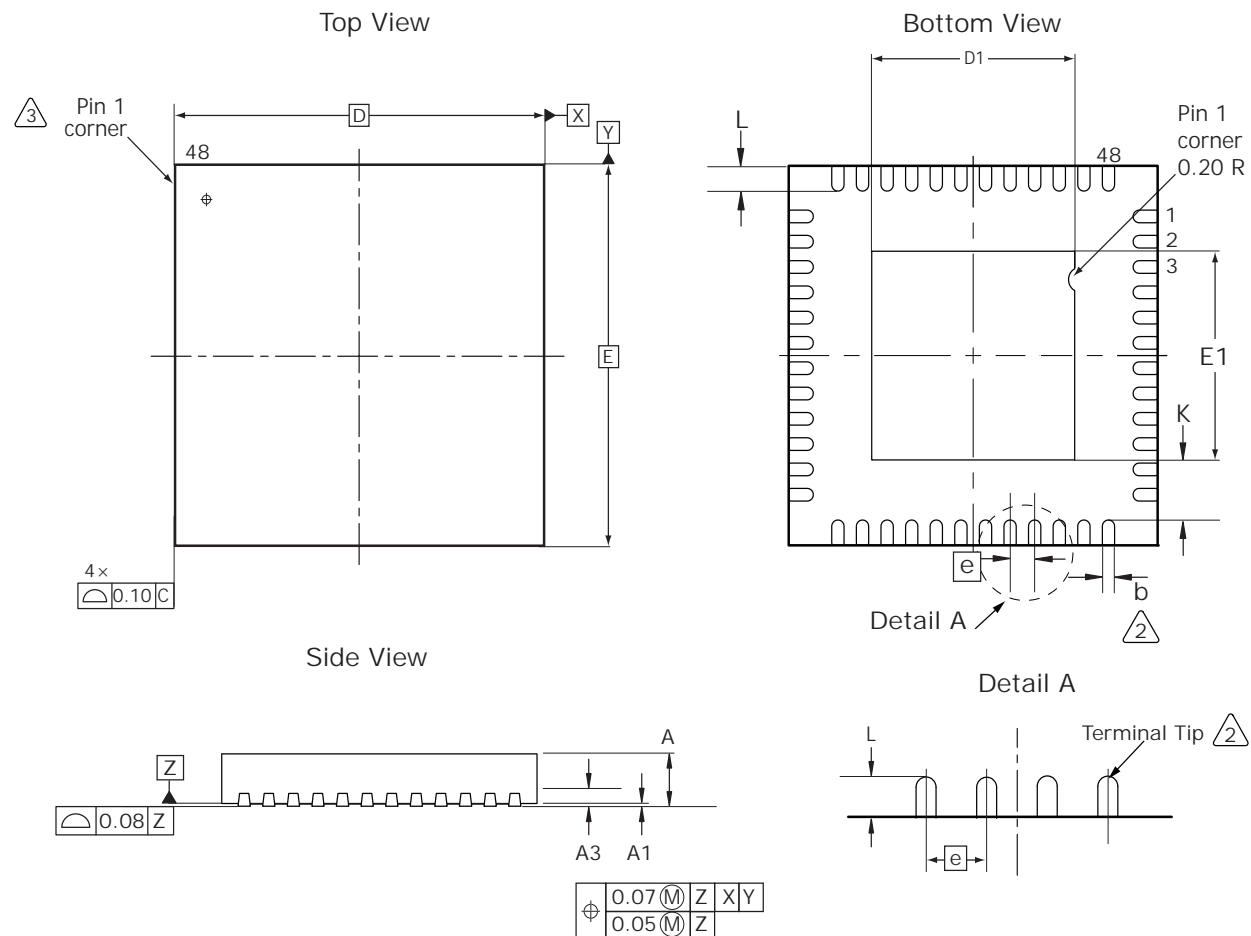
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8530-05 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8530-05 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 28 • Package Drawing



Notes

- All dimensions and tolerances are in millimeters (mm).
- Dimension b applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
- Maximum package warpage is 0.08 mm.

Dimensions and Tolerances

| Reference | Minimum | Nominal | Maximum |
|-----------|---------|-----------|---------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 Ref | |
| D | | 6.00 BSC | |
| D1 | 3.20 | 3.30 | 3.40 |
| E | | 6.00 BSC | |
| E1 | 3.20 | 3.30 | 3.40 |
| K | | 0.95 Ref | |
| e | | 0.40 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.15 | 0.20 | 0.25 |

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC website at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p

PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 107 • Thermal Resistances

| Symbol | °C/W | Parameter |
|-------------------------|-------|--|
| $\theta_{J\text{Ctop}}$ | 31.62 | Die junction to package case top |
| θ_{JB} | 9.34 | Die junction to printed circuit board |
| θ_{JA} | 31.73 | Die junction to ambient |
| θ_{JMA} at 1 m/s | 25.0 | Die junction to moving air measured at an air speed of 1 m/s |
| θ_{JMA} at 2 m/s | 23.75 | Die junction to moving air measured at an air speed of 2 m/s |

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using QFN packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Considerations

This section provides information about design considerations for the VSC8530-05 device.

8.1 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages. Additionally, associated templates may be marginal or have failures.

This issue is not estimated to present any system-level impact. Performance is not impaired with cables up to 130 m with various link partners.

8.2 Receive error counter only clears when NRESET applied in RMII mode

When operating in RMII MAC interface mode, the receive error counter of register 19 ([Table 32](#), page 31) does not clear upon read-back or software reset of the device. The only way to clear this register while in RMII mode is to assert the NRESET pin of the device.

The receive error counter at register address 19 operates normally in MAC interface modes other than RMII.

8.3 Anomalous PCS error indications in Energy Efficient Ethernet mode

When a port is processing traffic with EEE enabled on the link, certain PCS errors (such as false carriers, spurious start-of-stream detection, and idle errors) and EEE wake errors may occur. There is no effect on traffic bit error rate for cable lengths up to 75 meters, and minor packet loss may occur on links longer than 75 meters.

Regardless of cable length, some error indications should not be used while EEE is enabled. These error indications include false carrier interrupts ([Interrupt Status](#), page 35, bit 3), receive error interrupts ([Interrupt Status](#), page 35, bit 0), and EEE wake error interrupts.

Contact Microsemi for a script that needs to be applied during system initialization if EEE will be enabled.

9 Ordering Information

The VSC8530XMW-05 package is a lead-free (Pb-free), 48-pin, plastic quad flat no-lead (QFN) package with an exposed pad, 6 mm × 6 mm body size, 0.4 mm pin pitch, and 0.9 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8530-05 device.

Table 108 • Ordering Information

| Part Order Number | Description |
|-------------------|---|
| VSC8530XMW-05 | Lead-free, 48-pin, plastic QFN package with an exposed pad, 6 mm × 6 mm body size, 0.4 mm pin pitch, and 0.9 mm maximum height. |



Microsemi Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

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