LTC2000, LTC2000A
16-, 14-, 11-Bit, 2.5Gsps to 2.7Gsps DACs

DESCRIPTION

Demonstration circuit 2303 supports the LTC®2000 and LTC2000A, a high speed, high dynamic range family of DACs. It was specially designed for applications that require differential DC coupled outputs. DC2303 supports the complete family of the LTC2000 including 16-, 14- and 11-bit parts. For all the variations see Table 1.

The DC2303 was designed to conform to the FMC form factor allowing this board to be used with standard FMC FPGA demo boards and mounted into FMC chassis.

The circuitry on the analog outputs is optimized for analog frequencies from DC-1.08GHz.

Design files for this circuit board are available at http://www.linear.com/demo/DC2303

Table 1. DC2303 Variants

DC2303 VARIANTS	PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	OUTPUT FREQUENCY
DC2303A-A	LTC2000-16	16-Bit	2.5Gsps	DC-1000MHz
DC2303A-B	LTC2000-14	14-Bit	2.5Gsps	DC-1000MHz
DC2303A-C	LTC2000-11	11-Bit	2.5Gsps	DC-1000MHz
DC2303A-D	LTC2000A-16	16-Bit	2.7Gsps	DC-1080MHz
DC2303A-E	LTC2000A-14	14-Bit	2.7Gsps	DC-1080MHz
DC2303A-F	LTC2000A-11	11-Bit	2.7Gsps	DC-1080MHz

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC2303	This supply must provide up to 800mA	4.8	5.0	5.2	V
Sampling Frequency (Sample Clock Frequency)		300		2500 or 2700	MHz
Sample Clock Level (Single-Ended)	Use a 50Ω Source	0		15	dBm
LVDS Inputs	Differential Input Voltage Range	±0.2		±0.6	V
	Common Mode Voltage Range	0.4		1.8	V

QUICK START PROCEDURE

DC2303 is easy to set up to evaluate the performance of the LTC2000. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

Setup

The Xilinx KC705 development kit and a DC2159 was supplied with the DC2303 demonstration circuit. If these boards were not provided, follow the KC705 demo manual to install the required software and for connecting the KC705 board to the DC2303 and DC2159 and to a PC.

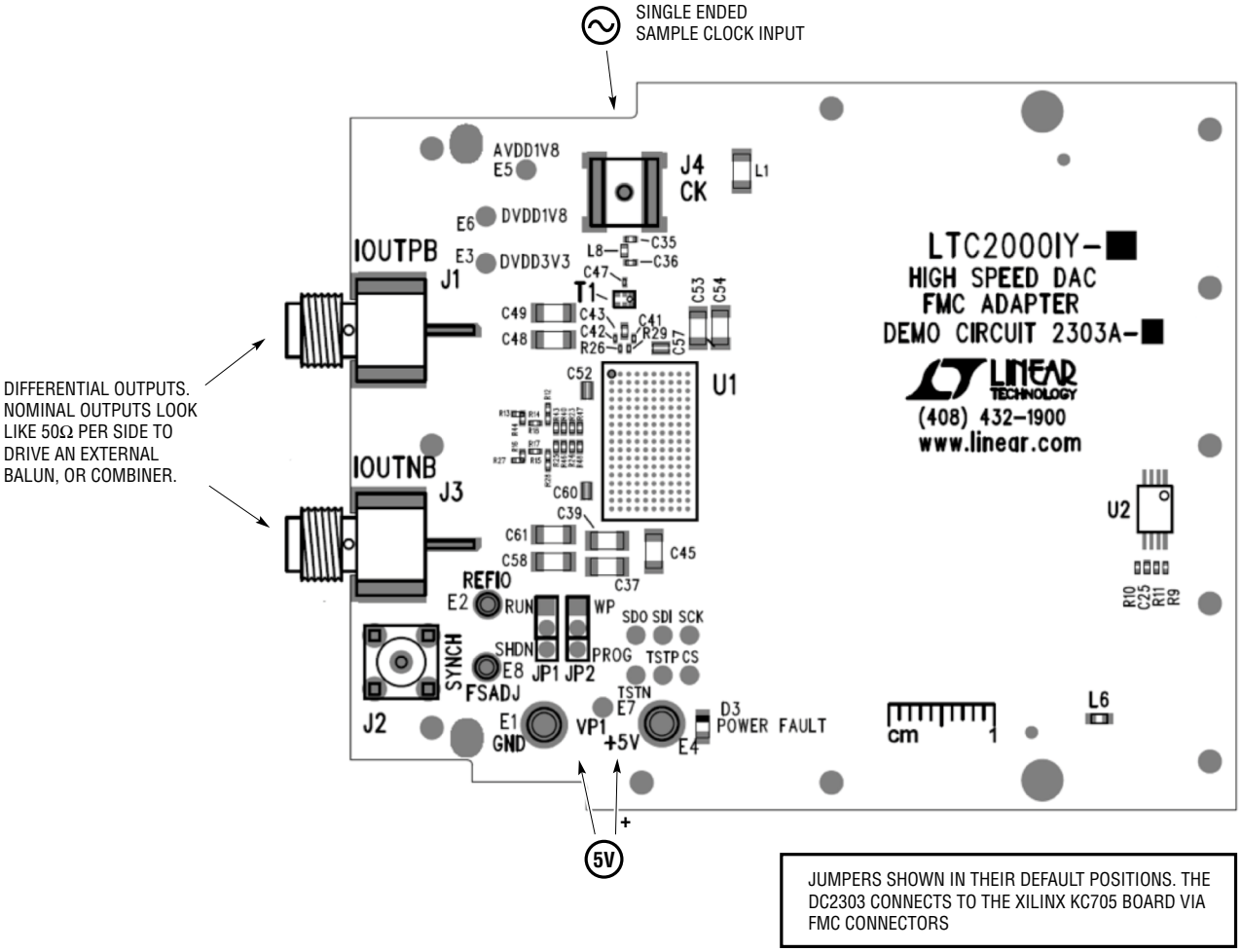

Figure 1. DC2303 Setup (Zoom for Details)

QUICK START PROCEDURE

HARDWARE SETUP

SMAs

J4: Sample Clock Input. Apply a clock signal to this SMA connector from a 50Ω driver. A 0dBm clock source should be sufficient, but for best phase noise and jitter performance, use the highest possible amplitude and slew rate, up to 15dBm.

J1, J3: Differential Output Signals. These SMAs provide access to the differential outputs of the DAC. The output impedance is designed to be 50Ω at each SMA, or 100Ω differential. Connect an external balun or combiner to these pins to drive a single-ended spectrum analyzer. Linear Technology has various adaptor boards for specific frequencies and applications. More information is available at www.linear.com/LTC2000#demoboards.

J2: SYNCH. This SMA is to provide access to the sync pin of the LT8614. It is not used in normal use.

Turrets

5V (E4): Positive Input Voltage for the DAC and Digital Circuits. This voltage feeds a series of regulators that supply the proper voltages for the DAC. The voltage range for this turret is 4.8V to 5.2V. Note: For close-in phase noise plots, driving this voltage is not ideal. There is a known 20kHz noise hump in the spectrum that is generated by the regulators. For the best phase noise performance, back drive the onboard regulators with the provided turrets from a low noise supply.

GND (E1): Ground Connection. This demo board has only a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

FSADJ (E8): This is an optional pin that is tied directly to the FSADJ pin of the DAC. It can be used to set the full-scale output current of the DAC. In normal operation this pin is tied to GND through 500Ω to set a current of 40mA at the output. See data sheet for equations to set different current levels, then replace R45 on the backside of the board.

REFIO (E2): This pin is tied directly to the REFIO pin of the DAC and is used to set the reference voltage for the DAC. Normally it is internally set to 1.25V but can be overdriven with an external voltage from 1.1V to 1.4V.

TEST POINTS

AVDD1V8 (E5): Optional 1.8V Input. This pin is connected directly to the AVDD18 pin of the DAC. It requires a supply that can deliver up to 1A. Driving this pin will override the onboard regulator.

DVDD3V3 (E3): Optional 3.3V Input. This pin is connected directly to the DVDD33, AVDD33 and SVDD pins of the DAC. It requires a supply that can deliver up to 50mA. Driving this pin will override the onboard regulator.

DVDD1V8 (E6): Optional 1.8V Input. This pin is connected directly to the DVDD18 pin of the DAC. It requires a supply that can deliver up to 500mA. Driving this pin will override the onboard regulator.

VP1 (E7): This is a test point that is at the output of the onboard switching regulator. It is meant for test purposes. It can also be driven to 2.5V to shut down the output of the switching regulator.

TSTP, TSTN: These pins are tied directly to the TSTP and TSTN pins of the DAC. They can be used to measure the internal temperature and timing of the LVDS inputs.

CS: Chip Select. This pin connects directly to the $\overline{CS}$ pin of the LTC2000.

SCK: Serial Clock. This pin connects directly to the SCK pin of the LTC2000.

SDI: Serial Data Input. This pin connects directly to the SDI pin of the LTC2000.

SDO: Serial Data Output. This pin connects directly to the SDO pin of the LTC2000.

QUICK START PROCEDURE

Jumpers

The DC2303 demonstration circuit should have the following jumper settings as default positions.

JP1: In the RUN position this pin results in normal operation of the DAC. In the SHDN position the DAC is powered down. (Default: RUN or up)

JP2: EEPROM Write Protect. For factory use only. Should be left in the protected (WP) position.

Connectors

P1: FMC Connector. This connector is designed to connect to the Xilinx KC705 board or any other FMC compatible FPGA board. All of the communication between the FPGA and the DAC is routed through this connector.

APPLYING POWER AND SIGNALS TO THE DC2303 DEMONSTRATION CIRCUIT

If a KC705 demo board is used to supply data to the DC2303, the two boards should first be bolted together for a proper electrical connection.

If Linear Technology provided the KC705 board the proper FPGA programming file (bit file) is already installed in flash memory and will begin to operate when the board is powered on. A DC2159 was also provided for a USB connection between the LTDACGen software and the FPGA. If an unprogrammed FPGA board is used, refer to the appropriate documentation on how to program it.

Power should be applied to the system in this order:

1. Connect the DC2303 to the KC705 board on HPC FMC connector, J22. Connect the DC2159 demo board into the LPC FMC connector, J2.
2. Connect the USB cable to J3 of the provided DC2159.
3. Apply a clock to J4 of the DC2303.
4. Connect any optional output board, like the DC2266, to J1 and J3.
5. Connect the 5V from a bench supply to the 5V turret on the DC2303.

QUICK START PROCEDURE

6. Turn on the voltage to the KC705.
7. Open the LTDACGen software and hit connect.

LTDACGen should report back that it is connected to the FPGA. See Figure 2.

ANALOG OUTPUT NETWORK

The analog output network of the DC2303 has been designed to maximize the performance of the LTC2000. The LTC2000 drives two 50Ω resistors on each side to minimize the impedance it sees. This maximizes the SFDR the DAC is able to produce. If a larger signal swing is required this impedance can be increased, but the SFDR might degrade. The output also has a pi network of 50Ω resistors to pad the output impedance of the board up to 50Ω per side. This allows the demo board to drive a 50Ω analyzer through a balun or other combiner.

Linear Technology has various adaptor boards for specific frequencies and applications. More information is available at http://www.linear.com/product/LTC2000#demoboards.

SAMPLE CLOCK

The sample clock to the DC2303 demonstration circuit board is marked J4. As a default it is a single-ended 50Ω input port. There is an onboard balun that does a single-ended to differential translation.

For the best noise performance, the sample input must be driven with a very low jitter signal generator source. The amplitude should be as large as possible up to ±3.6V or 15dBm.

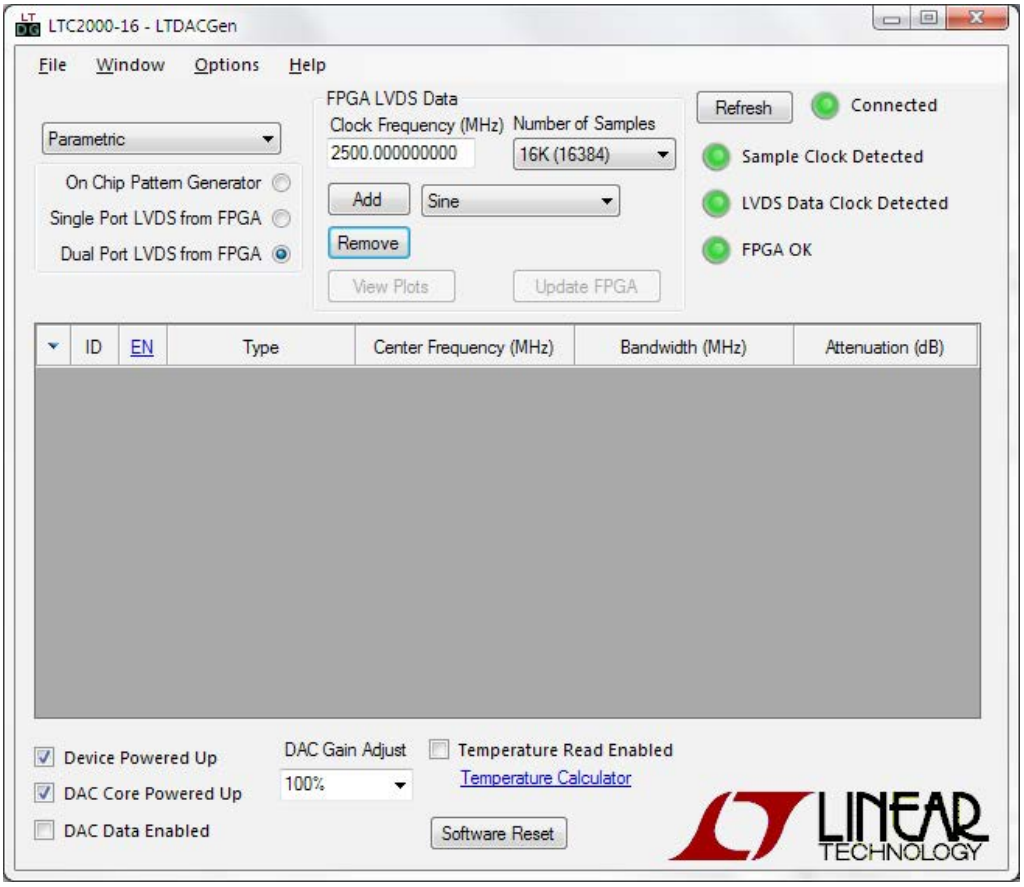

Figure 2. LTDACGen Connected to FPGA

QUICK START PROCEDURE

POWER

There are several options for powering the DC2303 demo board. The preferred option is to apply 5V from a bench supply to the 5V turret on the demo board. This voltage feeds a series of regulators that supply the proper voltages for the DAC. The voltage range for this turret is 4.8V to 5.2V. For applications that are sensitive to close in phase noise, driving this voltage is not ideal. There is a known 20kHz noise hump in the spectrum that is generated by the regulators. For the best phase noise performance, back drive the onboard regulators with the provided turrets from a low noise supply. The DC2303 demo board can also be powered from the 12V supply on the FMC connector. By populating L6 the 12V power supply from the FPGA board will be used instead of an external supply.

SOFTWARE

The software for the DC2303, LTDACGen is available at http://www.linear.com/designtools/software/#DAC free of charge. It simplifies the creation of complex waveforms and loading them into the FPGA to test the DC2303. For more information about how to use the LTDACGen software, refer to the help files that come with the software.

RESULTS

After everything is set up and the software is connected to the DAC demo system, a sine wave can be added to the output waveform. The default frequency is 399.932861328MHz (Figure 3). By clicking Update FPGA, the data is sent to the FPGA and is then used to program the DAC. A spectrum analyzer can then be used to view the results (Figure 4).

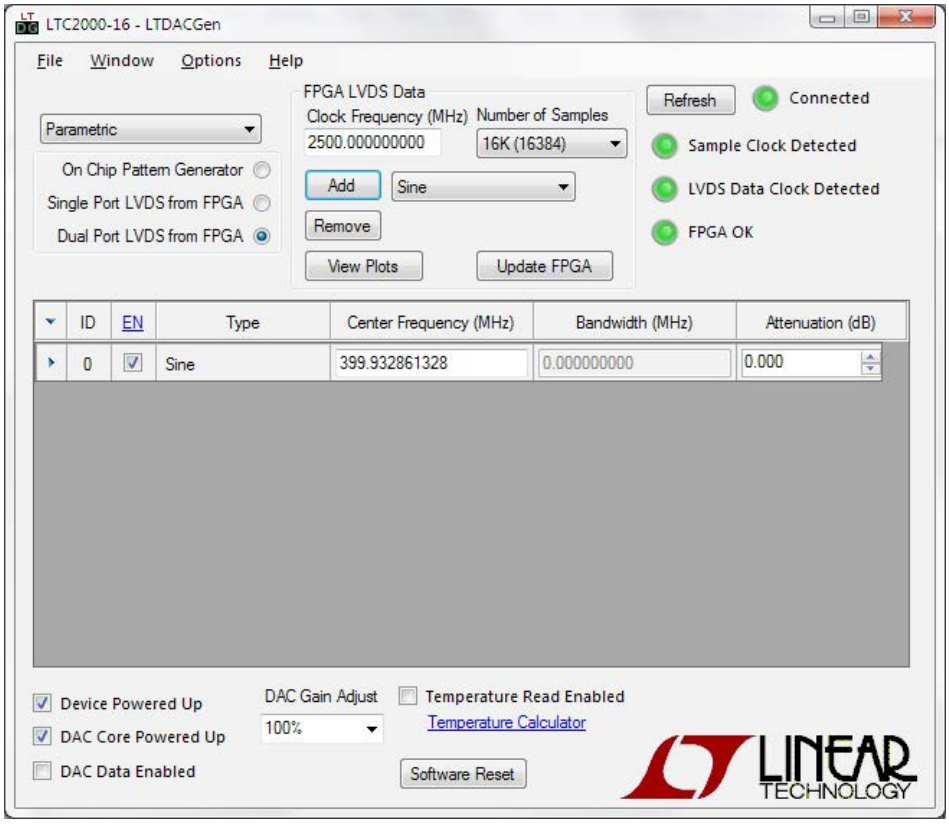

Figure 3. Default Frequency

QUICK START PROCEDURE

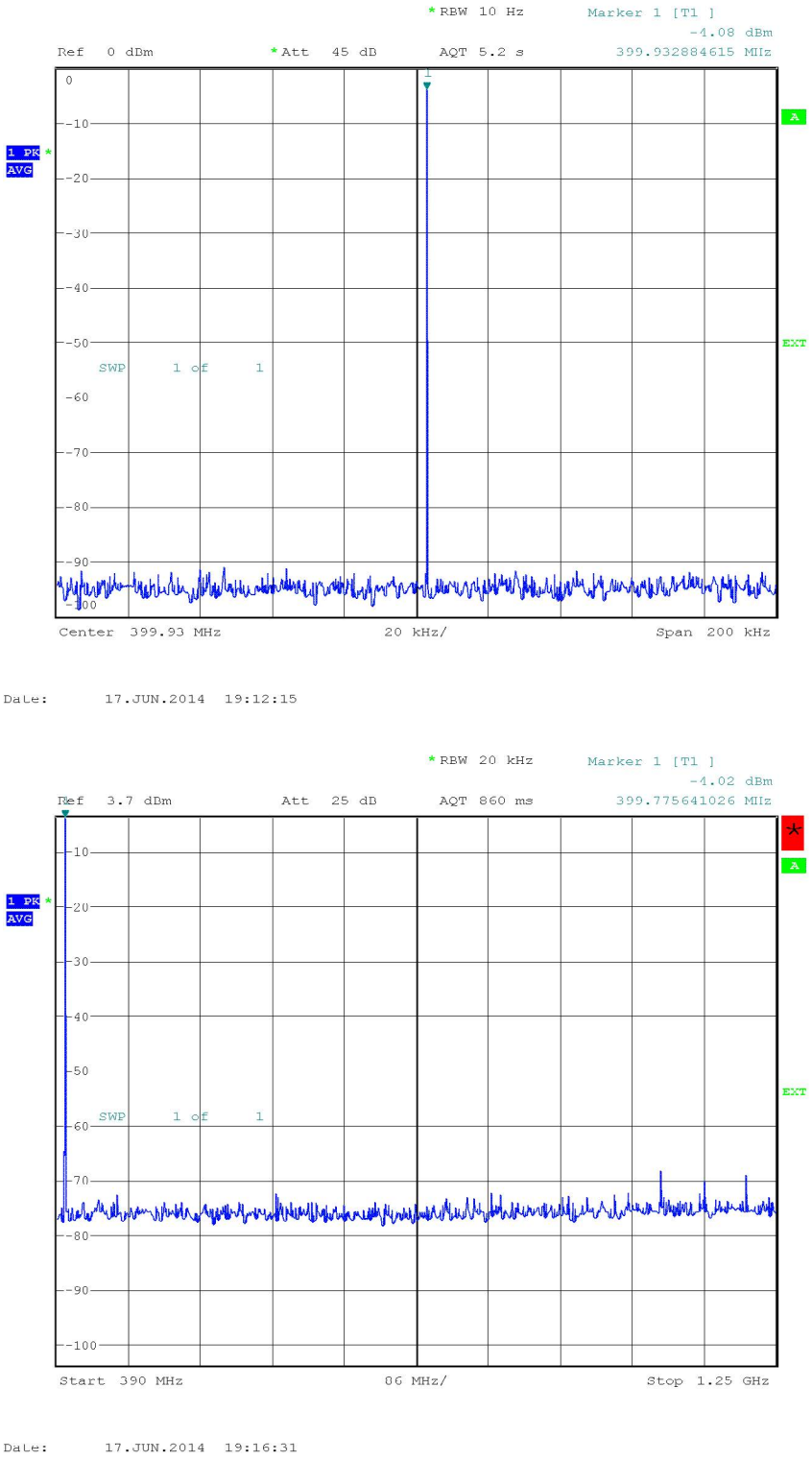

Figure 4. DC2303 Results. Close-In (Top) and Wideband (Bottom)

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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