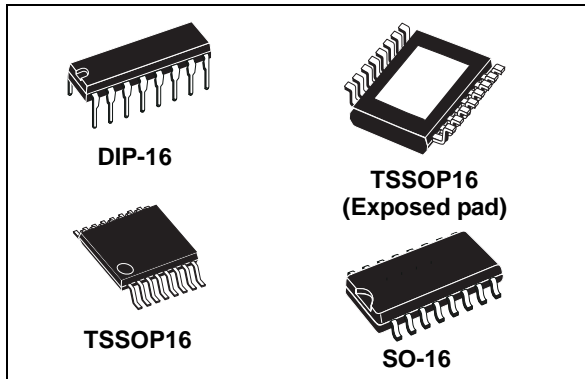


Low voltage 8-bit constant current LED sink with full outputs error detection

Datasheet - production data



serial-in, parallel-out shift register that feeds a 8-bit D-type storage register. In the output stage, eight regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs.

The STP08DP05 is backward compatible in the functionality and footprint with STP8C/L596 and extends its functionality with open and short detection on the outputs. The detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to V_O or open line. The data detection results are loaded in the shift register and shifted out via the serial line output.

The detection functionality is implemented without increasing the pin number, through a secondary function of the output enable and latch pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave from detection mode. Through an external resistor, users can adjust the STP08DP05 output current, controlling in this way the light intensity of LEDs, in addition, user can adjust LED's brightness intensity from 0% to 100% via $\overline{OE}/DM2$ pin.

The STP08DP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is well useful for applications that interface any micro from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Features

- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM, 200 V MM

Description

The STP08DP05 is a monolithic, low voltage, low current power 8-bit shift register designed for LED panel displays. The STP08DP05 contains a 8-bit

Table 1. Device summary

| Order codes | Package | Packaging |
|---------------|-------------------------------------|---------------------|
| STP08DP05B1R | DIP-16 | 25 parts per tube |
| STP08DP05MTR | SO-16 (Tape and reel) | 2500 parts per reel |
| STP08DP05TTR | TSSOP16 (Tape and reel) | 2500 parts per reel |
| STP08DP05XTTR | TSSOP16 exposed-pad (Tape and reel) | 2500 parts per reel |

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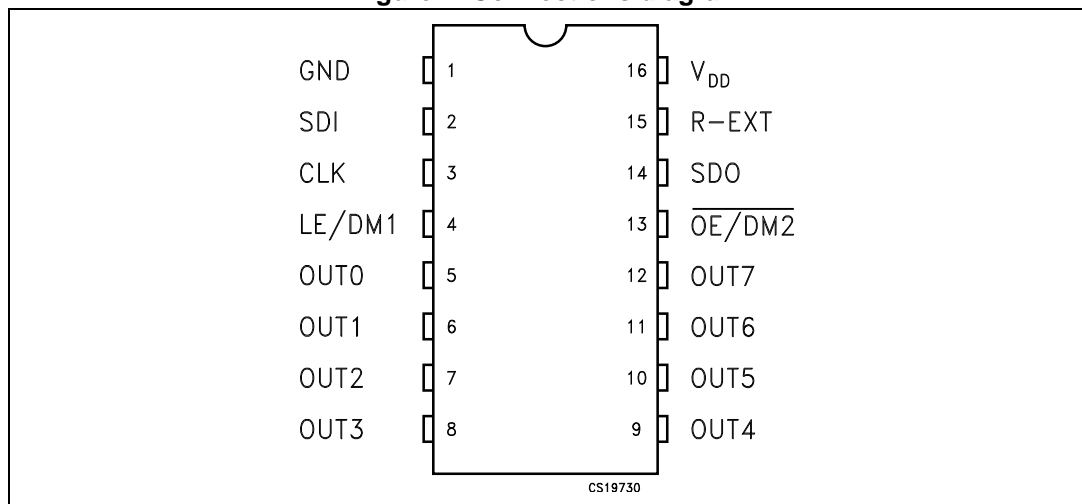
1 Summary description

Table 2. Typical current accuracy

| Output voltage | Current accuracy | | Output current |
|----------------|------------------|-------------|----------------|
| | Between bits | Between ICs | |
| ≥1.3 V | ±1.5% | ±5% | 20 to 100 mA |

1.1 Pin connection and description

Figure 1. Connections diagram



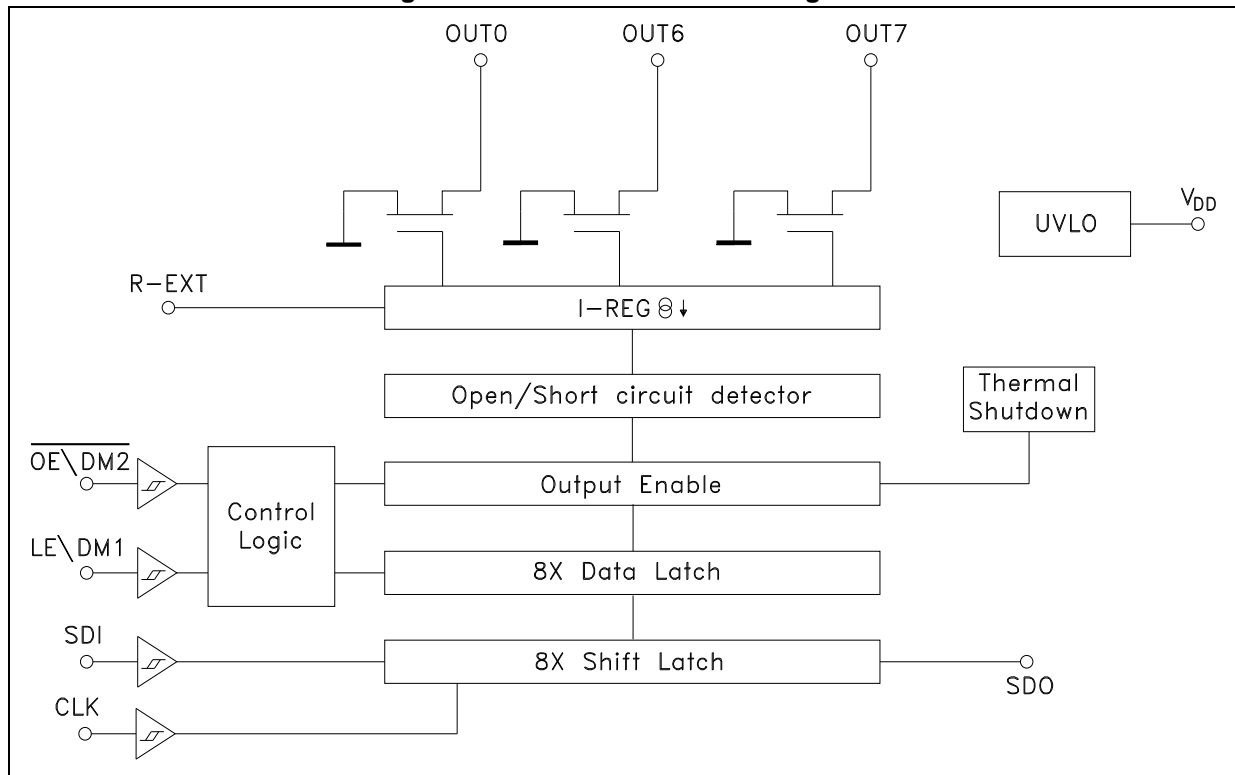
Note: The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3. Pin description

| Pin n° | Symbol | Name and function |
|--------|----------------------------|---|
| 1 | GND | Ground terminal |
| 2 | SDI | Serial data input terminal |
| 3 | CLK | Clock input terminal |
| 4 | LE/DM1 | Latch input terminal |
| 5-12 | OUT 0-7 | Output terminal |
| 13 | $\overline{\text{OE/DM2}}$ | Output enable input terminal (active low) |
| 14 | SDO | Serial data out terminal |
| 15 | R-EXT | Constant current programming |
| 16 | V _{DD} | 5 V supply voltage terminal |

2 Block diagram

Figure 2. Normal mode - block diagram



3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|-----------------------------|-------------|------|
| V_{DD} | Supply voltage I_{GND} | 0 to 7 | V |
| V_O | Output voltage | -0.5 to 20 | V |
| I_O | Output current | 100 | mA |
| I_{GND} | GND terminal current | 800 | mA |
| f_{CLK} | Clock frequency | 50 | MHz |
| T_{OPR} | Operating temperature range | -40 to +125 | °C |
| T_{STG} | Storage temperature range | -55 to +150 | °C |

3.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | DIP-16 | SO-16 | TSSOP-16 | TSSOP-16 ⁽¹⁾ (exposed pad) | Unit |
|------------|-------------------------------------|--------|-------|----------|--|------|
| R_{thJA} | Thermal resistance junction-ambient | 90 | 125 | 140 | 37.5 | °C/W |

1. The exposed-pad should be soldered to the PBC to realize the thermal benefits

3.3 Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------|----------------------------------|-------------|------|--------------|------|
| V_{DD} | Supply voltage | | 3.0 | - | 5.5 | V |
| V_O | Output voltage | | | - | 20 | V |
| I_O | Output current | OUTn | 5 | - | 100 | mA |
| I_{OH} | Output current | SERIAL-OUT | | - | +1 | mA |
| I_{OL} | Output current | SERIAL-OUT | | - | -1 | mA |
| V_{IH} | Input voltage | | $0.7V_{DD}$ | - | $V_{DD}+0.3$ | V |
| V_{IL} | Input voltage | | -0.3 | - | $0.3V_{DD}$ | V |
| t_{wLAT} | LE/DM1 pulse width | $V_{DD} = 3.0$ to $5.0V$ | 20 | - | | ns |
| t_{wCLK} | CLK pulse width | | 20 | - | | ns |
| t_{wEN} | $\overline{OE/DM2}$ pulse width | | 200 | - | | ns |
| $t_{SETUP(D)}$ | Setup time for DATA | | 7 | - | | ns |
| $t_{HOLD(D)}$ | Hold time for DATA | | 4 | - | | ns |
| $t_{SETUP(L)}$ | Setup time for LATCH | | 15 | - | | ns |
| f_{CLK} | Clock frequency | Cascade operation ⁽¹⁾ | | - | 30 | MHz |

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

4 Electrical characteristics

$V_{DD} = 3.3 \text{ V to } 5 \text{ V}$, $T = 25 \text{ }^\circ\text{C}$, unless otherwise specified.

Table 7. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|--|---|------------------------------------|-----------|--------------|------------------|
| V_{IH} | Input voltage high level | | $0.7 V_{DD}$ | | V_{DD} | V |
| V_{IL} | Input voltage low level | | GND | | $0.3 V_{DD}$ | V |
| I_{OH} | Output leakage current | $V_{OH} = 20 \text{ V}$ | | 0.5 | 10 | μA |
| V_{OL} | Output voltage (Serial-OUT) | $I_{OL} = 1 \text{ mA}$ | | 0.03 | 0.4 | V |
| V_{OH} | Output voltage (Serial-OUT) | $I_{OH} = -1 \text{ mA}$ | $V_{OH} - V_{DD} = -0.4 \text{ V}$ | | | V |
| I_{OL1} | Output current | $V_O = 0.3 \text{ V}$, $R_{ext} = 3.9 \text{ k}\Omega$ | 4.25 | 5 | 5.75 | mA |
| I_{OL2} | | $V_O = 0.3 \text{ V}$, $R_{ext} = 970 \Omega$ | 19 | 20 | 21 | |
| I_{OL3} | | $V_O = 1.3 \text{ V}$, $R_{ext} = 190 \Omega$ | 96 | 100 | 104 | |
| ΔI_{OL1} | Output current error between bit (All Output ON) | $V_O = 0.3 \text{ V}$, $R_{EXT} = 3.9 \text{ k}\Omega$ | | ± 5 | ± 8 | % |
| ΔI_{OL2} | | $V_O = 0.3 \text{ V}$, $R_{EXT} = 970 \Omega$ | | ± 1.5 | ± 3 | |
| ΔI_{OL3} | | $V_O = 1.3 \text{ V}$, $R_{EXT} = 190 \Omega$ | | ± 1.2 | ± 3 | |
| $R_{SIN(up)}$ | Pull-up resistor | | 150 | 300 | 600 | $\text{k}\Omega$ |
| $R_{SIN(down)}$ | Pull-down resistor | | 100 | 200 | 400 | $\text{k}\Omega$ |
| $I_{DD(OFF1)}$ | Supply current (OFF) | $R_{EXT} = 980$ OUT 0 to 7 = OFF | | 4 | 5 | mA |
| $I_{DD(OFF2)}$ | | $R_{EXT} = 250$ OUT 0 to 7 = OFF | | 11.2 | 13.5 | |
| $I_{DD(ON1)}$ | Supply current (ON) | $R_{EXT} = 980$ OUT 0 to 7 = ON | | 4.5 | 5 | |
| $I_{DD(ON2)}$ | | $R_{EXT} = 250$ OUT 0 to 7 = ON | | 11.7 | 13.5 | |
| Thermal | Thermal protection ⁽¹⁾ | | | 170 | | $^\circ\text{C}$ |

1. Guaranteed by design (not tested)
The thermal protection switches OFF only the outputs current

5 Switching characteristics

$V_{DD} = 5\text{ V}$, $T = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Table 8. Switching characteristics

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit | |
|------------|--|--|---|-------------------------|------|------|------|----|
| t_{PLH1} | Propagation delay time, CLK-OUTn, LE\DM1 = H, OE\DM2 = L | $V_{DD} = 3.3\text{ V}$ $V_{IL} = \text{GND}$ $I_O = 20\text{ mA}$ $R_{EXT} = 1\text{ K}\Omega$ | $V_{IH} = V_{DD}$ $C_L = 10\text{ pF}$ $V_L = 3.0\text{ V}$ $R_L = 60\text{ }\Omega$ | $V_{DD} = 3.3\text{ V}$ | | 36 | 46.8 | ns |
| | | | | $V_{DD} = 5\text{ V}$ | | 19 | 24.7 | |
| t_{PLH2} | Propagation delay time, LE\DM1 -OUTn, OE\DM2 = L | | | $V_{DD} = 3.3\text{ V}$ | | 38 | 49.4 | ns |
| | | | | $V_{DD} = 5\text{ V}$ | | 21 | 27.3 | |
| t_{PLH3} | Propagation delay time, OE\DM2-OUTn, LE\DM1 = H | | | $V_{DD} = 3.3\text{ V}$ | | 42 | 54 | ns |
| | | | | $V_{DD} = 5\text{ V}$ | | 23 | 30 | |
| t_{PLH} | Propagation delay time, CLK-SDO | | | $V_{DD} = 3.3\text{ V}$ | | 22 | 28.6 | ns |
| | | | | $V_{DD} = 5\text{ V}$ | | 18 | 23.4 | |
| t_{PHL1} | Propagation delay time, CLK-OUTn, LE\DM1 = H, OE\DM2 = L | | | $V_{DD} = 3.3\text{ V}$ | | 9 | 11.7 | ns |
| | | | | $V_{DD} = 5\text{ V}$ | | 5 | 6.5 | |
| t_{PHL2} | Propagation delay time, LE\DM1 -OUTn, OE\DM2 = L | $V_{DD} = 3.3\text{ V}$ | | 4 | 5.2 | ns | | |
| | | $V_{DD} = 5\text{ V}$ | | 3 | 3.9 | | | |
| t_{PHL3} | Propagation delay time, OE\DM2-OUTn, LE\DM1 = H | $V_{DD} = 3.3\text{ V}$ | | 6 | 7.8 | ns | | |
| | | $V_{DD} = 5\text{ V}$ | | 3 | 3.9 | | | |
| t_{PHL} | Propagation delay time, CLK-SDO | $V_{DD} = 3.3\text{ V}$ | | 25 | 32.5 | ns | | |
| | | $V_{DD} = 5\text{ V}$ | | 20 | 26 | | | |
| t_{ON} | Output rise time 10~90% of voltage waveform | $V_{DD} = 3.3\text{ V}$ | | 30 | 39 | ns | | |
| | | $V_{DD} = 5\text{ V}$ | | 15 | 19.5 | | | |
| t_{OFF} | Output fall time 90~10% of voltage waveform | $V_{DD} = 3.3\text{ V}$ | | 7 | 9.1 | ns | | |
| | | $V_{DD} = 5\text{ V}$ | | 6 | 7.8 | | | |
| t_r | CLK rise time ⁽¹⁾ | | | | | 5000 | ns | |
| t_f | CLK fall time ⁽¹⁾ | | | | | 5000 | ns | |

1. In order to achieve high cascade data transfer, please consider tr/ff timings carefully.

6 Equivalent circuit and outputs

Figure 3. OE/DM2 terminal

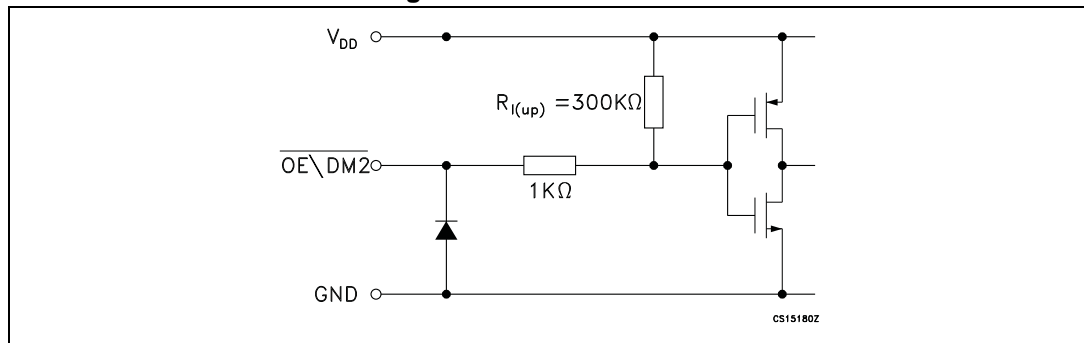


Figure 4. LE/DM1 terminal

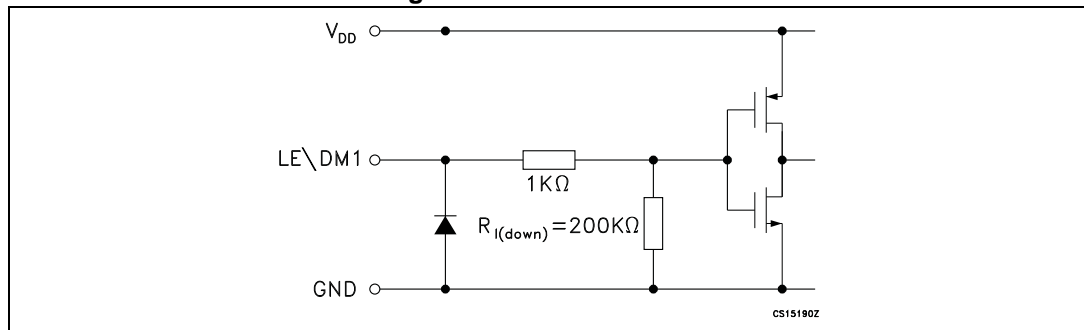


Figure 5. CLK, SDI terminal

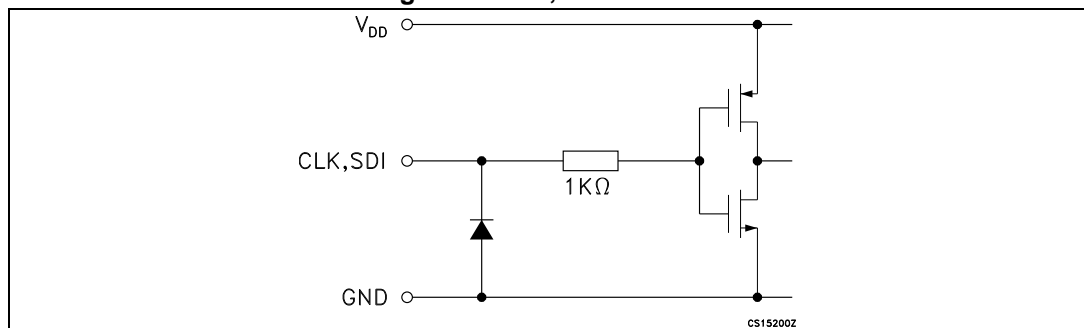
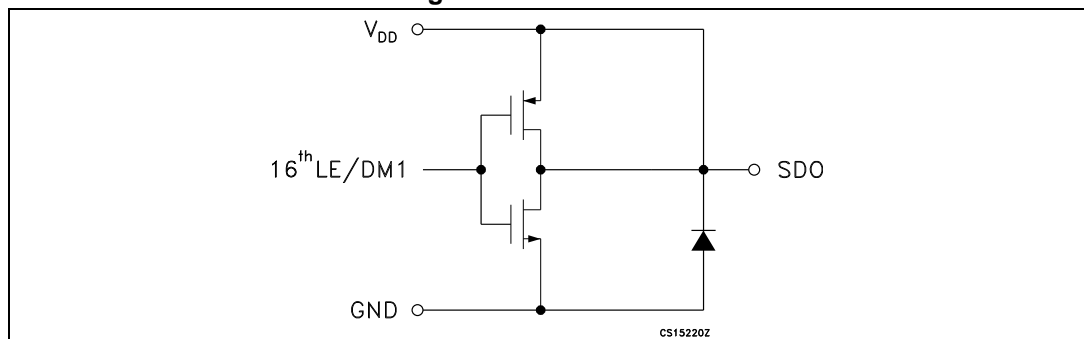


Figure 6. SDO terminal



7 Truth table and timing diagram

7.1 Truth table

Table 9. Truth table

| Clock | $\overline{\text{LE}}/\text{DM1}$ | $\overline{\text{OE}}/\text{DM2}$ | SDI | $\overline{\text{OUT0}}$ $\overline{\text{OUT0}}$ $\overline{\text{OUT7}}$ | SDO |
|-------|-----------------------------------|-----------------------------------|--------|---|-------|
| | H | L | Dn | Dn Dn -5 Dn -7 | Dn -7 |
| | L | L | Dn + 1 | No change | Dn -7 |
| | H | L | Dn + 2 | $\overline{\text{Dn}} +2$ $\overline{\text{Dn}} -3$ $\overline{\text{Dn}} -5$ | Dn -5 |
| | X | L | Dn + 3 | $\overline{\text{Dn}} +2$ $\overline{\text{Dn}} -3$ $\overline{\text{Dn}} -5$ | Dn -5 |
| | X | H | Dn + 3 | OFF | Dn -5 |

Note: OUT0 to $\text{OUT7} = \text{ON}$ when $Dn = H$; OUT0 to $\text{OUT7} = \text{OFF}$ when $Dn = L$.

7.2 Timing diagram

Figure 7. Timing diagram - normal mode

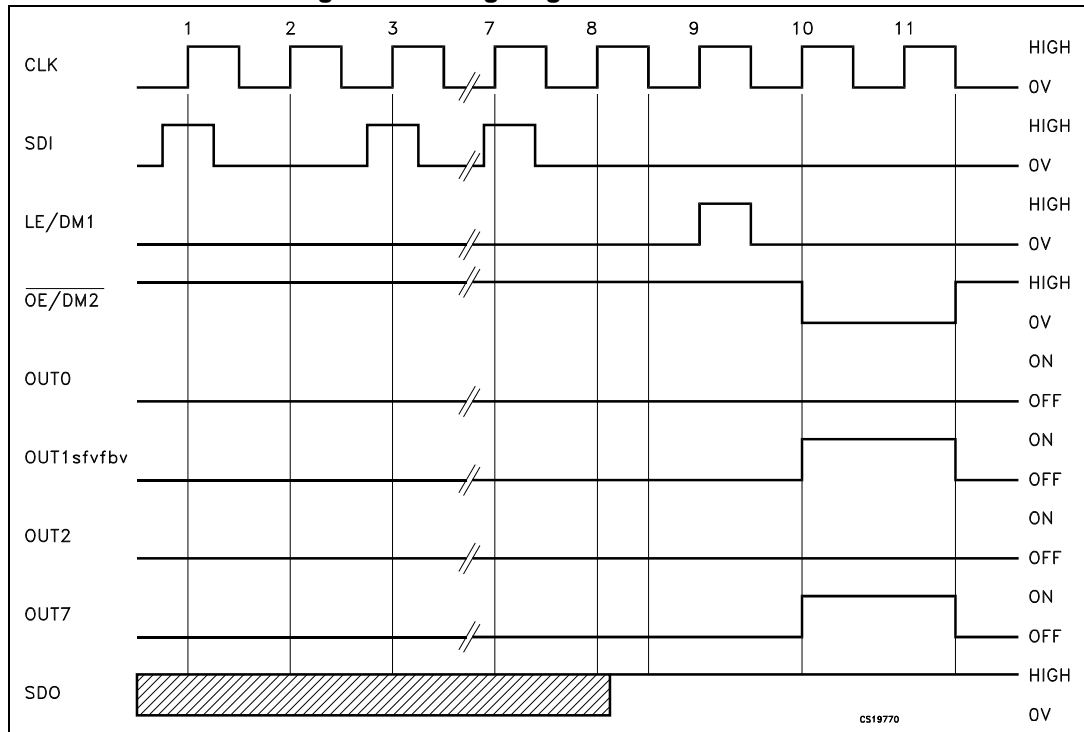


Figure 8. Clock, serial-in, serial-out

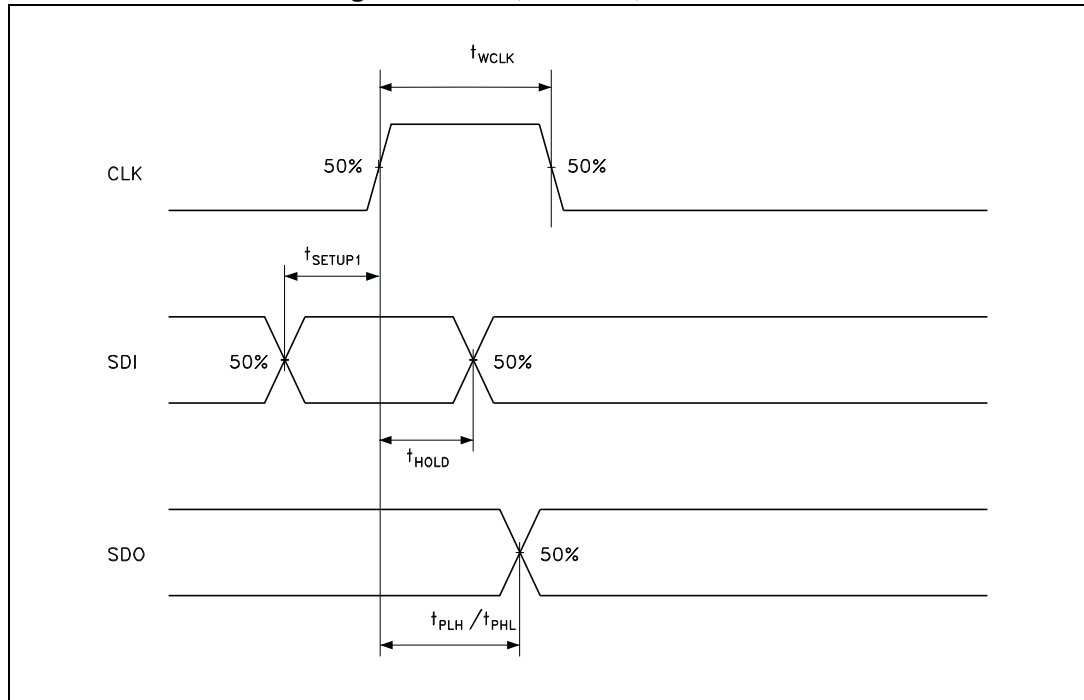


Figure 9. Clock, serial-in, latch, enable, outputs

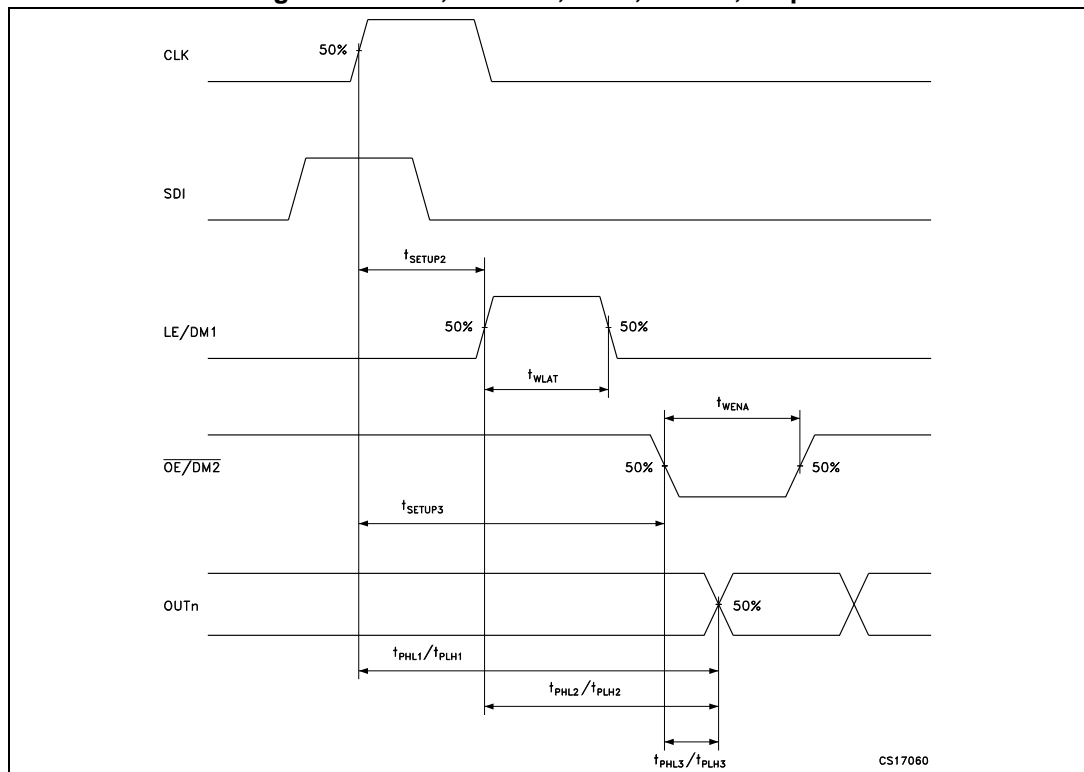
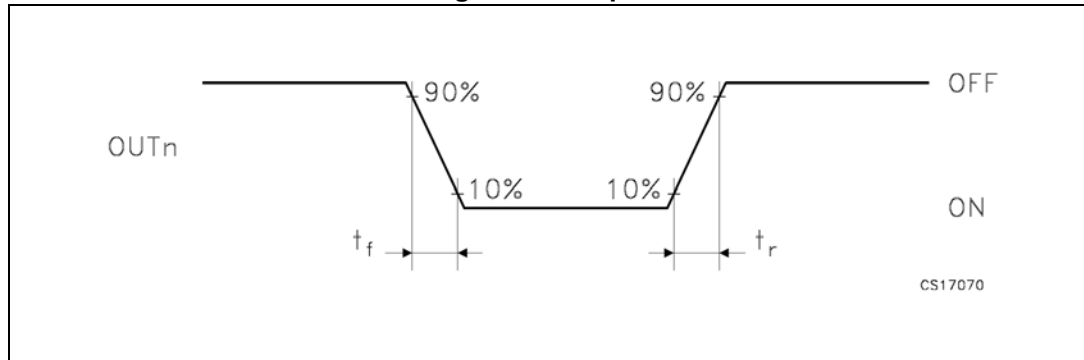


Figure 10. Outputs



8 Typical characteristics

Figure 11. Output current- R_{EXT} resistor

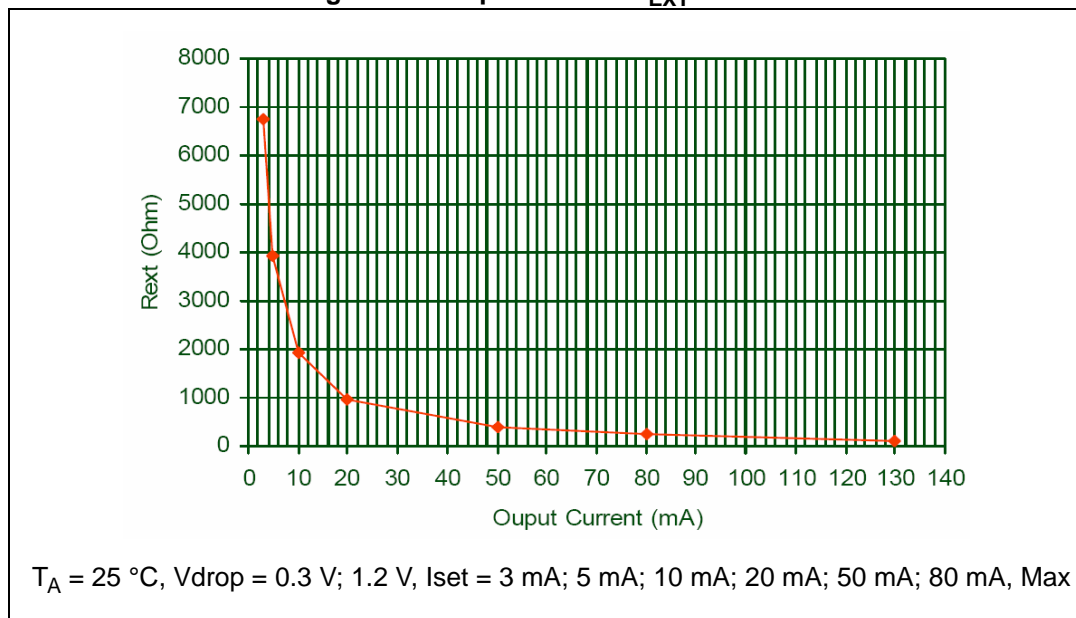


Table 10. Output current- R_{EXT} resistor

| Output current (mA) | 3 | 5 | 10 | 20 | 50 | 80 | 130 |
|---------------------|------|------|------|-----|-----|-----|-----|
| Rext (Ω) | 6740 | 3930 | 1913 | 963 | 386 | 241 | 124 |

Note: Maximum output current capabilities setting was 130 mA applying a $R_{ext} = 124\ \Omega$

Figure 12. I_{SET} vs drop out voltage (V_{DROP})

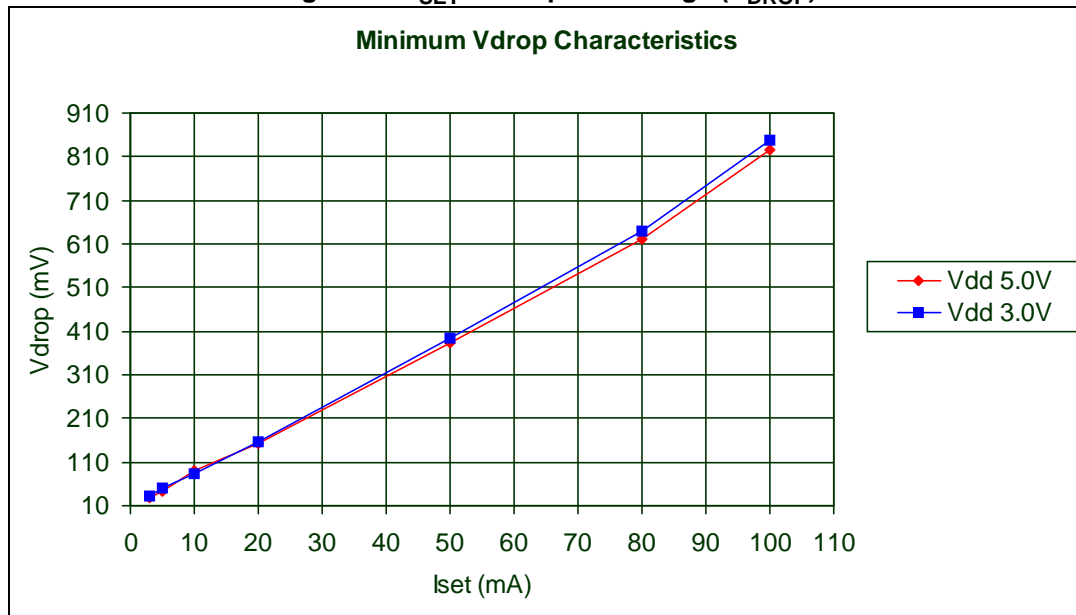
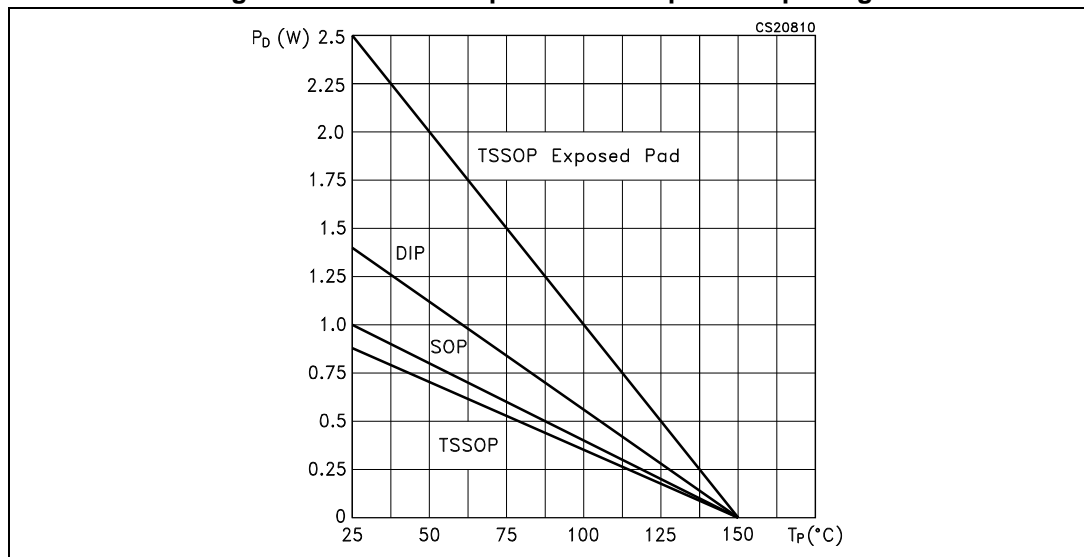


Table 11. I_{SET} vs. drop out voltage (V_{DROP})

| Vdd (V) | I set (mA) | Rext (Ω) | Vdrop min (mV) | Vdrop max (mV) | Vdrop AVG (mV) |
|---------|------------|----------|----------------|----------------|----------------|
| 3 | 3 | 6470 | 30.6 | 31.2 | 30.93 |
| | 5 | 3930 | 46.5 | 52.9 | 48.63 |
| | 10 | 1910 | 80.9 | 100 | 82.26 |
| | 20 | 963 | 150 | 161 | 157 |
| | 50 | 386 | 392 | 396 | 394.3 |
| | 80 | 241 | 636 | 646 | 640.3 |
| | 100 | 192 | 846 | 850 | 848 |
| 5 | 3 | 6470 | 25.6 | 29 | 26.96 |
| | 5 | 3930 | 40.8 | 41.7 | 41.16 |
| | 10 | 1910 | 80.1 | 105 | 89.2 |
| | 20 | 963 | 153 | 154 | 154 |
| | 50 | 386 | 379 | 386 | 382 |
| | 80 | 241 | 618 | 626 | 621 |
| | 100 | 192 | 825 | 830 | 827 |

Figure 13. Power dissipation vs. temperature package



Note: The exposed-pad should be soldered to the PBC to realize the thermal benefits.

9 Test circuit

Figure 14. DC characteristics

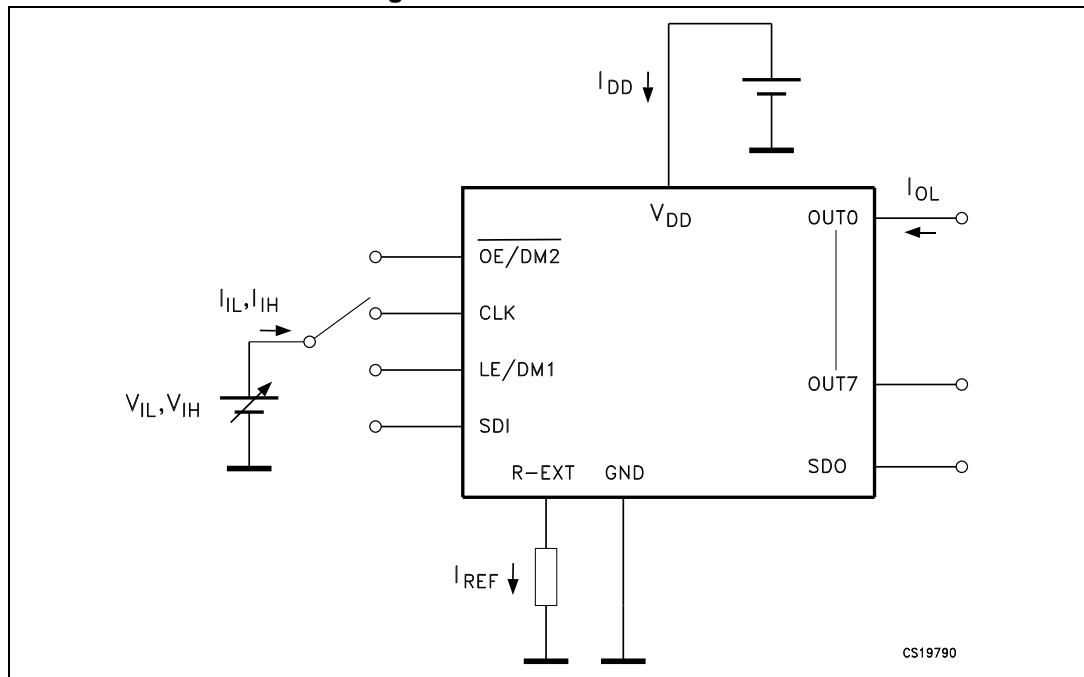


Figure 15. AC characteristics

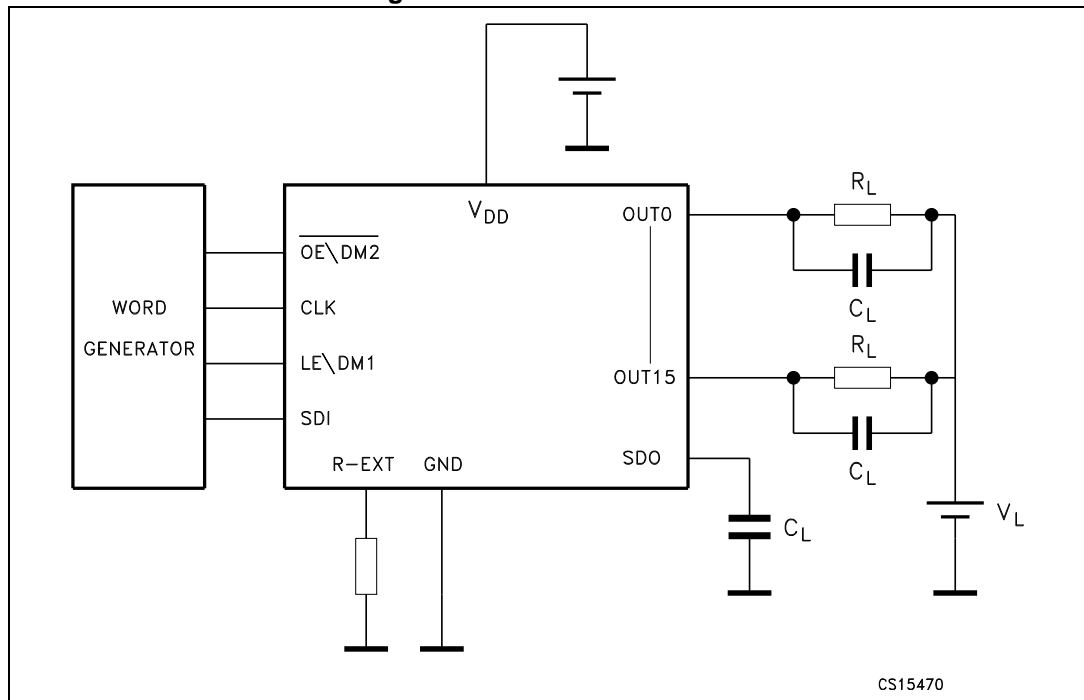
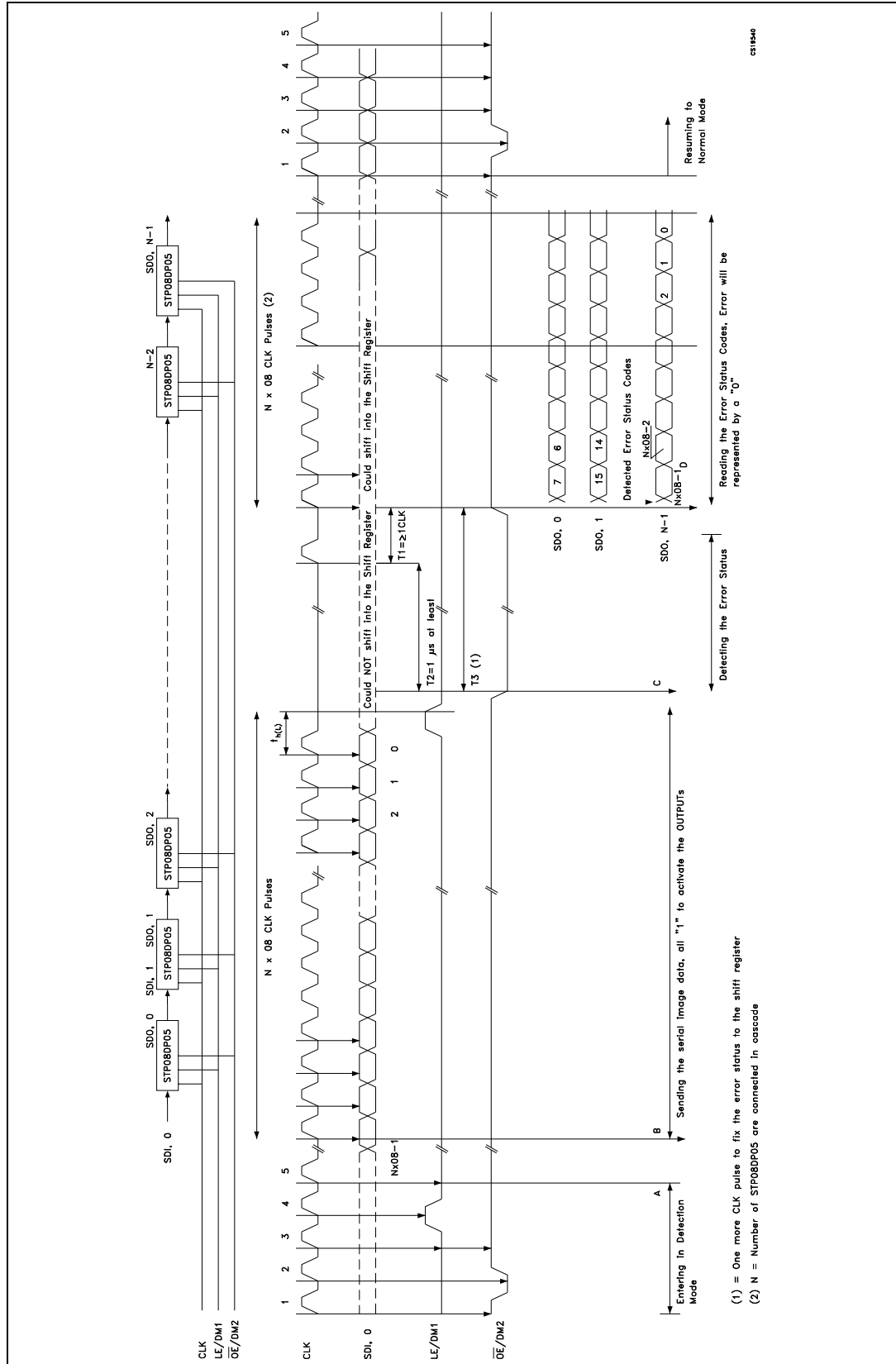


Figure 16. Timing example for open and/or short detection



10 Detection mode functionality

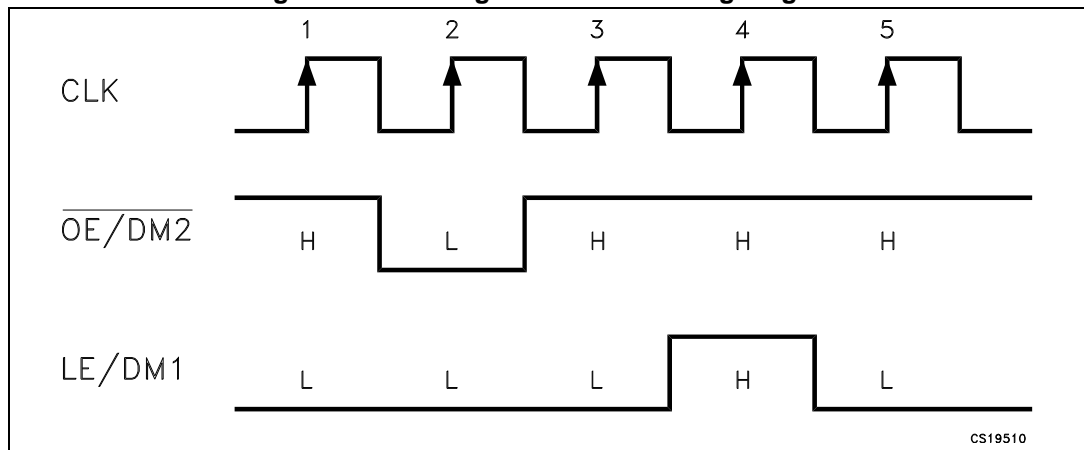
10.1 Phase one: “entering in detection mode“

From the “normal mode” condition the device can switch to the “error mode” by a logic sequence on the $\overline{\text{OE/DM2}}$ and LE/DM1 pins as showed in the following table and diagram:

Table 12. Entering in detection truth table

| CLK | 1° | 2° | 3° | 4° | 5° |
|----------------------------|----|----|----|----|----|
| $\overline{\text{OE/DM2}}$ | H | L | H | H | H |
| LE/DM1 | L | L | L | H | L |

Figure 17. Entering in detection timing diagram

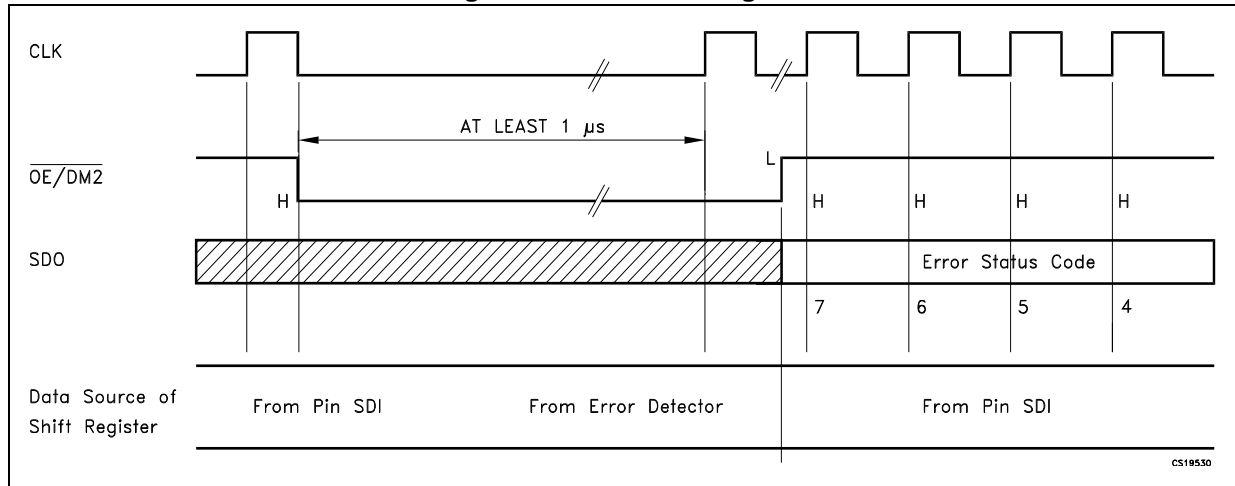


After these five CLK cycles the device goes into the “error detection mode” and at the 6th rise front of CLK the SDI data are ready for the sampling.

10.2 Phase two: “error detection“

The eight data bits must be set “1” in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the micro controller switches the $\overline{\text{OE/DM2}}$ to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

Figure 18. Detection diagram



The LEDs status will be detected at least in 1 microsecond and after this time the microcontroller sets $\overline{OE/DM2}$ in HIGH state and the output data detection result will go to the microprocessor via SDO.

Detection mode and normal mode use both the same format data. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status the device must go back in normal mode and re-entering in error detection mode.

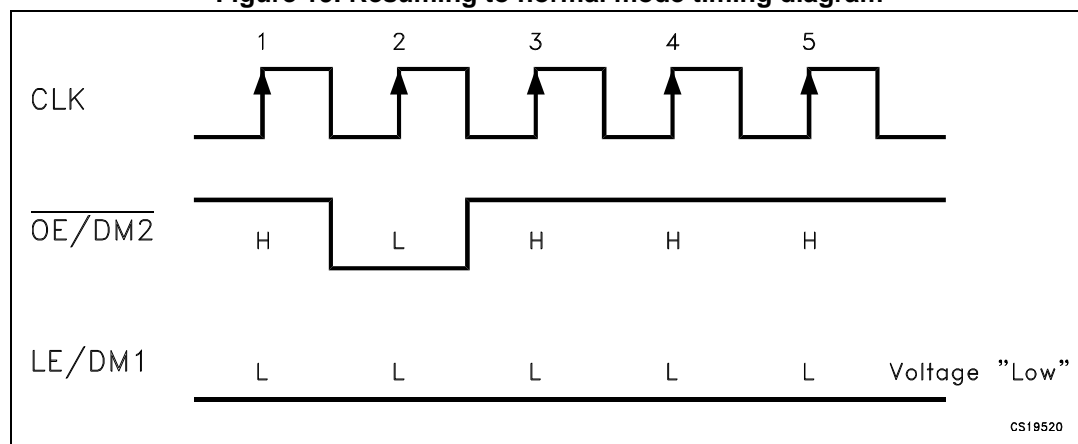
10.3 Phase three: “resuming to normal mode”

The sequence for re-entering in normal mode is showed in the following table and diagram:

Table 13. Resuming to normal mode timing diagram

| CLK | 1° | 2° | 3° | 4° | 5° |
|----------------------------|----|----|----|----|----|
| $\overline{\text{OE/DM2}}$ | H | L | H | H | H |
| $\overline{\text{LE/DM1}}$ | L | L | L | L | L |

Figure 19. Resuming to normal mode timing diagram



Note: For proper device operation the “entering in detection” sequence must follow by a “resume mode” sequence, isn’t possible to insert consecutive equal sequence.

10.4 Error detection conditions

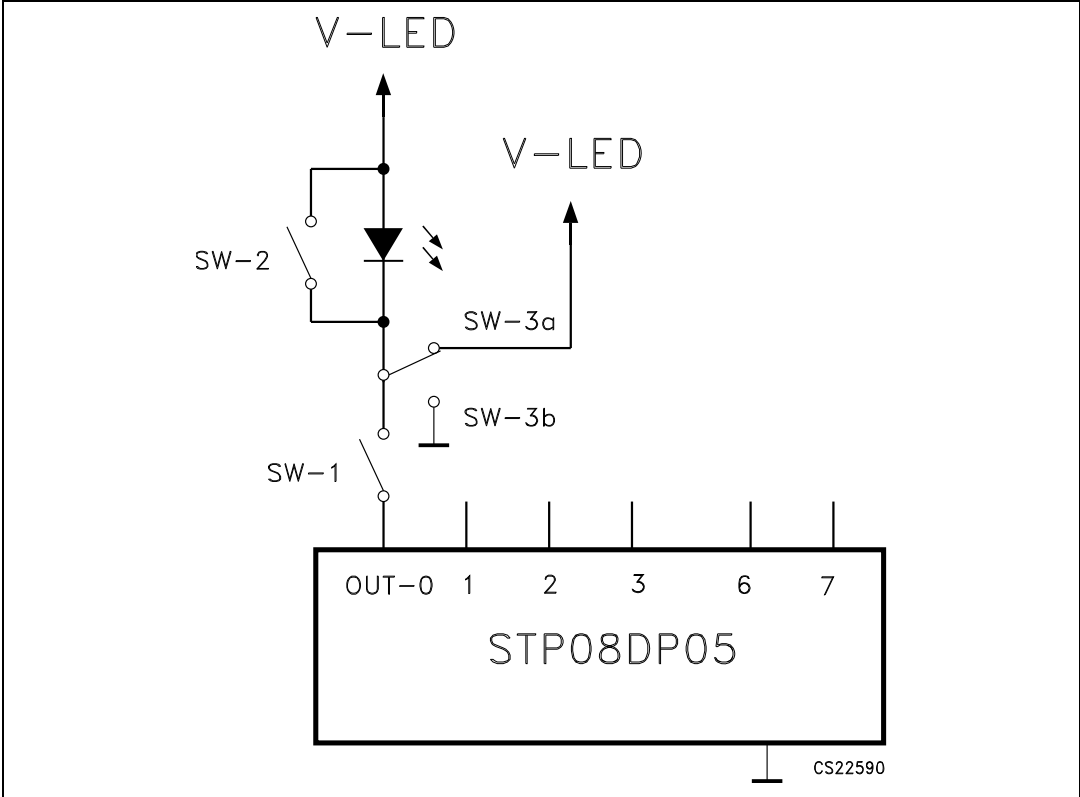
$V_{DD} = 3.3$ to 5 V temperature range 25 °C.

Table 14. Detection condition

| | | | | |
|----------------------|---|---|-------------------|---|
| SW-1 or SW-3b | Open line or output short to GND detected | $\implies I_{ODEC} \leq 0.5 \times I_O$ | No error detected | $\implies I_{ODEC} \geq 0.5 \times I_O$ |
| SW-2 or SW-3a | Short on LED or short to V-LED detected | $\implies V_O \geq 2.5V$ | No error detected | $\implies V_O \leq 2.2 V$ |

Note: Where: I_O = the output current programmed by the R_{EXT} ,
 I_{ODEC} = the detected output current in detection mode.

Figure 20. Detection circuit



11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 15. DIP16 mechanical data

| Dim. | mm | | |
|------|------|-------|------|
| | Min. | Typ. | Max. |
| a1 | 0.51 | | |
| B | 0.77 | | 1.65 |
| b | | 0.5 | |
| b1 | | 0.25 | |
| D | | | 20 |
| E | | 8.5 | |
| e | | 2.54 | |
| e3 | | 17.78 | |
| F | | | 7.1 |
| I | | | 5.1 |
| L | | 3.3 | |
| Z | | | 1.27 |

Figure 21. DIP16 drawing

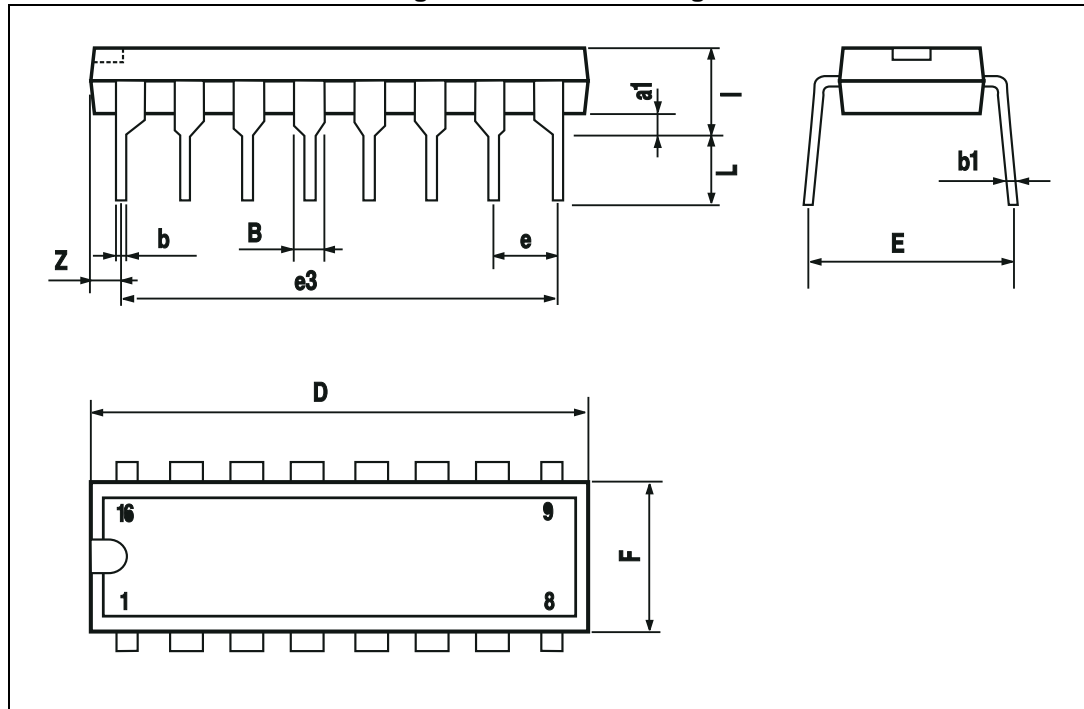


Table 16. HTSSOP16 exposed pad mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | | 3.00 | |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | | 3.00 | |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0.00 | | 8.00 |
| aaa | | | 0.10 |

Figure 22. HTSSOP16 exposed pad drawing

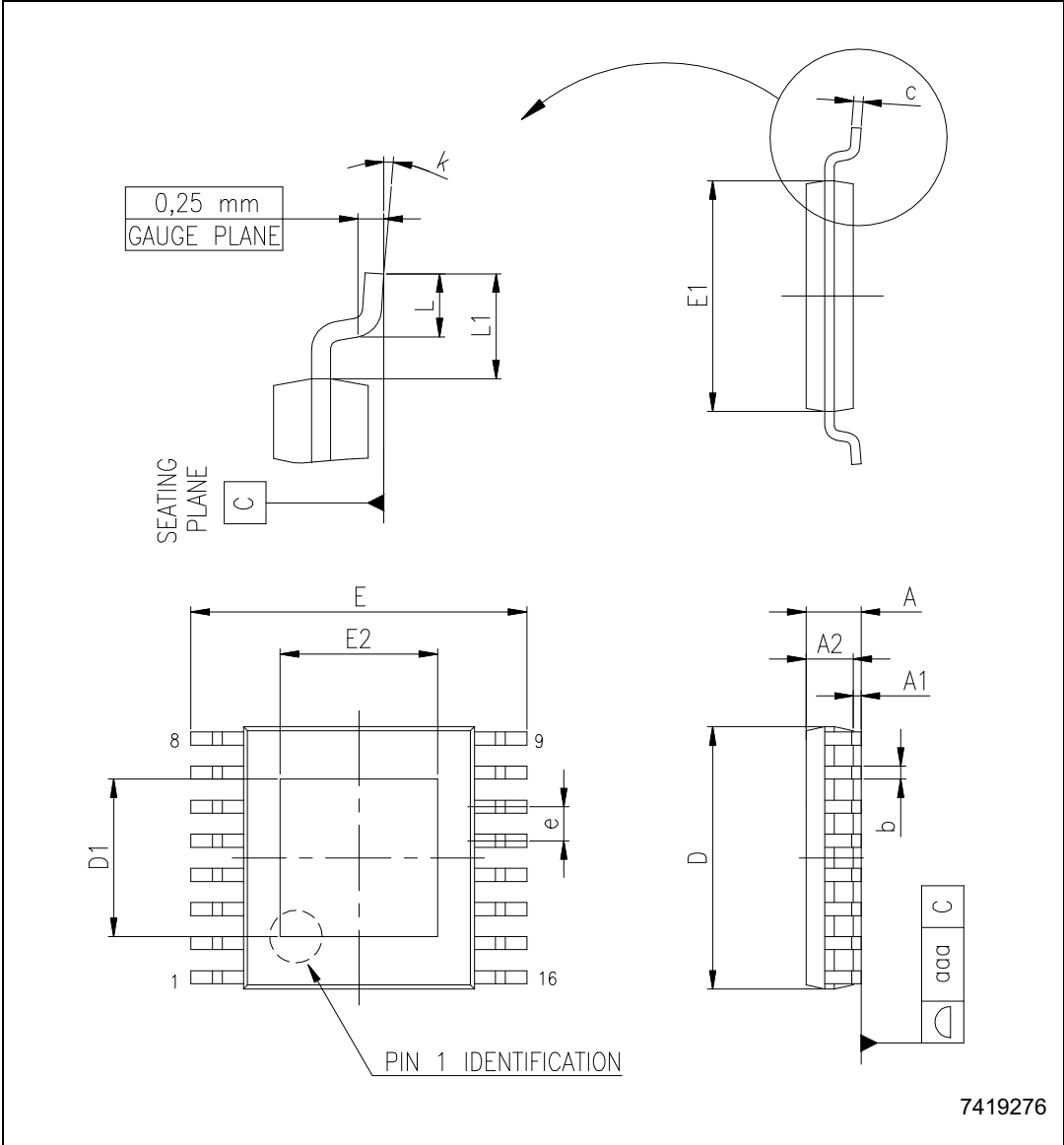


Table 17. TSSOP16 mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0 | | 8 |
| aaa | | | 0.10 |

Figure 23. TSSOP16 mechanical drawing

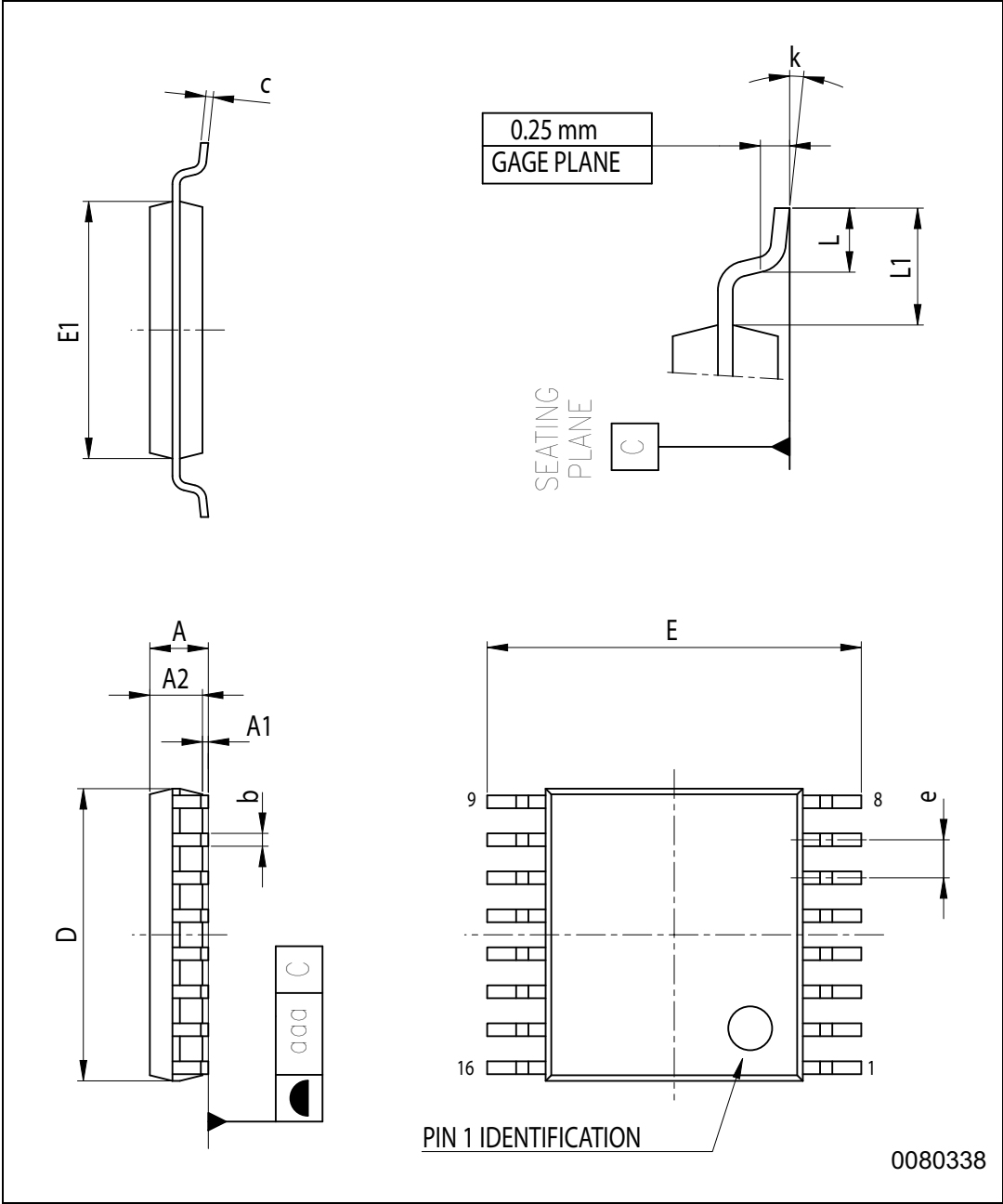
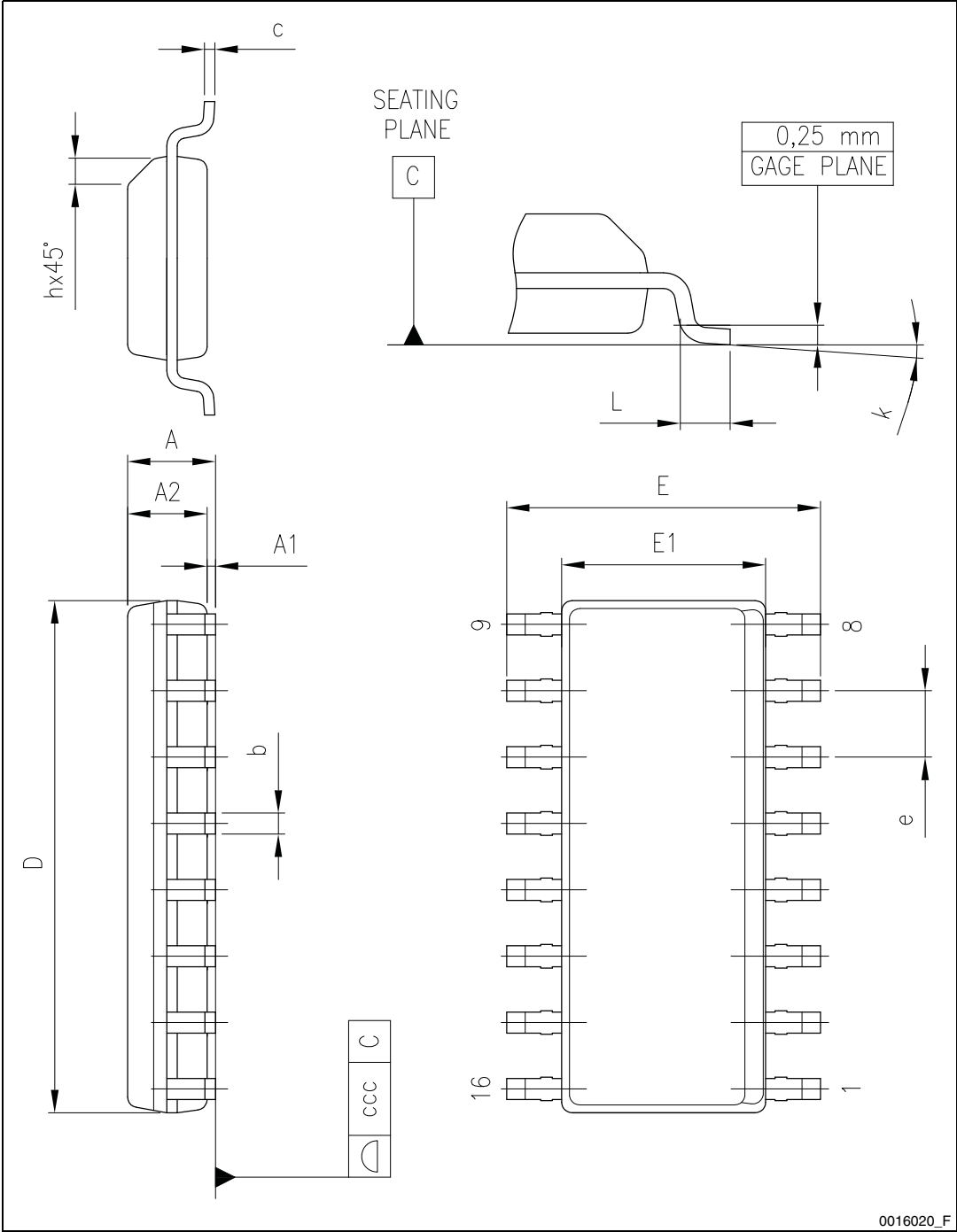


Table 18. SO16 dimensions

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| k | 0 | | 8° |
| ccc | | | 0.10 |

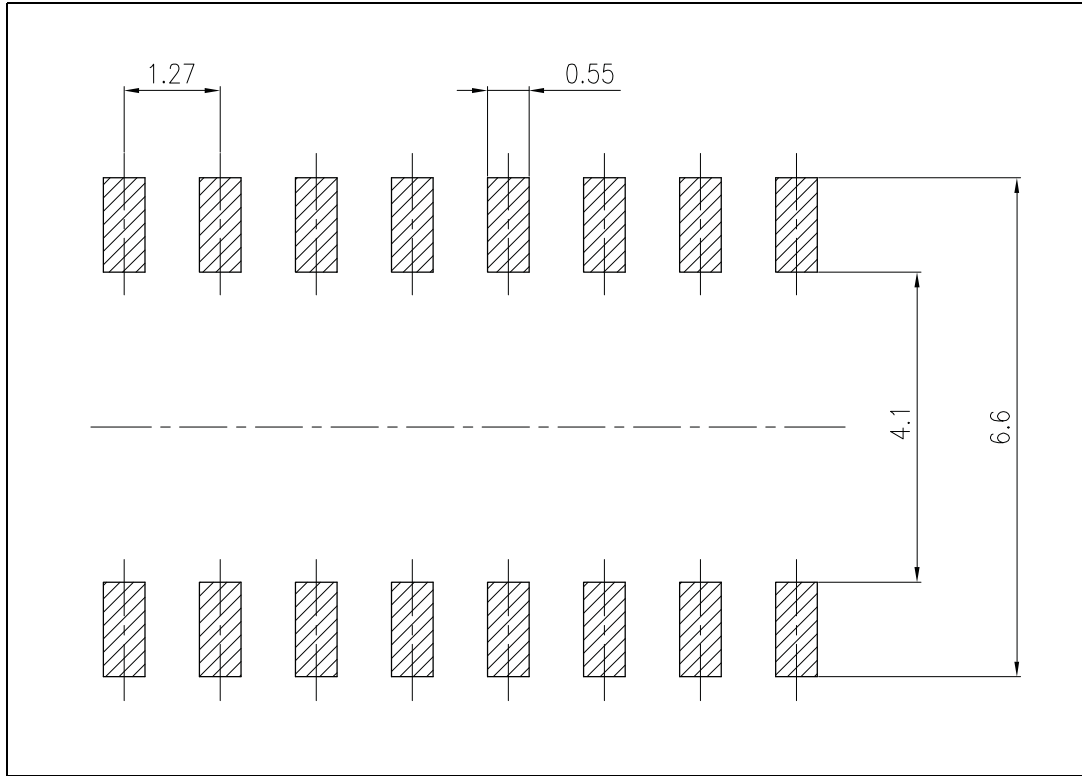
Figure 24. Package drawing



0016020_F



Figure 25. Recommended footprint (dimensions are in mm)

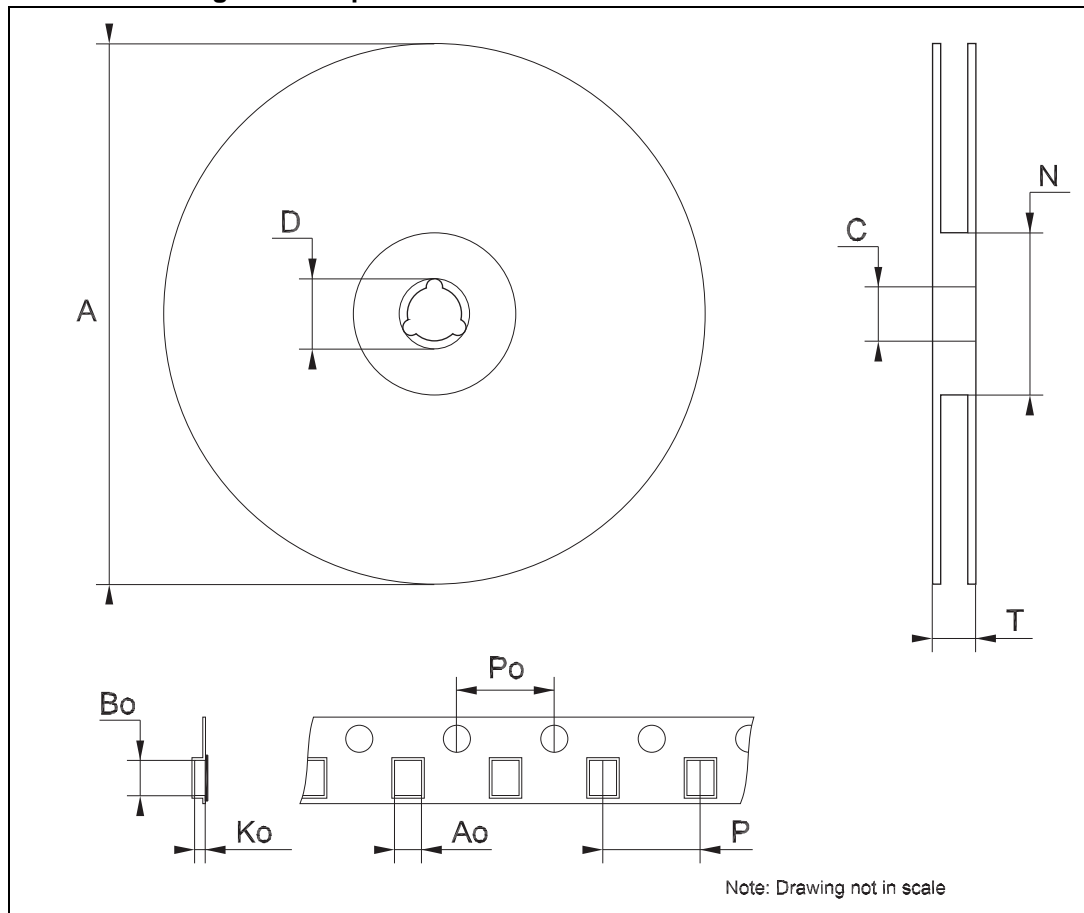


12 Packaging mechanical data

Table 19. HTSSOP16 EP and TSSOP16 tape and reel mechanical data

| Dim. | (mm) | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 6.7 | | 6.9 |
| Bo | 5.3 | | 5.5 |
| Ko | 1.6 | | 1.8 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

Figure 26. Tape and reel for HTSSOP16 EP and TSSOP16



13 Revision history

Table 20. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 3-Apr-2007 | 1 | First release |
| 21-May-2007 | 2 | Updated Table 7 on page 8 |
| 08-Aug-2008 | 3 | Updated Section 8: Typical characteristics on page 14 added Figure 13 and Figure 11 on page 15 updated Figure 14 on page 16. |
| 22-Oct-2009 | 4 | Updated Note: on page 3. |
| 29-Jul-2013 | 5 | Updated Section 11: Package mechanical data, Figure 4: OE/DM2 terminal and Figure 5: LE/DM1 terminal. Added Section 12: Packaging mechanical data. |
| 28-Jun-2018 | 6 | Updated Table 16: HTSSOP16 exposed pad mechanical data and Figure 22: HTSSOP16 exposed pad drawing . |

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