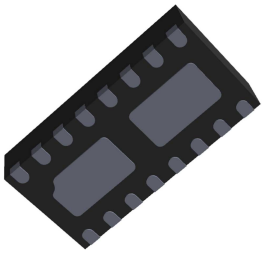
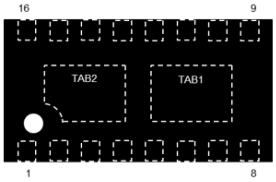
CLT03-2Q3

Datasheet

Self powered digital input current limiter



QFN 2X4-16L



Product status link
CLT03-2Q3

Product summary	
Order code	CLT03-2Q3
Package	QFN 2X4-16L
Packing	Tape and reel

Features

- 2 isolated channels device
- No power supply needed
- Digital input current limitation
- Deglitch filter for EMC robustness
- High side / Low side compatible
- Inputs are reverse plugin compatible
- Direct opto-coupler or 3.3 V LVTTL output
- Operating ambient temperature range from – 30 °C to 125 °C
- QFN 2 x 4 – 16L - 500 µm pitch
- Exceeds IEC 61000-4-2 level 1 standard:
  - ±4 kV (air discharge)
  - ±2 kV (contact discharge)
- IEC61131-2 type 1 and 3
- IEC 61508

Applications

Where current limitation is required in factory automation applications:

- Programmable logic controller
- Remote input module

Description

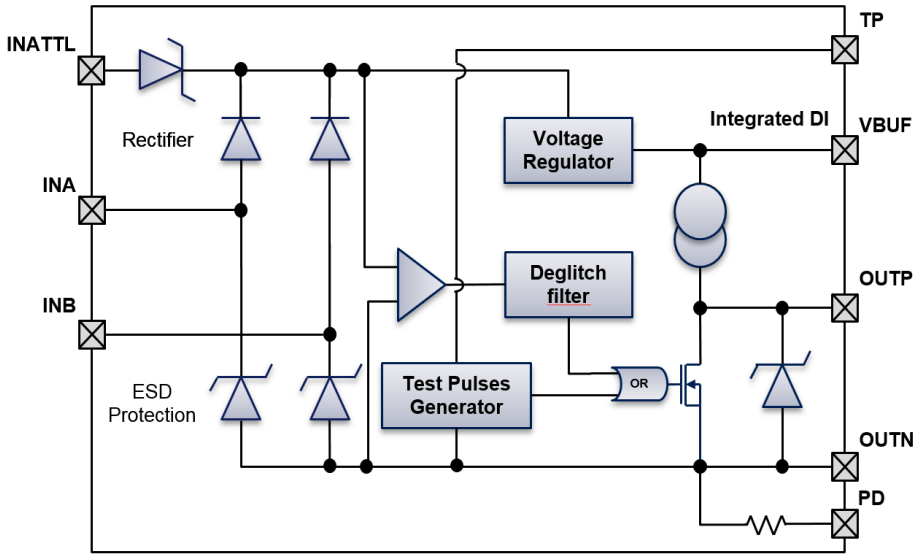
The CLT03-2Q3 is a digital input current limiter which does not require external power supply.

The product is housed in a QFN 2 x 4 -16L and is high side and low side compatible, as well as reverse plugin compatible.

The CLT03-2Q3 can drive either opto-coupler or 3.3 V LVTTL circuit.

1 Circuit block diagram

Figure 1. **One channel diagram**



1.1 I/O pin description

Table 1. **Pins name, type and description**

Name	Pin #	Type	Description
INA1 / INA2	7 / 3	Signal input	Logic input with current limitation
INATTL1 / INATTL2	6 / 2	Signal input	Logic input with current limitation for non-isolated configuration
INB1 / INB2	8 / 4	Signal input	Logic input with current limitation
TP1 / TP2	9 / 14	Test input	Test pulse input for capacitor
VBUF1 / VBUF2	10 / 15	Power output	Buffer capacitor
OUTN1	5 / TAB1	Ground	Logic output ground (channel 1 output ground)
OUTN2	13 / TAB2	Ground	Logic output ground (channel 2 output ground)
OUTP1 / OUTP2	11 / 16	Signal output	Data output
PD1/PD2	12 / 1	Ground	Logic output ground with pull down resistor (non-isolated mode)

Figure 2. **QFN 2x4-16L pinout (top view)**

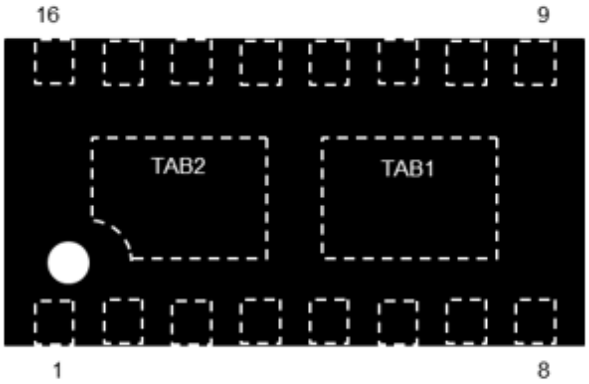


Table 2. **Thermal resistance parameter**

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Thermal resistance junction to ambient, according to EIA/ JEDEC JESD51-7 and JESD51-5	41	°C/W

2 Characteristics

2.1 Absolute ratings

Stresses outside the absolute ratings range may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

Table 3. Absolute ratings (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter name	Value	Unit
V_{PP}	Peak pulse voltage, HBM, MIL STD 883J-Method 3015.9	2	kV
V_{PP} (1)(2)	Peak pulse voltage (pins INA, INATTL & INB), IEC 61000-4-2 (contact)	2	kV
V_{IN}	Input voltage	-60 to +60	V
V_{ISO}	Isolation between channel 1 and 2	230	V_{AC}
T_j	Junction temperature	-30 to +125	°C
T_{STG}	Storage temperature	-55 to +150	°C

1. *See application schematic*
2. *Performance level depends on layout and environment*

2.2 Electrical characteristics

Table 4. Electrical characteristics (-30 °C < $T_{ambient}$ < +125 °C, unless otherwise specified) (values)

Symbol	Description	Name	Min.	Typ.	Max.	Unit
Input						
I_{LIM}	Input current – On state		2.5		4	mA
V_{TLH}	Low to High state input voltage			9.4	11	V
V_{THL}	High to Low state input voltage		5	7.5		V
V_{HYST}	Input triggering voltage hysteresis		1.2		2.6	V
V_{FAULT}	Fault mode threshold voltage		30	40		V
I_{FAULT}	Input current in fault region V_{IN} > V_{FAULT}		1		3	mA
Timing parameters						
f_{IN}	Input frequency				35	kHz
t_{FAULT}	Fault mode triggering latency after V_{IN} > V_{FAULT}			25		µs
t_{PLH}	Input to output low to high propagation time (including deglitch filter)(1)		2		5	µs
t_{PHL}	Input to output high to low propagation time (including deglitch filter) (1)		2		5	µs
Ouput						
I_{OUT}	On state	Isolated mode	2		4	mA
		Non-isolated mode			1	mA
	Off state	Isolated and non-isolated mode	-10		10	µA
V_{OUT}	On state	Isolated mode	0.7		3.6	V
		Non-isolated mode	3		3.6	V
	Off state	Isolated and non-isolated mode	-0.3		0.4	V
R_{OUT}	OUTP to OUTN internal equivalent output resistance (V_{INA} - V_{INB} = 0 V)			24		kΩ
R_{PD}	OUTN to PD internal pull down resistor		2.85		4.25	kΩ

1. *See Figure 8. t_{PLH} and t_{PHL} test condition*

3 U-I operation description

Figure 3. **Input U-I operation**

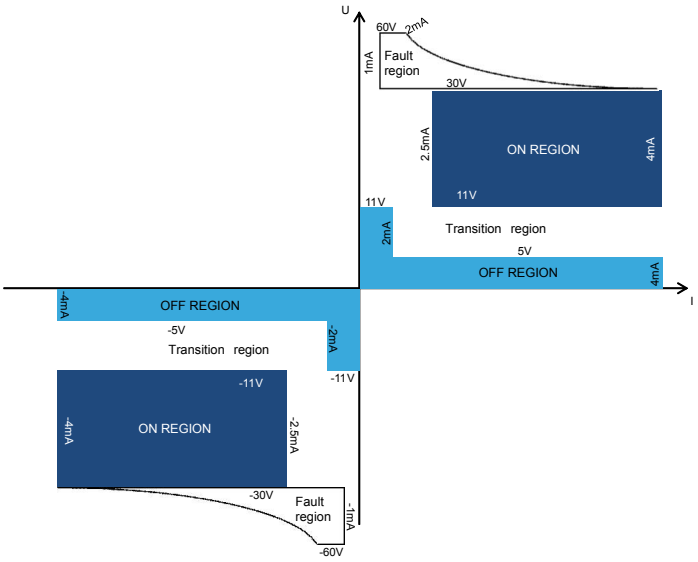
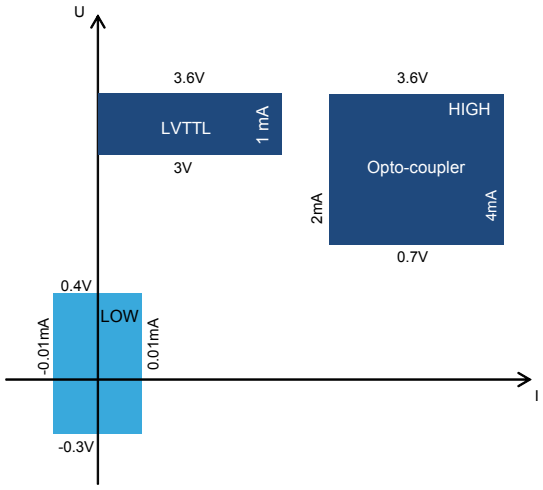


Figure 4. **Output U-I operation**



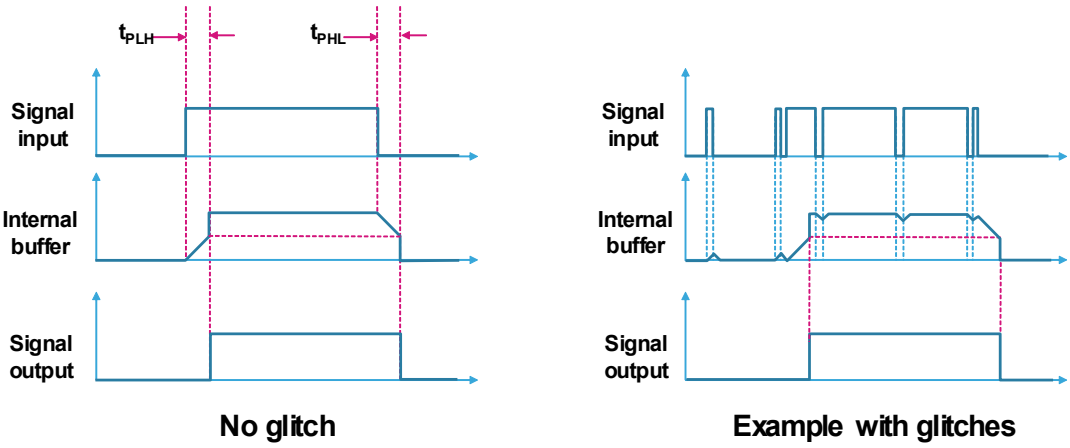
4 Fault mode description

When the input voltage V_{IN} exceeds a threshold V_{FAULT} = 30V the CLT03-2Q3 activates the Fault Mode with a defined latency t_{FAULT}. In this mode the CLT03-2Q3 further reduces the input current limitation down to I_{FAULT} and the corresponding output channel is deactivated.

Fault mode ensures defined and safe operation of the CLT03-2Q3 in overvoltage condition as it is often required by safety regulations.

5 Deglitch filter

Figure 5. **Deglitch filter**



To provide the best EMI robustness solution, a deglitch filter based on a non-resettable mono-stable has been integrated. As described in Deglitch filter, to avoid parasitic spike in output signal when glitches occur in input signals, the integrated internal buffer cleans the glitch effect. The output activation and deactivation action times is defined by t_{PLH} and t_{PHL} when no glitch.

6 Test pulse feature description

The built-in test pulse feature complies with the latest safety standards. Thus, it is possible to know on a regular basis that CLT03-2Q3 is still working properly.

In order, to enable the Test Pulse feature a capacitor should be connected between TP and OUTN pins. When such a capacitor is connected, the OUTP value will be forced to low state every TP period (P_{TP}) for a define test pulse width (t_{TP}). TP period is equal to 256 times t_{TP}.

The frequency of the “Test Pulse low state” is managed through the capacitor value. In order to disable this feature, TP should be shorted to OUTN.

Table 5. Test pulse parameters

Symbol	Description	Min.	Typ.	Max.	Unit
f_{TP}	PTest pulse frequency	4.1		219	kHz
C_{TP}	External capacitor range	100		4700	pF
t_{TP}	Test pulse width	$1/f_{TP}$			ms
P_{TP}	Test pulse period	256 x t_{TP}			ms
Δf_{TP}	Test pulse frequency variation (out of capacitance variation)	-60		+60	%

Figure 6. Test Pulse parameters description

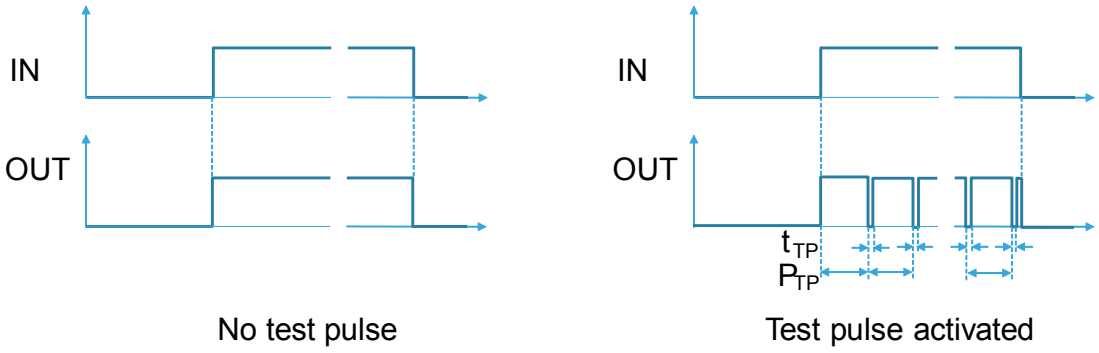
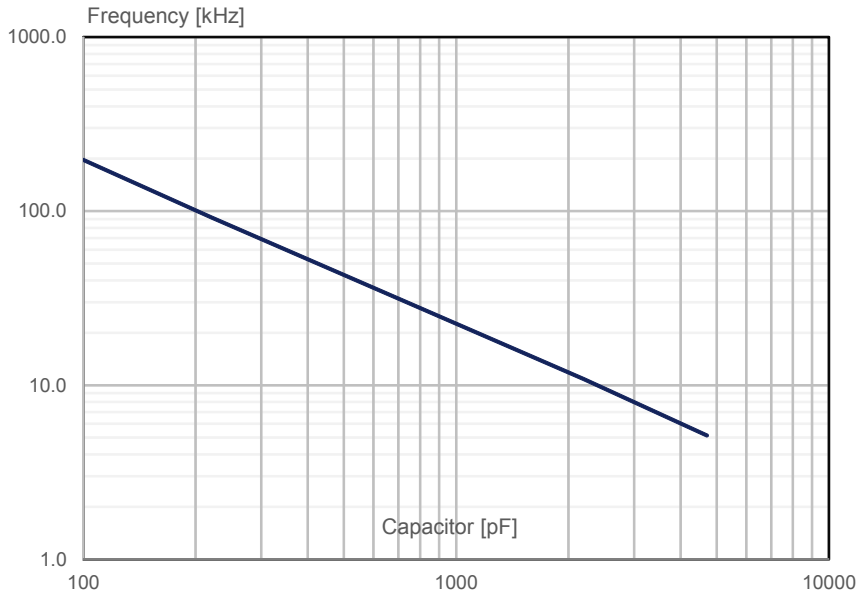
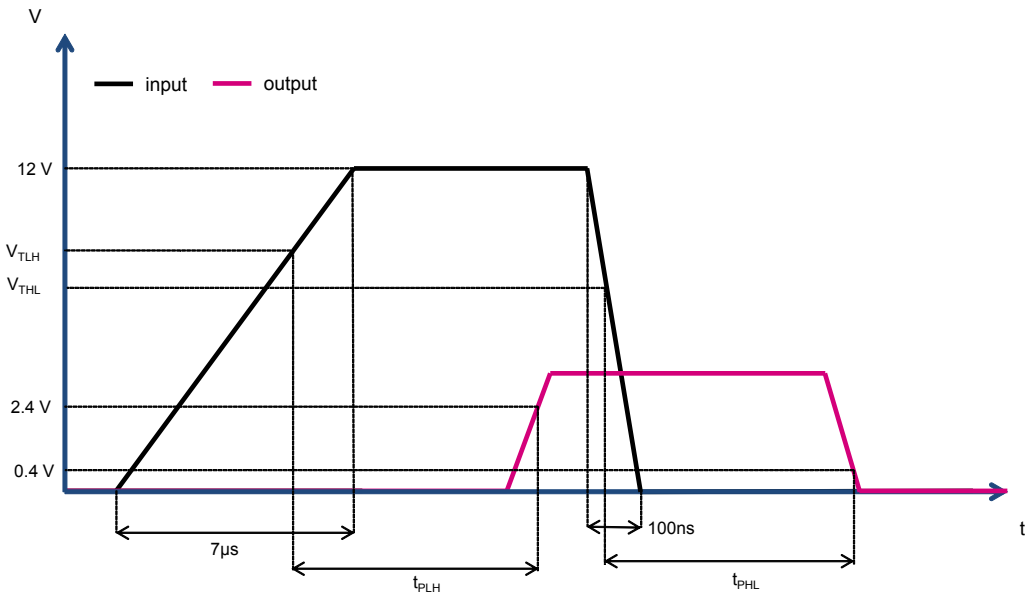


Figure 7. f_{TP} versus C_{TP} value



7 Propagation time measurement description

Figure 8. t_{PLH} and t_{PHL} test condition



Note: for t_{PLH} and t_{PHL} measurement, V_{TLH} and V_{THL} should be determined for each sample. Timing measurement should be done with these samples specific V_{TLH} and V_{THL} thresholds.

8 Simplified application schematic

Table 6. Configuration compatibility of CLT03-2Q3

Symbol	High Side	Low Side
Isolated	Yes	Yes
Non-isolated	Yes	No

Each circuit given in this section is given for 1 channel only.

Figure 9. High side – isolated configuration

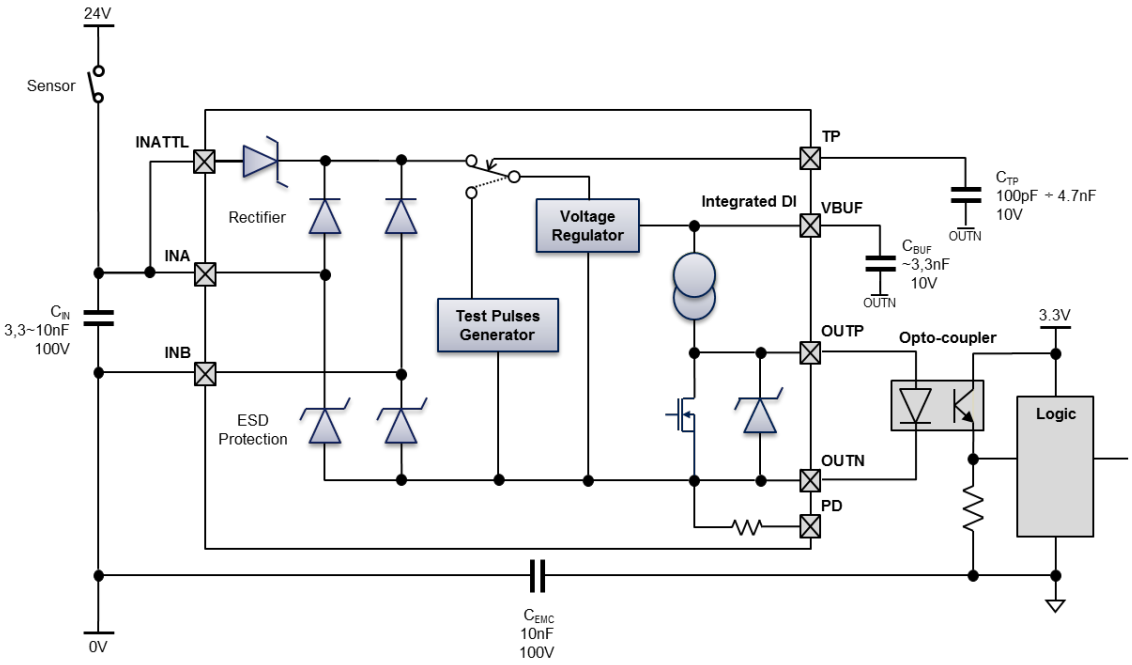


Figure 10. **Low side – isolated configuration**

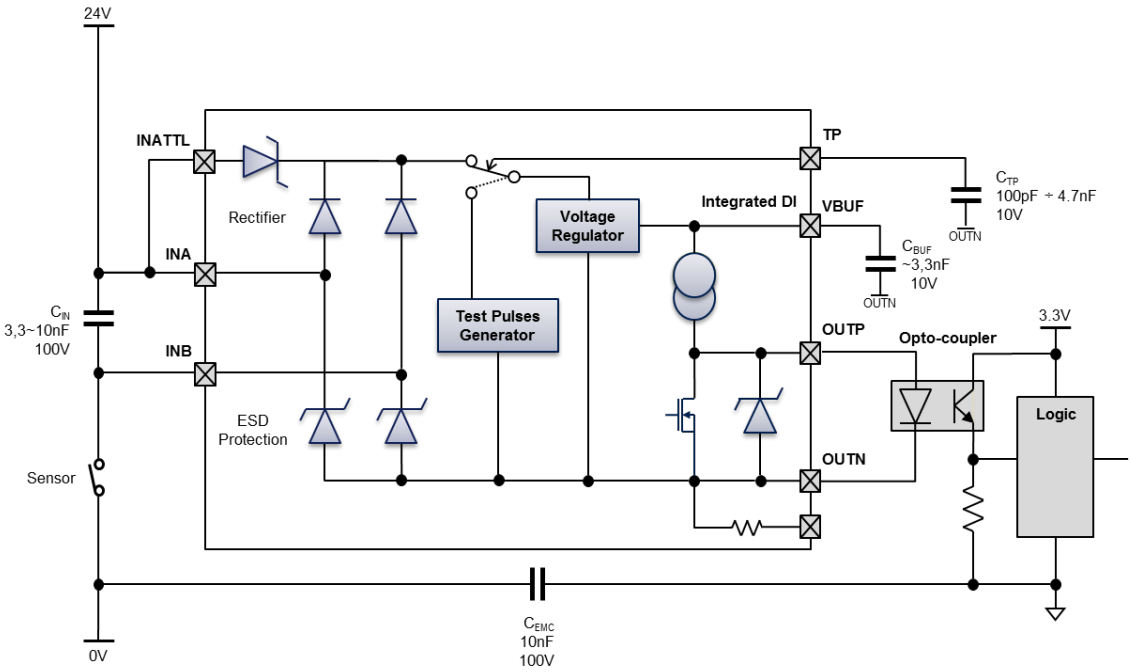
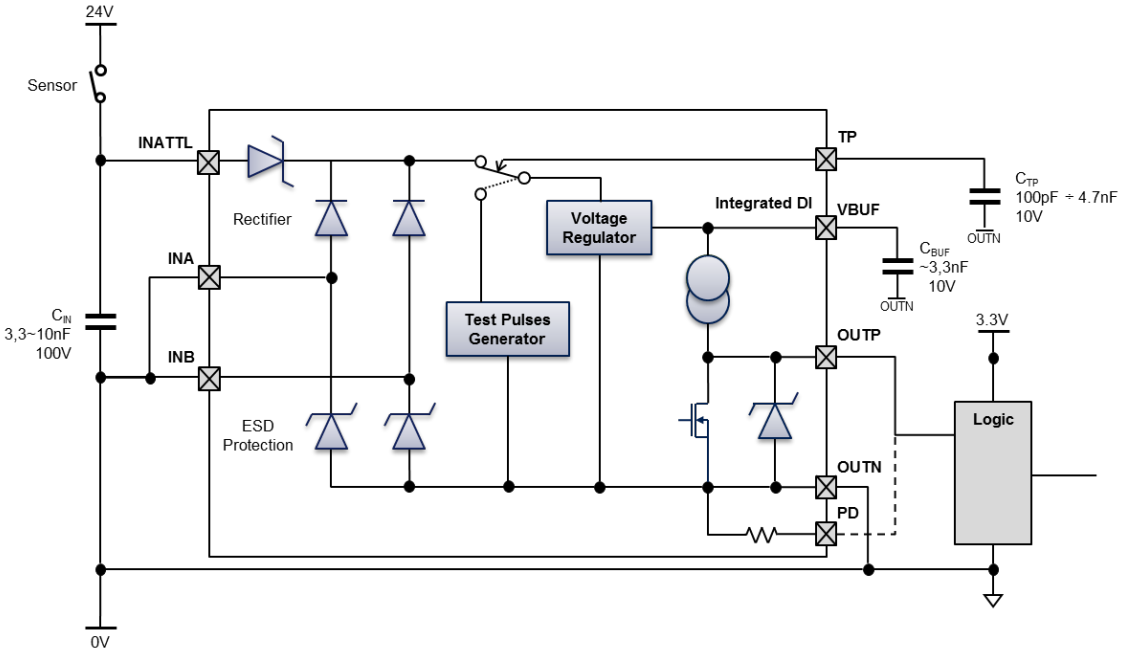


Figure 11. **High side – non-isolated configuration**



Note: OUTP to PD connection is optional.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN 2X4 -16L package information

Figure 12. QFN 2X4-16L package outline

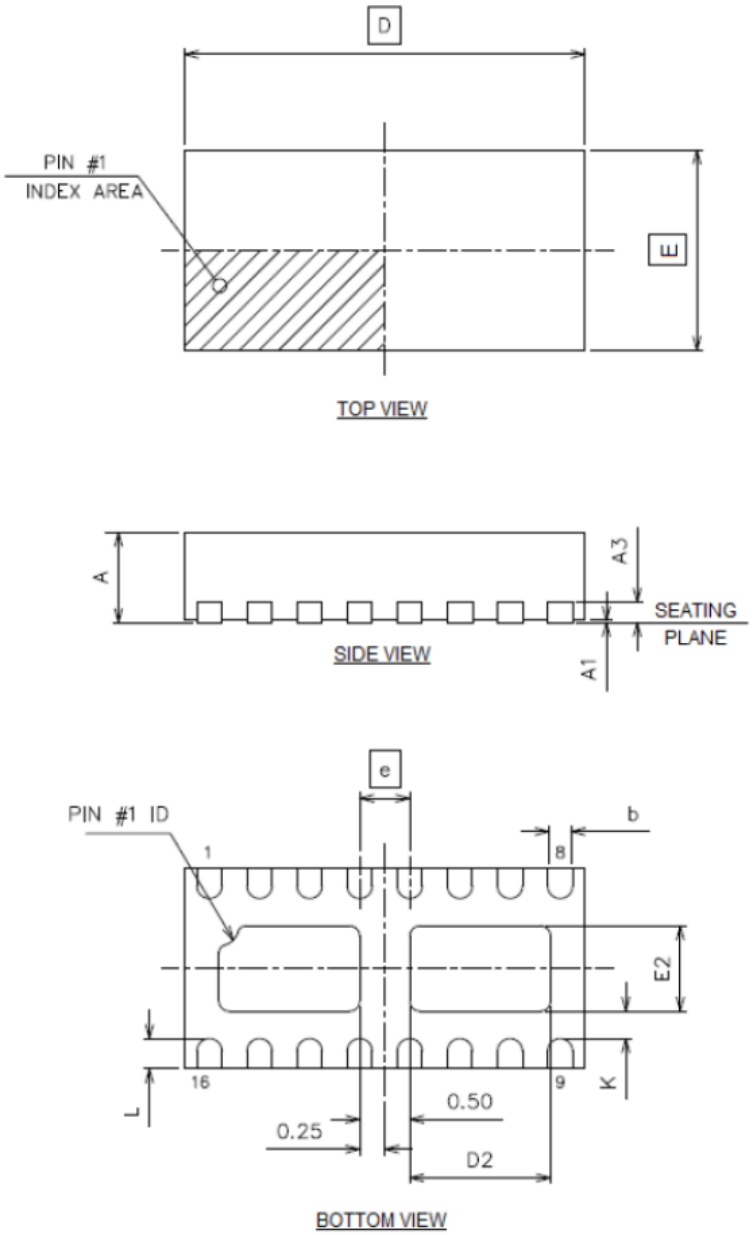


Table 7. QFN 2X4-16L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.20			0.008	
B	0.18	0.25	0.30	0.0071	0.0100	0.0118
D	3.95	4.00	4.05	0.1555	0.1574	0.1594
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D2	1.25	1.40	1.51	0.0492	0.0551	0.0594
E2	0.70	0.85	0.95	0.0276	0.0334	0.0374
e		0.50			0.0197	
K	0.15			0.0059		
L	0.20	0.30	0.40	0.0079	0.0118	0.0157

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 13. Footprint recommendations

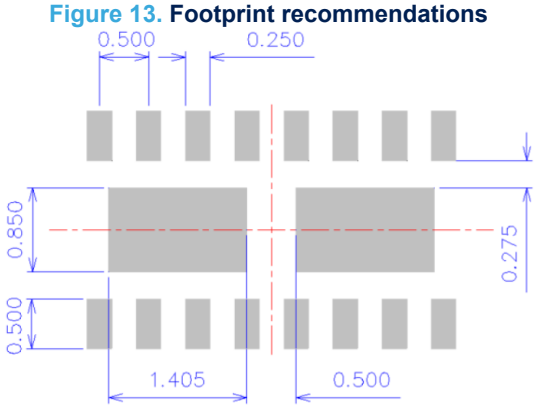


Figure 14. Marking

Figure 15. **Tape and reel outline**

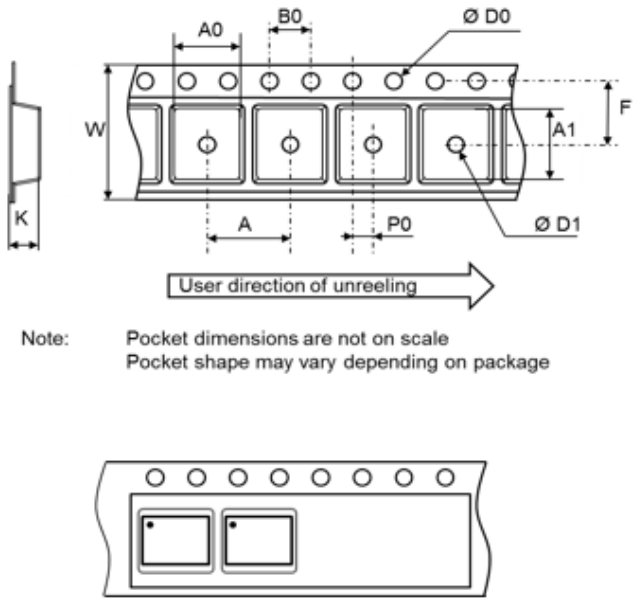
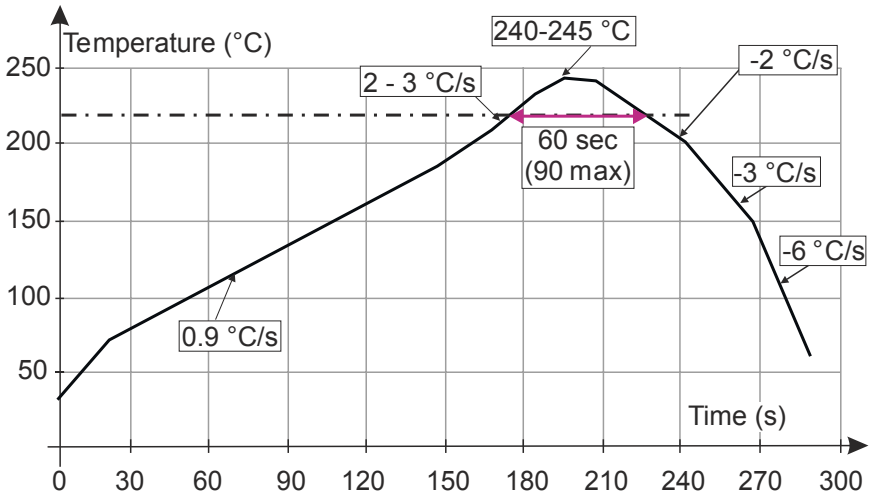


Table 8. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	3.90	4.00	4.10
A0	2.20	2.25	2.30
A1	4.20	4.25	4.30
B0	3.90	4.00	4.10
ØD0	1.50		1.60
ØD1	1.00		
F	1.65	1.75	1.85
K	1.10	1.15	1.20
P0	1.95	2.00	2.05
W	11.90	12.00	12.30

10 Reflow profile

Figure 16. **ST ECOPACK® recommended soldering reflow profile for PCB mounting**



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-ST-020.

11 Ordering information

Figure 17. **Ordering information scheme**

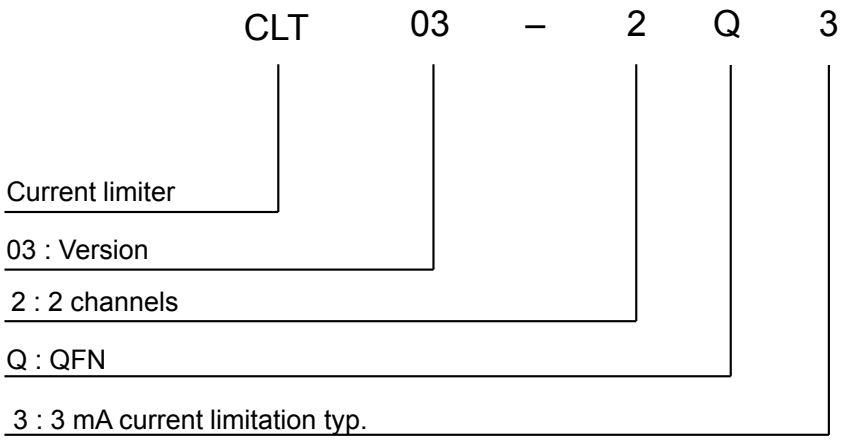


Table 9. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
CLT03-2Q3	CLT03	QFN 2 x 4 – 16L	20 mg	3000	Tape and reel

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
18-Dec-2017	1	Initial release.
11-Dec-2018	2	Minor text change to improve readability.
23-Dec-2019	3	Updated Section Features, Table 4. Electrical characteristics (-30 °C < Tj < +125 °C, unless otherwise specified) (values), Section 8 Simplified application schematic and Figure 6. Test Pulse parameters description. Added Table 2. Thermal resistance parameter and Section 5 Deglitch filter.
06-Feb-2020	4	Updated Table 4. Electrical characteristics (-30 °C < Tj < +125 °C, unless otherwise specified) (values) and Figure 4. Output U-I operation..
04-Mar-2020	5	Updated Section Features, Section 2.1 Absolute ratings and Section 2.2 Electrical characteristics.

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