

FEATURES

- 2-Channel Ideal Diode ORing or Load Sharing
- Low Loss Replacement for ORing Diodes
- Low Forward On-Resistance (100mΩ Max at 3.6V)
- Low Reverse Leakage Current (1μA Max)
- Small Regulated Forward Voltage (28mV Typ)
- 2.5V to 5.5V Operating Range
- 2.6A Maximum Forward Current
- Internal Current Limit and Thermal Protection
- Slow Turn-On/Off to Protect Against Inductive Source Impedance-Induced Voltage Spiking
- Ultralow Quiescent Current Consumption, Low Power Alternative to the LTC4413-1
- Status Output to Indicate if Selected Channel is Conducting
- Programmable Channel On/Off
- Low Profile (0.75mm) 10-Lead 3mm × 3mm DFN Package

APPLICATIONS

- Battery and Wall Adapter Diode ORing in Handheld Products
- Backup Battery Diode ORing
- Power Switching
- USB Peripherals
- Uninterruptable Supplies

LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and ThinSOT and PowerPath are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

DESCRIPTION

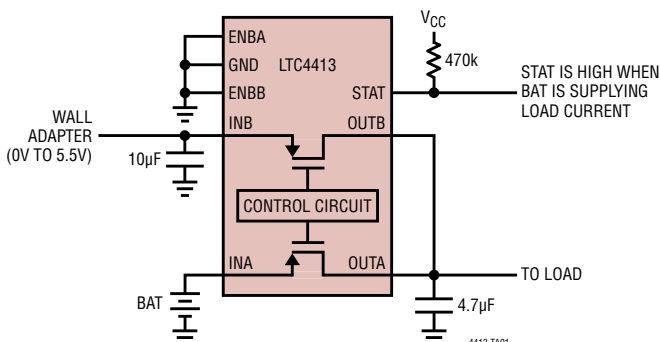
The LTC[®]4413 contains two monolithic ideal diodes, each capable of supplying up to 2.6A from input voltages between 2.5V and 5.5V. Each ideal diode uses a 100mΩ P-channel MOSFET that independently connects INA to OUTA and INB to OUTB. During normal forward operation the voltage drop across each of these diodes is regulated to as low as 28mV. Quiescent current is less than 40μA for diode currents up to 1A. If either of the output voltages exceeds its respective input voltages, that MOSFET is turned off and less than 1μA of reverse current will flow from OUT to IN. Maximum forward current in each MOSFET is limited to a constant 2.6A and internal thermal limiting circuits protect the part during fault conditions.

Two active-high control pins independently turn off the two ideal diodes contained within the LTC4413, controlling the operation mode as described by Table 1. When the selected channel is reverse biased, or the LTC4413 is put into low power standby, a status signal indicates this condition with a low voltage.

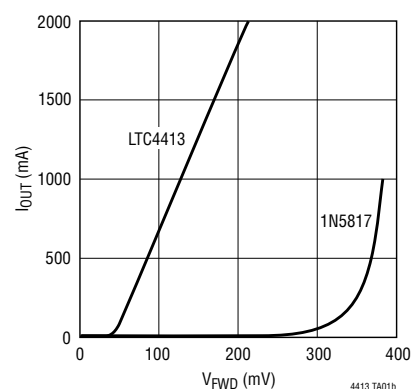
A 9μA open-drain STAT pin is used to indicate conduction status. When terminated to a positive supply through a 470k resistor, the STAT pin can be used to indicate that the selected diode is conducting with a high voltage. This signal can also be used to drive an auxiliary P-channel MOSFET power switch to control a third alternate power source when the LTC4413 is not conducting forward current.

The LTC4413 is housed in a 10-lead DFN package.

TYPICAL APPLICATION



LTC4413 vs 1N5817 Schottky



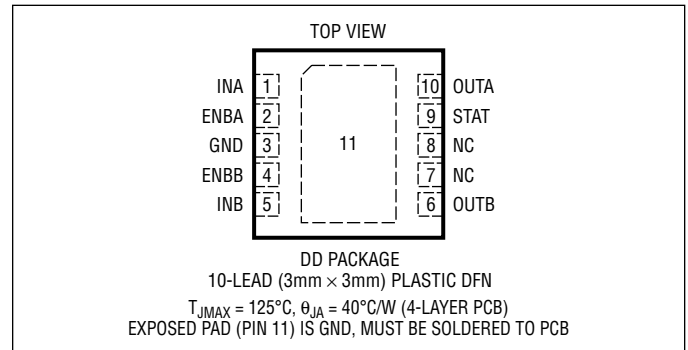
4413fd

ABSOLUTE MAXIMUM RATINGS

(Note 1)

INA, INB, OUTA, OUTB, STAT, ENBA, ENBB Voltage	-0.3V to 6V
Operating Temperature Range.....	-40°C to 85°C
Storage Temperature Range.....	-65°C to 125°C
Junction Temperature (Note 4)	125°C
Continuous Power Dissipation (Derate 25mW/°C Above 70°C).....	1500mW

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4413EDD#PBF	LTC4413EDD#TRPBF	LBGN	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN} , V _{OUT}	Operating Supply Range for Channel A or B	V _{IN} and/or V _{OUT} Must Be in This Range for Proper Operation	● 2.5		5.5	V
UVLO	UVLO Turn-On Rising Threshold	Max (V _{INA} , V _{INB} , V _{OUTA} , V _{OUTB})	●		2.4	V
	UVLO Turn-Off Falling Threshold	Max (V _{INA} , V _{INB} , V _{OUTA} , V _{OUTB})	● 1.7			V
I _{QF}	Quiescent Current in Forward Regulation (Note 3)	V _{INA} = 3.6V, I _{OUTA} = -100mA, V _{INB} = 0V, I _{OUTB} = 0mA	●	25	40	μA
I _{QRIN}	Quiescent Current While in Reverse Turn-Off, Current Drawn from V _{IN}	V _{IN} = 3.6V, V _{OUT} = 5.5V (Note 6)	● -1	0.5	2	μA
I _{QRGND}	Quiescent Current While in Reverse Turn-Off, Measured Via GND	V _{INA} = V _{INB} = V _{OUTB} = 0V, V _{OUTA} = 5.5V, V _{STAT} = 0V		22	30	μA
I _{QROUTA}	Quiescent Current While in Reverse Turn-Off, Current Drawn from V _{OUTA} When OUTA Supplies Chip Power	V _{INA} = V _{INB} = V _{OUTB} = 0V, V _{OUTA} = 5.5V	●	17	31	μA
I _{QROUTB}	Quiescent Current While in Reverse Turn-Off, Current Drawn from V _{OUTA} When OUTB Supplies Chip Power	V _{INA} = V _{INB} = 0V, V _{OUTA} < V _{OUTB} = 5.5V	●	2	3	μA
I _{QOFF}	Quiescent Current with Both ENBA and ENBB High	V _{INA} = V _{INB} = 3.6V, V _{ENBA} and V _{ENBB} High, V _{STAT} = 0V	●	20	31	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Notes 2, 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LEAK}	V_{INA} or V_{INB} Current When V_{OUTA} or V_{OUTB} Supplies Power	$V_{IN} = 0\text{V}$, $V_{OUT} = 5.5\text{V}$	-1		1	μA
V_{RTO}	Reverse Turn-Off Voltage ($V_{OUT} - V_{IN}$)	$V_{IN} = 3.6\text{V}$	-5		10	mV
V_{FWD}	Forward Voltage Drop ($V_{IN} - V_{OUT}$) at $I_{OUT} = -1\text{mA}$	$V_{IN} = 3.6\text{V}$	●	28	38	mV
R_{FWD}	On-Resistance, R_{FWD} Regulation (Measured as $\Delta V/\Delta I$)	$V_{IN} = 3.6\text{V}$, $I_{OUT} = -100\text{mA}$ to -500mA (Note 5)		100	140	$\text{m}\Omega$
R_{ON}	On-Resistance, R_{ON} Regulation (Measured as V/I at $I_{IN} = 1\text{A}$)	$V_{IN} = 3.6\text{V}$, $I_{OUT} = -1.0\text{A}$ (Note 5)		140	200	$\text{m}\Omega$
t_{ON}	PowerPath™ Turn-On Time	$V_{IN} = 3.6\text{V}$, from ENBA, ENBB Falling to I_{IN} Ramp Starting (Note 7)		50		μs
t_{OFF}	PowerPath Turn-Off Time	$V_{IN} = 3.6\text{V}$, $I_{OUT} = -100\text{mA}$ (Note 7)		4		μs

Short-Circuit Response

I_{OC}	Current Limit	$V_{INX} = 3.6\text{V}$ (Notes 4, 5)		1.8		A
I_{OOC}	Quiescent Current While in Overcurrent Operation	$V_{INX} = 3.6\text{V}$, $I_{OUT} = 1.9\text{A}$ (Notes 4, 5)		150	300	μA

STAT Output

I_{SOFF}	STAT Off Current	Shutdown	●	-1	0	1	μA
I_{SON}	STAT Sink Current	$V_{IN} > V_{OUT}$, $V_{ENBA} < V_{ENBIL}$, $V_{ENBB} < V_{ENBIL}$, $I_{OUT} < I_{MAX}$		7	9	17	μA
$t_{S(ON)}$	STAT Pin Turn-On Time			1			μs
$t_{S(OFF)}$	STAT Pin Turn-Off Time			1			μs

ENB Inputs

V_{ENBIH}	ENBA, ENBB Inputs Rising Threshold Voltage	V_{ENBA} , V_{ENBB} Rising	●	540	600		mV
V_{ENBIL}	ENBA, ENBB Inputs Falling Threshold Voltage	V_{ENBA} , V_{ENBB} Falling	●	400	460		mV
$V_{ENBHYST}$	ENBA, ENBB Inputs Hysteresis	$V_{ENBHYST} = (V_{ENBIH} - V_{ENBIL})$		90			mV
I_{ENB}	ENBA, ENBB Inputs Pull-Down Current	$V_{OUT} < V_{IN} = 3.6\text{V}$, $V_{ENBA} > V_{ENBIL}$, $V_{ENBB} > V_{ENBIL}$	●	1.5	3	4.5	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4413 is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Quiescent current increases with diode current, refer to plot of I_{OQ} vs I_{OUT} .

Note 4: This IC includes overtemperature protection that is intended

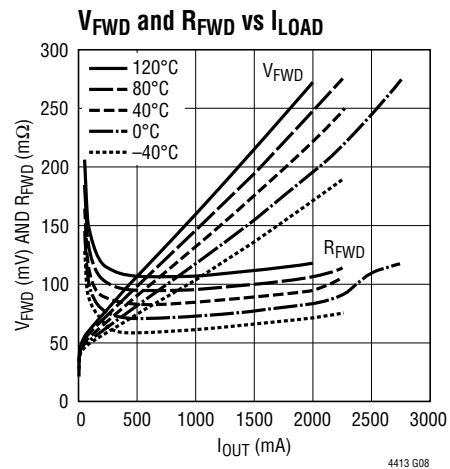
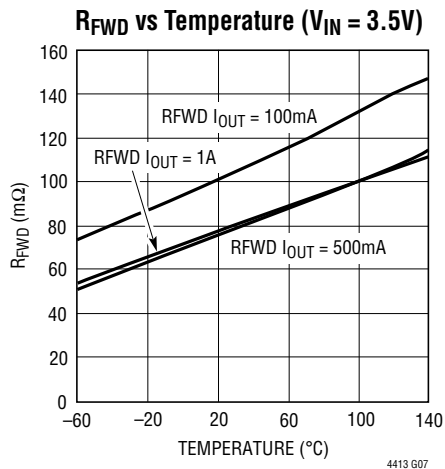
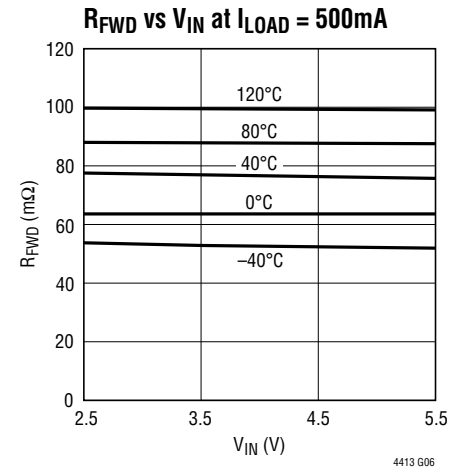
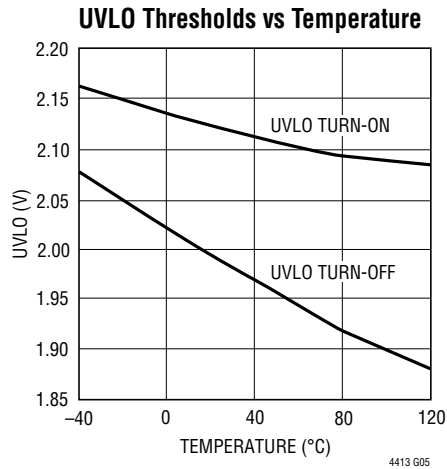
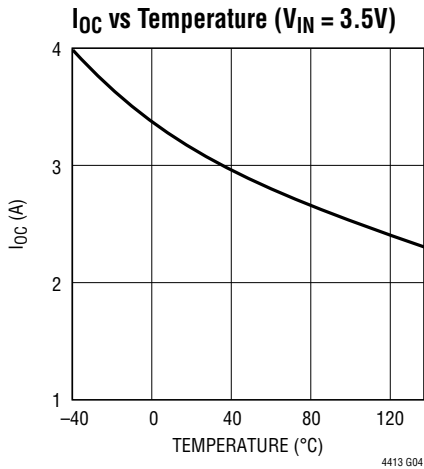
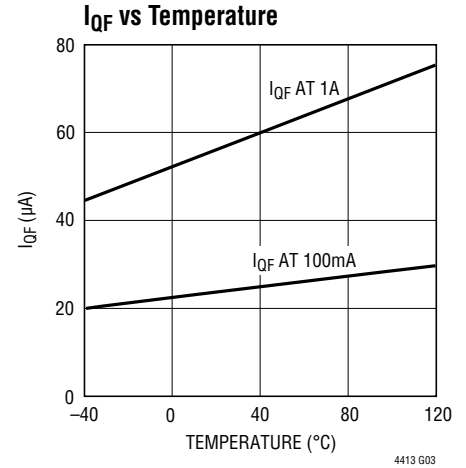
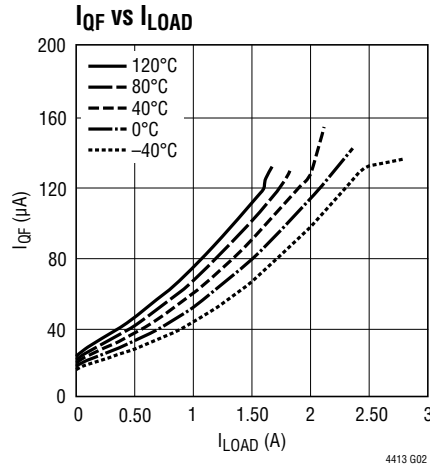
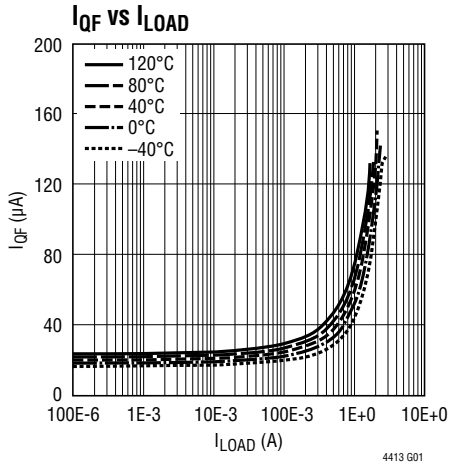
to protect the device during momentary overload conditions. Overtemperature protection will become active at a junction temperature greater than the maximum operating temperature. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: This specification is guaranteed by correlation to wafer-level measurements.

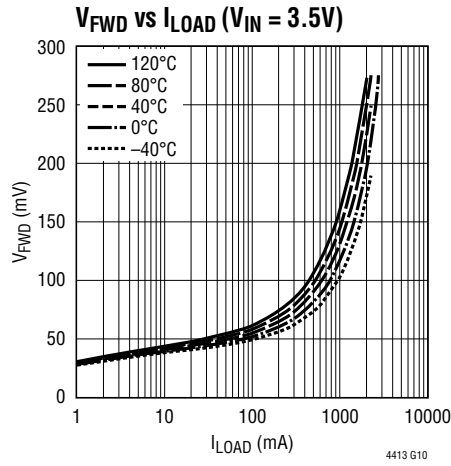
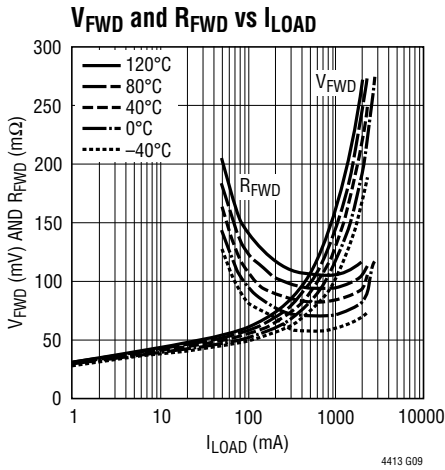
Note 6: Unless otherwise specified, current into a pin is positive and current out of a pin is negative. All voltages referenced to GND.

Note 7: Guaranteed by design.

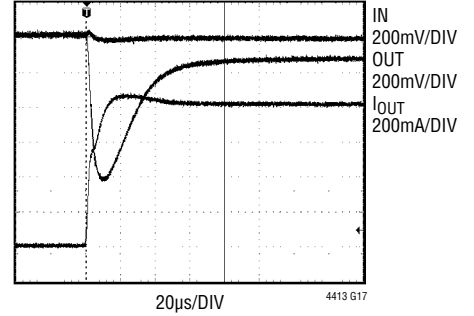
TYPICAL PERFORMANCE CHARACTERISTICS



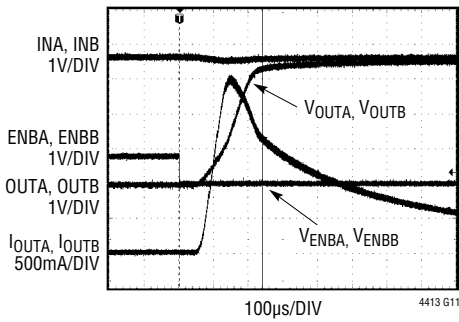
TYPICAL PERFORMANCE CHARACTERISTICS



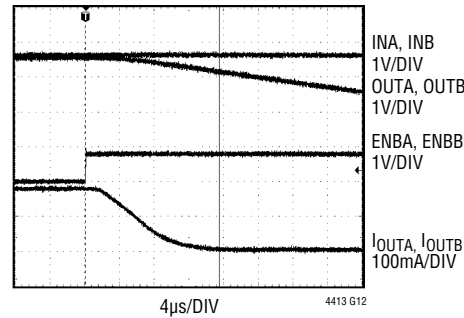
Response to 800mA Load Step in 80μs



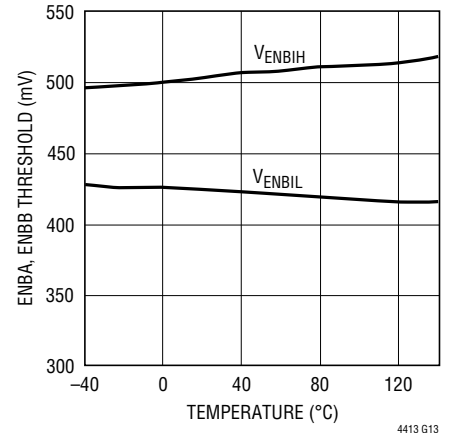
ENBA, ENBB Turn-On, 240μs to Recover with 180mA Load



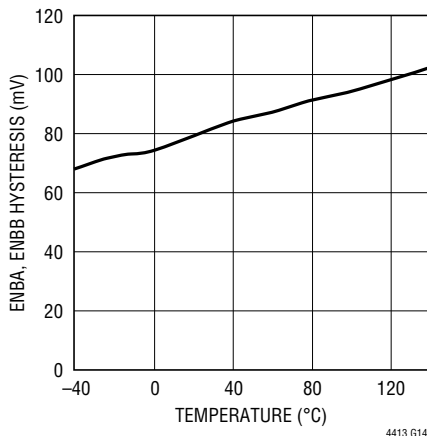
ENBA, ENBB Turn-Off, 16μs to Disconnect IN from 180mA Load



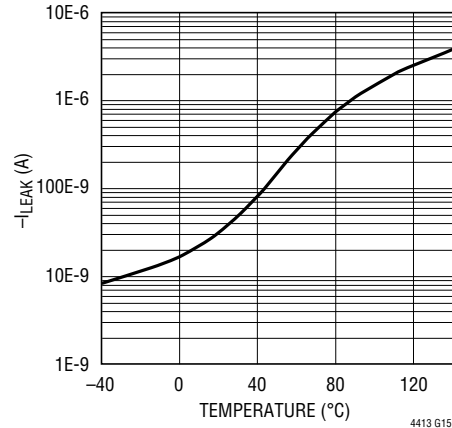
ENBA, ENBB Threshold vs Temperature



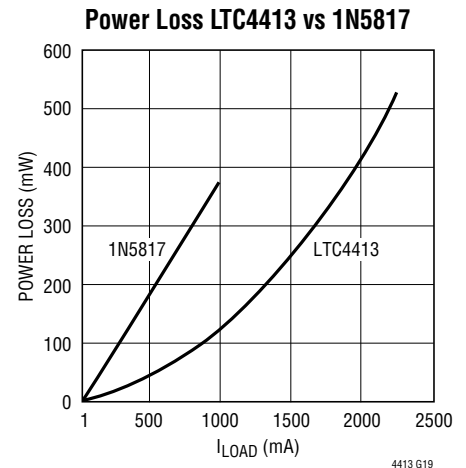
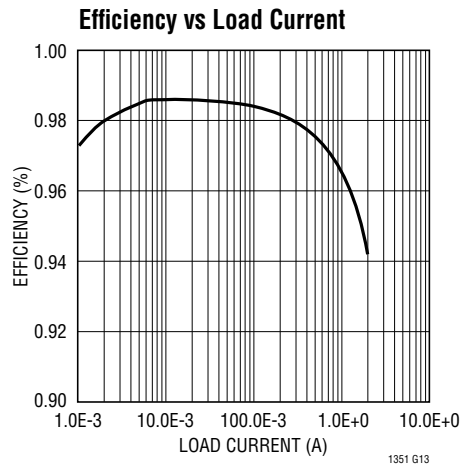
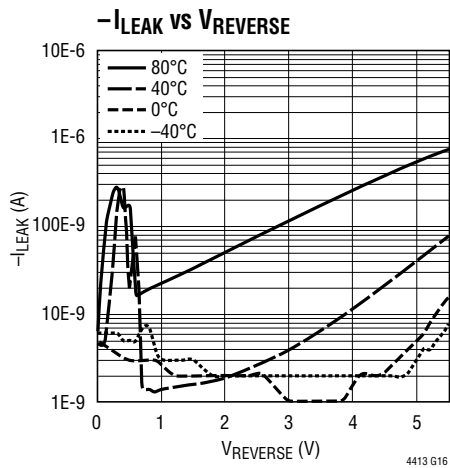
ENBA, ENBB Hysteresis vs Temperature



-I_{LEAK} vs Temperature at V_{REVERSE} = 5.5V



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

INA (Pin 1): Primary Ideal Diode Anode and Positive Power Supply. Bypass INA with a ceramic capacitor of at least 1 μ F. 1 Ω snub resistors in series with a capacitor and higher valued capacitances are recommended when large inductances are in series with this input. Limit slew rate on this pin to less than 0.5V/ μ s. This pin can be grounded when not used.

ENBA (Pin 2): Enable Low for Diode A. Weak (3 μ A) pull-down. Pull this pin high to shut down this power path. Tie to GND to enable. Refer to Table 1 for mode control functionality. This pin can be left floating, weak pull-down internal to the LTC4413.

GND (Pins 3, Exposed Pad Pin 11): Power and Signal Ground for the IC. The exposed pad of the package, Pin 11, must be soldered to PCB ground to provide both electrical contact to ground and good thermal contact to the PCB.

ENBB (Pin 4): Enable Low for Diode B. Weak (3 μ A) pull-down. Pull this pin high to shut down this power path. Tie to GND to enable. Refer to Table 1 for mode control functionality. This pin can be left floating, weak pull-down internal to the LTC4413.

INB (Pin 5): Secondary Ideal Diode Anode and Positive Power Supply. Bypass INB with a ceramic capacitor of at least 1 μ F. 1 Ω snub resistors in series with a capacitor and

higher valued capacitances are recommended when large inductances are in series with this input. Limit slew rate on this pin to less than 0.5V/ μ s. This pin can be grounded when not used.

OUTB (Pin 6): Secondary Ideal Diode Cathode and Output. Bypass OUTB with a high (1m Ω min) ESR ceramic capacitor of at least 4.7 μ F. Limit slew rate on this pin to less than 0.5V/ μ s. This pin must be left floating when not in use.

NC (Pin 7): No Internal Connection.

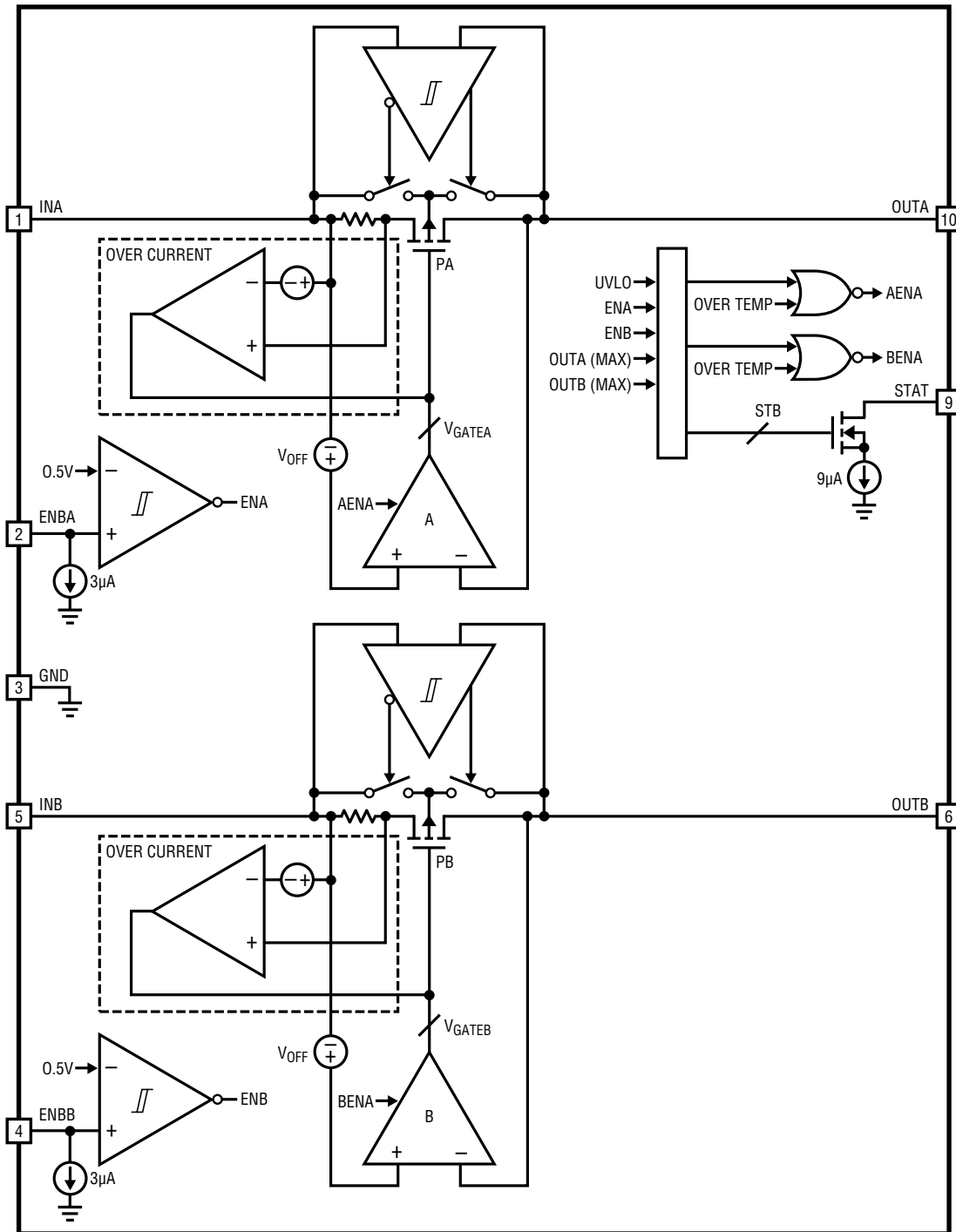
NC (Pin 8): No Internal Connection.

STAT (Pin 9): Status Condition Indicator. Weak (9 μ A) pull-down current output. When terminated, STAT = high indicates diode conducting.

The function of the STAT pin depends on the mode that has been selected. Table 2 describes the STAT pin output current as a function of the mode selected as well as the conduction state of the two diodes. This pin can also be left floating or grounded.

OUTA (Pin 10): Primary Ideal Diode Cathode and Output. Bypass OUTA with a high (1m Ω min) ESR ceramic capacitor of at least 4.7 μ F. Limit slew rate on this pin to less than 0.5V/ μ s. This pin must be left floating when not in use.

BLOCK DIAGRAM



4413 F01

Figure 1

OPERATION

The LTC4413 is described with the aid of the Block Diagram (Figure 1). Operation begins when the power source at V_{INA} or V_{INB} rises above the undervoltage lockout (UVLO) voltage of 2.4V and either of the ENBA or ENBB control pins is low. If only the voltage at the V_{INA} pin is present, the power source to the LTC4413 (V_{DD}) will be supplied from the V_{INA} pin. The amplifier (A) pulls a current proportional to the difference between V_{INA} and V_{OUTA} from the gate (V_{GATEA}) of the internal PFET (PA), driving this gate voltage below V_{INA} . This turns on PA. As V_{OUTA} is pulled up to a forward voltage drop (V_{FWD}) of 20mV below V_{INA} , the LTC4413 regulates V_{GATEA} to maintain the small forward voltage drop. The system is now in forward regulation and the load at V_{OUTA} is powered from the supply at V_{INA} . As the load current varies, V_{GATEA} is controlled to maintain V_{FWD} until the load current exceeds the transistor's (PA) ability to deliver the current as V_{GATEA} approaches GND. At this point the PFET behaves as a fixed resistor with resistance R_{ON} , whereby the forward voltage increases slightly with increased load current. As the magnitude of I_{OUT} increases further (such that $I_{LOAD} > I_{OC}$), the LTC4413 fixes the load current to the constant value I_{OC} to protect the device. The characteristics for parameters R_{FWD} , R_{ON} , V_{FWD} and I_{OC} are specified with the aid of Figure 2, illustrating the LTC4413 forward voltage drop versus that of a Schottky diode.

If another supply is provided at V_{INB} , the LTC4413 likewise regulates the gate voltage on PB to maintain the output voltage V_{OUTB} just below the input voltage V_{INB} . If this

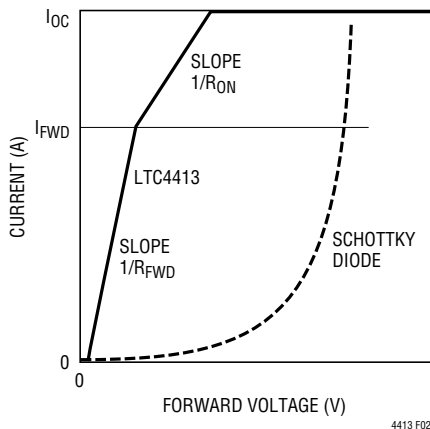


Figure 2

alternate supply, V_{INB} , exceeds the voltage at V_{INA} , the LTC4413 selects this input voltage as the internal supply (V_{DD}). This second ideal diode operates independently of the first ideal diode function.

When an alternate power source is connected to the load at V_{OUTA} (or V_{OUTB}), the LTC4413 senses the increased voltage at V_{OUTA} and amplifier A increases the voltage V_{GATEA} , reducing the current through PA. When V_{OUTA} is higher than $V_{INA} + V_{RTO}$, V_{GATEA} is pulled up to V_{DD} , which turns off PA. The internal power source for the LTC4413 (V_{DD}) is then diverted to source current from the V_{OUTA} pin, only if V_{OUTA} is larger than V_{INB} (or V_{OUTB}). The system is now in the reverse turn-off mode. Power to the load is being delivered from an alternate supply and only a small current is drawn from V_{INA} to sense the potential at V_{INA} .

When the selected channel of the LTC4413 is in reverse turn-off mode or both channels are disabled, the STAT pin sinks 9 μ A of current (I_{SON}) if connected.

Channel selection is accomplished using the two ENB pins, ENBA and ENBB. For example with channel A, when the ENBA input is asserted (high), PA's gate voltage is pulled to V_{DD} at a controlled rate, limiting the turn-off time to avoid voltage spiking at the input when being driven by an inductive source impedance. A 3 μ A pull-down current on the ENBA, ENBB pins ensures a low level at these inputs if left floating.

Slow Response Time

The LTC4413-1 (or LTC4413-2) is recommended for applications with demanding load step or fast slew rate requirements. The LTC4413-1 and LTC4413-2 provide better load regulation in these environments at the expense of higher quiescent current. The LTC4413 is optimized for lower power consumption and should not be used in high slew rate environments or when large and fast load transients are anticipated.

Overcurrent and Short-Circuit Protection

During an overcurrent condition, the output voltage droops as the load current exceeds the amount of current that the LTC4413 can supply. At the time when an overcurrent condition is first detected, the LTC4413 takes some time to

OPERATION

detect this condition before reducing the current to I_{MAX} . For short durations after the output is shorted, the current may exceed I_{MAX} . The magnitude of this peak short-circuit current can be large, depending on the load current immediately before the short circuit occurs. During overcurrent operation, the power consumption of the LTC4413 is large, and is likely to cause an overtemperature condition as the internal die temperature exceeds the thermal shutdown temperature.

Overtemperature Protection

The overtemperature condition is detected when the internal die temperature increases beyond 150°C. An overtemperature condition causes the gate amplifiers (A and B) as well as the two P-channel MOSFETs (PA and PB) to be shut off. When the internal die temperature cools to below 140°C, the amplifiers turn on and revert to normal operation. Note that prolonged operation under overtemperature conditions degrades reliability.

Channel Selection and Status Output

Two active-high control pins independently turn off the two ideal diodes contained within the LTC4413, controlling the operation mode as described by Table 1. When the selected channel is reverse biased, or the LTC4413 is put into low power standby, the status signal indicates this condition with a low voltage.

Table 1. Mode Control

ENBA	ENBB	STATE
Low	Low	Diode OR (NB: The Two Outputs Are Not Connected Internal to the Device)
Low	High	Diode A = Enabled, Diode B = Disabled
High	Low	Diode A = Disabled, Diode B = Enabled
High	High	All Off (Low Power Standby)

The function of the STAT pin depends on the mode that has been selected. The following table describes the STAT pin output current as a function of the mode selected, as well as the conduction state of the two diodes.

Table 2. STAT Output Pin Function

ENBA	ENBB	CONDITIONS	STAT
Low	Low	Diode A Forward Bias, Diode B Forward Bias	$I_{SNK} = 0\mu A$
		Diode A Forward Bias, Diode B Reverse Bias	$I_{SNK} = 0\mu A$
		Diode A Reverse Bias, Diode B Forward Bias	$I_{SNK} = 9\mu A$
		Diode A Reverse Bias, Diode B Reverse Bias	$I_{SNK} = 9\mu A$
Low	High	Diode A Forward Bias, Diode B Disabled	$I_{SNK} = 0\mu A$
		Diode A Reverse Bias, Diode B Disabled	$I_{SNK} = 9\mu A$
High	Low	Diode A Disabled, Diode B Forward Bias	$I_{SNK} = 0\mu A$
		Diode A Disabled, Diode B Reverse Bias	$I_{SNK} = 9\mu A$
High	High	Diode A Disabled, Diode B Disabled	$I_{SNK} = 9\mu A$

APPLICATIONS INFORMATION

Introduction

The LTC4413 is intended for power control applications that include low loss diode ORing, fully automatic switchover from a primary to an auxiliary source of power, microcontroller controlled switchover from a primary to an auxiliary source of power, load sharing between two or more batteries, charging of multiple batteries from a single charger and high side power switching. The LTC4413 is optimized for low quiescent power consumption at the expense of transient response. For more demanding slew

rate or load transient applications, the pin compatible LTC4413-1 is recommended.

Dual Battery Load Sharing with Automatic Switchover to a Wall Adapter

An application circuit for dual battery load sharing with automatic switchover of load from batteries to a wall adapter is shown in Figure 3. When the wall adapter is not present, whichever battery that has the higher voltage provides the load current until it has discharged to the voltage of the other battery. The load is then shared between the two

4413fd

APPLICATIONS INFORMATION

If the AUX is present when a wall adapter is applied, as the resistive divider to ENBB rises through the turn-off threshold, the STAT pin voltage falls and MP1 conducts, allowing the wall adapter to power the load. When the wall adapter is removed while the AUX supply is present, the load voltage falls until the voltage divider at the ENBB pin falls through its turn-on threshold. Once this occurs, the LTC4413 automatically connects the AUX supply to the load when the AUX voltage exceeds the output voltage, causing the STAT voltage to rise and disabling the external PFET.

When an AUX supply is attached, the voltage divider at ENBA (R4 and R5) disconnects the battery from the load, and the auxiliary supply provides load current, unless a wall adapter is present as described earlier. If the auxiliary supply is removed, the battery may again power the load, depending on if a wall adapter is present.

Multiple Battery Charging

Figure 6 illustrates an application circuit for automatic dual battery charging from a single charger. Whichever battery has the lower voltage will receive the larger charging current

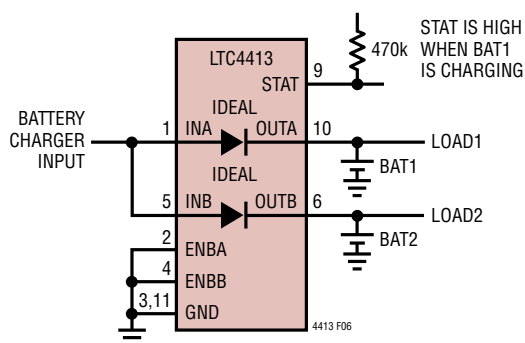


Figure 6

until both battery voltages are equal, then both are charged. While both batteries are charging simultaneously, the higher capacity battery gets proportionally higher current from the charger. For Li-Ion batteries, both batteries achieve the float voltage minus the forward regulation voltage of 20mV. This concept can apply to more than two batteries. The STAT pin provides information as to when battery 1 is being charged. For intelligent control, the ENBA/ENBB pin inputs can be used with a microcontroller as shown in Figure 4.

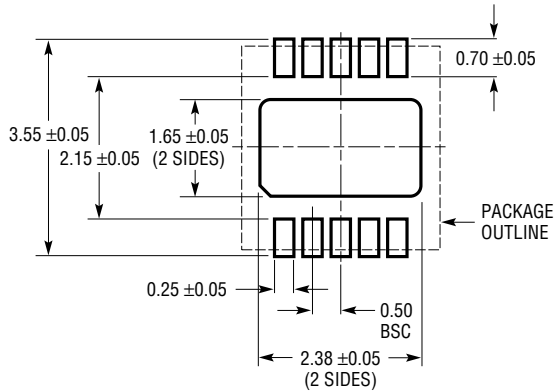
Automatic Switchover from a Battery to a Wall Adapter and Charger

Figure 7 illustrates the LTC4413 performing the function of automatically switching a load over from a battery to a wall adapter while controlling an LTC4059 battery charger. When no wall adapter is present, the LTC4413 connects the load at OUTA from the Li-Ion battery at INA. In this condition, the STAT voltage is high, thereby disabling the battery charger. If a wall adapter of a higher voltage than the battery is connected to INB, the load voltage rises as the second ideal diode conducts. As soon as the OUTA voltage exceeds INA voltage, the BAT is disconnected from the load and the STAT voltage falls, turning on the LTC4059 battery charger and beginning a charge cycle. If the wall adapter is removed, the voltage at INB collapses until it is below the load voltage. When this occurs, the LTC4413 automatically reconnects the battery to the load and the STAT voltage rises, disabling the LTC4059 battery charger. One major benefit of this circuit is that when a wall adapter is present, the user may remove the battery and replace it without disrupting the load.

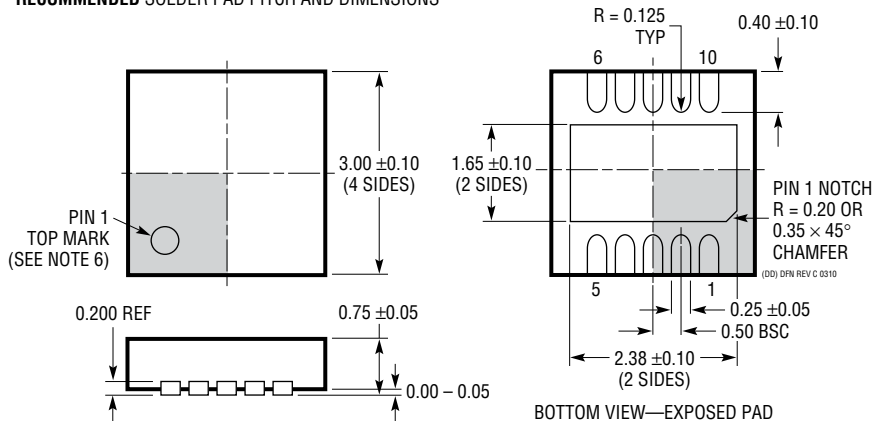
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	07/15	Changed V_{ENB} to $V_{ENBA,B}$ in electrical characteristics	3
		Changed ENB to ENBA,B IN to INA,B and OUT to OUTA,B on plots 3 to 7	5
		Added exposed pad to GND Pin Function label	6
		Added sentence to paragraph prior to Slow Response section and added A,B references	8
		Changed ENBA and ENBB on Tables 1 and 2	9
		Added LTC4415 to Related Parts table	12

