



SY898533L

Precision Differential 3.3V Low Skew LVPECL 1:4 Fanout Buffer

General Description

The SY898533L is a 3.3V, low skew, 1:4 LVPECL fanout buffer with two selectable clock input pairs. Most standard differential input levels can be applied to the CLK, /CLK pair while LVPECL, CML, or SSTL input levels can be applied to the PCLK, /PCLK pair. To eliminate runt pulses on the outputs during asynchronous assertion/de-assertion of the clock enable pin, the clock enable is synchronized with the input signal.

The SY898533L operates from a 3.3V $\pm 5\%$ supply and is guaranteed over the full industrial temperature range of 0°C to +70°C. The SY898533L is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

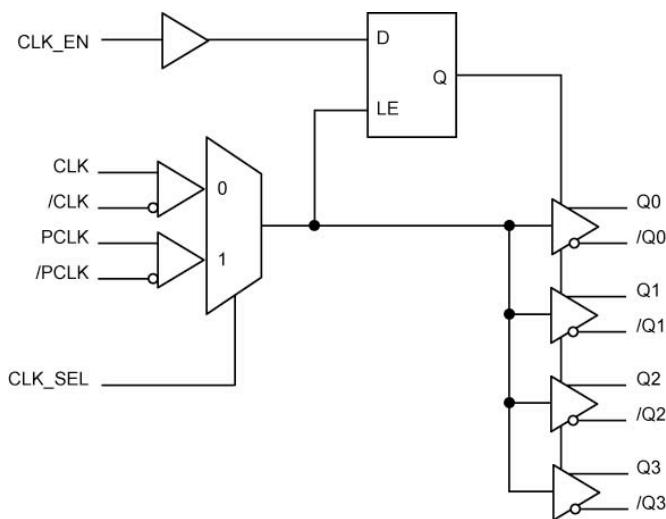


Precision Edge[®]

Features

- Provides four differential 3.3V LVPECL copies
- Selects between differential CLK, /CLK or LVPECL clock inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL input levels
- PCLK, /PCLK pair accepts LVPECL, CML, SSTL input levels
- Guaranteed AC performance over temperature and supply voltage:
 - 650MHz Maximum output frequency
 - < 1.4ns Propagation delay (In-to-Q)
 - < 30ps Output skew
 - < 150ps Part-to-part skew
 - Additive phase jitter, RMS: 0.06ps (typical)
- 3.3V $\pm 5\%$ supply voltage
- 0°C to +70°C temperature operating range
- Available in a 20-pin TSSOP package

Functional Block Diagram



Applications

- SONET clock distribution
- Backplane distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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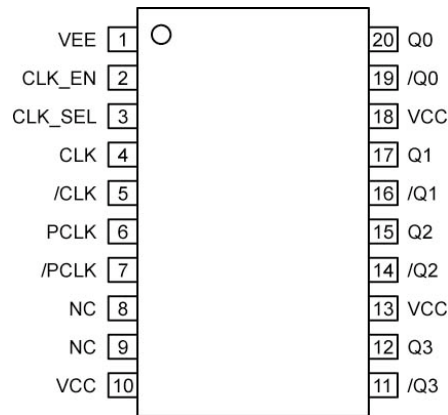
Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|------------------------------|--------------|-----------------|--|-------------------|
| SY898533LKZ | K4-20-1 | Commercial | SY898533 with Pb-Free bar-line Indicator | Matte-tin Pb-Free |
| SY898533LKZTR ⁽²⁾ | K4-20-1 | Commercial | SY898533 with Pb-Free bar-line Indicator | Matte-tin Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



20-Pin TSSOP (K4-20-1)

Pin Description

| Pin Number | Pin Name | Pin Function |
|--------------------------------------|--|--|
| 1 | V _{EE} | Ground. |
| 2 | CLK_EN | Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q3 outputs. It is internally connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. CLK_EN being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. V _{TH} = is approximately 1.5V. |
| 3 | CLK_SEL | Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the input to the multiplexer. Note that this input is internally connected to a 50kΩ pull-down resistor and will default to logic LOW state if left open. V _{TH} = is approximately 1.5V. |
| 4, 5 | CLK, /CLK | Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. CLK is internally connected to a 28kΩ pull-down resistor and will default to a logic LOW state if left open while /CLK is connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. This input pair is selected when CLK_SEL is set to logic LOW. |
| 6, 7 | PCLK, /PCLK | Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. PCLK is internally connected to a 50kΩ pull-down resistor and will default to a logic LOW state if left open while /PCLK is connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. This input pair is selected when CLK_SEL is set to logic HIGH. |
| 8, 9 | NC | Unused Pins |
| 10, 13, 18 | V _{CC} | Positive Power Supply Pins: Bypass with 0.1μF 0.01μF low ESR capacitors as close to the V _{CC} pins as possible. |
| 20, 19 17, 16 15, 14 12, 11 | Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 | LVPECL Differential Output Pairs: Differential buffered output copies of the selected input signal. The output swing is typically 800mV. Unused output pairs may be left floating with no impact on jitter. These differential LVPECL outputs are a logic function of the CLK, /CLK and PCLK, /PCLK, and CLK_SEL inputs. See "Truth Table" below. |

Truth Table

| Inputs | | | Outputs | |
|--------|---------|-----------------|----------------|-----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0 :Q3 | /Q0:/Q3 |
| 0 | 0 | CLK, /CLK | Disabled : LOW | Disabled : HIGH |
| 0 | 1 | PCLK, /PCLK | Disabled : LOW | Disabled : HIGH |
| 1 | 0 | CLK, /CLK | CLK | /CLK |
| 1 | 1 | PCLK, /PCLK | PCLK | /PCLK |

Absolute Maximum Ratings⁽¹⁾

| | |
|---------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +4.6V |
| Input Voltage (V_{IN}) | -0.5V to $V_{CC} + 0.5V$ |
| LVPECL Output Current (I_{OUT}) | |
| Continuous | 50mA |
| Surge | 100mA |
| Lead Temperature (soldering, 20 sec.) | +260°C |
| Storage Temperature (T_s) | -65°C to 150°C |

Operating Ratings⁽²⁾

| | |
|---|--------------------|
| Supply Voltage (V_{CC}) | +3.135V to +3.465V |
| Ambient Temperature (T_A) | 0°C to +70°C |
| Package Thermal Resistance ⁽³⁾ | |
| TSSOP (θ_{JA}) | |
| Still-Air | 73.2°C/W |

Power Supply DC Electrical Characteristics⁽⁴⁾

$V_{CC} = 3.3V \pm 5\%$; $T_A = 0^\circ C$ to +70°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|----------------------|-----------------------|-------|-----|-------|-------|
| V_{CC} | Power Supply | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | No load, max V_{CC} | | | 50 | mA |

LVC MOS/LVTTL DC Electrical Characteristics⁽⁴⁾

$V_{CC} = 3.3V \pm 5\%$; $T_A = 0^\circ C$ to +70°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|---|------|-----|-----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK_EN $V_{IN} = V_{CC} = 3.465V$ | | | 5 | μA |
| | | CLK_SEL $V_{IN} = V_{CC} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK_EN $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | | μA |
| | | CLK_SEL $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | | μA |

Differential DC Electrical Characteristics⁽⁴⁾

$V_{CC} = 3.3V \pm 5\%$; $T_A = 0^\circ C$ to +70°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------|---|--|----------------|-----|-----------------|---------|
| I_{IH} | Input High Current | CLK $V_{IN} = V_{CC} = 3.465V$ | | | 150 | μA |
| | | /CLK $V_{IN} = V_{CC} = 3.465V$ | | | 5 | μA |
| I_{IL} | Input Low Current | CLK $V_{IN} = 0.5V, V_{CC} = 3.465V$ | -5 | | | μA |
| | | /CLK $V_{IN} = 0.5V, V_{CC} = 3.465V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage ^(5, 6) | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. θ_{JA} value is determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Maximum input voltage for PCLK and /PCLK is $V_{CC} + 0.3V$ for single ended applications.
6. V_{IH} is defined as the common mode voltage.

LVPECL DC Electrical Characteristics⁽⁷⁾

$V_{CC} = 3.3V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|---|---|----------------|-----|----------------|---------|
| I_{IH} | Input High Current | PCLK $V_{IN} = V_{CC} = 3.465V$ | | | 150 | μA |
| | | /PCLK $V_{IN} = V_{CC} = 3.465V$ | | | 5 | μA |
| I_{IL} | Input Low Current | PCLK $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | | μA |
| | | /PCLK $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.3 | | 1 | V |
| V_{CMR} | Common Mode Input Voltage ^(8, 9) | | $V_{EE} + 1.5$ | | V_{CC} | V |
| V_{OH} | Output High Voltage ⁽¹⁰⁾ | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Voltage ⁽¹⁰⁾ | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

Notes:

- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Maximum input voltage for PCLK and /PCLK is $V_{CC} + 0.3V$ for single ended applications.
- V_{IH} is defined as the common mode voltage.
- 50Ω to $V_{CC}-2V$ terminated outputs.

AC Electrical Characteristics⁽¹¹⁾

$V_{CC} = 3.3V \pm 5\%$; $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|---|--------------------|-----|------|-----|-------------------|
| f_{MAX} | Maximum Operating Frequency | | 650 | | | MHz |
| t_{PD} | Differential Propagation Delay IN-to-Q | $f \leq 650MHz$ | 1.0 | | 1.4 | ns |
| t_{SKEW} | Output-to-Output Skew ⁽¹²⁾ | | | | 30 | ps |
| | Part-to-Part Skew ⁽¹³⁾ | | | | 150 | ps |
| t_{JITTER} | Additive Phase Jitter ⁽¹⁴⁾ | | | 0.06 | | ps _{RMS} |
| t_r, t_f | Output Rise/Fall Time | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

Notes:

- High-frequency AC-parameters are guaranteed by design and characterization.
- Output-to-Output skew is measured between two different outputs under identical transitions.
- Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. This parameter is defined in accordance with JEDEC Standard 65.
- Driving only one input clock.

Timing Diagrams

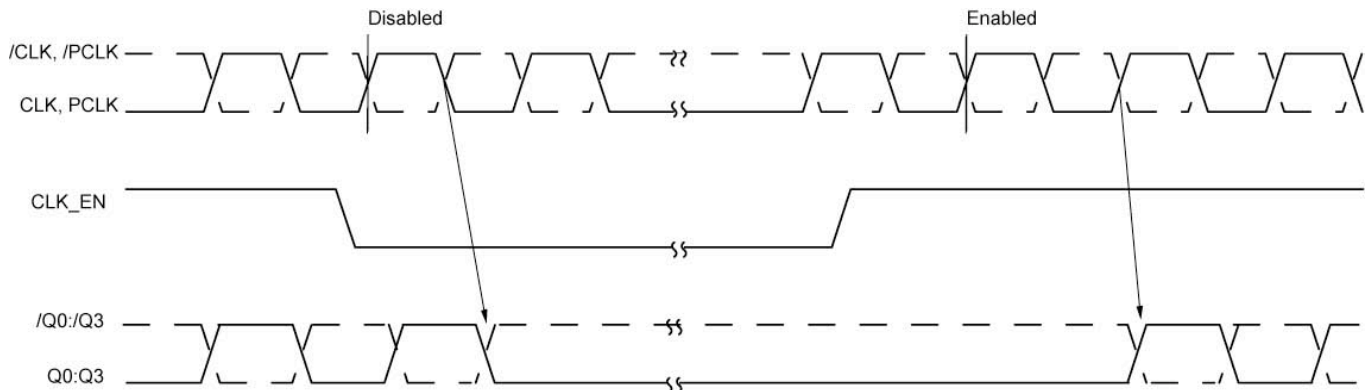


Figure 1a. CLK_EN Timing Diagram

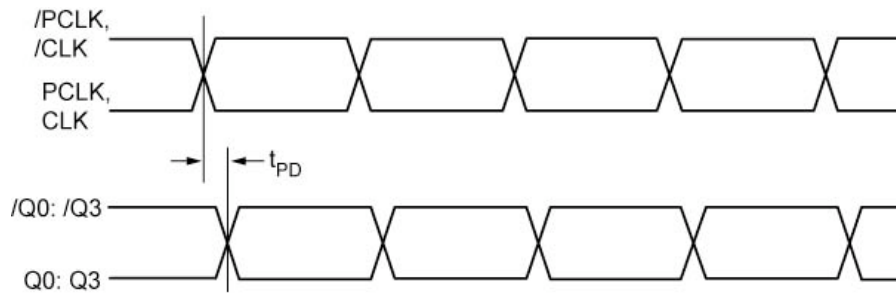


Figure 1b. Propagation Delay

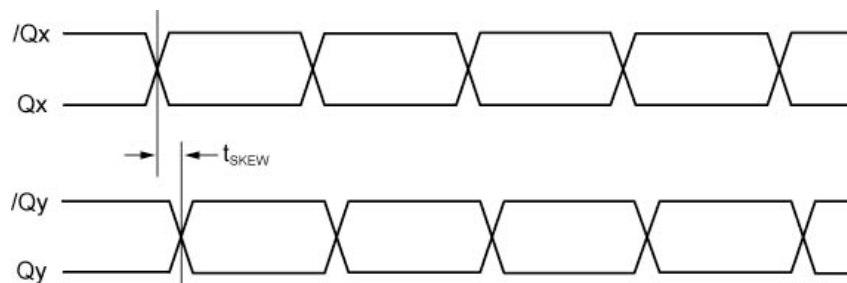
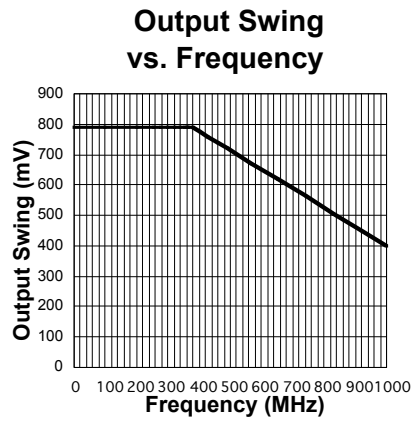


Figure 1c. Output-to-Output Skew

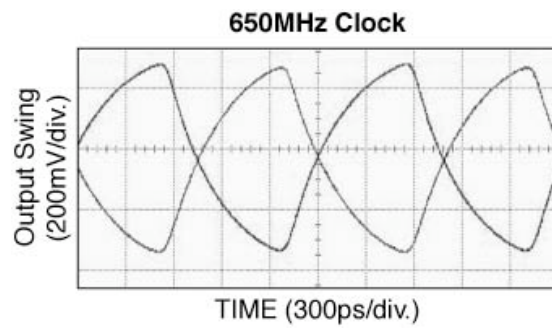
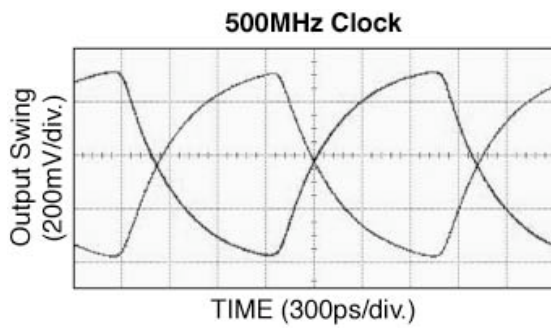
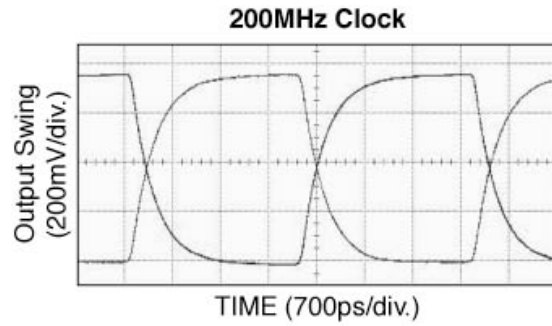
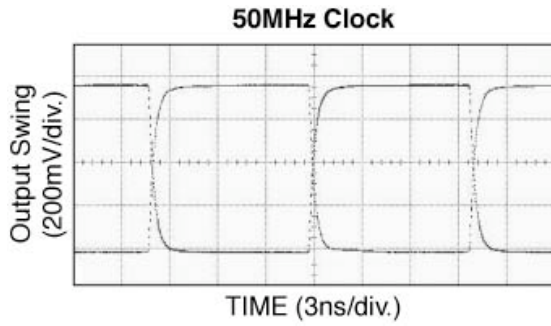
Typical Operating Characteristics

$V_{CC} = 3.3V$, $V_{EE} = 0V$, $V_{IN} = 800mV$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 3.3V$, $V_{EE} = 0V$, $V_{IN} = 800mV$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = 25^\circ C$, unless otherwise stated



CLK, /CLK Input Interface Applications

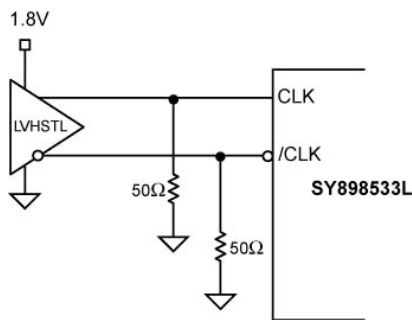


Figure 2a. LVHSTL Interface (DC-Coupled)

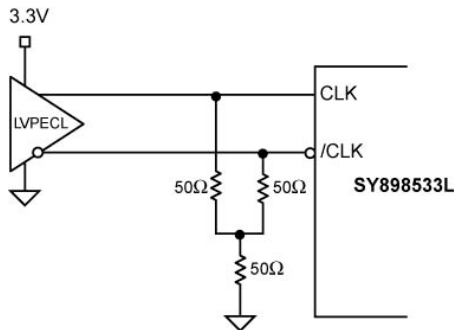


Figure 2b. LVPECL Interface (DC-Coupled)

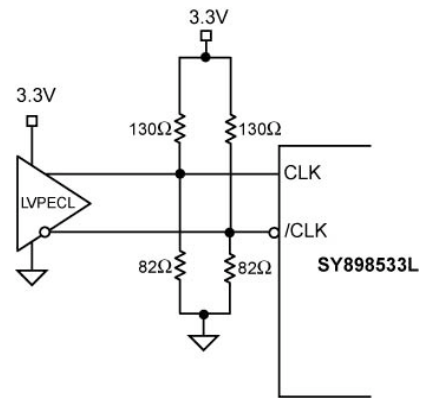


Figure 2c. LVPECL Interface (DC-Coupled)

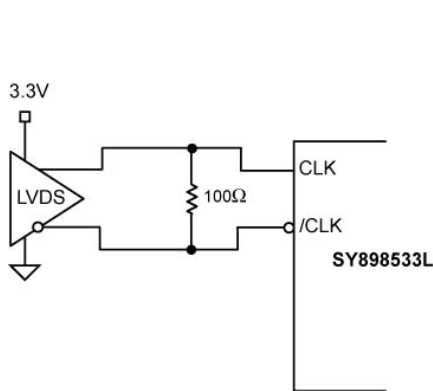


Figure 2d. LVDS Interface (DC-Coupled)

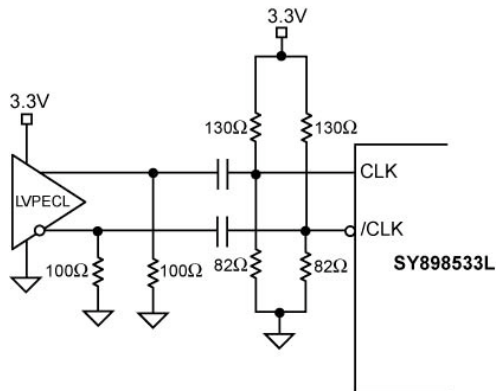


Figure 2e. LVPECL Interface (AC-Coupled)

PCLK, /PCLK Input Interface Applications

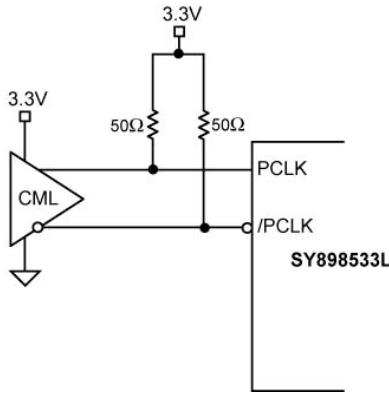


Figure 3a. CML Open Collector Interface (DC-Coupled)

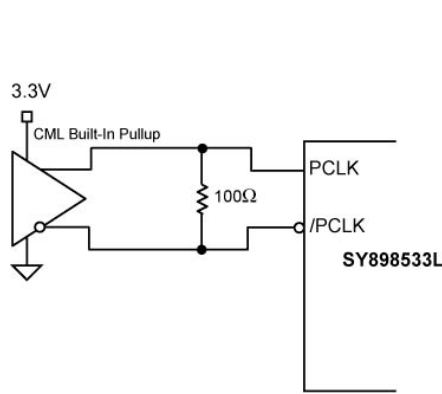


Figure 3b. CML Built-in Pull-up Interface (DC-Coupled)

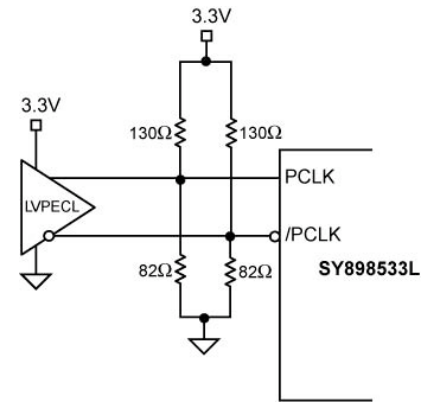


Figure 3c. LVPECL Interface (DC-Coupled)

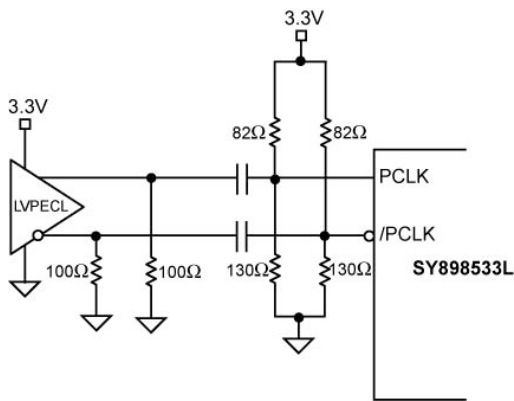


Figure 3d. LVPECL Interface (AC-Coupled)

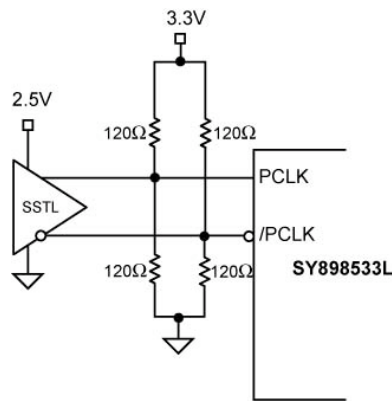


Figure 3e. SSTL Interface (DC-Coupled)

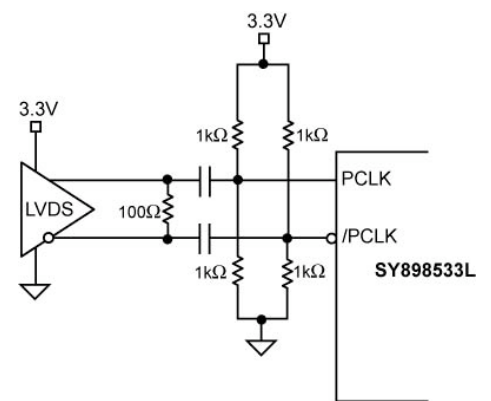
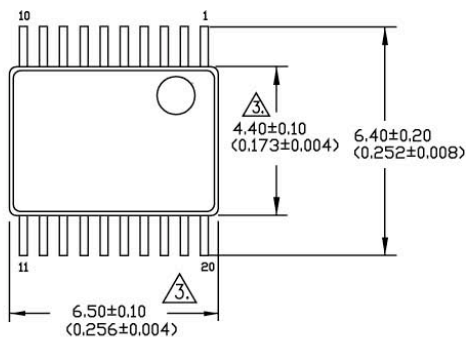
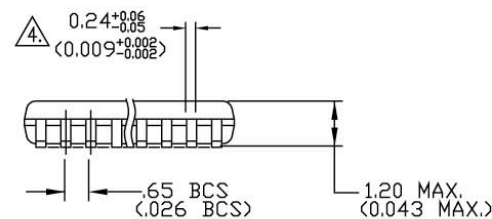


Figure 3f. LVDS Interface (AC-Coupled)

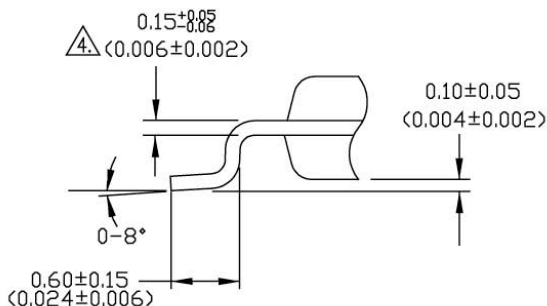
Package Information



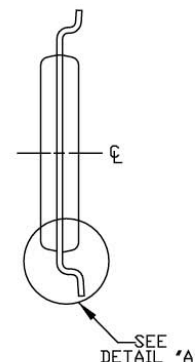
TOP VIEW



SIDE VIEW



DETAIL 'A'
(VIEW ROTATED 90° C.W.)



END VIEW

NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

20-Pin TSSOP (K4-20-1)

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