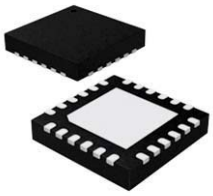
# ALED7707

## Automotive 6-row 85 mA LEDs driver with boost regulator for LCD panels backlight

**Datasheet - production data**



**QFN 5x5 - 24L**

## Features

- AEC-Q100 qualification
- Boost section
  - 4.5 V to 36 V input voltage range
  - Internal power MOSFET
  - Internal +5 V LDO for device supply
  - Up to 36 V output voltage
  - Constant frequency peak current-mode control
  - 250 kHz to 1 MHz adjustable switching frequency
  - External synchronization for multi-device application
  - Pulse skip power saving mode at light load
  - Programmable soft-start
  - Programmable OVP protection
  - Stable with ceramic output capacitors
  - Thermal shutdown
- Backlight driver section
  - Six rows with 85 mA maximum current capability (adjustable)
  - Rows disable option
  - Less than 10 µs minimum dimming on-time
  - ± 3% current matching between rows
  - LED failure (open and short-circuit) detection

## Applications

- Infotainment LCD backlight
- Daytime running lights
- Car interior/exterior lights
- Dashboard backlight

## Description

The ALED7707 device consists of an automotive grade (AEC Q100 compliant) monolithic boost converter and six controlled current generators (rows) specifically designed to supply LED arrays used in the backlighting of LCD panels. The device can manage an output voltage up to 36 V (i.e.: 10 white LEDs per row).

The generators can be externally programmed to sink up to 85 mA and can be dimmed via a PWM signal (1% dimming duty cycle at 1 kHz can be managed). The device allows the open and shorted LED faults to be detected and managed and unused rows to be let floating. Basic protections (output overvoltage, internal MOSFET overcurrent and thermal shutdown) are provided.

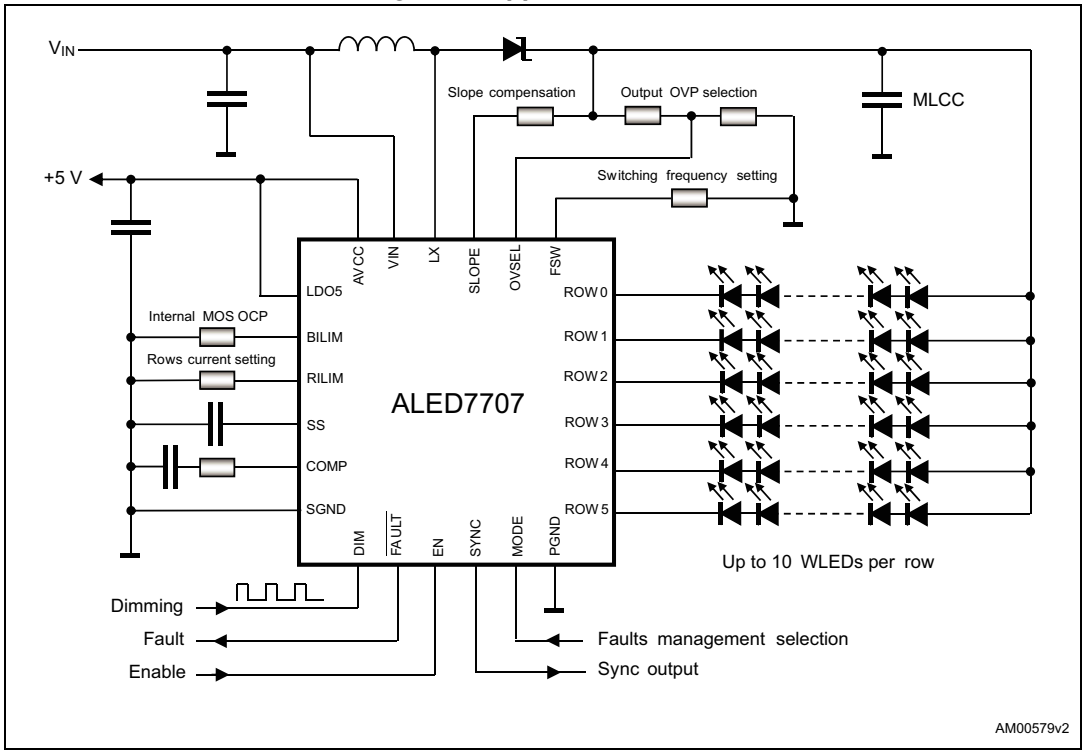
**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| ALED7707 | QFN 5x5 - 24L | Tube |
| ALED7707T | | Tape and reel |

# Contents

# 1 Typical application circuit

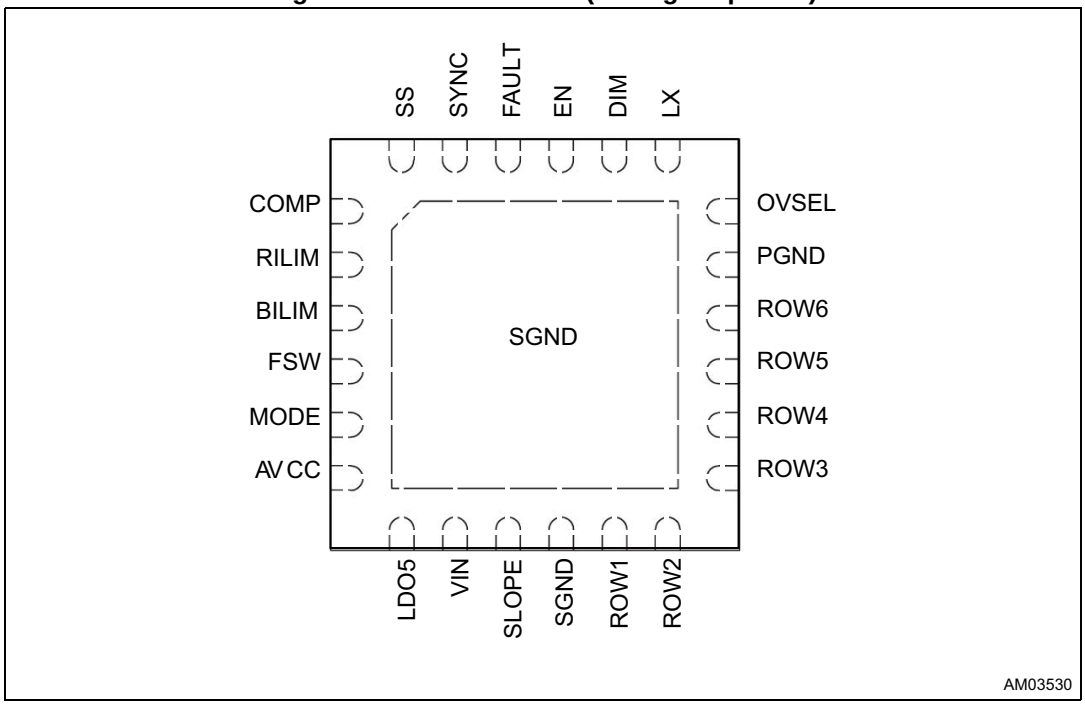
**Figure 1. Application circuit**



# 2 Pin settings

## 2.1 Connections

**Figure 2. Pin connection (through top view)**



## 2.2 Pin description

**Table 2. Pin functions**

| No. | Pin | Function |
|---|---|---|
| 1 | COMP | Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator. |
| 2 | RILIM | Output generators current limit setting. The output current of the rows can be programmed connecting a resistor to SGND. |
| 3 | BILIM | Boost converter current limit setting. The internal MOSFET current limit can be programmed connecting a resistor to SGND. |
| 4 | FSW | Switching frequency selection and external sync input. A resistor to SGND is used to set the desired switching frequency. The pin can also be used as external synchronization input. See *Section 5.1.5 on page 15* for details. |
| 5 | MODE | Current generators fault management selector. It allows LEDs failures to be detected and managed. See *Section 5.3.2 on page 21* for details. |
| 6 | AVCC | + 5 V analog supply. Connect to LDO5 through a simple RC filter. |
| 7 | LDO5 | + 5 V LDO output and power section supply. Bypass to SGND with a 1 µF ceramic capacitor. |
| 8 | VIN | Input voltage. Connect to the main supply rail. |
| 9 | SLOPE | Slope compensation setting. A resistor between the output of the boost converter and this pin is needed to avoid sub-harmonic instability. Refer to *Section 6.1 on page 25* for details. |
| 10 | SGND | Signal ground. Supply return for the analog circuitry and the current generators. |
| 11 | ROW1 | Row driver output #1. |
| 12 | ROW2 | Row driver output #2. |
| 13 | ROW3 | Row driver output #3. |
| 14 | ROW4 | Row driver output #4. |
| 15 | ROW5 | Row driver output #5. |
| 16 | ROW6 | Row driver output #6. |
| 17 | PGND | Power ground. Source of the internal power MOSFET. |
| 18 | OVSEL | Overvoltage selection. Used to set the desired 0 V threshold by an external divider. See *Section 5.1.4 on page 14* for details. |
| 19 | LX | Switching node. Drain of the internal power MOSFET. |
| 20 | DIM | Dimming input. Used to externally set the brightness by using a PWM signal. |
| 21 | EN | Enable input. When low, the device is turned off. If tied high or left open, the device is turned on and a soft-start sequence takes place. |
| 22 | FAULT | Fault signal output. Open drain output. The pin goes low when a fault condition is detected (see *Section 5.3.1 on page 21* for details). |
| 23 | SYNC | Synchronization output. Used as external synchronization output. |
| 24 | SS | Soft-start. Connect a capacitor to SGND to set the desired soft-start duration. |
| 25 | TPAD | Thermal pad. Electrically connected to SGND. Do not leave floating. |

# 3 Electrical data

## 3.1 Maximum ratings

**Table 3. Absolute maximum ratings(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{AVCC}$ | AVCC to SGND | -0.3 to 6 | V |
| $V_{LDO5}$ | LDO5 to SGND | -0.3 to 6 | |
| | PGND to SGND | -0.3 to 0.3 | |
| $V_{IN}$ | VIN to PGND | -0.3 to 40 | |
| $V_{LX}$ | LX to SGND | -0.3 to 40 | |
| | LX to PGND | -0.3 to 40 | |
| | RILIM, BILIM, SYNC, OVSEL, SS to SGND | -0.3 to $V_{AVCC}$ + 0.3 | |
| | EN, DIM, SW, MODE, FAULT to SGND | -0.3 to 6 | |
| | ROWx to PGND/ SGND | -0.3 to 40 | |
| | SLOPE to VIN | $V_{IN}$ - 0.3 to $V_{IN}$ + 6 | |
| | SLOPE to SGND | -0.3 to 40 | |
| | Internal switch maximum RMS current (flowing through LX node) | 2.0 | A |
| $P_{TOT}$ | Power dissipation at $T_A$ = 25 °C | 2.3(2) | W |
| | Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”. | ± 2000 | V |

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. Power dissipation referred to the device mounted on a standard JESD51-5 test board.

## 3.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction-to-ambient | 35 | °C/W |
| $T_{STG}$ | Storage temperature range | -50 to 150 | °C |
| $T_J$ | Junction operating temperature range | -40 to 150 | °C |

# 4 Electrical characteristics

$V_{IN}$ = 12 V, AVCC connected to LDO5 and $T_J$ = -40 °C to 125 °C if not otherwise specified.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply section** | | | | | | |
| $V_{IN}$ | Input voltage range | | 4.5 | | 36 | V |
| $V_{LDO5}$ | LDO output and IC supply | EN high | 4.5 | 5 | 5.5 | V |
| $V_{AVCC}$ | voltage | | | | | |
| $I_{IN,Q}$ | Operating quiescent current | $R_{RILIM}$ = 51 kΩ, $R_{BILIM}$ = 220 kΩ, $R_{SLOPE}$ = 680 kΩ DIM tied to SGND | | 1 | 2.8 | mA |
| $I_{IN,SHDN}$ | Operating current in shutdown | EN low | | 20 | 30 | µA |
| $V_{UVLO,ON}$ | LDO5 under voltage lockout upper threshold | | 3.7 | 4.0 | 4.4 | V |
| $V_{UVLO,HYST}$ | LDO5 under voltage lockout hysteresis | | 0.24 | 0.3 | 0.46 | |
| **LDO linear regulator** | | | | | | |
| | Line regulation | 6 V ≤ $V_{IN}$ ≤ 36 V, $I_{LDO5}$ = 30 mA | | 10 | 30 | mV |
| | LDO dropout voltage | $I_{LDO5}$ = 10 mA (-10% drop) | | 80 | 120 | |
| | LDO maximum output current | $V_{LDO5}$ > $V_{UVLO,ON}$ | 25 | 40 | 60 | mA |
| | | $V_{LDO5}$ < $V_{UVLO,OFF}$ | 11 | 20 | 36 | |
| **Boost section** | | | | | | |
| $t_{ON,min}$ | Minimum switching on-time | | | 130 | 200 | ns |
| $f_{SW}$ | Default switching frequency | FSW connected to AVCC | 550 | 660 | 750 | kHz |
| | Minimum FSW sync frequency | | | 220 | | |
| | FSW sync frequency range(1) | FSW sync signal: 200 mV to 400 mV, 270 ns pulse duration | 200 | | 1000 | |
| | SYNC output duty cycle | FSW connected to AVCC (internal oscillator selected) | 28 | 34 | 40 | % |
| | SYNC output high level | $I_{SYNC}$ = 10 µA | $V_{AVCC}$ -20 | | | mV |
| | SYNC output low level | $I_{SYNC}$ = -10 µA | | | 20 | |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power switch** | | | | | | |
| $K_B$ | LX current coefficient | $R_{BILIM}$ = 600 kΩ | $1 \cdot 10^6$ | $1.2 \cdot 10^6$ | $1.45 \cdot 10^6$ | V |
| $R_{DS(on)}$ | Internal MOSFET on-resistance | | | 280 | 570 | mΩ |
| **OC and OV protections** | | | | | | |
| $V_{TH,OVP}$ | Overvoltage protection reference threshold | | 1.1 | 1.145 | 1.2 | V |
| **Soft-start and power management** | | | | | | |
| | EN, turn-on threshold | | 1.6 | | | V |
| | EN, turn-off threshold | | | | 0.8 | |
| | DIM, high level threshold | | 1.3 | | | |
| | DIM, low level threshold | | | | 0.8 | |
| | EN, pull-up current | | 1.5 | 2.5 | 3.8 | µA |
| | SS, charge current | | 3.5 | 5 | 6 | |
| | SS, end-of-startup threshold | | 2.0 | 2.4 | 2.7 | V |
| | SS, reduced switching frequency release threshold | | 0.6 | 0.8 | 1.0 | |
| **Current generators section** | | | | | | |
| $K_R$ | Current generators gain | | 1776 | 1850 | 1924 | V |
| $\Delta K_R$(2) | Current generators gain accuracy | | | 3 | 4 | % |
| $V_{IFB}$ | Feedback regulation voltage | | | 700 | 830 | mV |
| $V_{rowx, FAULT}$ | LED short-circuit detection threshold | MODE tied to SGND | 3.5 | 3.8 | 4.2 | V |
| $V_{FAULT, LOW}$ | FAULT pin low level voltage | $I_{FAULT,SINK}$ = 4 mA | | 250 | 400 | mV |
| **Thermal shutdown** | | | | | | |
| $T_{SHDN}$ | Thermal shutdown turn-off temperature | | | 150 | | °C |
| | Thermal shutdown hysteresis | | | 30 | | |

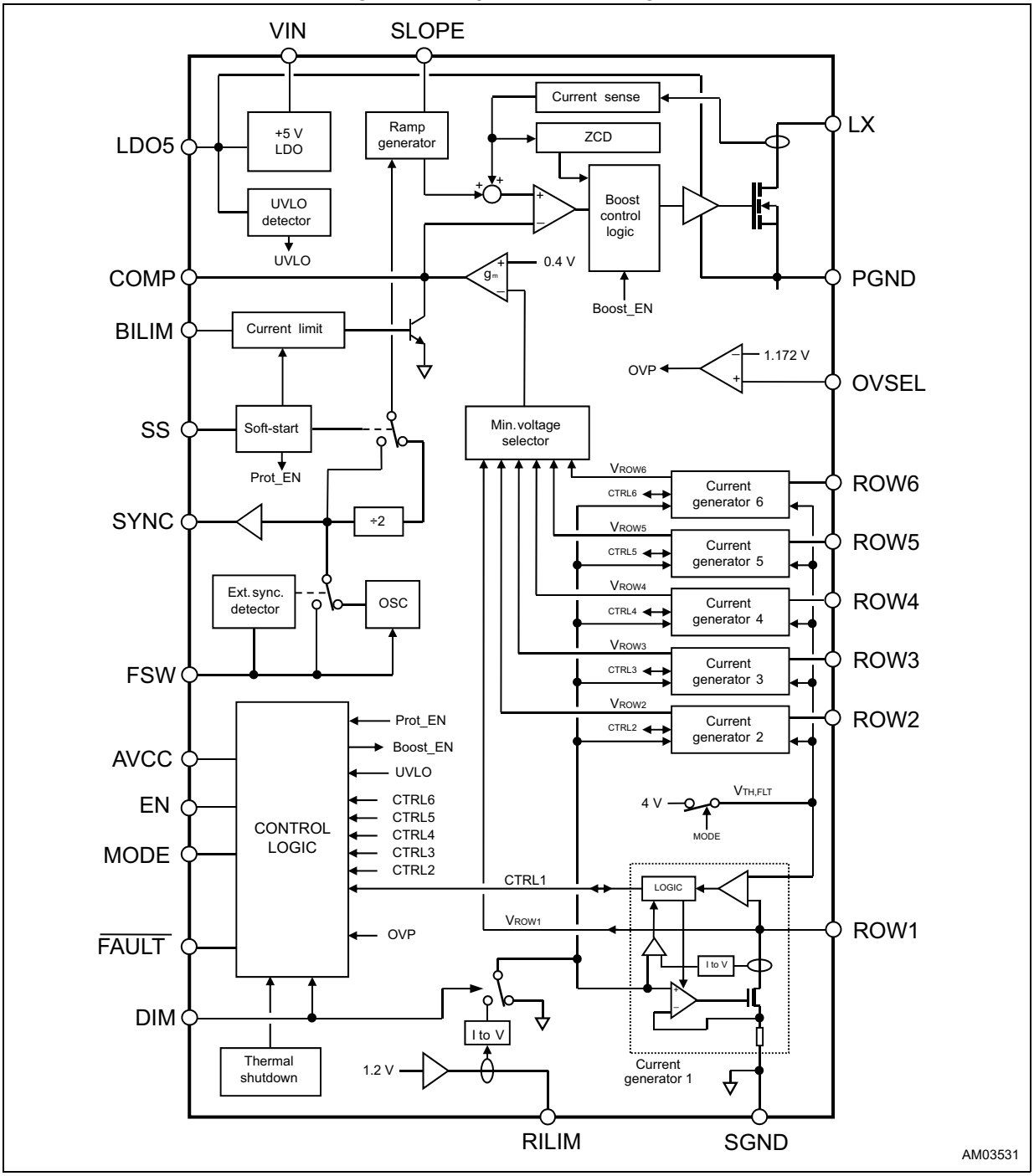
1. Tested at $T_A$ = 25 °C.
2. $I_{ROW} = K_R / R_{RILIM}$, $\Delta I_{ROW} / I_{ROW} \approx \Delta K_R / K_R + \Delta R_{RILIM} / R_{RILIM}$.

# 5 Operation description

The device can be divided into two sections: the boost section and the backlight driver section. These sections are described in the next paragraphs.

*Figure 3* provides an overview of the internal blocks of the device.

**Figure 3. Simplified block diagram**



## 5.1 Boost section

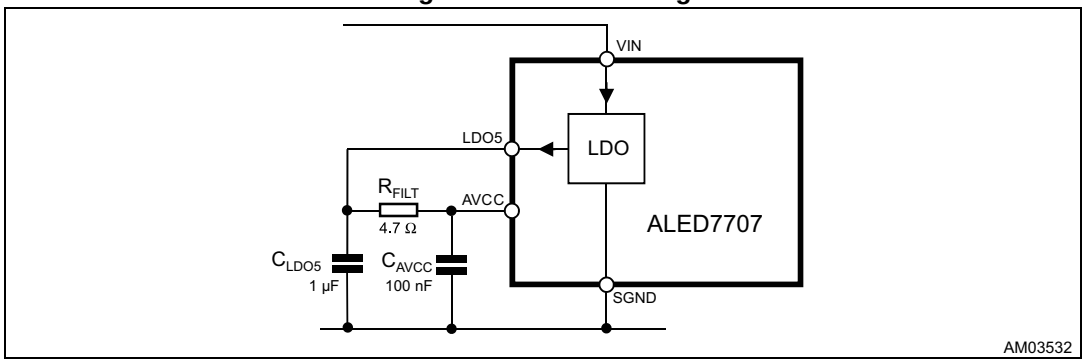
### 5.1.1 Functional description

The ALED7707 device is a monolithic LED driver for the backlight of LCD panels and it consists of a boost converter and six PWM-dimmable current generators.

The boost section is based on a constant switching frequency, peak current-mode architecture. The boost output voltage is controlled such that the lowest row's voltage, referred to SGND, is equal to an internal reference voltage (700 mV typ.). The input voltage range is from 4.5 V up to 36 V. In addition, the ALED7707 has an internal LDO that supplies the internal circuitry of the device and is capable to deliver up to 40 mA. The input of the LDO is the VIN pin.

The LDO5 pin is the LDO output and the supply for the power MOSFET driver at the same time. The AVCC pin is the supply for the analog circuitry and should be connected to the LDO output through a simple RC filter in order to improve the noise rejection.

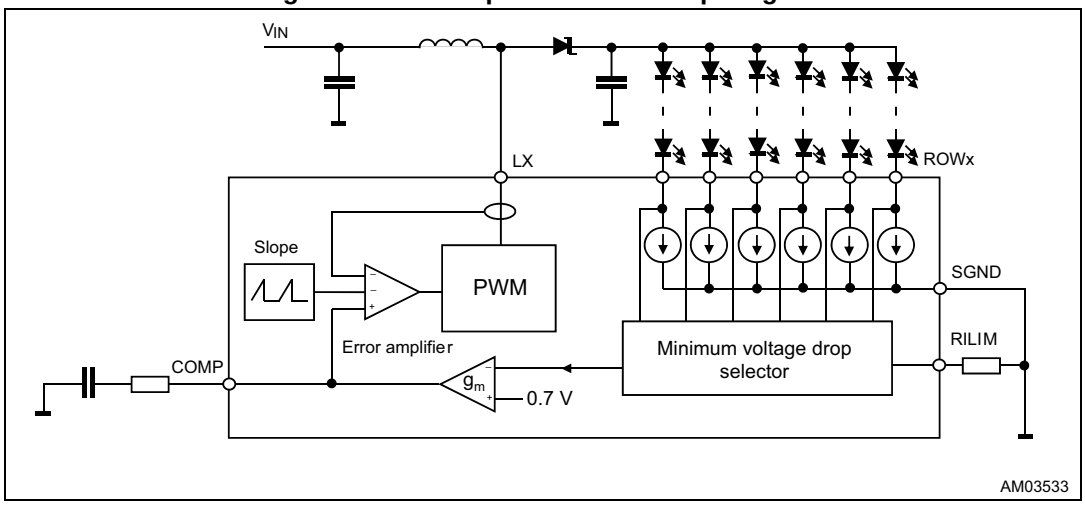
**Figure 4. AVCC filtering**




Two loops are involved in regulating the current sunk by the generators.

The main loop is related to the boost regulator and uses a constant frequency peak current-mode architecture to regulate the power rail that supplies the LEDs (*Figure 5*), while an internal current loop regulates the same current (flowing through the LEDs) at each row according to the set value (RILIM pin).

**Figure 5. Main loop and current loop diagram**



A dedicated circuit automatically selects the lowest voltage drop among all the rows and provides this voltage to the main loop that, in turn, regulates the output voltage. In fact, once the reference generator has been detected, the error amplifier compares its voltage drop to the internal reference voltage and varies the COMP output. The voltage at the COMP pin determines the inductor peak current at each switching cycle. The output voltage of the boost regulator is thus determined by the total forward voltage of the LED strings (see *Figure 6*):

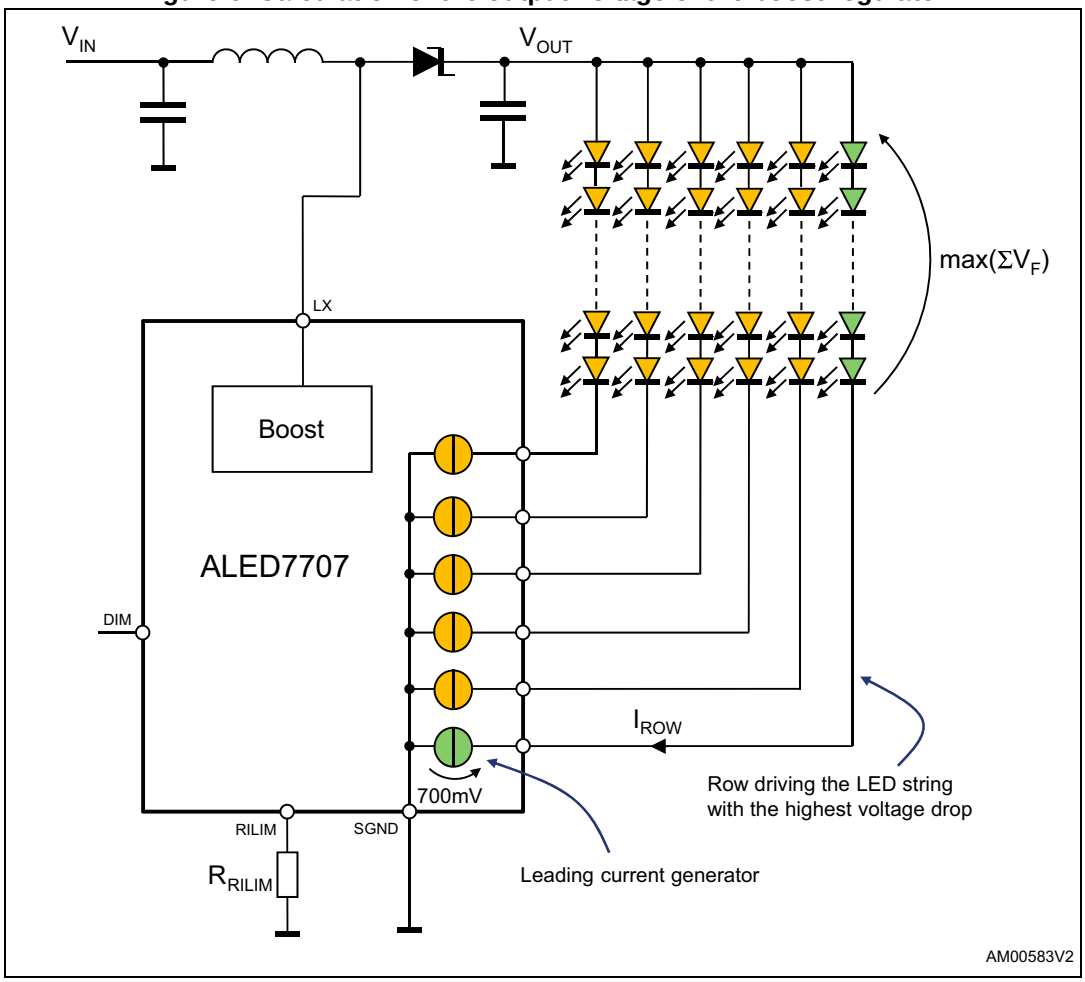
**Equation 1**

$$V_{OUT} = \max_{i=1}^{N_{ROWS}} \left( \sum_{j=1}^{m_{LEDS}} V_{F,j} \right) + 700mV$$

where the first term represents the highest total forward voltage drop over N active rows and the second is the voltage drop across the leading generator (700 mV typ.).

The device continues to monitor the voltage drop across all the rows and automatically switches to the current generator having the lowest voltage drop.

**Figure 6. Calculation of the output voltage of the boost regulator**



### 5.1.2 Enable function

The ALED7707 device is enabled by the EN pin. This pin is active high and, when forced to SGND, the device is turned off. This pin is connected to a permanently active 2.5 µA current source; when sudden device turn-on at power-up is required, this pin must be left floating or connected to a delay capacitor. Starting from an ON state, when the ALED7707 is turned off, it quickly discharges the soft-start capacitor and turns off the power MOSFET, the current generators and the LDO. The power consumption is thus reduced to 20 µA only.

The correct sequence to turn-on the device is the following:

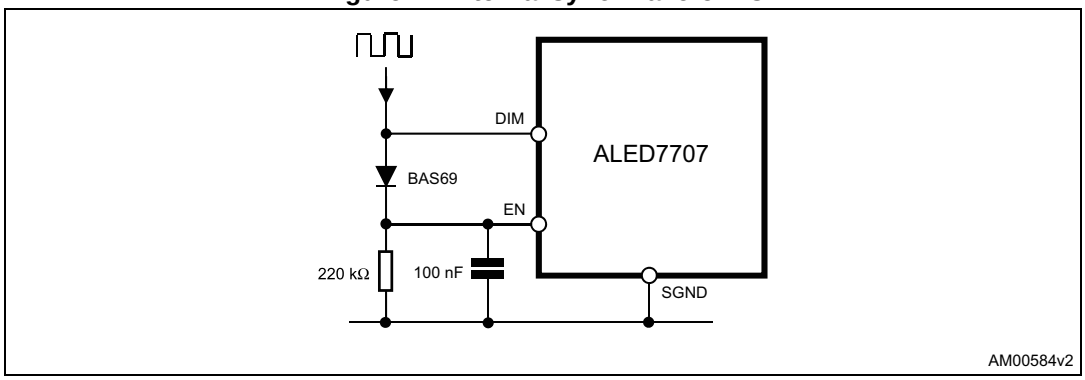
1. Applying the input voltage with the EN and DIM pins low
2. Applying the PWM signal to the DIM pin
3. Setting high the EN pin

Applying the PWM signal to the DIM pin after the EN pin has been asserted could lead to excessive inrush current, especially if the output capacitors are allowed to discharge.

The above sequence ensures that the soft-start is properly executed.

In applications where the dimming signal is used to turn on and off the device, the EN pin can be connected to the DIM pin as shown in *Figure 7*.

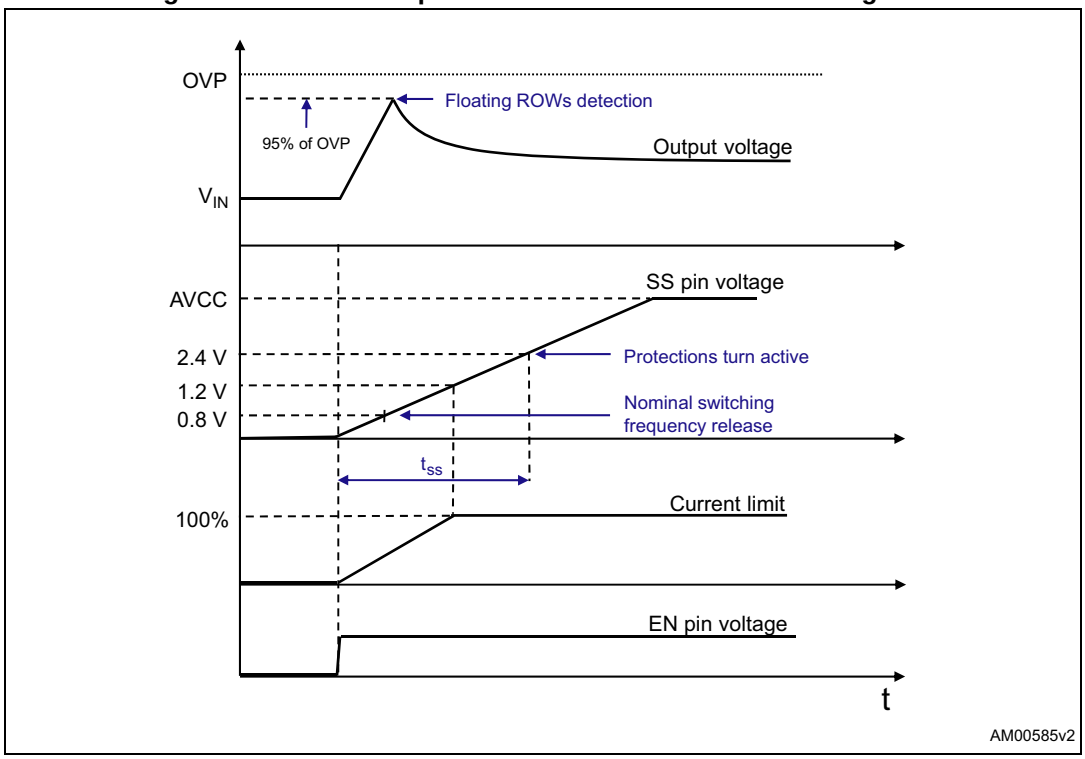
**Figure 7. External sync. waveforms**




### 5.1.3 Soft-start

The soft-start function is required to perform a correct start-up of the system, controlling the inrush current required to charge the output capacitor and to avoid output voltage overshoot. The soft-start duration is set connecting an external capacitor between the SS pin and ground. This capacitor is charged with a 5 µA (typ.) constant current, forcing the voltage on the SS pin to ramp up. When this voltage increases from zero to nearly 1.2 V, the current limit of the power MOSFET is proportionally released from zero to its final value. However, because of the limited minimum on-time of the switching section, the inductor might saturate due to current runaway. To solve this problem the switching frequency is reduced to one half of the nominal value at the beginning of the soft-start phase. The nominal switching frequency is restored after the SS pin voltage has crossed 0.8 V.

**Figure 8. Soft-start sequence waveforms in case of floating rows**




During the soft-start phase the floating rows detection is also performed. In presence of one or more floating rows, the voltage across the involved current generator drops to zero. This voltage becomes the inverting input of the error amplifier through the minimum voltage drop selector (see *Figure 5*). As a consequence the error amplifier is unbalanced and the loop reacts by increasing the output voltage. When it reaches the floating row detection (FRD) threshold (which coincides with the OVP threshold, see *Section 5.1.4*, the floating rows are managed according to *Table 6* (see *Section 5.3 on page 21*). After the SS voltage reaches a 2.4 V threshold, the start-up finishes and all the protections turn active. The soft-start capacitor Css can be calculated according to *Equation 2*.

**Equation 2**

$$C_{SS} \cong \frac{I_{SS} \cdot t_{SS}}{2.4}$$

Where *Iss* = 5 µA and $t_{SS}$ is the desired soft-start duration.

### 5.1.4 Overvoltage protection

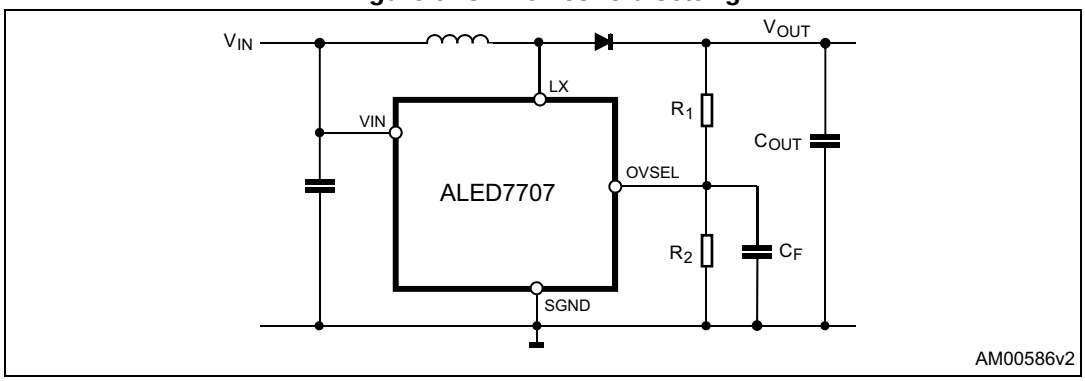
An adjustable overvoltage protection is available. It can be set feeding the OVSEL pin with a partition of the output voltage. The voltage of the central tap of the divider is thus compared to a fixed 1.145 V threshold. When the voltage of the OVSEL pin exceeds the OV threshold, the switching activity is suspended. It is resumed as OVSEL returns below the OV threshold. A 10 mV hysteresis is provided. No device turn-off is performed. Normally, the value of the high-side resistors of the divider is in the order of 100 kΩ to reduce the output capacitor discharge when the boost converter is off (during the off phase of the dimming cycle), whereas the low-side resistor can be calculated as:

**Equation 3**

$$R_2 = R_1 \cdot \frac{1.145V}{V_{OUT,MAX} + 4V - 1.145V}$$

An additional filtering capacitor $C_F$ (typically in the 100 pF - 330 pF range) may be required to improve noise rejection at the OVSEL pin (see *Figure 9*).

**Figure 9. OVP threshold setting**




## 5.1.5 Switching frequency selection and synchronization

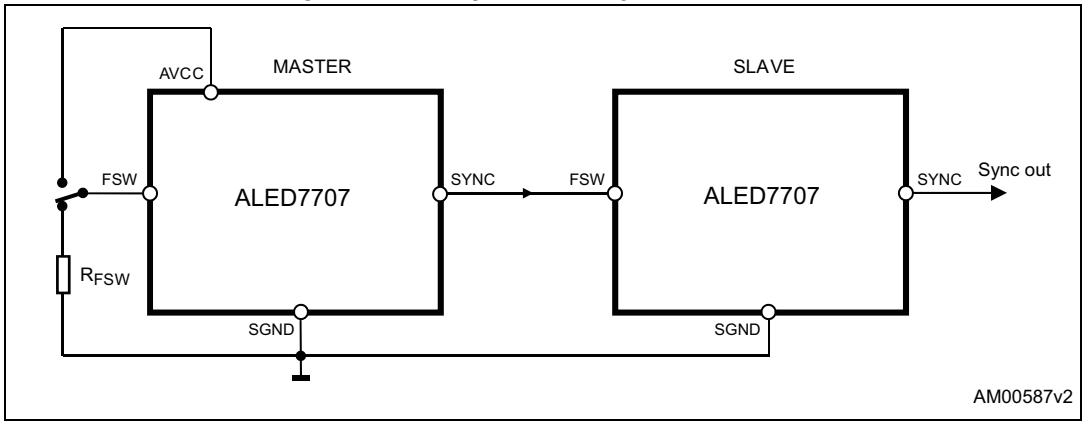
The switching frequency of the boost converter can be set in the 250 kHz - 1 MHz range by connecting the FSW pin to ground through a resistor. Calculation of the setting resistor is made using *Equation 4* and should not exceed the 100 kΩ - 400 kΩ range.

**Equation 4**

$$R_{FSW} = \frac{F_{SW}}{2.5}$$

In addition, when the FSW pin is tied to AVCC, the ALED7707 uses a default 660 kHz fixed switching frequency, allowing a resistor to be saved in minimum component-count applications.

**Figure 10. Multiple device synchronization**



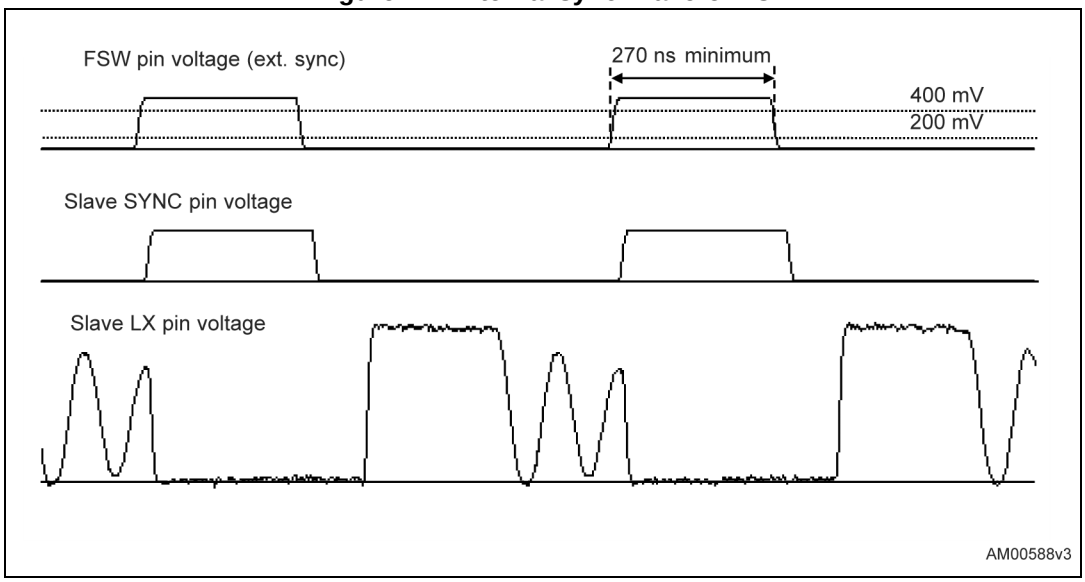

The FSW pin can also be used as synchronization input, allowing the ALED7707 to operate both as master or slave device. If a clock signal with a 220 kHz minimum frequency is applied

to this pin, the device locks synchronized. The signal provided to the FSW pin must cross the 200 mV (lower) and 400 mV (upper) thresholds in order to be recognized. The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns. An internal time-out allows synchronization as long as the external clock frequency is greater than 220 kHz.

Keeping the FSW pin voltage lower than 200 mV for more than 4.5 µs results in a stop of the device switching activity. Normal operation is resumed as soon as FSW rises above the mentioned threshold and the soft-start sequence is repeated.

The SYNC pin is a synchronization output and provides a 35% (typ.) duty cycle clock when the ALED7707 is used as master or a replica of the FSW pin when used as slave. It is used to connect multiple devices in a daisy-chain configuration or to synchronize other switching converters running in the system with the ALED7707 (master operation). When an external synchronization clock is applied to the FSW pin, the internal oscillator is overdriven: each switching cycle begins at the rising edge of clock, while the slope compensation (*Figure 11*) ramp starts at the falling edge of the same signal. Thus, to prevent sub-harmonic instability (see *Section 5.1.6*), the external synchronization clock is required to have a 40% maximum duty cycle when the boost converter is working in continuous-conduction mode (CCM) in order to assure that the slope compensation is effective (starts with duty cycle lower than 40%).

**Figure 11. External sync. waveforms**




## 5.1.6 Slope compensation

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor.

On the other side, this topology has a drawback: there is an inherent open loop instability when operating with a duty-ratio greater than 0.5. This phenomenon is known as “Sub-Harmonic Instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”.

In *Figure 12*, where the switching duty cycle is higher than 0.5, the small perturbation $\Delta I_L$ dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.

The SLOPE pin allows the amount of slope compensation to be properly set connecting a simple resistor $R_{SLOPE}$ between the SLOPE pin and the output. The compensation ramp starts at 35% (typ.) of each switching period and its slope is given by *Equation 5*:

**Equation 5**

$$S_E = K_S\left(\frac{V_{OUT} - V_{IN} - V_{BE}}{R_{SLOPE}}\right)$$

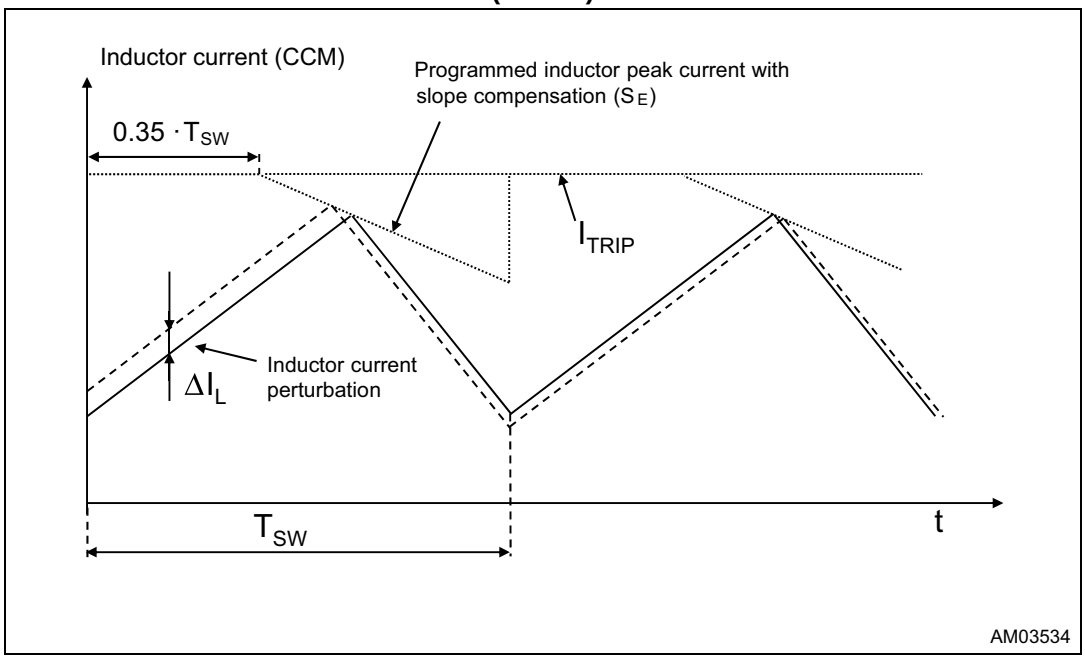
Where $K_S$ = 5.8 ·10$^{10}$ s$^{-1}$, $V_{BE}$ = 2 V (typ.) and $S_E$ is the slope ramp in [A/s].

To avoid sub-harmonic instability, the compensating slope should be at least half the slope of the inductor current during the off phase when the duty cycle is greater than 50%. The value of $R_{SLOPE}$ can be calculated according to *Equation 6*.

**Equation 6**

$$R_{SLOPE} \le \frac{2 \cdot K_S \cdot L \cdot (V_{OUT} - V_{IN} - V_{BE})}{(V_{OUT} - V_{IN})}$$

**Figure 12. Effect of slope compensation on small inductor current perturbation (D > 0.5)**



### 5.1.7 Boost current limit

The design of the external components, especially the inductor and the flywheel diode, must be optimized in terms of size relying on the programmable peak current limit. The ALED7707 improves the reliability of the final application giving the way to limit the maximum current flowing into the critical components. A simple resistor connected between the BILIM pin and ground sets the desired value. The voltage at the BILIM pin is internally fixed to 1.23 V and the current limit is proportional to the current flowing through the setting resistor, according to *Equation 7*:

**Equation 7**

$$I_{BOOST,PEAK} = \frac{K_B}{R_{BILIM}}$$

where

$$K = 1.2 \cdot 10^6 V$$

The maximum allowed current limit is 5 A, resulting in a minimum setting resistor $R_{BILIM} > 240\ k\Omega$. The maximum guaranteed RMS current in the power switch is 2 A.

In a boost converter the RMS current through the internal MOSFET depends on both the input and output voltages, according to *Equation 8*a (DCM) and *Equation 8*b (CCM).

The current limitation works by clamping the COMP pin voltage proportionally to $R_{BILIM}$. Peak inductor current is limited to the above threshold decreased by the slope compensation contribution.

**Equation 8a**

$$I_{MOS,rms} = \frac{V_{IN} \cdot D}{F_{SW} \cdot L}\sqrt{\frac{D}{3}}$$

**Equation 8b**

$$I_{MOS,rms} = I_{OUT}\sqrt{\left(\frac{D}{(1-D)^2} + \frac{1}{12}\left(\frac{V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot L}\right)^2 (D(1-D))^3\right)}$$

### 5.1.8 Thermal protection

In order to avoid damage due to high junction temperature, a thermal shutdown protection is implemented. When the junction temperature rises above 150 °C (typ.), the device turns off both the control logic and the boost converter and holds the FAULT pin low. The LDO is kept alive and normal operation is automatically resumed after the junction temperature has been reduced by 30 °C.

## 5.2 Backlight driver section

### 5.2.1 Current generators

The ALED7707 is a LEDs driver with six channels (rows); each row is able to drive multiple LEDs in series (max. 36 V) and to sink up to 85 mA maximum current, allowing different kinds of LEDs. to be managed.

The LEDs current can be set by connecting an external resistor ($R_{RILIM}$) between the RILIM pin and ground. The voltage across the RILIM pin is internally set to 1.23 V and the rows current is proportional to the RILIM current according to *Equation 9*:

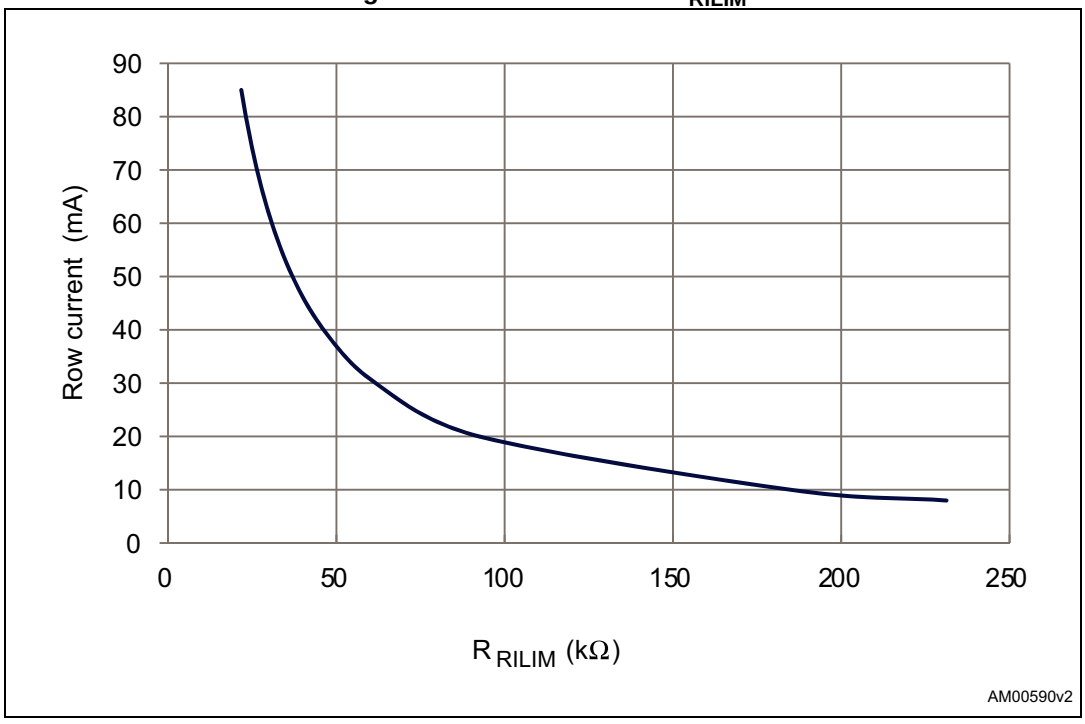
**Equation 9**

$$I_{ROWx} = \frac{K_R}{R_{RILIM}}$$

Where $K_R$ = 1850 V.

The graph in *Figure 13* better shows the relationship between $I_{ROW}$ and $R_{RILIM}$ and helps to choose the correct value of the resistor to set the desired row current.

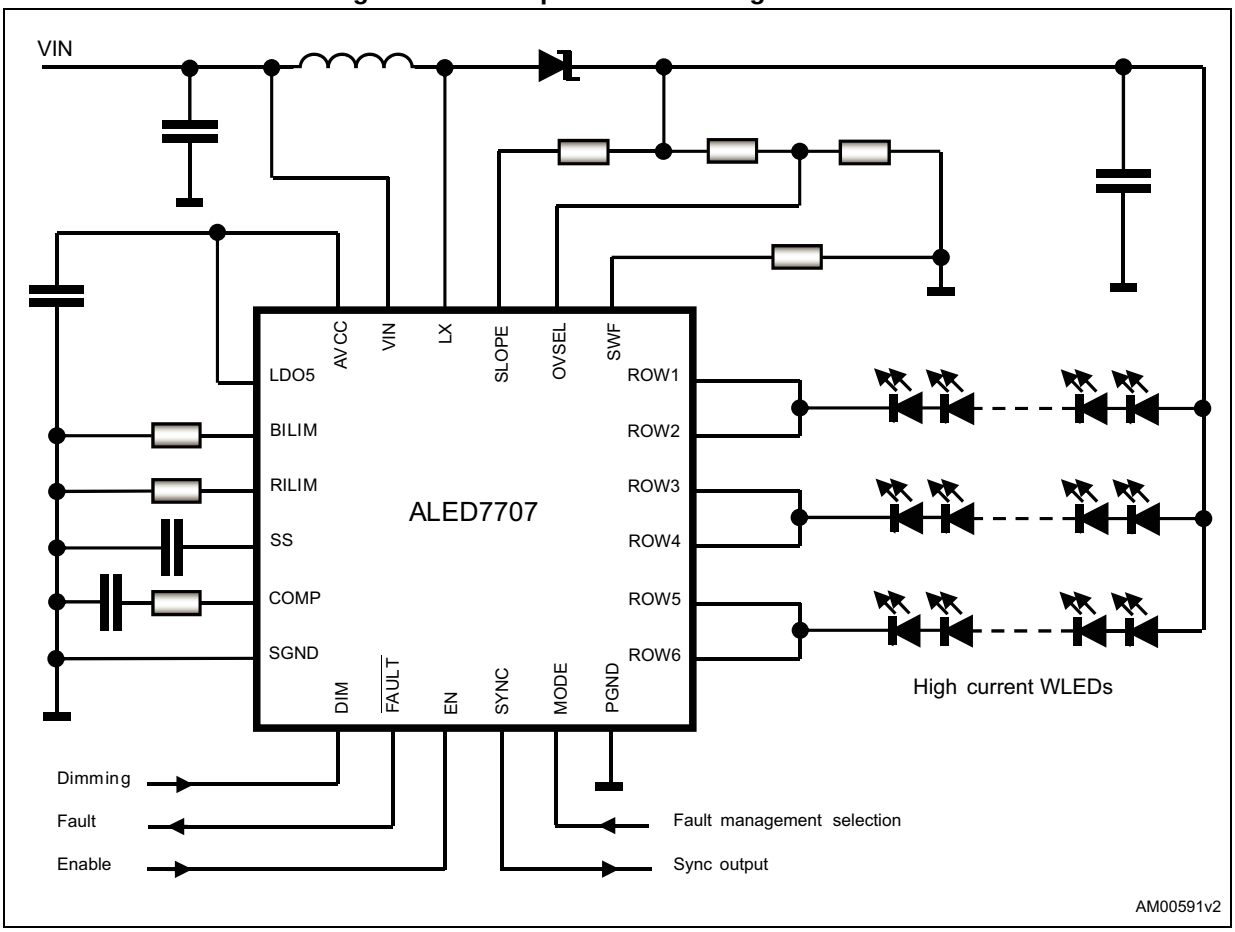
**Figure 13. Row current vs $R_{RILIM}$**




The maximum current mismatch between the rows is ± 4% at $I_{rowx}$ = 60 mA.

The ALED7707 allows parallelism different rows if required by the application. If the maximum current provided by a single row (85 mA) is not enough for the load, two or more current generators can be connected together, as shown in *Figure 14*. To keep the parallelism generators stable, the row current should be higher than 10 mA. The connection between channels in parallel must be done as close as possible to the device in order to minimize parasitic inductance.

**Figure 14. Rows parallelism for higher current**




## 5.2.2 PWM dimming

The brightness control of the LEDs is performed by a pulse width modulation of the rows current. When a PWM signal is applied to the DIM pin, the current generators are turned on and off mirroring the DIM pin behavior. Actually, the minimum dimming duty cycle depends on the dimming frequency.

The PWM dimming ratio is limited by the minimum conduction time of the current generators in closed loop operation. A 10 µs minimum on-time is suggested for proper device operation assuming $I_{ROWs}$ = 20 mA, otherwise a higher dimming ratio may be required.

Thus, the minimum dimming duty cycle depends on the dimming frequency according to *Equation 10*:

**Equation 10**

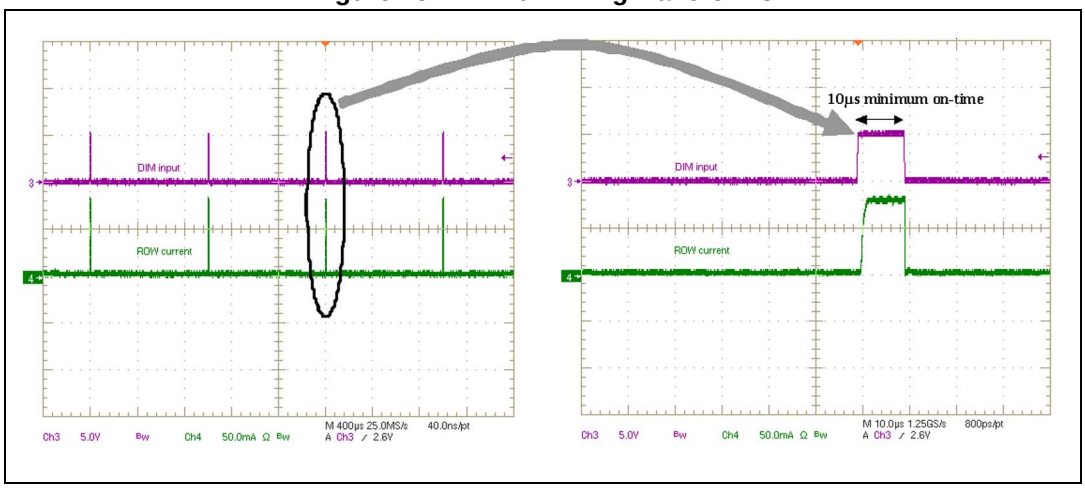
$$D_{DIM,min} = 10\mu s \cdot f_{DIM}$$

For example, at a dimming frequency of 1 kHz, 1% of dimming duty cycle can be managed.

During the off phase of the PWM signal the boost converter is paused and the current generators are turned off. The output voltage can be considered almost constant because of the relatively slow discharge of the output capacitor. During the start-up sequence (see *Section 5.1.3 on page 13*) the dimming duty cycle is forced to 100% to detect floating rows

regardless of the applied dimming signal.

**Figure 15. PWM dimming waveforms**




## 5.3 Fault management

The main loop keeps the row having the lowest voltage drop regulated to about 700 mV. This value slightly depends on the voltage across the remaining active rows. After the soft- start sequence, all protections turn active and the voltage across the active current generators is monitored to detect shorted LEDs.

### 5.3.1 FAULT pin

The FAULT pin is an open-collector output, (with 4 mA current capability) active low, which gives information regarding faulty conditions eventually detected. This pin can be used either to drive a status LED or to warn the host system.

The FAULT pin status is strictly related to the MODE pin setting (see *Table 6* for details).

### 5.3.2 MODE pin

The MODE pin is a digital input and can be connected to AVCC or SGND in order to choose the desired fault detection and management. The ALED7707 can manage a faulty condition in two different ways, according to the application needs. *Table 6* summarizes how the device detects and handles the internal protections related to the boost section (overcurrent, overtemperature and overvoltage) and to the current generators section (open and shorted LEDs).

**Table 6. Fault management summary**

| FAULT | MODE to GND | MODE to VCC |
|---|---|---|
| **Internal MOSFET overcurrent** | FAULT pin HIGH<br>Power MOS turned OFF | |
| **Output overvoltage** | FAULT pin low. Automatic restart after the voltage at the OVSEL pin has dropped below the OVP lower threshold. The FAULT pin is released as soon as the normal operation is resumed. | |
| **Thermal shutdown** | FAULT pin LOW. device turned OFF.<br>Automatic restart after 30 ºC temperature drop. | |
| **LED short-circuit** | FAULT pin LOW, device turned OFF (100 s masking time), latched condition (Vth = 4.0 V) | - |
| **Open row(s)** | FAULT pin LOW<br>Device turned OFF at first occurrence, latched condition | FAULT pin HIGH faulty row(s) disconnected |

### 5.3.3 Open LED fault

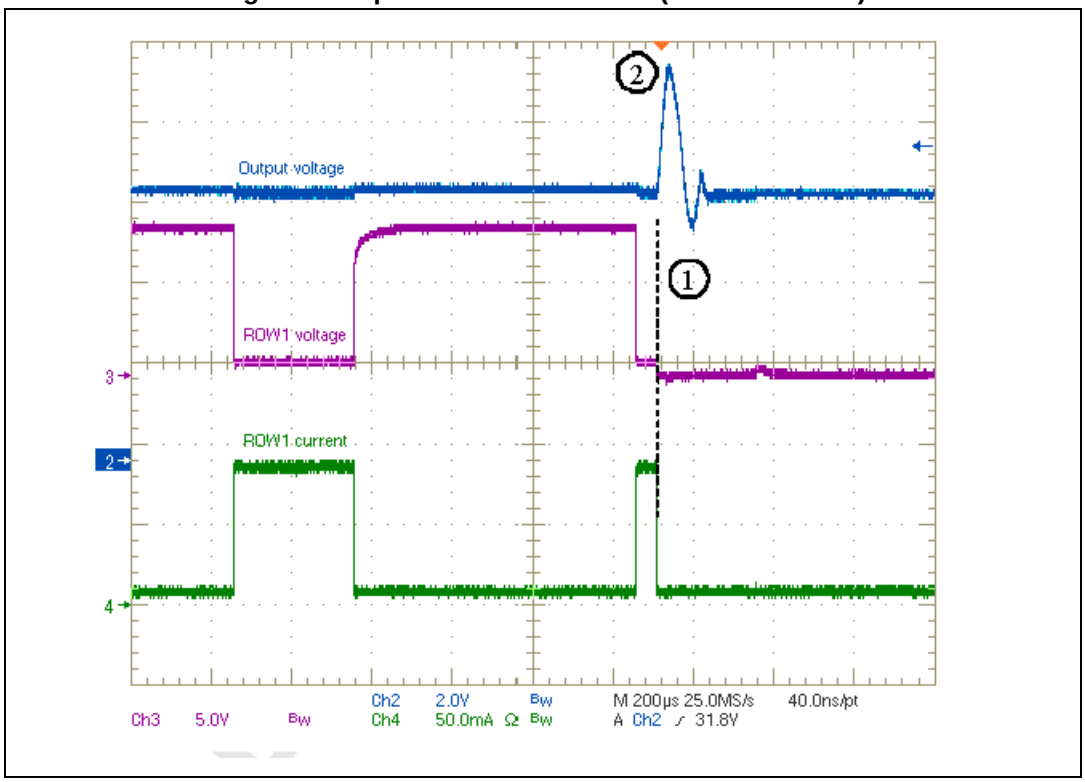
In case a row is not connected or a LED fails open, the device has two different behaviors according to the MODE pin status. If the MODE pin is high (i.e.: connected to AVCC), the FAULT pin is set high as soon as the device recognizes the event; the open row is excluded from the control loop and the device continues to work properly with the remaining rows. Thus, if less than six rows are used in the application, the MODE pin must be set high.

Connecting the MODE pin to SGND, the ALED7707 behaves in a different manner: as soon as an open row is detected the FAULT pin is tied low and the device is turned off. The internal logic latches this status: to restore the normal operation, the device must be restarted by toggling the EN pin or performing a power-on reset (POR occurs when the voltage at the LDO5 pin falls below the lower UVLO threshold and subsequently rises above the upper one).

*Figure 16* shows an example of open channel detection in case of MODE connected to AVCC.

At the point marked as “1” in *Figure 16*, the row opens (row current drops to zero). From this point on the output voltage is increased as long as the output voltage reaches the floating row detection threshold (see *Section 5.1.3 on page 13*). Then (point marked as “2”) the faulty row is disconnected and the device keeps on working only with the remaining rows.

**Figure 16. Open channel detection (MODE to AVCC)**



### 5.3.4 Shorted LED fault

When a LED is shorted, the voltage across the related current generator increases of an amount equal to the missing voltage drop of the faulty LED. Since the feedback voltage on each active generator is constantly compared with a fault threshold $V_{TH,FAULT}$, the device detects the faulty condition and acts according to the MODE pin status.

A 100 µs masking time is introduced to support ESD capacitors eventually connected across the LEDs strings.

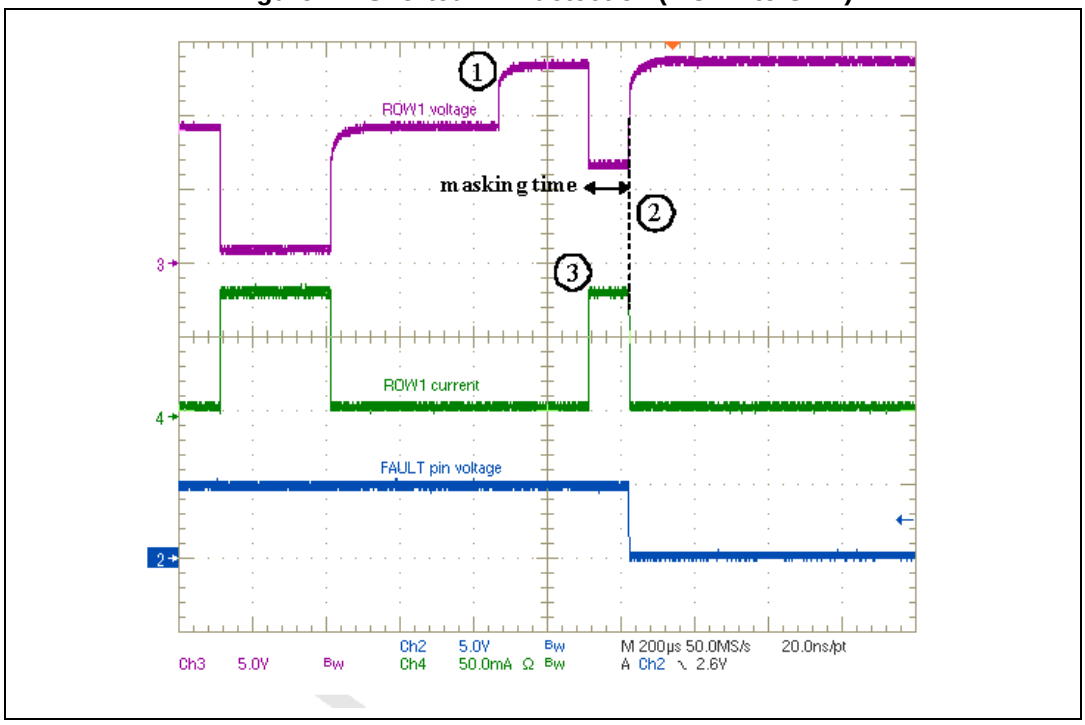
If the MODE pin is low, the fault threshold is $V_{TH,FAULT}$ = 4.0 V. When the voltage across a row is higher than this threshold for more than 100 µs, the FAULT pin is set low and the device is turned off. The internal logic latches this status until the EN pin is toggled or a POR is performed.

In case the MODE pin is connected to AVCC, the LED short-circuit protection is disabled. The ALED7707 simply keeps on regulating the set current without affecting the FAULT pin. Despite the higher power dissipation, this option is useful to avoid undesired triggering of the shorted-LED protection simply due to the high voltage drop spread across the LEDs.

*Figure 17* shows an example of shorted LED detection in case MODE is connected to GND.

At the point marked as “1” in *Figure 17* one LED fails becoming a short-circuit. The voltage across the current generator of the channel where the failed LED is connected increases by an amount equal to the forward voltage of the faulty LED. Since the voltage across the current generator is above the threshold (4 V), the device is turned off and the fault pin is set low (point “2”). Note that, once a new dimming cycle starts (point “3”), the device waits the masking time (approximately 100 µs) and then sets the FAULT pin low and turns off.

**Figure 17. Shorted LED detection (MODE to GND)**



# 6 Application information

## 6.1 System stability

The boost section of the ALED7707 is a fixed frequency, current-mode converter. During normal operation, a minimum voltage selection circuit compares all the voltage drops across the active current generators and provides the minimum one to the error amplifier. The output voltage of the error amplifier determines the inductor peak current in order to keep its inverting input equal to the reference voltage (700 mV typ.). The compensation network consists of a simple RC series ($R_{COMP}$ - $C_{COMP}$) between the COMP pin and ground.

The calculation of $R_{COMP}$ and $C_{COMP}$ is fundamental to achieve optimal loop stability and dynamic performance of the boost converter and is strictly related to the operating conditions.

### 6.1.1 Loop compensation

The compensation network can be quickly calculated using *Equation 11* to *Equation 16*. Once both $R_{COMP}$ and $C_{COMP}$ have been determined, a fine-tuning phase may be required in order to get the optimal dynamic performance from the application.

The first parameter to be fixed is the switching frequency. Normally, a high switching frequency allows reducing the size of the inductor and positively affects the dynamic response of the converter (wider bandwidth) but increases the switching losses. For most of applications, the fixed value (660 kHz) represents a good trade-off between power dissipation and dynamic response, allowing an external resistor to be saved at the same time. In low-profile applications, the inductor value is often kept low to reduce the number of turns; an inductor value in the 4.7 µH - 15 µH range is a good starting choice.

In order to avoid instability due to interaction between the DC-DC converter's loop and the current generators' loop, the bandwidth of the boost should not exceed the bandwidth of the current generators. A unity-gain frequency ($f_U$) in the order of 30 - 40 kHz is acceptable. Also, take care not to exceed the CCM-mode right half-plane zero (RHPZ).

**Equation 11**

$$f_U \leq 0.2 \cdot F_{SW}$$

**Equation 12**

$$f_U \leq 0.2 \cdot \frac{M^2 R}{2\pi \cdot L} = 0.2 \cdot \frac{\left(\frac{V_{IN,min}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \cdot L}$$

**Equation 13a**

$$M = \frac{V_{IN,min}}{V_{OUT}}$$

**Equation 13b**

$$R = \frac{V_{OUT}}{I_{OUT}}$$

Where $V_{IN,min}$ is the minimum input voltage and $I_{OUT}$ is the overall output current.

Note that, the lower the inductor value (and the higher the switching frequency), the higher the bandwidth can be achieved. The output capacitor is directly involved in the loop of the boost converter and must be large enough to avoid excessive output voltage drop in case of a sudden line transition from the maximum to the minimum input voltages.

However a more significant requirement concerns the output voltage ripple. The output capacitor should be chosen in accordance with *Equation 14*:

**Equation 14**

$$C_{OUT} > \frac{(I_{L,peak} - I_{OUT}) \cdot T_{OFF}}{2 \cdot \Delta V_{OUT,max}}$$

where $\Delta V_{OUT, max}$ is the maximum acceptable output voltage ripple, $I_{L, peak}$ is the peak inductor current, $T_{OFF}$ is the off-time of the switching cycle.

Once the output capacitor has been chosen, the $R_{COMP}$ can be calculated as:

**Equation 15**

$$R_{COMP} = \frac{2\pi \cdot f_U \cdot C}{G_M \cdot g_{EA} \cdot M}$$

Where $G_M$ = 2.7 S and $g_{EA}$ = 375 µS.

*Equation 15* places the loop bandwidth at $f_U$. Then, the $C_{COMP}$ capacitor is determined to place the frequency of the compensation zero 5 times lower than the loop bandwidth:

**Equation 16**

$$C_{COMP} = \frac{1}{2\pi \cdot f_Z \cdot R_{COMP}}$$

Where $f_Z = f_U/5$.

In most of the applications an experimental approach is also very valid to compensate the circuit. A simple technique to optimize different applications is to choose $C_{COMP}$ = 4.7 nF and to replace $R_{COMP}$ with a 10 kΩ trimmer adjusting its value to properly damp the output transient response. Insufficient damping will result in excessive ringing at the output and poor phase margin.

*Figure 18* (a and b) gives an example of compensation adjustment for a typical application.

**Figure 18. Poor phase margin (a) and properly damped (b) load transient responses**

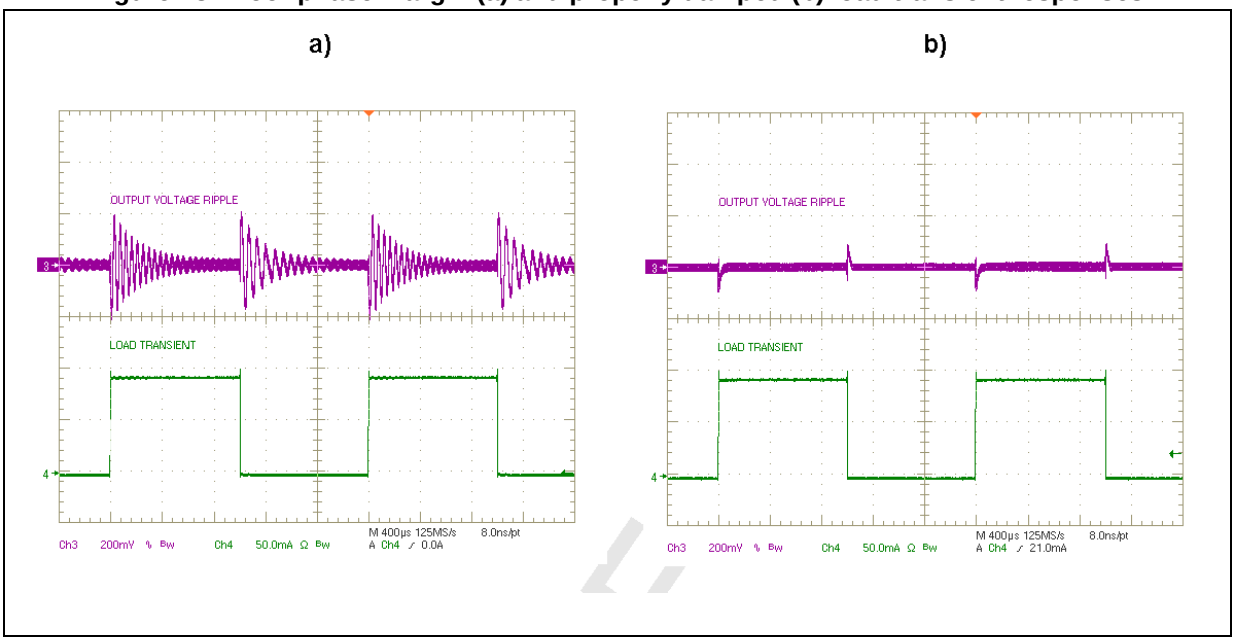
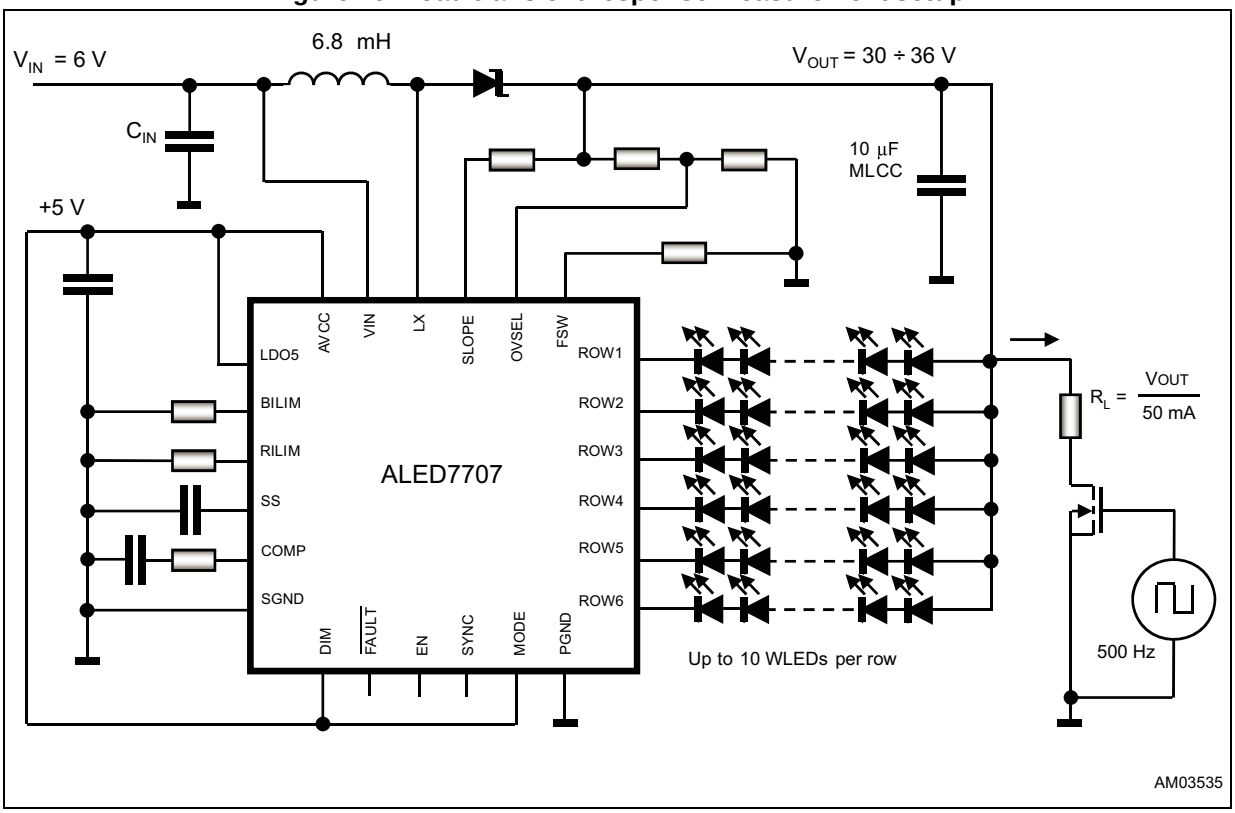



**Figure 19. Load transient response measurement setup**



## 6.2 Thermal considerations

In order to prevent the device from exceeding the thermal shutdown threshold (150 °C), it is important to estimate the junction temperature through the equation below:

**Equation 17**

$$T_J = T_A + R_{th,JA} \cdot P_{D,tot}$$

where $T_A$ is the ambient temperature, $R_{th,JA}$ is the equivalent thermal resistance junction to ambient and $P_{D,tot}$ is the power dissipated by the device.

The $R_{th,JA}$ measured on the application demonstration board, (described in *Section 7*) is 42 °C/W.

The $P_{D,tot}$ has several contributions, listed below.

a) Conduction losses due to the $R_{DS(on)}$ of the internal power switch, equal to:

**Equation 18**

$$P_{D,cond} = R_{DSon} \cdot I_{IN}^2 \cdot D \cdot D_{DIM}$$

where $D$ is defined as:

**Equation 19**

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

and $D_{DIM}$ is the duty cycle of the PWM dimming signal.

b) Switching losses due to the power MOSFET turn on and off, calculated as:

**Equation 20**

$$P_{D,sw} = V_{OUT} \cdot I_{IN} \cdot f_{sw} \cdot \frac{(t_r + t_f)}{2} \cdot D_{DIM}$$

where $t_r$ and $t_f$ are the power MOSFET rise time and fall time respectively.

c) Current generators losses. This contribution is strictly related to the LEDs used in the application. Only the contribution of the leading current generator (“master” current generator) can be predicted, regardless of the LEDs forward voltage:

**Equation 21**

$$P_{GEN,Master} = I_{ROW} \cdot V_{IFB} \cdot D_{DIM}$$

where $I_{ROW}$ is the current flowing through the row, whereas $V_{IFB}$ is the voltage across the master current generator (typically 700 mV).

The voltages across the other current generators depend on the spread of the LEDs forward voltage. The worst case for power dissipation (maximum forward voltage LEDs in the master row, minimum forward voltage LEDs in all other rows) can be estimated as:

**Equation 22**

$$P_{GEN} = I_{ROW} \cdot (n_{ROWs} - 1) \cdot (V_{IFB} + \Delta V_{f,LEDs} \cdot n_{LEDs}) \cdot D_{DIM}$$

where $n_{ROWs}$ is the number of active rows, $\Delta V_{f,LEDs}$ is the spread of the LEDs forward voltage and $n_{LEDs}$ is the number of LEDs per row.

d) LDO losses, due to the dissipation of the 5 V linear regulator:

**Equation 23**

$$P_{D,LDO} = (V_{IN} - V_{LDO}) \cdot I_{LDO}$$

The ALED7707 device is housed in a QFN 5x5 - 24L package that allows good thermal performance. However it is also important to design properly the demonstration board layout in order to assure correct heat dissipation.

# 7 Electrical characteristics (curves)

**Figure 20. Efficiency versus DIM duty cycle, $V_{IN}$ = 12 V, 6 rows, 10 white LEDs (60 mA) in series, $F_{SW}$ = 660 kHz**

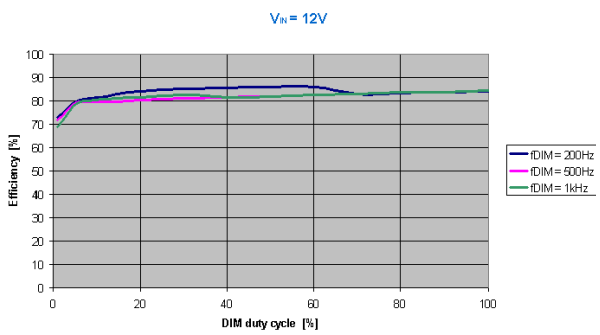



**Figure 21. Efficiency versus DIM duty cycle, $V_{IN}$ = 18 V, 6 rows, 10 white LEDs (60 mA) in series, $F_{SW}$ = 660 kHz**

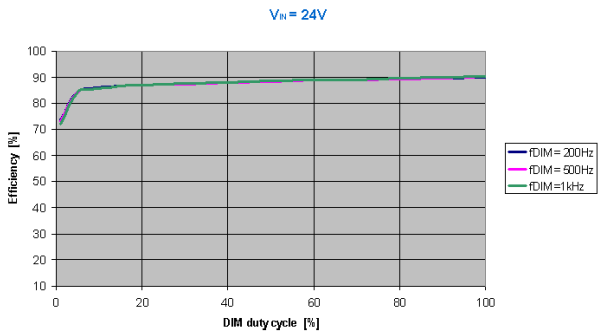



**Figure 22. Efficiency versus DIM duty cycle, $V_{IN}$ = 24 V, 6 rows, 10 white LEDs (60 mA) in series, $F_{SW}$ = 825 kHz**

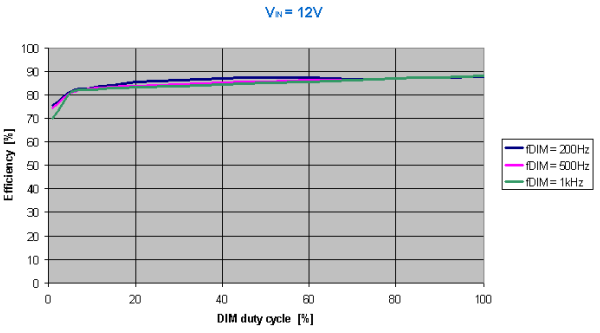



**Figure 23. Efficiency versus DIM duty cycle, $V_{IN}$ = 24 V, 6 rows, 10 white LEDs (60 mA) in series, $F_{SW}$ = 825 kHz**

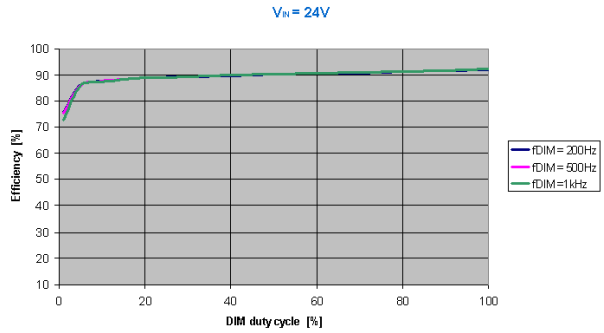



**Figure 24. Soft-start waveforms (EN, SS, and $V_{OUT}$ monitored)**

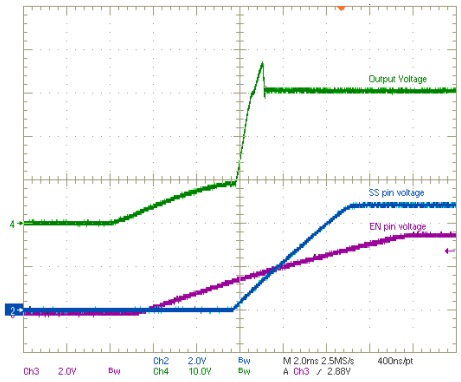



**Figure 25. Boost section switching signals (LX, SYNC and inductor current monitored), $V_{IN}$ = 12 V, 10 LEDs**

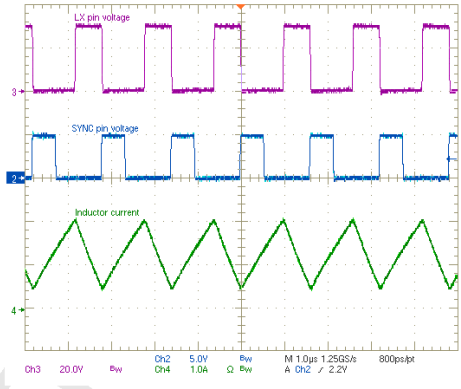


**Figure 26. Dimming waveforms ($F_{DIM}$ = 200 Hz)**

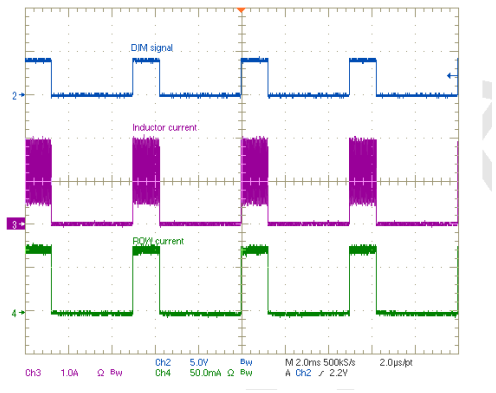
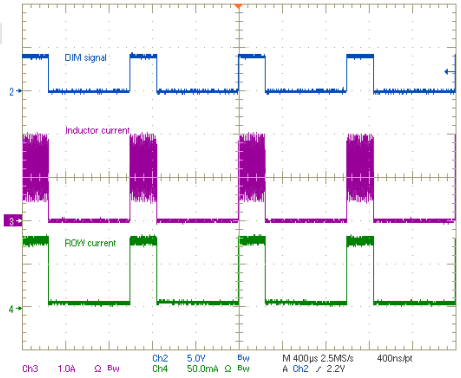



**Figure 27. Dimming waveforms ($F_{DIM}$ = 1 kHz)**



# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 8.1 QFN 5x5 - 24L package information

**Figure 28. QFN 5x5 - 24L package outline**

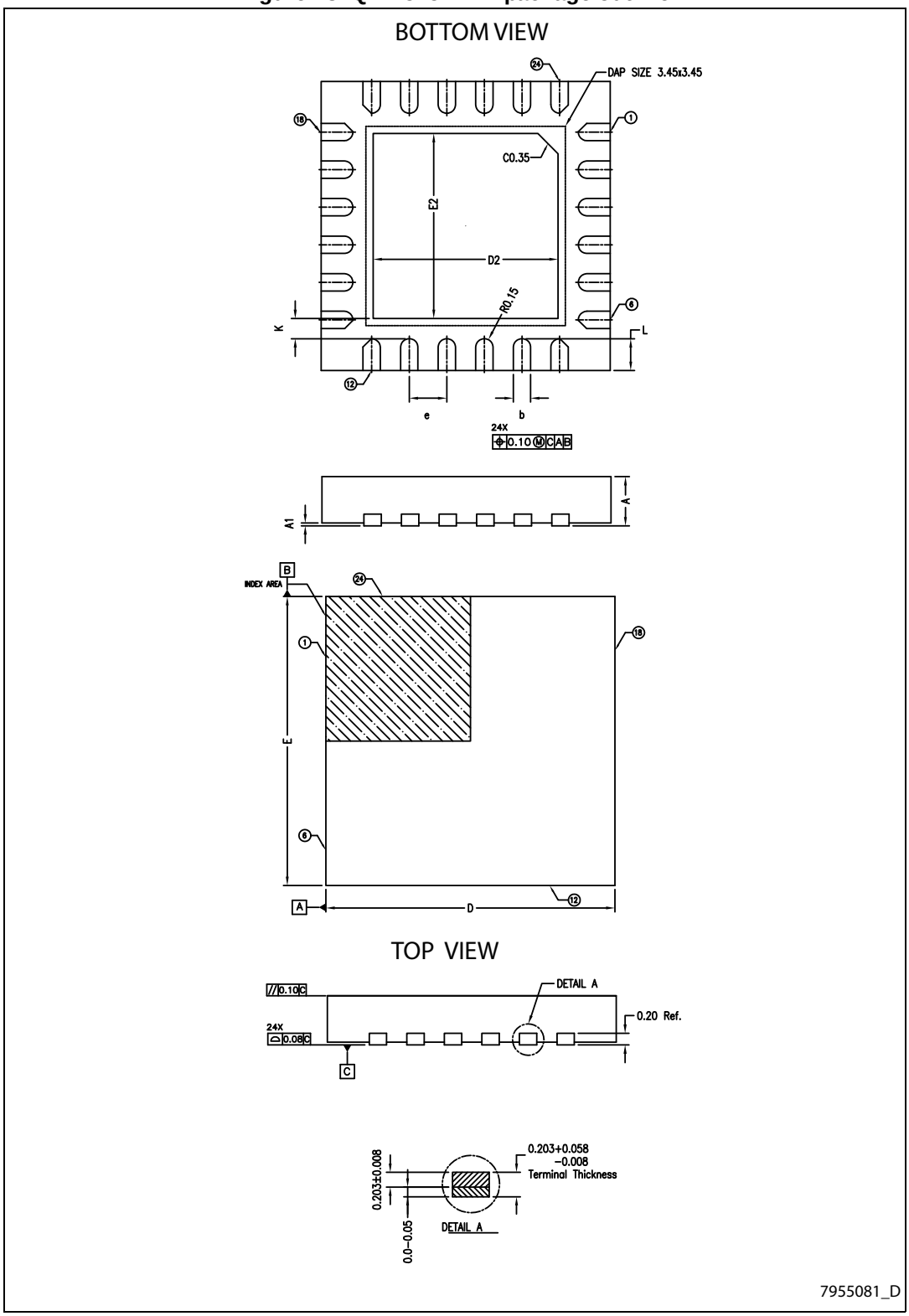
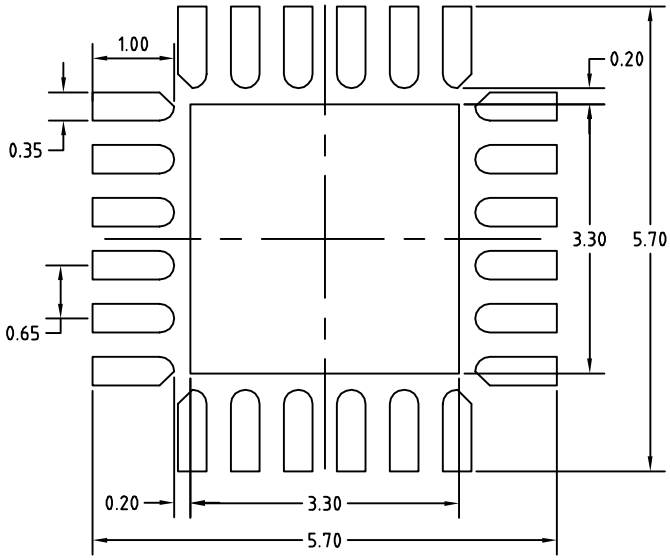


**Table 7. QFN 5x5 - 24L package mechanical data**

| Symbol | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | - | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| e | | 0.65 | |
| D2 | 3.10 | 3.20 | 3.30 |
| E2 | 3.10 | 3.20 | 3.30 |
| K | 0.20 | - | - |
| L | 0.45 | 0.55 | 0.65 |
| N | 24 | | |
| ND | 6 | | |
| NE | 6 | | |

**Figure 29. QFN 5x5 - 24L recommended footprint**



# 9 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 11-May-2015 | 1 | Initial release. |
| 23-Jan-2017 | 2 | Updated features in cover page.<br>Updated *Table 7: QFN 5 x 5 - 24L package mechanical data*.<br>Minor text changes. |
| 09-Oct-2018 | 3 | Minor text changes. |