DEMO CIRCUIT 1489A
QUICK START GUIDE

LTC3619EDD/LTC3619BEDD
SYNCHRONOUS BUCK DUAL REGULATOR WITH ADJUSTABLE INPUT CURRENT LIMIT

DESCRIPTION

Demonstration circuit 1489A is a synchronous buck dual regulator with adjustable input current limit featuring the LTC3619EDD/ LTC3619BEDD and is ideally suited for pulsed load applications where the input current needs to be limited. The LTC3619EDD operates in burst mode for higher light load efficiency, while the LTC3619BEDD operates in pulse-skip mode for lower output ripple. The package style for the LTC3619EDD/ LTC3619BEDD is a 10 lead 3mm x 3mm plastic DFN.

Demonstration circuit 1489A is configured for 500mA maximum input current limit. The outputs are configured for a 3.3V / 400mA continuous current output and a 3.4V output that can handle pulsed load currents of up to 2A, with duty cycles of up to 15%. The input voltage range is 5V ±10%. The fixed input current limit can be adjusted by replacing one resistor. Please see the datasheets for more information.

The LTC3619/LTC3619B datasheets gives complete descriptions of these parts, operation and application information and must be read in conjunction with this quick start guide for demo circuit 1489A.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITIONS / NOTES	VALUE
Input Voltage Range V_{IN}		4.5V – 5.5V
Input Current Limit		500mA ± 5%
Output Voltage V_{OUT1}	V_{IN} = 4.5V to 5.5V, I_{OUT1} = 0A to 400mA	3.3V ± 3%
Output Voltage V_{OUT2}	V_{IN} = 4.5V to 5.5V, I_{IN} = 0A to 500mA	3.4V ± 3%
Efficiency (Figures 4 and 5)	V_{IN} = 4.5V, I_{OUT1} = 400mA V_{IN} = 5.5V, I_{OUT1} = 400mA V_{IN} = 4.5V, I_{OUT2} = 500mA V_{IN} = 5.5V, I_{OUT2} = 500mA	92.6% typical 92.3% typical 93.4% typical 92.6% typical

QUICK START PROCEDURE

Demonstration circuit 1489A is easy to set up to evaluate the performance of the LTC3619EDD/ LTC3619BEDD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the V_{IN} or V_{OUT} and GND terminals or directly across the capacitor. See Figure 2 for proper scope probe technique.

1. Place the jumper in the following position:

   JP1 On JP2 On

2. With power off, connect the input power supply to V_{IN} and GND.
3. Turn on the power at the input.

   NOTE: Make sure that the input voltage does not exceed 5.5V.

4. Check for the proper output voltage.

   V_{OUT1} = 3.200 to 3.400V,

   V_{OUT2} = 3.298 to 3.502V

   If there is no output, temporarily disconnect the load to make sure that the load is not set too high.

5. Once the proper output voltages are established, adjust the loads within the operating range and ob-

serve the output voltage regulation, ripple voltage, efficiency and other parameters.

6. The method for evaluating pulsed loads will be discussed in the next section.

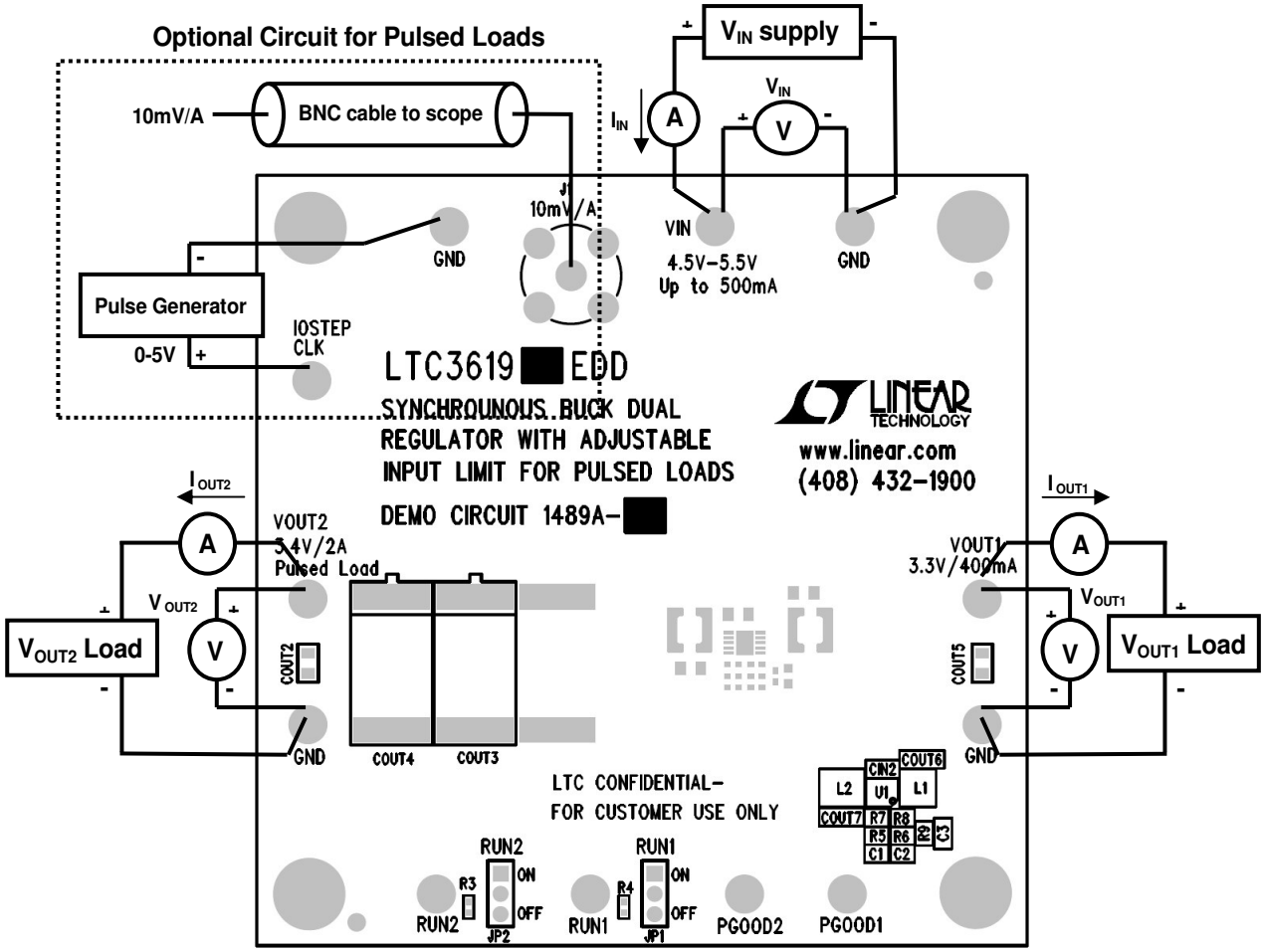


Figure 1. Proper Measurement Equipment Setup

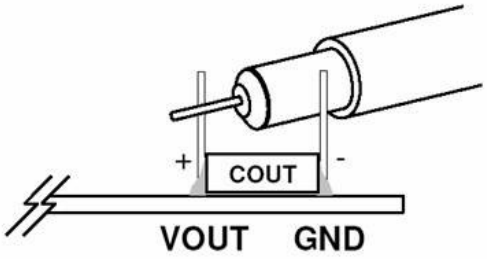


Figure 2. Measuring Input or Output Ripple Directly Across Bulk Capacitor

PULSED LOAD TESTING

Demonstration circuit 1489A can be setup for simple evaluation of pulse loads – please see optional circuit in Figure 1 for proper setup. The circuit is capable of pulsed load of up to 2A with duty cycles up to 15% on V_{OUT2}.

Starting from step 5 in the quick start procedure above, follow the procedure below:

1. Disconnect all loads from V_{OUT2} as the pulse load circuitry is on board.
2. The pulsed load current is measured by connecting J1 to the scope using a BNC cable and setting the oscilloscope to 10mV/div
3. Input current and output voltage can be measured on an oscilloscope for evaluation.
4. A pulse generator with adjustable amplitude is connected between IOSTEP CLK and GND as indicated in Figure 1. The pulse generator should be capable of generating up to 5V pulses. Adjust the period and duty cycle of this signal to match that of the required load prior to attaching the pulse generator.
5. Adjust pulse generator amplitude until the required load current is achieved as measured on J1 (10mV/A).
6. An example result showing V_{OUT2}, I_{IN} and a pulse load I_{OUT2} is given in Figure 3.

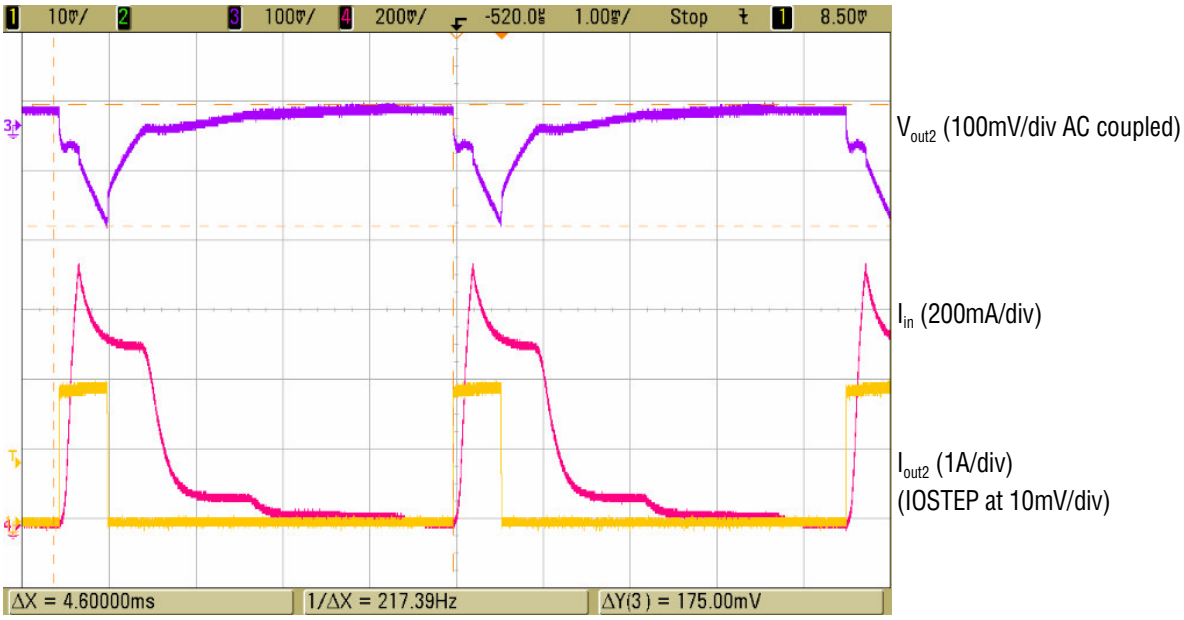


Figure 3. Pulse Load Waveforms for 2A pulsed load, 1/8th duty cycle, 4.6ms period

ADJUSTING INPUT CURRENT LIMIT

It is possible to modify the demonstration circuit for either higher or lower input current limits. This is accomplished by changing resistor R9 to the required value as suggested in the LTC3619EDD/ LTC3619BEDD datasheets. Note that for these different current values, the inductor may not be optimum and may have to be changed as well. Please refer to the datasheet for more information.

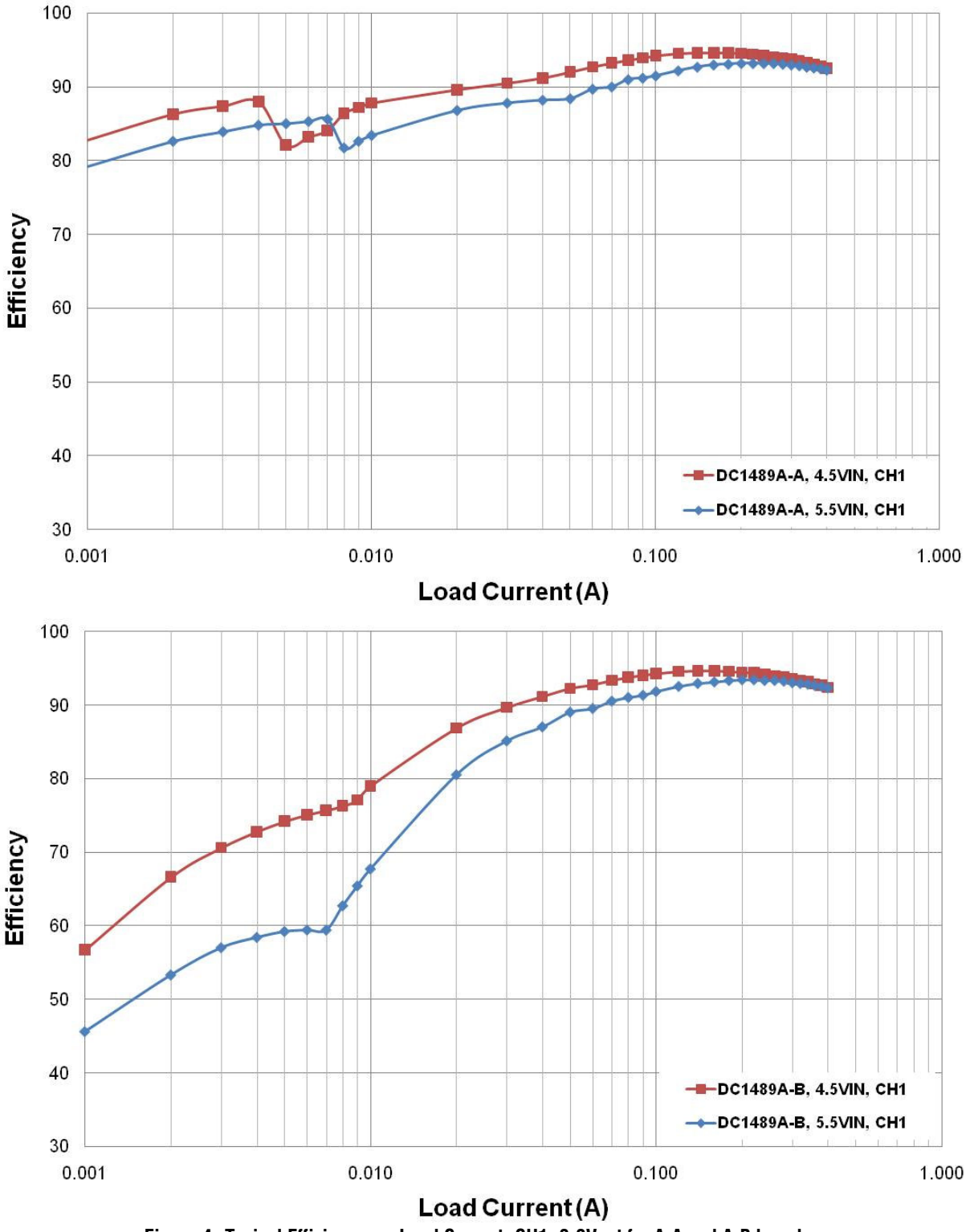


Figure 4. Typical Efficiency vs. Load Current, CH1, 3.3Vout for A-A and A-B boards

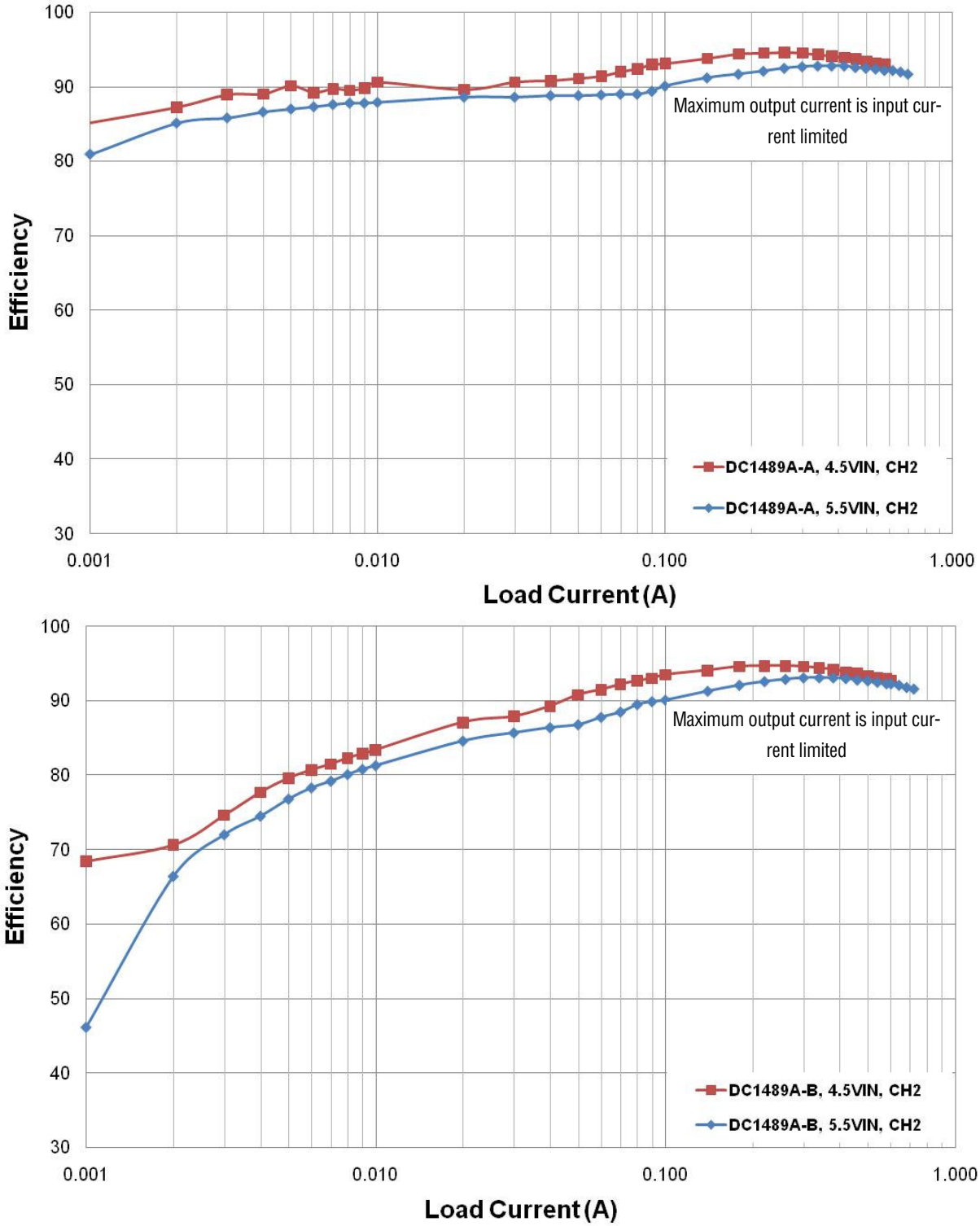
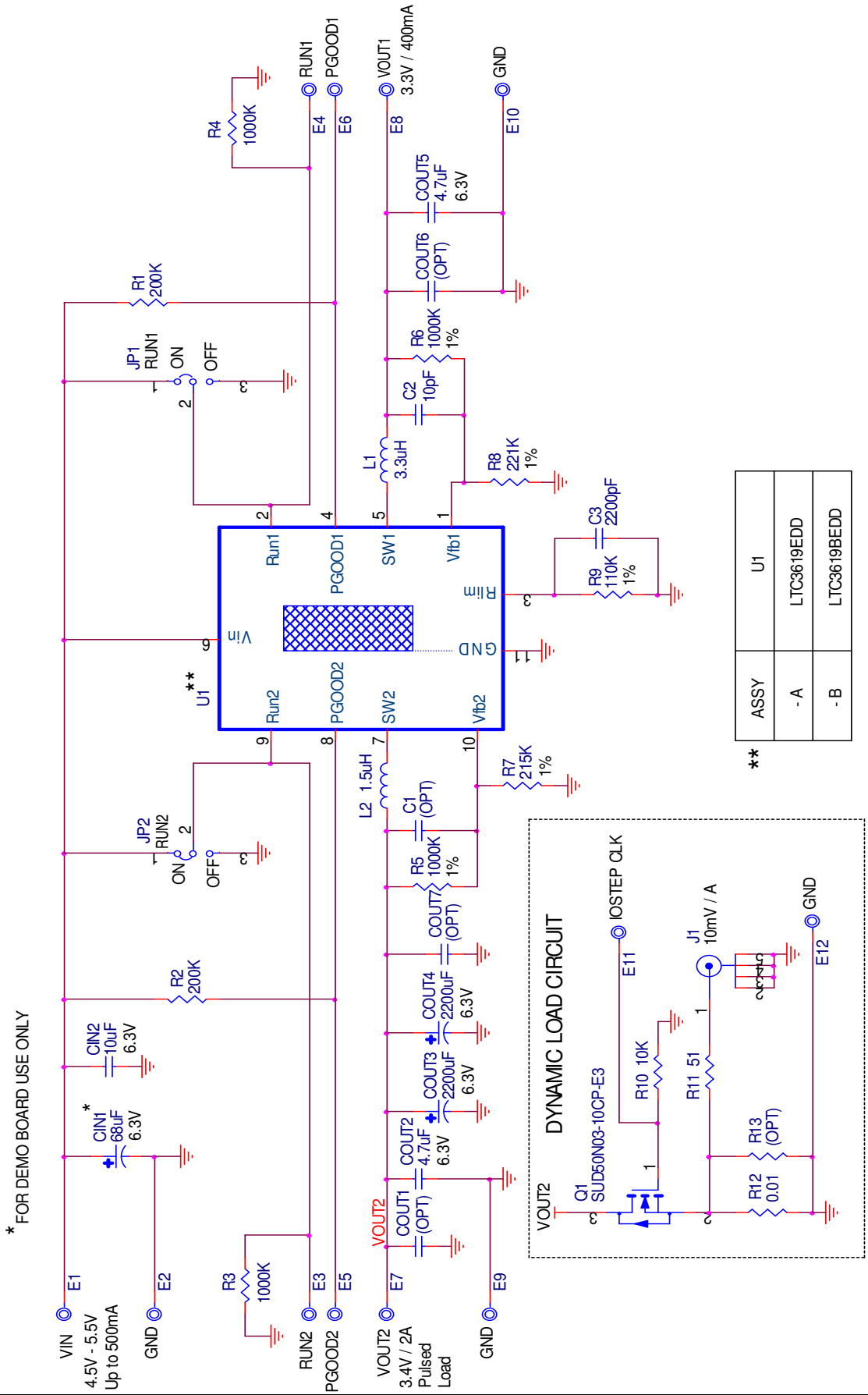


Figure 5. Typical Efficiency vs. Load Current, CH2, 3.4Vout for A-A and A-B boards


* FOR DEMO BOARD USE ONLY
VIN
4.5V - 5.5V
Up to 500mA
GND
RUN2
PGOOD2
VOUT2
3.4V / 2A
Pulsed
Load
GND
E1
E2
E3
E5
E7
E9
CIN2 10uF 6.3V
CIN1 68uF 6.3V
R3 1000K
R2 200K
JP2 RUN2 ON OFF
R4 1000K
R1 200K
JP1 RUN1 ON OFF
RUN1
PGOOD1
VOUT1
3.3V / 400mA
GND
E4
E6
E8
E10
COUT5 4.7uF 6.3V
COUT6 (OPT)
R6 1000K 1%
C2 10pF
L1 3.3uH
R8 221K 1%
C3 2200pF
R9 110K 1%
U1 **
Run1
PGOOD1
SW1
Vfb1
RTTM
VIN
GND
Run2
PGOOD2
SW2
Vfb2
L2 1.5uH
C1 (OPT)
R7 215K 1%
R5 1000K 1%
COUT7 (OPT)
COUT4 2200uF 6.3V
COUT3 2200uF 6.3V
COUT2 4.7uF 6.3V
COUT1 (OPT)
DYNAMIC LOAD CIRCUIT
VOUT2
Q1 SUD50N03-10CP-E3
R10 10K
IOSTEP CLK
E11
R11 51
J1 10mV / A
R13 (OPT)
R12 0.01
GND
E12
** ASSY U1
- A LTC3619EDD
- B LTC3619BEDD