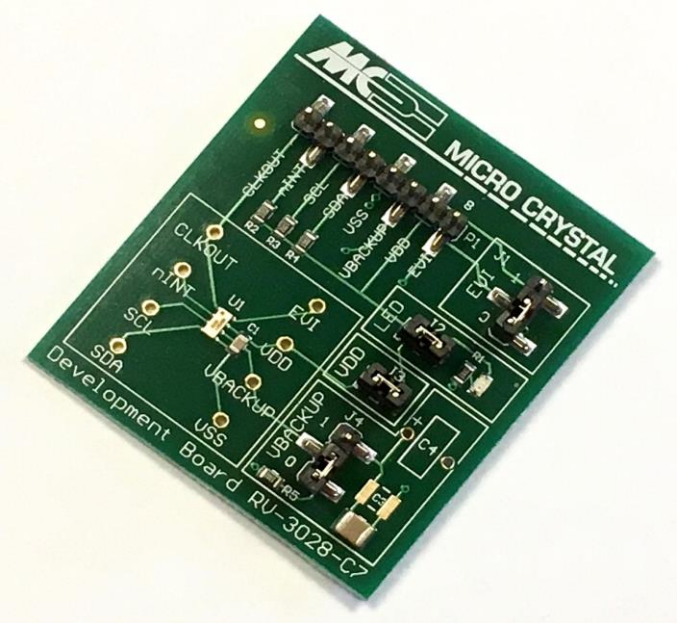
MICRO CRYSTAL SWITZERLAND

RV-3028-C7
Development Board

DEVELOPMENT BOARD



RV-3028-C7
Extreme Low Power RTC Module

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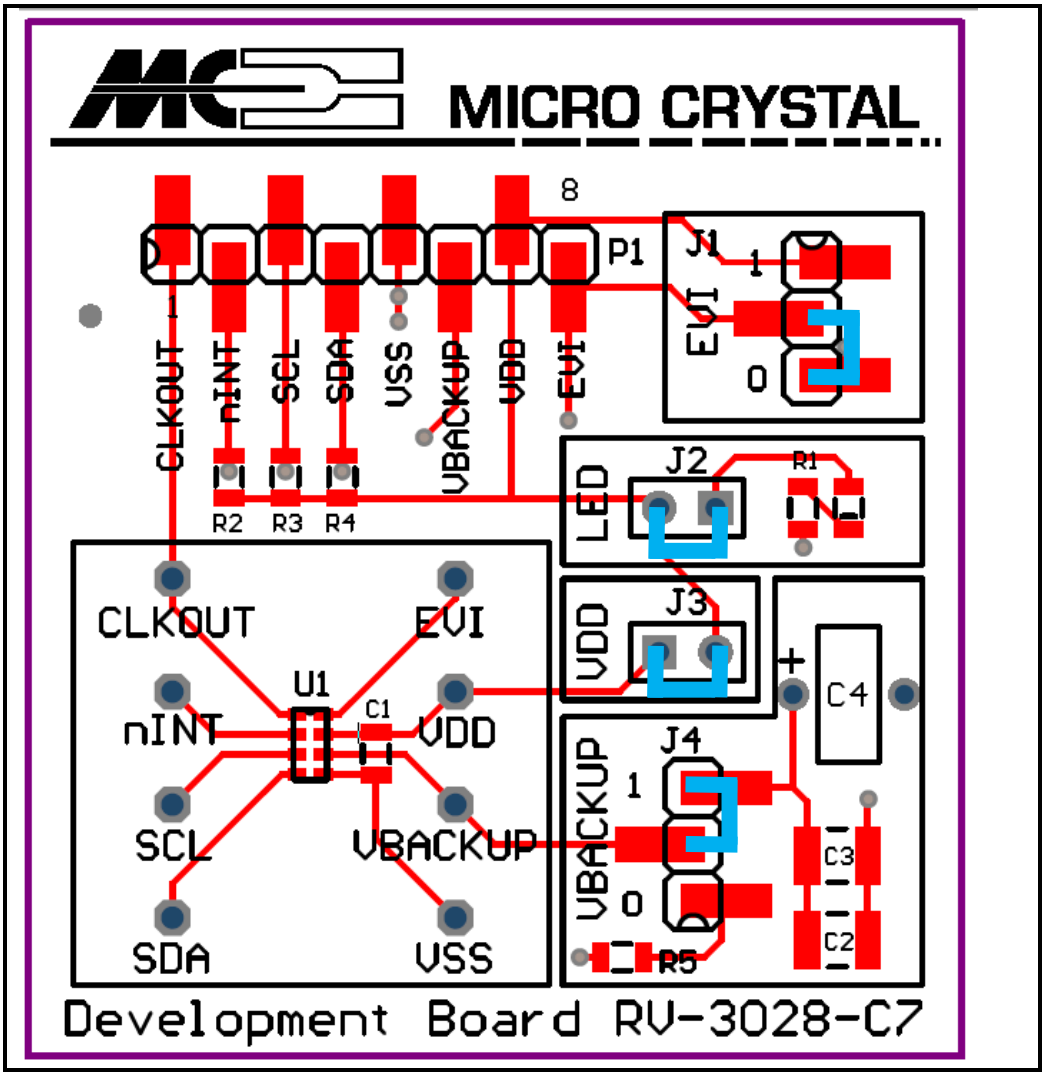
RV-3028-C7

The RV-3028-C7 is soldered onto the Development Board.
Every pin is accessible at test pins 1 – 8 and at the test vias situated around the device.

The following passive components are already soldered on the board:

C1	10 nF	Decoupling capacitor between V_{SS} and V_{DD}
C2	100uF	Capacitor for Back-up power
C3, C4		Option, to place alternative capacitors or battery for back-up power
R1	330 Ω	Current limiting resistor for LED
LED1	green	Supply, current consumption of the LED has to be considered, J2 to switch off
R2	10 kΩ	Pull-up resistor INT to V_{DD}
R3	10 kΩ	Pull-up resistor SCL to V_{DD}
R4	10 kΩ	Pull-up resistor SDA to V_{DD}
R5	10 kΩ	Pull-down resistor to define V_{BACKUP} input in case it is not used

DEVELOPMENT BOARD



JUMPER 1

EVI = HIGH

EVI = LOW

JUMPER 2

LED

JUMPER 3

VDD, CURRENT MEASURMENT

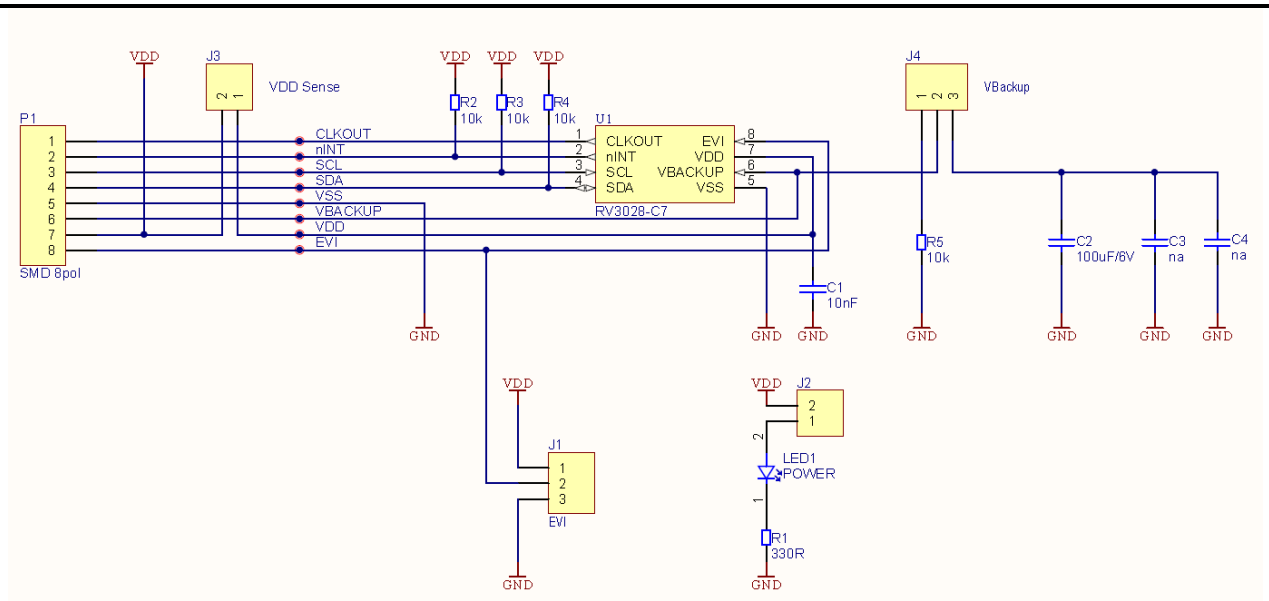
JUMPER 4

SUPERCAP

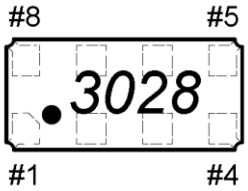
SET INPUT TO VSS

Development Board RV-3028-C7

SCHEMATICS



PINOUT RV-3028-C7



# 1	CLKOUT	# 8	EVI
# 2	$\overline{INT}$	# 7	V_{DD}
# 3	SCL	# 6	V_{BACKUP}
# 4	SDA	# 5	V_{SS}

PIN DESCRIPTION

Symbol	Pin #	Description
CLKOUT	1	Clock Output; push-pull; Normal and Interrupt driven clock output can be activated concurrently. 1. Normal clock output is controlled by the CLKOE bit. When CLKOE is set to 1 (default), the CLKOUT pin drives the square wave on the CLKOUT pin. When CLKOE bit is set to 0, the CLKOUT pin is LOW. 2. Interrupt driven clock output is controlled by an interrupt event. When CLKIE is set to 1 the occurrence of the interrupt selected in the Clock Interrupt Mask Register (12h) allows the square wave output on the CLKOUT pin. Writing 0 to CLKIE will disable new interrupts from driving square wave on CLKOUT. When CLKF flag is cleared, the CLKOUT pin is LOW. Depending of the settings in the FD field, the CLKOUT pin can drive the square wave of 32.768 kHz (default), 8192 Hz, 1024 Hz, 64 Hz, 32 Hz or 1 Hz, or the predefined periodic countdown timer interrupt. When FD field is 111 the CLKOUT pin is LOW.
$\overline{INT}$	2	Interrupt Output; open-drain; active LOW; requires pull-up resistor; used to output Alarm, Periodic Countdown Timer, Periodic Time Update and External Event Interrupt signals. Interrupt output also in V_{BACKUP} Power state.
SCL	3	I^2C Serial Clock Input; requires pull-up resistor. In VBACKUP Power state, the SCL pin is disabled.
SDA	4	I^2C Serial Data Input-Output; open-drain; requires pull-up resistor. In V_{BACKUP} Power state, the SDA pin is disabled (high impedance)
V_{SS}	5	Ground
V_{BACKUP}	6	Backup Supply Voltage. When the backup switchover function is not needed, V_{BACKUP} must be tied to V_{SS} with a 10 kΩ resistor
V_{DD}	7	Positive supply voltage; positive or negative steps in supply voltage may affect oscillator performance, recommend 10 nF decoupling capacitor close to the device
EVI	8	External Event Input; used for interrupt generation, interrupt driven clock output and time stamp function. Remains active also in V_{BACKUP} Power state. This pin should not be left floating

Datasheet and Application-Manual are available for download under: www.microcrystal.com