EL7155

High Performance Pin Driver

FN7279
Rev 3.00
October 24, 2014

The EL7155 high performance pin driver with 3-state is suited to many ATE and level-shifting applications. The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads.

Output pins OUT_H and OUT_L are connected to input pins V_H and V_L respectively, depending on the status of the IN pin. One of the output pins is always in tri-state, except when the OE pin is low, in which case both outputs are in tri-state mode. The isolation of the output FETs from the power supplies enables V_H and V_L to be set independently, enabling level-shifting to be implemented.

This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and ON-resistance characteristics.

Available in an 8 Ld SOIC package, the EL7155 is specified for operation over the full -40°C to +85°C temperature range.

Features

- Clocking speeds up to 40MHz
- 15ns tr/tf at 2000pF C_{LOAD}
- 0.5ns rise and fall times mismatch
- 0.5ns t_{ON}-t_{OFF} prop delay mismatch
- 3.5pF typical input capacitance
- 3.5A peak drive
- Low ON-resistance of 3.5Ω
- High capacitive drive capability
- Operates from 4.5V up to 16.5V
- Pb-free (RoHS compliant)

Applications

- ATE/burn-in testers
- Level shifting
- IGBT drivers
- CCD drivers

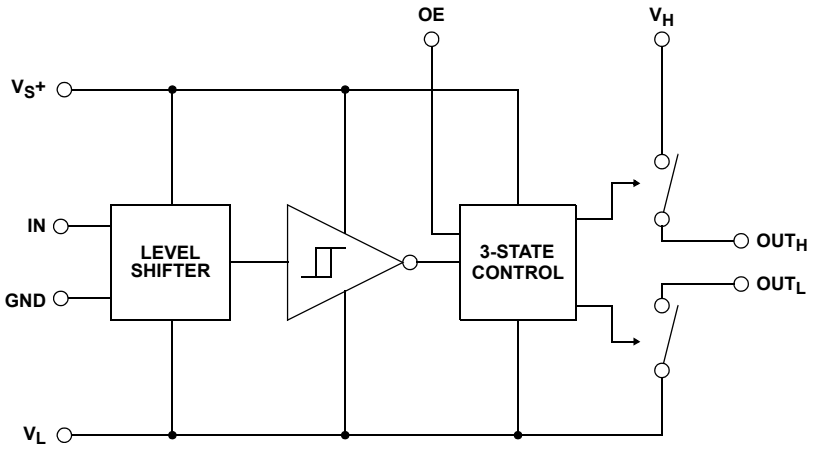
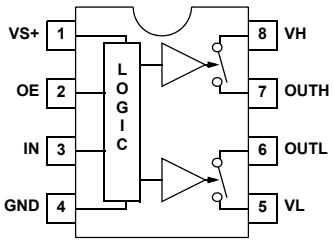


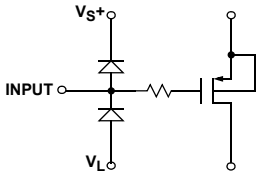
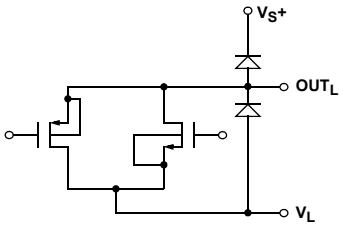
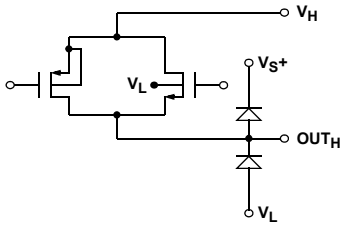
FIGURE 1. BLOCK DIAGRAM

Pin Configuration

EL7155
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VS+	Positive Supply Voltage	
2	OE	Output Enable	 Circuit 1
3	IN	Input	Reference Circuit 1
4	GND	Ground	
5	VL	Negative Supply and Lower Output Voltage	
6	OUTL	Lower Switch Output	 Circuit 2
7	OUTH	Upper Switch Output	 Circuit 3
8	VH	Upper Output Voltage	

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL7155CSZ	7155CSZ	8 Ld SOIC	M8.15E
EL7155CSZ-T7 (Note 3)	7155CSZ	8 Ld SOIC	M8.15E
EL7155CSZ-T7A (Note 3)	7155CSZ	8 Ld SOIC	M8.15E
EL7155CSZ-T13 (Note 3)	7155CSZ	8 Ld SOIC	M8.15E

NOTE:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see product information page for EL7155. For more information on MSL, please see tech brief TB363.
3. Please refer to TB347 for details on reel specifications.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S+ to V_L) . . . . . +18V
V_H-V_L, V_H to GND, V_S+ to V_H 16.5V
Input Voltage . . . . . .-0.3V below V_L to +0.3V above V_S
Continuous Output Current 200mA
Storage Temperature Range . . . . . .-65°C to +150°C

Thermal Information

Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+125°C
Power Dissipation . . . . . see curves
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

V_S+ = +15V, V_H = +15V, V_L = 0V, T_A = +25°C, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNITS
INPUT						
V_{IH}	Logic '1' Input Voltage		2.4			V
I_{IH}	Logic '1' Input Current	V_{IH} = V_S+		0.1	10	µA
V_{IL}	Logic '0' Input Voltage				0.8	V
I_{IL}	Logic '0' Input Current	V_{IL} = 0V		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OVH}	ON-Resistance V_H to OUT_H	I_{OUT} = -200mA		2.7	4.5	Ω
R_{OVL}	ON-Resistance V_L to OUT_L	I_{OUT} = +200mA		3.5	5.5	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUT_H = V_L, OUT_L = V_S+		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		1.3	3	mA
I_{VH}	Off Leakage at V_H	V_H = 0V		4	10	µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	C_L = 2000pF		14.5		ns
t_F	Fall Time	C_L = 2000pF		15		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 2000pF		0.5		ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000pF		9.5		ns
t_{D-2}	Turn-On Delay Time	C_L = 2000pF		10		ns
$t_{D\Delta}$	t_{D-1} - t_{D-2} Mismatch	C_L = 2000pF		0.5		ns
t_{D-3}	3-state Delay Enable			10		ns
t_{D-4}	3-state Delay Disable			10		ns

Electrical Specifications

$V_S+ = +5V$, $V_H = +5V$, $V_L = -5V$, $T_A = +25°C$, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP (Note 5)	MAX (Note 4)	UNIT
INPUT						
V_{IH}	Logic '1' Input Voltage		2.0			V
I_{IH}	Logic '1' Input Current	$V_{IH} = V_S+$		0.1	10	µA
V_{IL}	Logic '0' Input Voltage				0.8	V
I_{IL}	Logic '0' Input Current	$V_{IL} = 0V$		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OVH}	ON-Resistance V_H to OUT_H	$I_{OUT} = -200mA$		3.4	5	Ω
R_{OVL}	ON-Resistance V_L to OUT_L	$I_{OUT} = +200mA$		4	6	Ω
I_{OUT}	Output Leakage Current	$OE = 0V$, $OUT_H = V_L$, $OUT_L = V_S+$		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		1	2.5	mA
I_{VH}	Off Leakage at V_H	$V_H = 0V$		4	10	µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	$C_L = 2000pF$		17		ns
t_F	Fall Time	$C_L = 2000pF$		17		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	$C_L = 2000pF$		0		ns
t_{D-1}	Turn-Off Delay Time	$C_L = 2000pF$		11.5		ns
t_{D-2}	Turn-On Delay Time	$C_L = 2000pF$		12		ns
$t_{D\Delta}$	$t_{D-1} - t_{D-2}$ Mismatch	$C_L = 2000pF$		0.5		ns
t_{D-3}	3-state Delay Enable			11		ns
t_{D-4}	3-state Delay Disable			11		ns

NOTES:

4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
5. Typical values are for information purposes only.

Typical Performance Curves

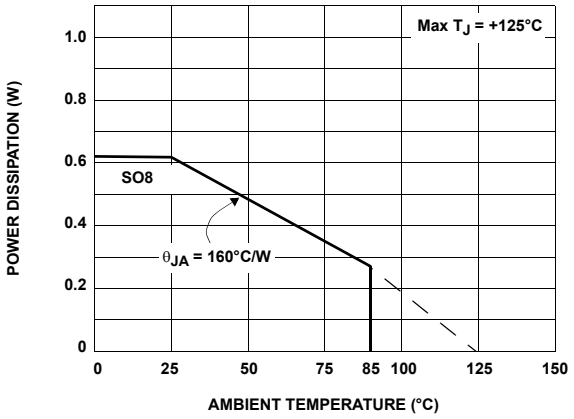


FIGURE 2. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE JEDEC JESD51-3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

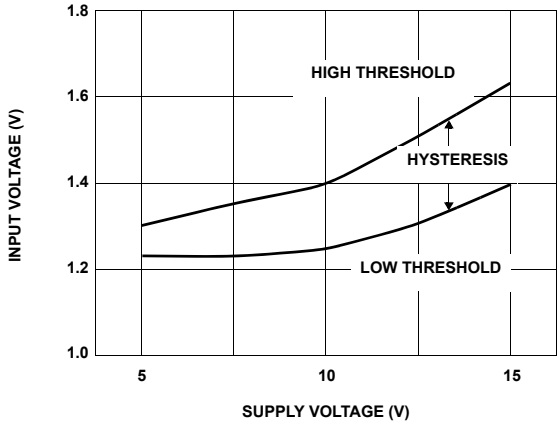


FIGURE 3. INPUT THRESHOLD vs SUPPLY VOLTAGE, T = 25°C

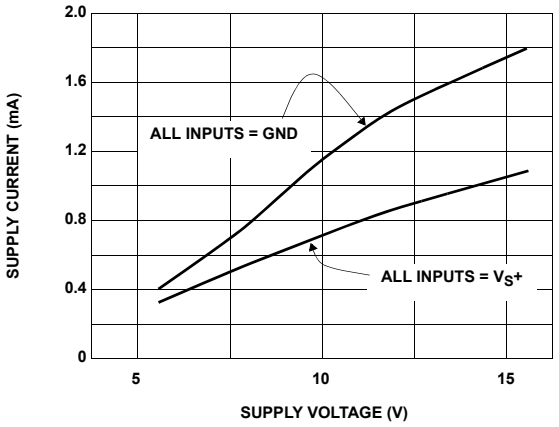


FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE, T = +25°C

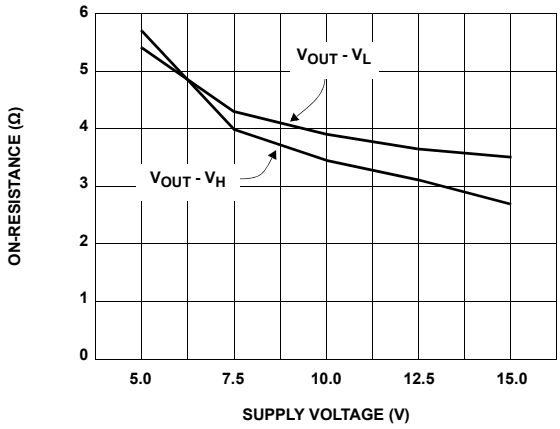


FIGURE 5. ON-RESISTANCE vs SUPPLY VOLTAGE, I_{OUT} = 200mA, T = +25°C, V_S+ = V_H, V_L = 0V

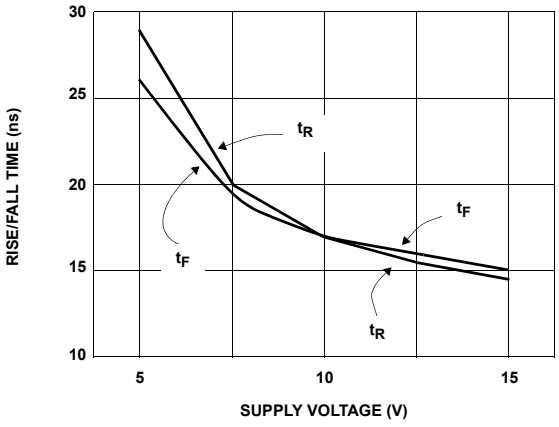


FIGURE 6. RISE/FALL TIME vs SUPPLY VOLTAGE C_L = 2000pF, T = +25°C

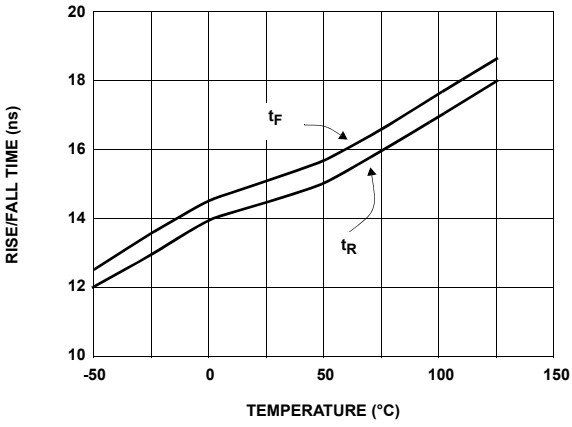


FIGURE 7. RISE/FALL TIME vs TEMPERATURE C_L = 2000PF, V_S+ = 15V

Typical Performance Curves (Continued)

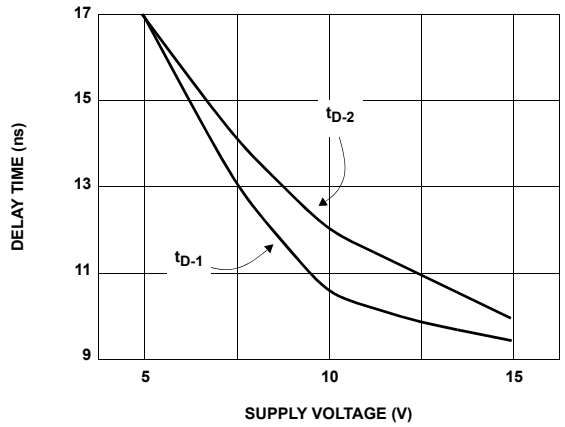


FIGURE 8. PROPAGATION DELAY vs SUPPLY VOLTAGE
C_L = 2000pF, T = +25°C

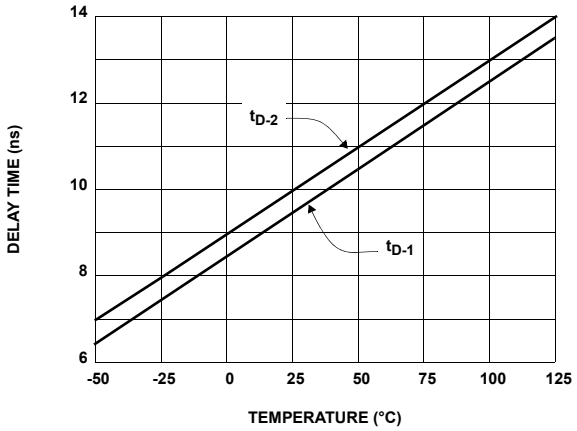


FIGURE 9. PROPAGATION DELAY vs TEMPERATURE
C_L = 2000pF, V_S+ = 15V

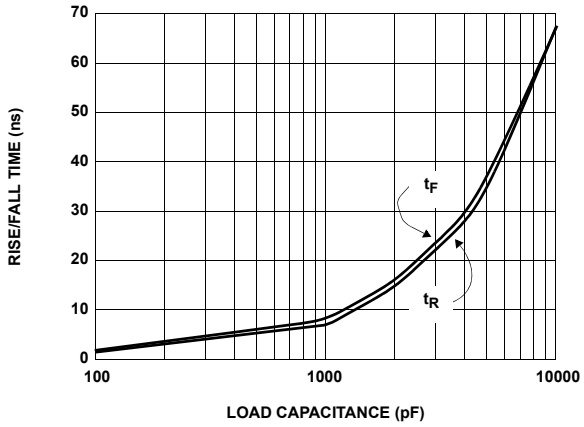


FIGURE 10. RISE/FALL TIME vs LOAD CAPACITANCE
V_S+ = +15V, T = +25°C

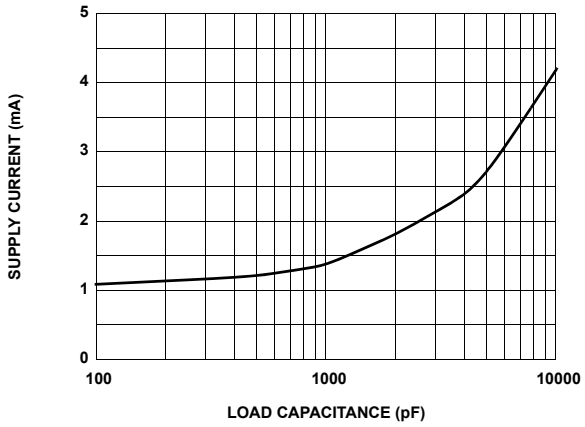


FIGURE 11. SUPPLY CURRENT vs LOAD CAPACITANCE,
V_S+ = V_H = 15V, V_L = 0V, T = +25°C, f = 20kHz

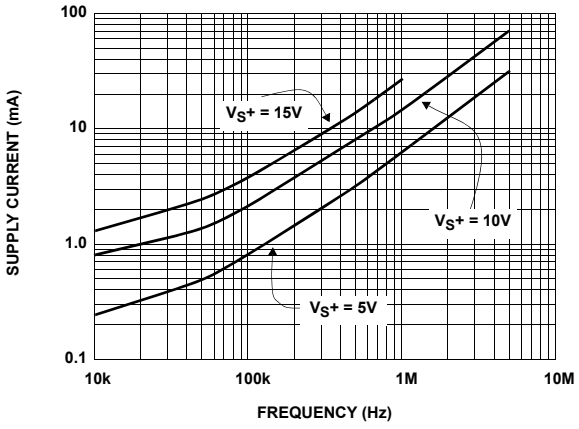


FIGURE 12. SUPPLY CURRENT vs FREQUENCY, C_L = 1000pF, T = +25°C

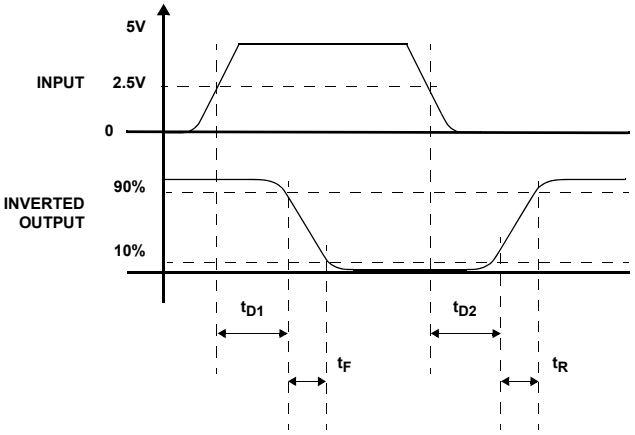
TABLE 1. TRUTH TABLE

OE	IN	V_H to OUT_H	OUT_L to V_L
0	0	Open	Open
0	1	Open	Open
1	0	Closed	Open
1	1	Open	Closed

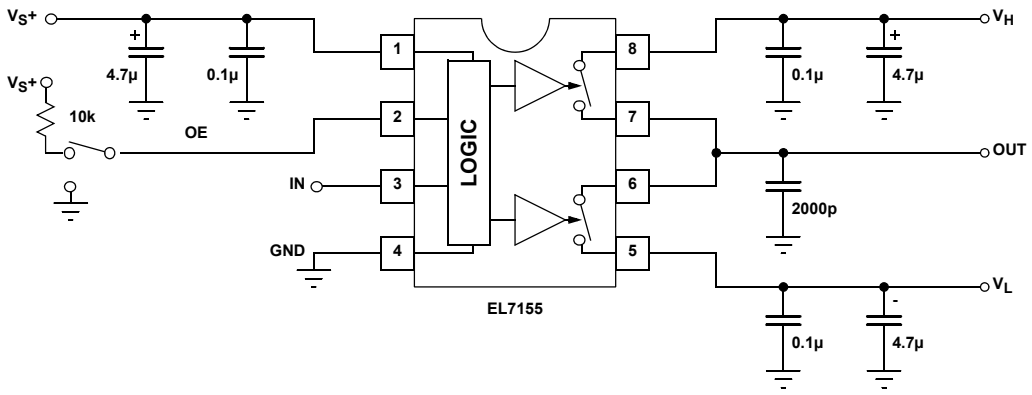
TABLE 2. OPERATING VOLTAGE RANGE

PIN	MIN (V)	MAX (V)
V_L - GND	-5	0
V_S+ - V_L	5	16.5
V_H - V_L	0	16.5
V_S+ - V_H	0	16.5
V_S+ - GND	5	16.5
3-State Output	V_L	V_H

TimingDiagrams



Standard Test Configuration



Applications Information

Product Description

The EL7155 is a high performance 40MHz pin driver. It contains two analog switches connecting V_H to OUT_H and V_L to OUT_L. Depending on the value of the IN pin, one of the two switches will be closed and the other switch open. An output enable (OE) is also supplied, which opens both switches simultaneously.

Due to the topology of the EL7155, V_L should always be connected to a voltage equal to or lower than GND. V_H can be connected to any voltage between V_L and the positive supply, V_S+.

The EL7155 is available in the 8 Ld SOIC package. Application dependent power dissipation should be calculated to ensure that the maximum junction temperature isn't violated.

3-state Operation

When the OE pin is low, the output is 3-state (floating.) The disabled output voltage is the parasitic capacitance's voltage. It can be any voltage between V_H and V_L, depending on the previous state. At 3-state, the output voltage can be driven to any voltage between V_H and V_L. The output voltage can't be driven higher than V_H or lower than V_L since the body diode at the output stage will turn on.

Supply Voltage Range and Input Compatibility

The EL7155 is designed for operation on supplies from 5V to 15V (4.5V to 16.5V maximum). Table 2 on page 7 shows the specifications for the relationship between the V_S+, V_H, V_L, and GND pins.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V_S+) of 5V, the EL7155 is also compatible with TTL inputs.

Power Supply Bypassing

When using the EL7155, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7155 necessitate the use of a bypass capacitor between the V_S+ and GND pins. It is recommended that a 2.2µF tantalum capacitor be used in parallel with a 0.1µF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the V_H and V_L pins have some level of bypassing, especially if the EL7155 is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7155 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (+125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f) \quad \text{(EQ. 1)}$$

where:

- V_S is the total power supply to the EL7155 (from V_S+ to GND)
- V_{OUT} is the swing on the output (V_H - V_L)
- C_L is the load capacitance
- C_{INT} is the internal load capacitance (100pF max)
- I_S is the quiescent supply current (3mA max)
- f is frequency

Having obtained the application's power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T_{JMAX}:

$$\theta_{JA} = \frac{(T_{JMAX} - T_{MAX})}{PD} \quad \text{(EQ. 2)}$$

where:

- T_{JMAX} is the maximum junction temperature (+125°C)
- T_{MAX} is the maximum operating temperature
- PD is the power dissipation calculated above
- θ_{JA} thermal resistance on junction to ambient

θ_{JA} is 160°C/W for the SO8 package when using a standard JEDEC JESD51-3 single-layer test board. If T_{JMAX} is greater than +125°C when calculated using the Equation 2, then one of the following actions must be taken:

1. Reduce θ_{JA} the system by designing more heatsinking into the PCB (as compared to the standard JEDEC JESD51-3).
2. Derate the application either by reducing the switching frequency, the capacitive load, or the maximum operating (ambient) temperature (T_{MAX}).

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 24, 2014	FN7279.3	Updated datasheet to new Intersil template. Updated the Ordering Information table on page 2 by removing the obsolete products and adding the -T7A part. Added revision history and about Intersil.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

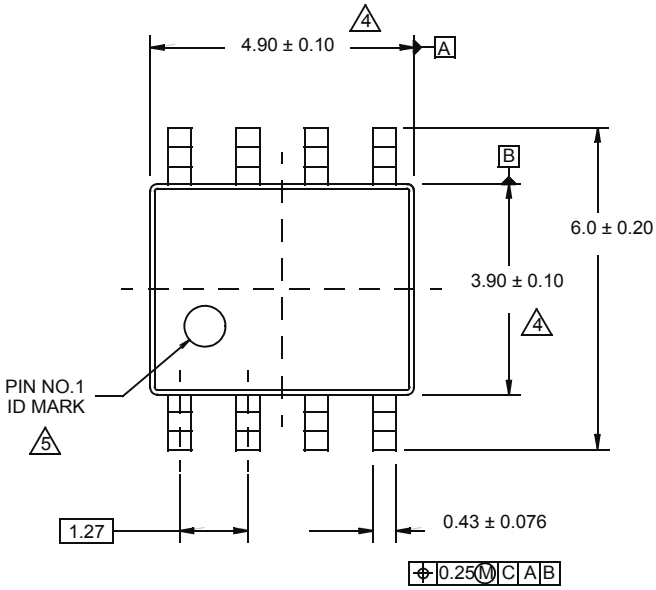
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

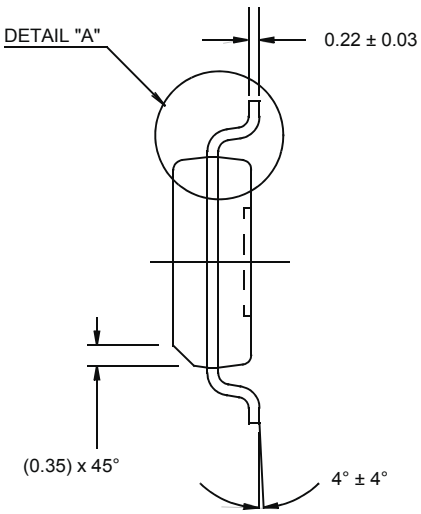
Package Outline Drawing

M8.15E

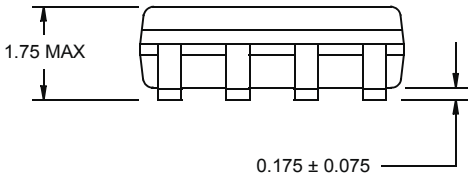
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



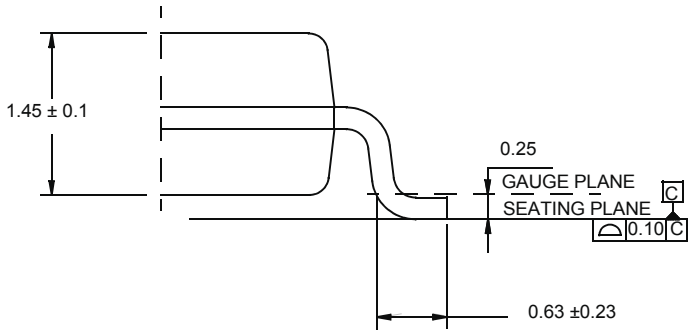
TOP VIEW



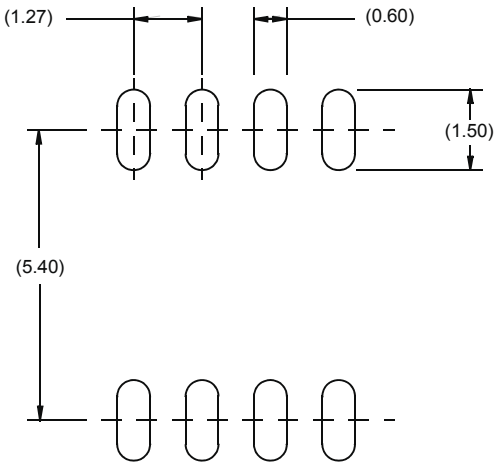
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.