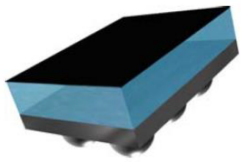
BALF-NRF01J5

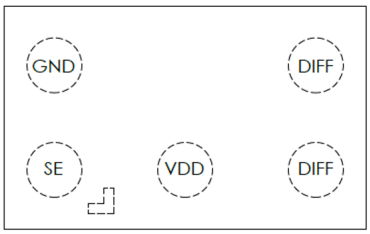
Datasheet

50 Ω ultra thin balun with integrated harmonic filter / conjugate match balun to nRF51822-CTAA/CTAC in WLCSP



Flip-Chip (5 bumps) package

Pin coordinates



Top view

Product status
BALF-NRF01J5

Features

- 50 Ω nominal input / conjugate match to Nordic Semiconductor chips nRF51822 WLCSP
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint: < 1.2 mm^2
- Extra low profile < 350 µm after reflow
- High RF performance
- RF BOM and area reduction

Applications

- 2.45 GHz impedance matched balun filter
- Optimized for Nordic's chip set nRF51822-CTAA, CTAC
- Wearable applications

Description

This device is an ultraminiature extra thin balun that integrates matching network and harmonics filter.

Matching impedance has been customized for the nRF51822-CTAA and CTAC WLCSP Nordic Semiconductor circuits.

Based on IPD technology on high resistivity silicium it optimizes the RF performance.

The BALF-NRF01J5 has been tested and approved by Nordic Semiconductor.

STMicroelectronics qualified this product intended to be used in System in Package module based on standard reliability procedure. For more details, please contact ST representatives.

It is the responsibility of the customer to perform qualification reliability verifications as it is related to customer specific application / mission profile and module design / process.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P_{IN}	Input power RF_{IN}		-	20	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114-C), all I/O one at a time while others connected to GND	2000	-		V
	ESD ratings charge device model (JESD22-C101-C)	500	-		
	ESD ratings machine model, all I/O	200	-		
T_{OP}	Operating temperature	-40	-	+85	°C

Table 2. Impedances (T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{OUT}	Nominal differential output impedance	-	matched	-	Ω
Z_{IN}	Nominal input impedance	-	50	-	Ω

Table 3. RF performances (T_{amb} = 25 °C)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f	Frequency range (bandwidth)		2400		2540	MHz
I_L	Insertion loss in bandwidth			2.2	2.4	dB
R_L	Return loss in bandwidth		9	12		dB
φimb	Phase imbalance		-7.2	7	7.2	°
Aimb	Amplitude imbalance		-0.5	0.3	0.5	dB
2f0	2nd harmonic S21 attenuation	4880 MHz	12	13.5		dB
3f0	3rd harmonic S21 attenuation	7320 MHz	24	25		dB

1.1 On-board measurements

Figure 1. Transmission (T_{amb} = 25 °C)

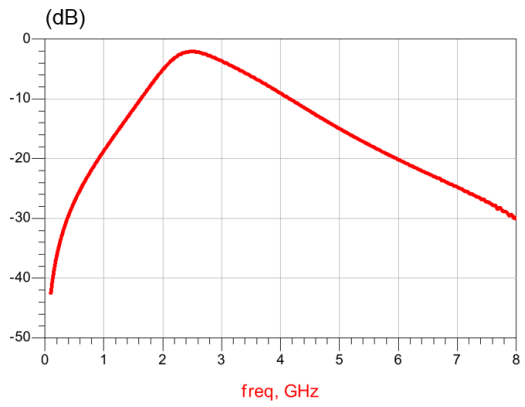


Figure 2. Insertion loss (T_{amb} = 25 °C)

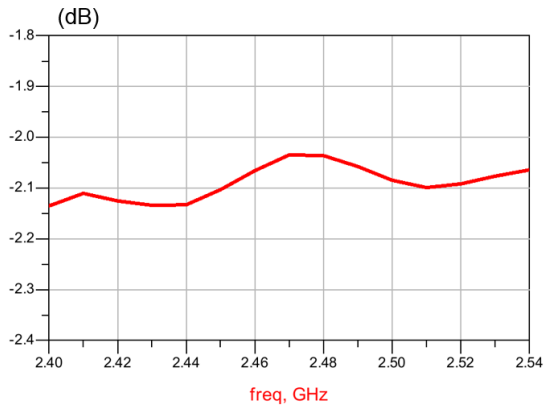


Figure 3. Return loss on SE port (T_{amb} = 25 °C)

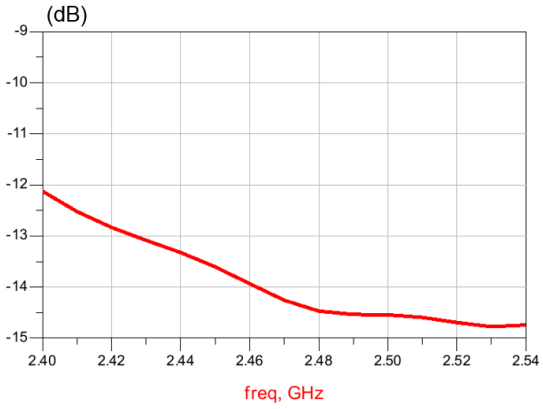


Figure 4. Return loss on DIFF port (T_{amb} = 25 °C)

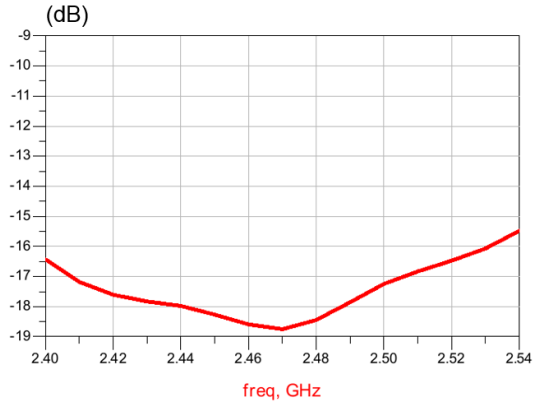


Figure 5. Amplitude imbalance (T_{amb} = 25 °C)

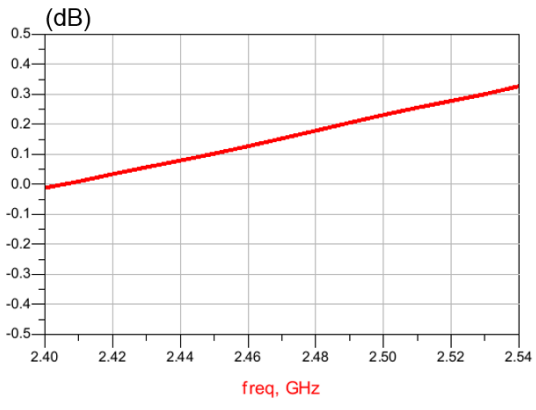
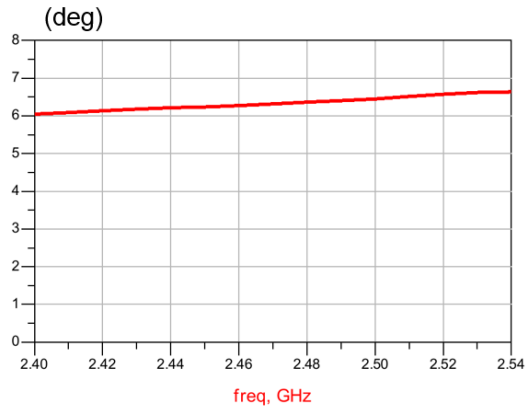


Figure 6. Phase imbalance (T_{amb} = 25 °C)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 Ultra thin Flip-Chip 5 bumps package information

- Epoxy meets UL94, V0
- Lead-free package

Figure 7. Ultra thin Flip-Chip 5 bumps package outline

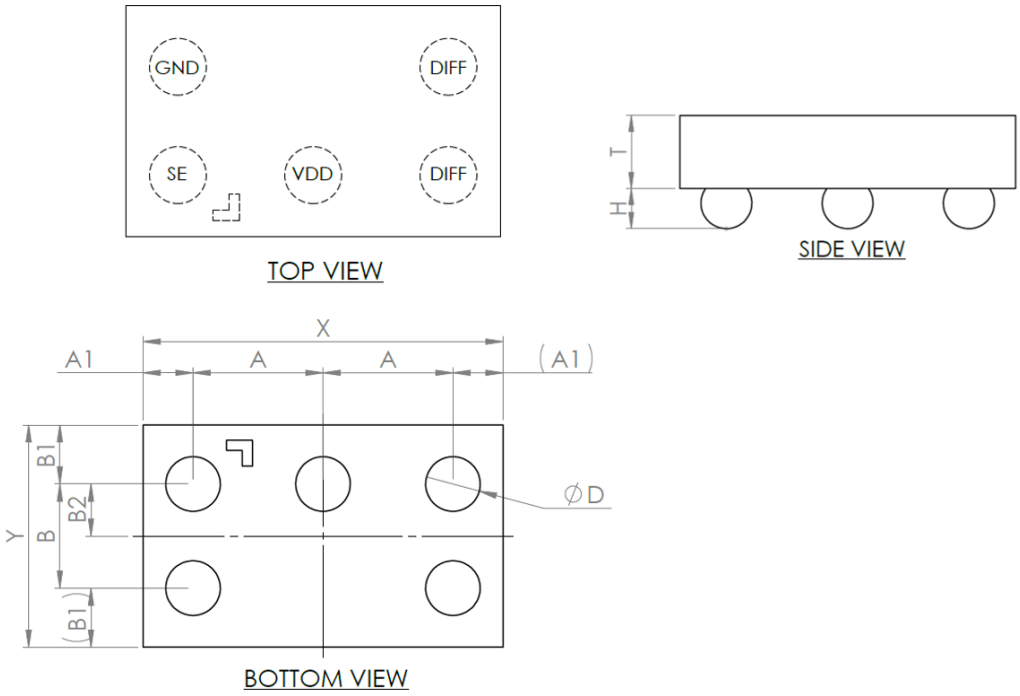
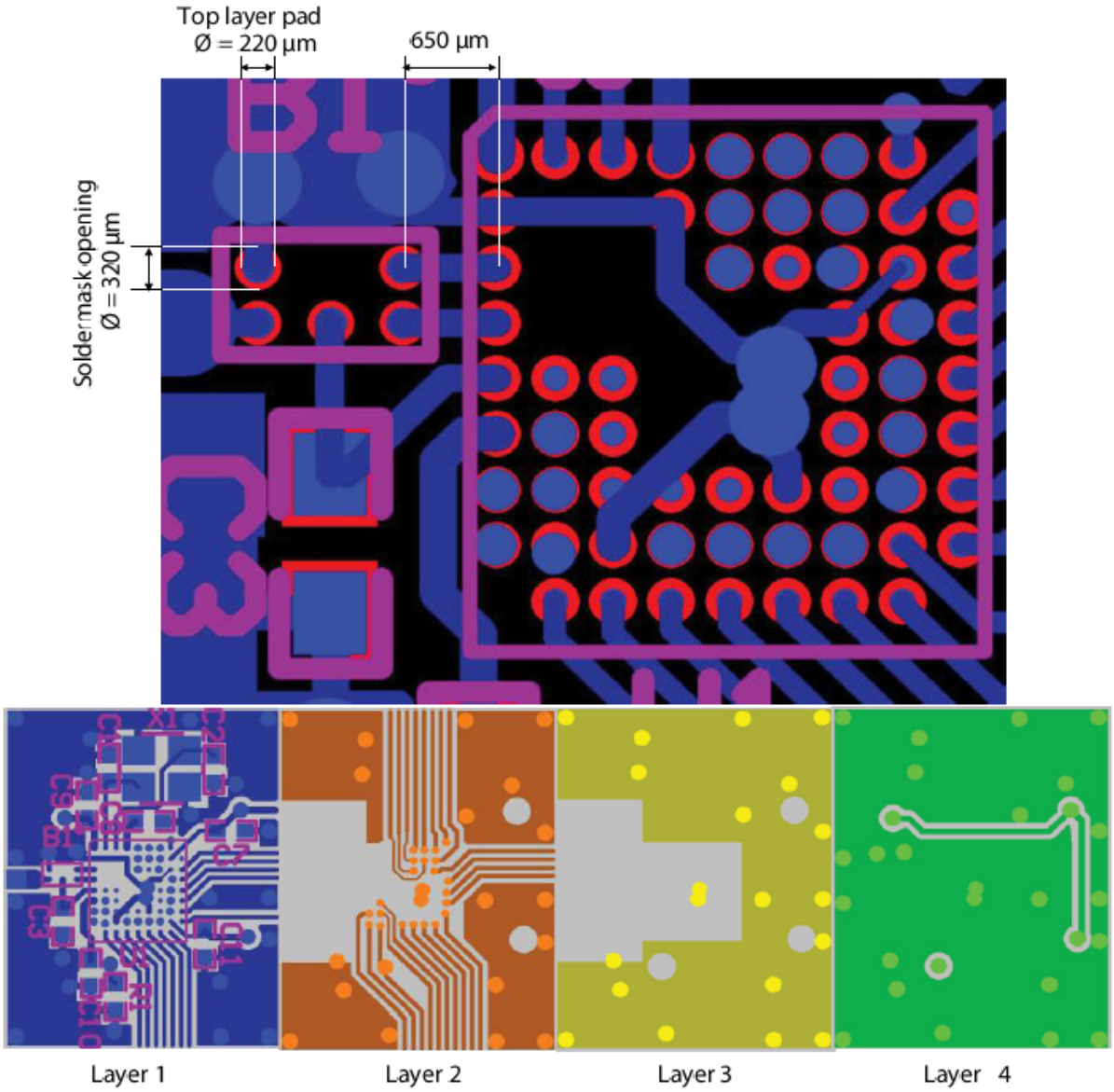


Table 4. Ultra thin Flip-Chip 5 bumps package mechanical data

Parameter	Description	Min.	Typ.	Max.	Unit
X	X dimension of the die	1315	1345	1375	µm
Y	Y dimension of the die	785	815	845	
A	X pitch		500		
B	Y pitch		400		
A1	Distance from bump to edge of die on X axis		172.5		
B1	Distance from bump to edge of die on Y axis		207.5		
B2	Distance from bump to center of die on Y axis		200		
D	Bump diameter	202	227	252	
T	Substrate thickness	190	200	210	
H	Bump height	117	142	167	

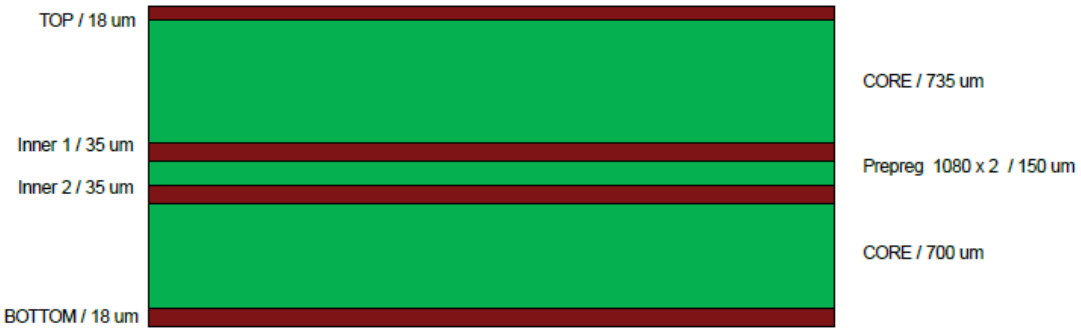
Figure 8. Recommended land pattern



Note: Screenprinting, stencil windows 290 x 290 x 100 µm3 (coeff 0.725)

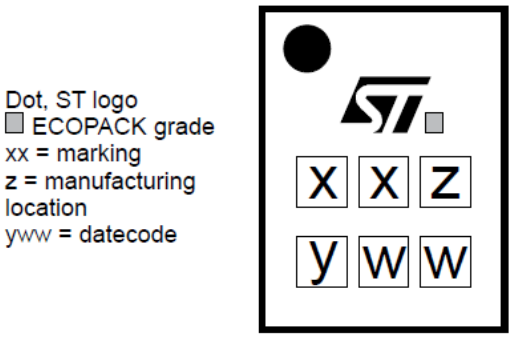
Note: to achieve minimum component height after PCB reflow, the below recommendations must be followed : in assembly process, a flux must be used, not a solder paste

Figure 9. **PCB stack-up recommendation**



2.2 Flip-chip 5 bumps packing information

Figure 10. **Marking**



Note: More packing information is available in the application note:

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

Figure 11. **Footprint - non solder mask defined**

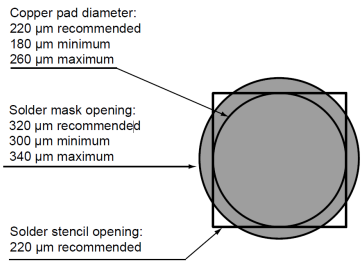
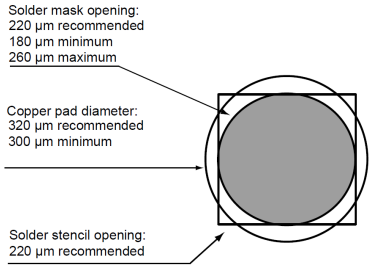


Figure 12. **Footprint - solder mask defined**



3 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BALF-NRF01J5	TL	Flip-Chip 5 bumps	0.631 mg	5000	Tape and reel

Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jun-2017	1	Initial release.
22-Feb-2018	2	Updated Description and Table 4. Ultra thin Flip-Chip 5 bumps package mechanical data.
04-Apr-018	3	Updated Table 4. Ultra thin Flip-Chip 5 bumps package mechanical data.

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