LTC4266A
Quad LTPoE++ PSE Controller

DESCRIPTION

Demonstration circuit 1815A features the LTC®4266A quad power sourcing equipment (PSE) controller, capable of delivering up to 90W of LTPoE++™ power to a compatible LTPoE++ powered device (PD). A proprietary detection/classification scheme allows mutual identification between an LTPoE++ PSE and LTPoE++ PD while remaining compatible and interoperable with existing Type 1 (13W) and Type 2 (25.5W) PDs. The LTC4266A feature set is a superset of the popular LTC4266. These PSE controllers utilize low R_{ON} external MOSFETs and 0.25Ω sense resistors which are especially important at the LTPoE++ current levels to maintain the lowest possible heat dissipation.

The LTC4266A is available in multiple power grades, allowing delivered PD power of 13W, 25.5W, 38.7W, 52.7W, 70W and 90W. The DC1815A has four variations DC1815A-A, DC1815A-B, DC1815A-C, and DC1815A-D which accommodate the four LTPoE++ power levels (Table 1).

Advanced power management features of the LTC4266A include: a 14-bit current monitoring ADC, DAC-programmable current limit, and versatile quick port shutdown. Advanced power management host software is available under a no-cost license. PD discovery uses a proprietary dual mode 4-point detection mechanism ensuring excellent immunity from false PD detection. The LTC4266A includes an I^2C serial interface operable up to 1MHz. Optional I^2C control is accessed on the DC1815A either with test points or a 14-pin ribbon cable for DC590 QuikEval™ GUI operation.

The LTC4266A is configurable on the DC1815A as an AUTO pin high, MID pin high, autonomous midspan power injector; input data from an existing network system is sent out, along with power, to a PD. The LTC4266A autonomously detects a PD, turns power on to the port, and disconnects port power without the need for a microcontroller. OUT*n* LEDs indicate that port power is present. A single 55V supply is required to power the DC1815A. A simple LDO regulator circuit on the board powers the digital supply of the LTC4266A. A $\overline{SHDN}$ pushbutton for each port shuts down the respective port and disables detection. Pre-programmed masked shutdown ports are shut down with the $\overline{MSD}$ pushbutton. A $\overline{RESET}$ pushbutton resets the LTC4266A to its AUTO pin logic state. Ports shut down with the $\overline{SHDN}$ or $\overline{MSD}$ pushbutton must be re-enabled via I^2C or a device reset with the AUTO pin high.

Design files for this circuit board are available at http://www.linear.com/demo/DC1815A

Table 1. DC1815A Power Levels and Power Supply

DEMO BOARD	PSE CONTROLLER	MAX DELIVERED PD POWER	POWER SUPPLY*
DC1815A-A	LTC4266A-1	38.7W	300W
DC1815A-B	LTC4266A-2	52.7W	300W
DC1815A-C	LTC4266A-3	70W	420W
DC1815A-D	LTC4266A-4	90W	540W

*Recommended DC1815A power supply minimum to avoid drooping in a worst-case scenario with I_{LIM} current at all four ports. Set the voltage between 54.75V to 57V for LTPoE++ compliance

QUICK START PROCEDURE

Demonstration circuit 1815A is easy to set up for evaluating the performance of the LTC4266A. Refer to Figure 1 for proper test equipment setup and follow the procedure below.

1. Set MID jumper JP5 to LO which disables midspan mode.
2. Set AUTO jumper JP4 to HI which enables AUTO pin high mode.
3. Connect a 55V to 57V power supply across AGND (+) and VEE (–). Size the power supply considering the maximum power delivered to the PDs.
4. Connect with an Ethernet cable an 802.3at Type 1 or Type 2, or LTPoE++ compatible PD to one of the four bottom ports of 2x4, RJ45 connector J1.
5. (Optional) For data tests, connect a PHY with an Ethernet cable to one of the four top ports of 2x4, RJ45 connector J1.
6. (Optional) Connect a DC590 via ribbon cable to the DC1814A and via USB to a PC. Open the QuikEval software for I²C GUI interfacing.

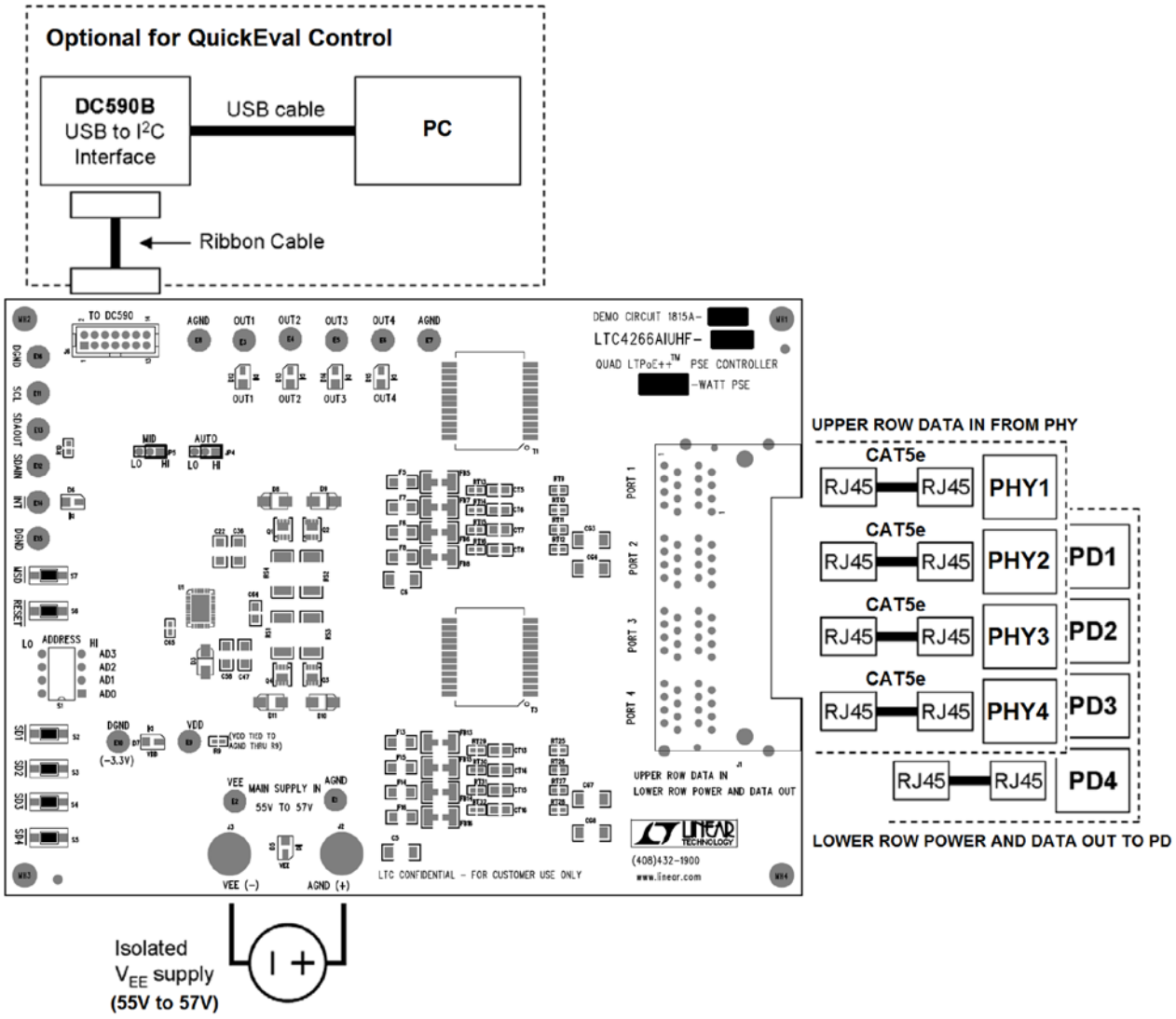


Figure 1. DC1815A Setup

OPERATION

Introduction

The DC1815A demonstrates the features and capabilities of the LTC4266A, a quad controller for LTPoE++ power sourcing equipment. The DC1815A provides a quick and simple PSE solution requiring only a VEE supply.

Supply Voltages

Select a VEE supply with enough power to sustain all four ports at maximum load. Table 1 shows the maximum delivered PD power of a single port as well as a recommended VEE power supply minimum to avoid drooping in a worst-case scenario with I_{LIM} current at all four ports.

The LTC4266A also requires a digital 3.3V supply. The DC1815A uses a simple LDO regulator circuit to power the 3.3V digital supply from the VEE supply. The LTC4266A VDD supply is allowed to be within 5V above or below AGND. On the DC1815A, VDD is tied to AGND and DGND is a negative voltage below AGND. D1, R5, Q5, R14, R15, and R25 generate the negative voltage referenced to AGND (Figure 2). These components are sized to handle the power required to supply the LTC4266A and LEDs on the DC1815A. Contact Linear Technology Applications for 3.3V options.

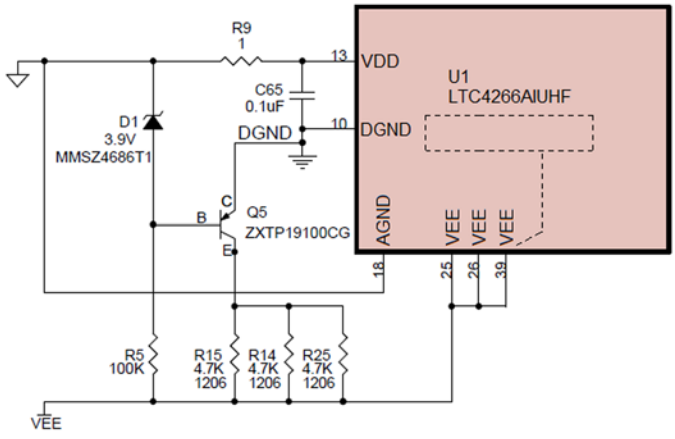


Figure 2. DC1815A LDO Circuit for the LTC4266A Digital Supply.

AUTO Pin

The LTC4266A AUTO pin is set high or low with jumper JP4 on the DC1815A. With the AUTO pin high after a device reset or power on, the LTC4266A operates in fully autonomous mode without the need for a microcontroller. The LTC4266A will automatically detect, classify, and power on IEEE 802.3at Type 1, Type 2 and LTPoE++ PDs up to the power level rating of the LTC4266A version used. For full control via I^2C, the AUTO pin is to be pulled low. Modification of the AUTO pin jumper requires a device reset or power cycle.

Endpoint vs Midspan

The LTC4266A can be configured either for endpoint or midspan operation by setting the MID pin high or low respectively. This is selected with jumper JP5 on the DC1815A. The MID pin high state enables a two second detection back-off timer. The LTC4266A must be reset or power-cycled for the MID pin to be detected. For proper midspan operation the AUTO pin must also be high.

I^2C Control

The LTC4266A is a slave-only I^2C device, and communicates with a host using a standard SMBus/I^2C 2-wire interface. On the DC1815A, a host can be connected to the SCL and SDA test points. Optionally, a DC590B board can be connected with a 14-pin ribbon cable to header J6.

The LTC4266A has separate pins for SDAIN and SDAOUT to facilitate the use of opto-couplers. The SDAIN and SDAOUT lines are tied together on the DC1815A with a shunt resistor (R10) to provide a traditional bi-directional SDA line.

The 7-bit I^2C address of the LTC4266A is $010A_3A_2A_1A_0b$, where A_3 through A_0 are determined by pins AD3 through AD0 respectively. On the DC1815A board the state of these pins are controlled by the quad DIP switch, S1. All LTC4266 chips also respond to the global address 0110000b regardless of the state of their AD3-AD0 pins.

Interrupts are signaled by the LTC4266A to the host via the $\overline{INT}$ pin. A red LED on the DC1815A indicates if the $\overline{INT}$ line is being pulled low.

OPERATION

Board Layout

Proper components placement and board layout with the LTC4266A is important to provide electrical robustness and correct operation. The following mentioned components, also shown in Figure 3, must be close to their respective LTC4266A pins with no other components in between on the connection path. Place a 0.1µF capacitor (C1) directly across VDD and DGND. Place a 1µF, 100V capacitor (C4) and a SMAJ58A TVS (D3) directly across AGND and VEE. Place the OUT 0.22µF, 100V capacitors (C22, C36, C47, and C58) directly to their respective OUT pins all going to an AGND plane.

The power path is from VEE to the sense resistor, to the MOSFET, and out to the port. Select a trace width appropriate for the maximum current.

Kelvin sensing is necessary to provide accurate current readings particularly with DC Disconnect. The sense resistors used with the LTC4266A must be 0.25Ω, 1% or better, and with a power rating that can handle the maximum DC current passed through them. A dedicated sense trace from each SENSE pin of the LTC4266A must go directly to the respective sense resistor solder pad (Figure 4). Do not connect to a copper area or trace between the sense resistor and the MOSFET.

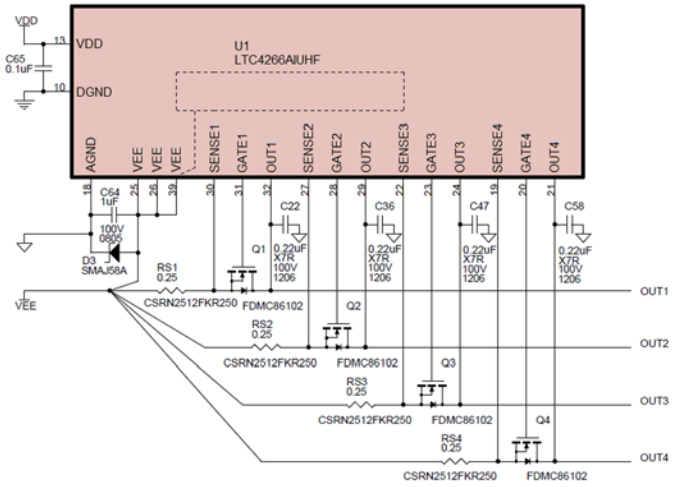


Figure 3. LTC4266A Key Application Components for Board Placement

The VEE side of the sense resistor must connect to a thick VEE plane through several large vias. At the LTC4266A, the VEE pins and exposed pad tie together on the top layer and connect to the VEE plane as well through its own multiple large vias. The via size, number of vias, copper thickness, trace width, and number of layers that connect VEE between the sense resistors and the LTC4266A VEE pins must total less than 15mΩ. A 2oz. copper thickness for the VEE copper plane must be used if there is only a single VEE plane connecting the LTC4266A VEE pins to the sense resistors.

The VEE current path from the sense resistors to the main VEE power supply must be either through a copper plane, or a thick trace. If a trace is used, it must not pass under the LTC4266A. Instead the path must go out to VEE from the sense resistors as shown in Figure 4. The VEE connection is from the VEE supply to the sense resistors to the LTC4266A VEE pins and must stay in that order.

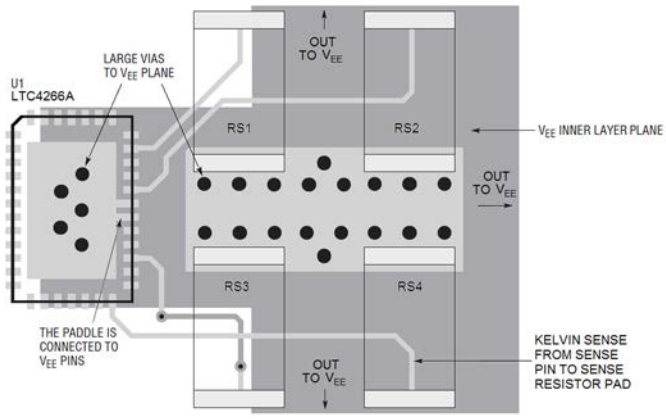


Figure 4. LTC4266A VEE Pins and Sense Resistors Connect to a VEE Inner Layer Plane. A Kelvin Sense Trace from each SENSE Pin Runs to the Respective Sense Resistor Pad. Connect the VEE Supply Path to the Sense Resistors First, Then to the LTC4266A VEE Pins

OPERATION

When laying out multiple LTC4266A devices, group the four sets of port MOSFET and sense resistor with their respective LTC4266A as shown in Figure 5. Each LTC4266A has its own copper fill area on the surface that connects to the VEE plane with multiple large vias. The net effect is to reduce the layout problem down to 4-port groups; this arrangement is expandable to any number of ports.

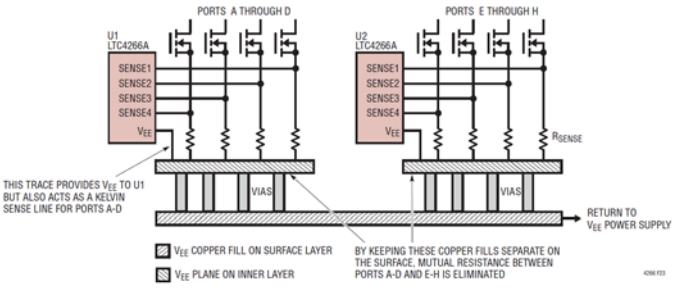


Figure 5. Multiple LTC4266 Layout Strategy to Reduce Mutual Resistance

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components are required at the main supply, at the LTC4266A supply pins and at the ports. Refer to DC1815A schematic.

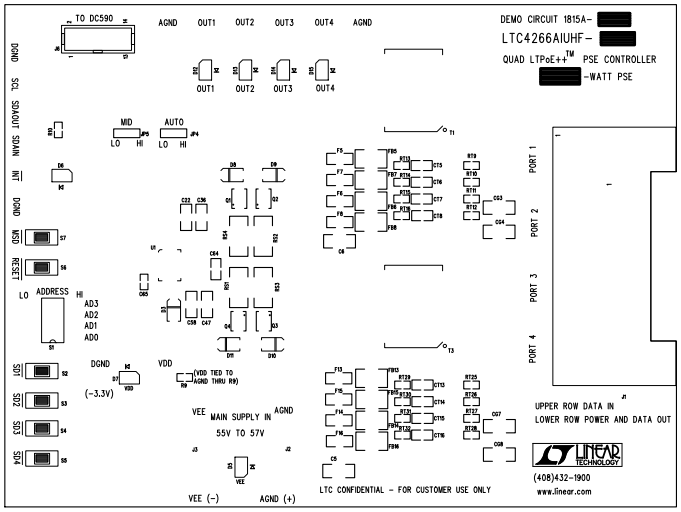
Bulk transient voltage suppression devices and bulk capacitance are required across the main PoE supply and should be sized to accommodate system level surge requirements. Across the LTC4266A AGND pin and VEE pin are an SMAJ58A, 58V TVS and a 1µF, 100V bypass capacitor. These components must be placed close to the LTC4266A pins.

In a high surge environment, a 10Ω, 0805 resistor in series from supply AGND to the LTC4266A AGND and VDD pin is recommended as shown in the schematic comments. The bulk TVS and capacitance remain on the supply side of this 10Ω resistor. The LTC4266A supply pins local TVS and capacitance remain at the LTC4266A side of this 10Ω resistor.

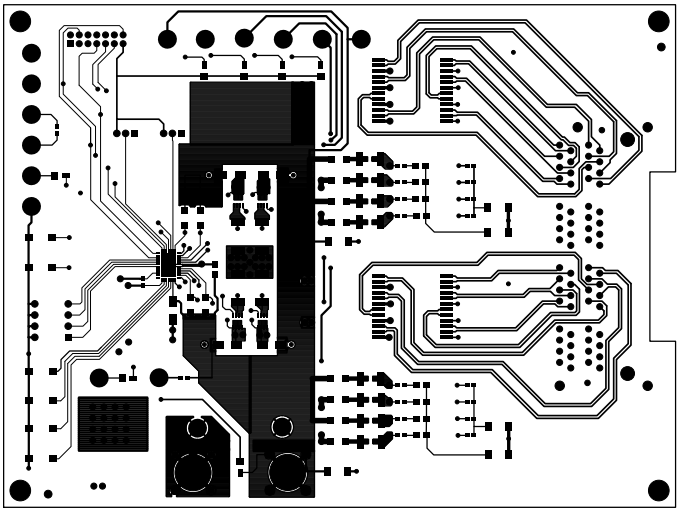
Each port requires a pair of S1B clamp diodes: one from OUT to supply AGND and one from supply VEE to OUTn. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the VEE bypass capacitance. The layout of these paths must be low impedance.

PCB LAYOUT

Top Silkscreen

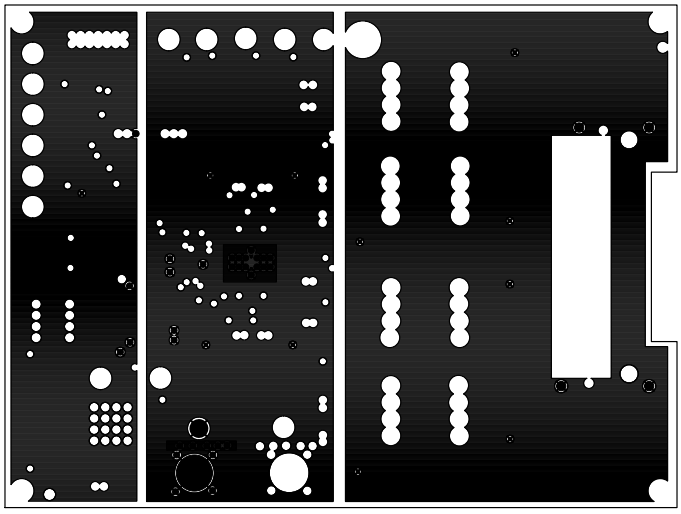


Layer 1: Top Layer

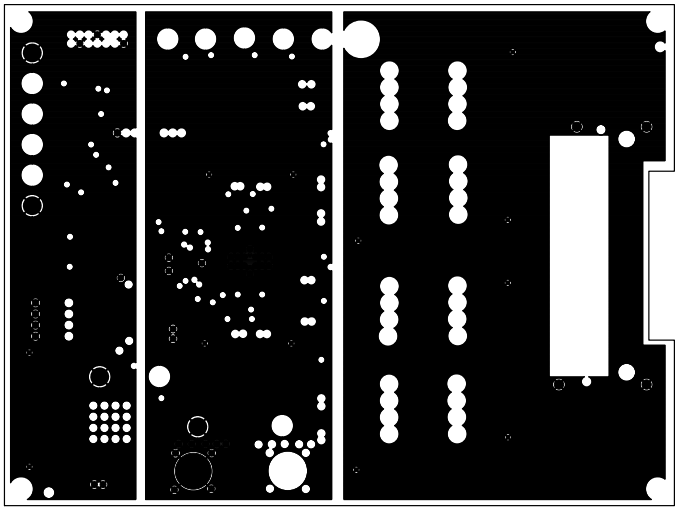


PCB LAYOUT

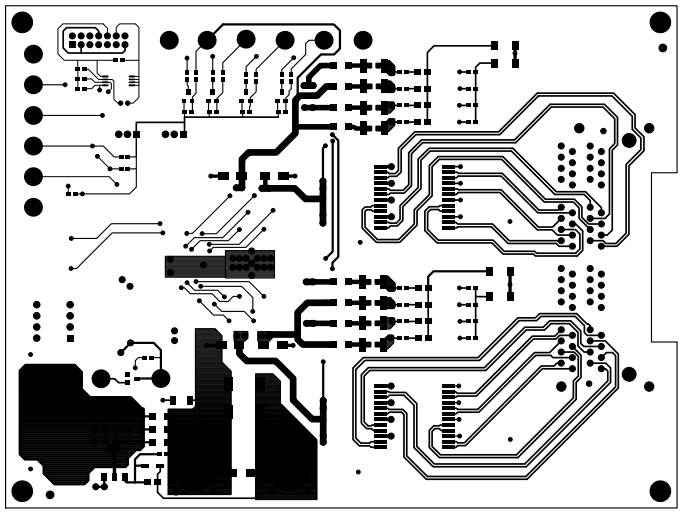
Layer 2: Plane Layer



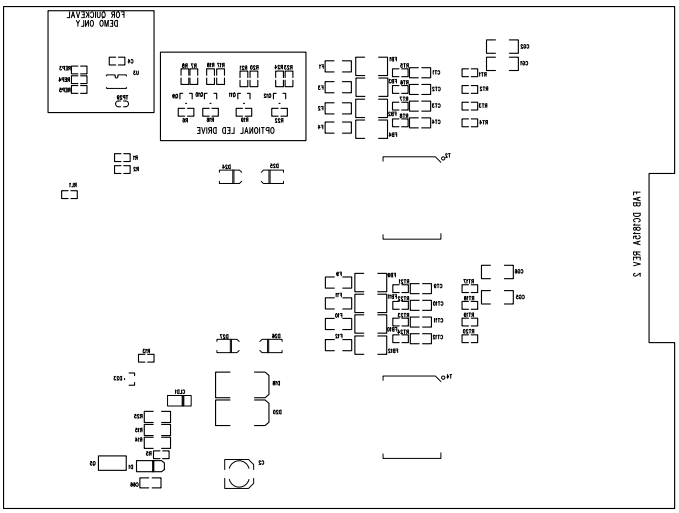
Layer 3: Plane Layer



Layer 4: Bottom Layer



Bottom Silkscreen



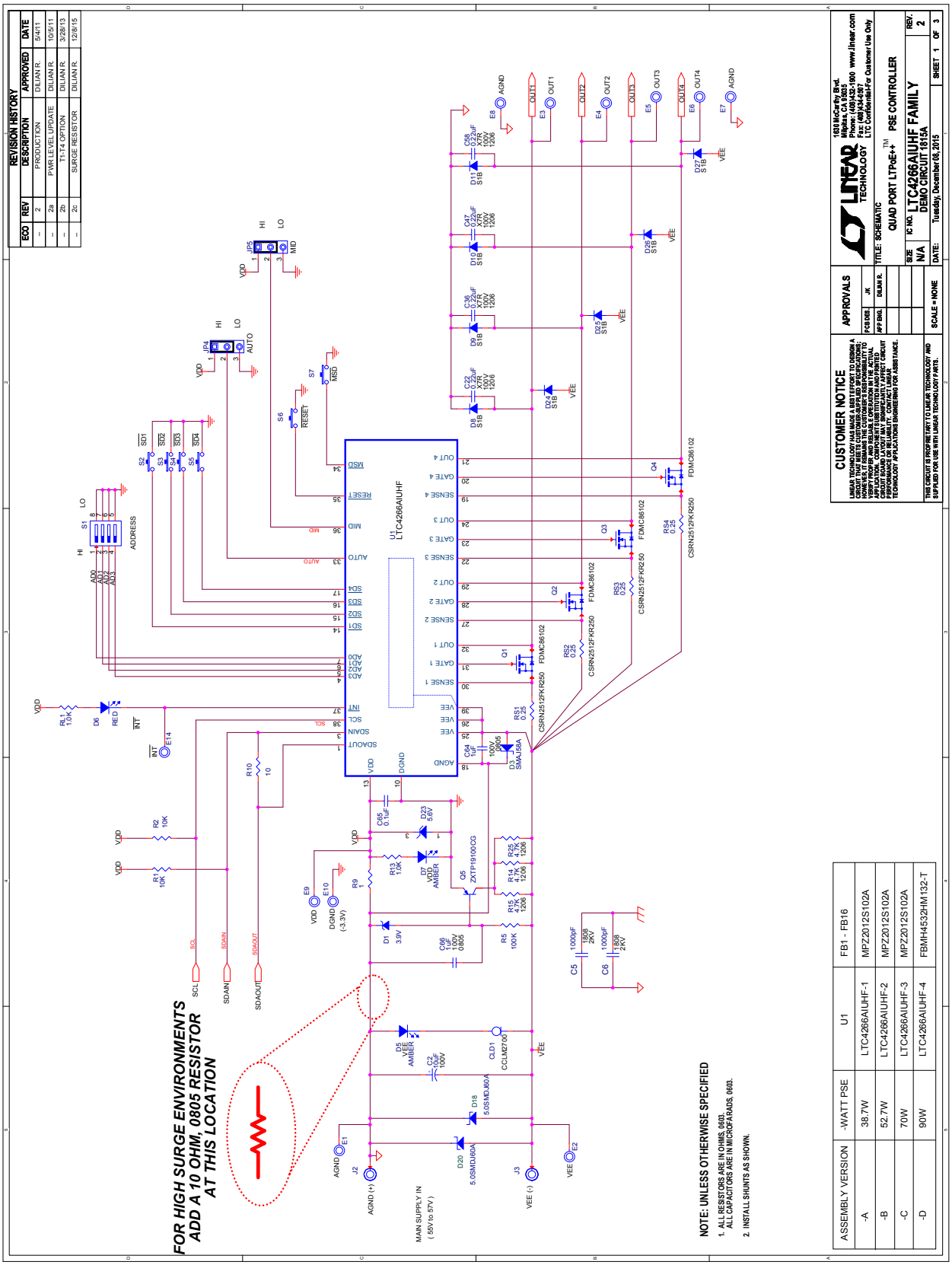
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C4, C65	CAP, 0603 0.1µF 10% 25V X7R	TDK C1608X7R1E104K
2	16	CT1-CT16	CAP, 0805 0.01µF 5% 100V X7R	AVX 0805C103JAT2A
3	2	C64, C66	CAP, 0805 1µF 10% 100V X7S	TDK C2012X7S2A105K
4	1	C2	CAP, 10uF 20% 100V ALUM.	PANASONIC EEE-2AA100UP
5	4	C22, C36, C47, C58	CAP, 1206 0.22µF 5% 100V X7R	AVX 12061C224JAT2A
6	10	C5, C6, CG1-CG8	CAP, 1808 1000pF 10% 2KV X7R	TDK C4520X7R3D102K
7	2	J2, J3	CONN, JACK, BANANA	KEYSTONE 575-4
8	1	J1	CONN, RJ45, 8-PORT DUAL ROW SHIELDED	TE CONNECTIVITY, 5569262-1
9	1	CLD1	DIODE, CURRENT LIMITING, 2.7mA, SOD-80	CENTRAL SEMI CCLM2700
10	8	D8-D11, D24-D27	DIODE, RECTIFIER, 100V 1A, SMA	FAIRCHILD S1B
11	1	D3	DIODE, TVS, 400W, 58V, SMA	DIODES INC. SMAJ58A
12	2	D18, D20	DIODE, TVS, 5000W, 60V, SMC	LITTLEFUSE 5.0SMDJ60A
13	1	D1	DIODE, ZENER 3.9V SOD-123	ON SEMI, MMSZ4686T1G
14	1	D23	DIODE, ZENER, 5.6V, SOT23	FAIRCHILD, BZX84C5V6
15	1	J6	HEADER, 2 × 7 2mm	MOLEX 87831-1420
16	2	JP4, JP5	HEADER, 3-PIN, 2mm	SAMTEC TMM-103-02-L-S
17	1	U3	IC, 24LC025, EEPROM, TSSOP	MICROCHIP 24LC025-I/ST
18	2	D5, D7	LED, AMBER	ROHM SML-010DTT86L
19	4	D12-D15	LED, GREEN	ROHM SML-010FTT86L
20	1	D6	LED, RED	ROHM SML-010VTT86L
21	16	F-1-F16	FUSE, 3A, 63VDC 1206	BEL FUSE C1Q3
22	1	R9	RES, 0603 1Ω 5% 1/10W	VISHAY CRCW06031R00JNEA
23	1	R10	RES, 0603 10Ω 5% 1/10W	VISHAY CRCW060310R0JNEA
24	1	R5	RES, 0603 100k 5% 1/10W	VISHAY CRCW0603100KJNEA
25	2	R1, R2	RES, 0603 10k 5% 1/10W	VISHAY CRCW060310K0JNEA
26	6	R8, R13, R18, R21, R24, RL1	RES, 0603 1.0k 5% 1/10W	VISHAY CRCW06031K00JNEA
27	4	R7, R17, R20, R23	RES, 0603 10M 5% 1/10W	VISHAY CRCW060310M0JNEA
28	4	R6, R16, R19, R22	RES, 0603 2M 5% 1/10W	VISHAY CRCW0603910KJNEA
29	3	REP3-REP5	RES, 0603 5.1k 5% 1/10W	VISHAY CRCW06035K10JNEA
30	32	RT1-RT32	RES, 0603 75Ω 5% 1/10W	VISHAY CRCW060375R0JNEA
31	3	R14, R15, R25	RES, 1206 4.7k 5% 1/4W	VISHAY CRCW12064K70JNEA
32	4	RS1-RS4	RES, 2512, 0.25Ω 1% 2W	STACKPOLE, CSRN2512FKR250
33	4	MH1-MH4	STAND-OFF, NYLON 0.75"	KEYSTONE, 8834(SNAP ON)
34	1	S1	SWITCH, DIP 4-POSITION	TYCO/ALCOSWITCH ADE04
35	6	S2-S7	SWITCH, MOMENTARY	WÜRTH 434 123 050 816
36	16	E1-E16	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
37	4	T1-T4	TRANSFORMER, POE++ (OPTION)	MIDCOM WÜRTH 749022016 COILCRAFT ETH1-460L
38	4	Q9-Q12	XSTR, MOSFET P-CHANNEL 30V (D-S), SOT-23	VISHAY Si2343DS
39	4	Q1-Q4	XSTR, MOSFET, N-CHANNEL 100V	FAIRCHILD FDMC86102
40	1	Q5	XSTR, PNP, 100V, SOT223	ZETEX ZXTP19100CG

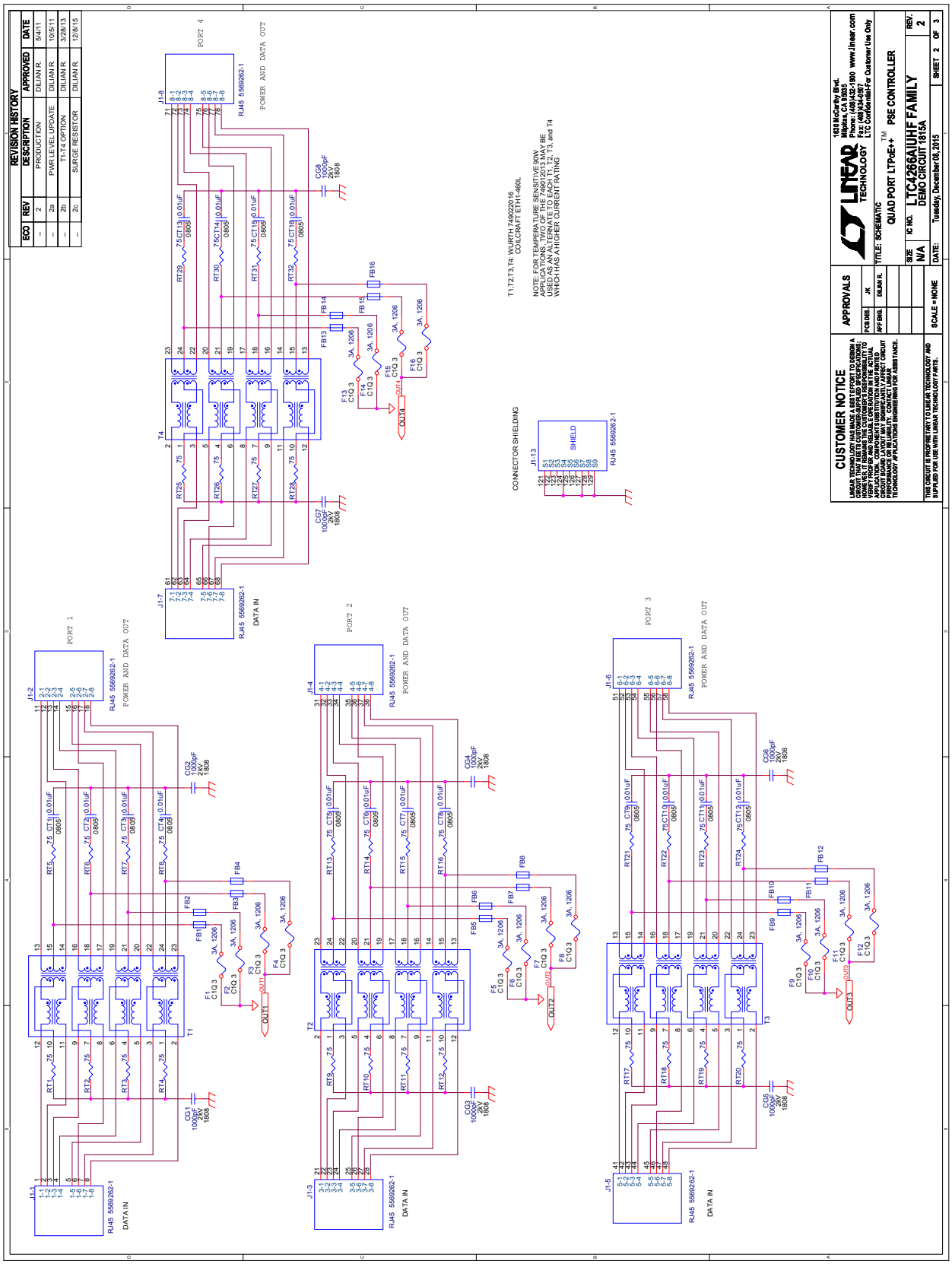
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
41	3	XJP4, XJP5	SHUNT, 2mm	SAMTEC 2SN-BK-G
42	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1815A-2
43	2		STENCIL TOP & BOTTOM	DC1815A-2
DC1815A-A				
1	1	DC1815A	GENERAL BOM	
2	16	FB1-FB16	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4274A-1, QUAD PORT 38.7W PSE CONTROLLER	LINEAR LTC4274AIUHF-1
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1815A
DC1815A-B				
1	1	DC1815A	GENERAL BOM	
2	16	FB1-FB16	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4266A-2 QUAD PORT 52.7W PSE CONTROLLER	LINEAR LTC4266AIUHF-2
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1815A
DC1815A-C				
1	1	DC1815A	GENERAL BOM	
2	16	FB1-FB16	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4266A-3, QUAD PORT 70W PSE CONTROLLER	LINEAR LTC4266AIUHF-3
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1815A
DC1815A-D				
1	1	DC1815A	GENERAL BOM	
2	16	FB1-FB16	FERRITE BEAD, 1300Ω, 1812	TAIYO YUDEN FBMH4532HM132-T
3	1	U1	IC, LTC4266A-4, QUAD PORT 90W PSE CONTROLLER	LINEAR LTC4266AIUHF-4
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1815A

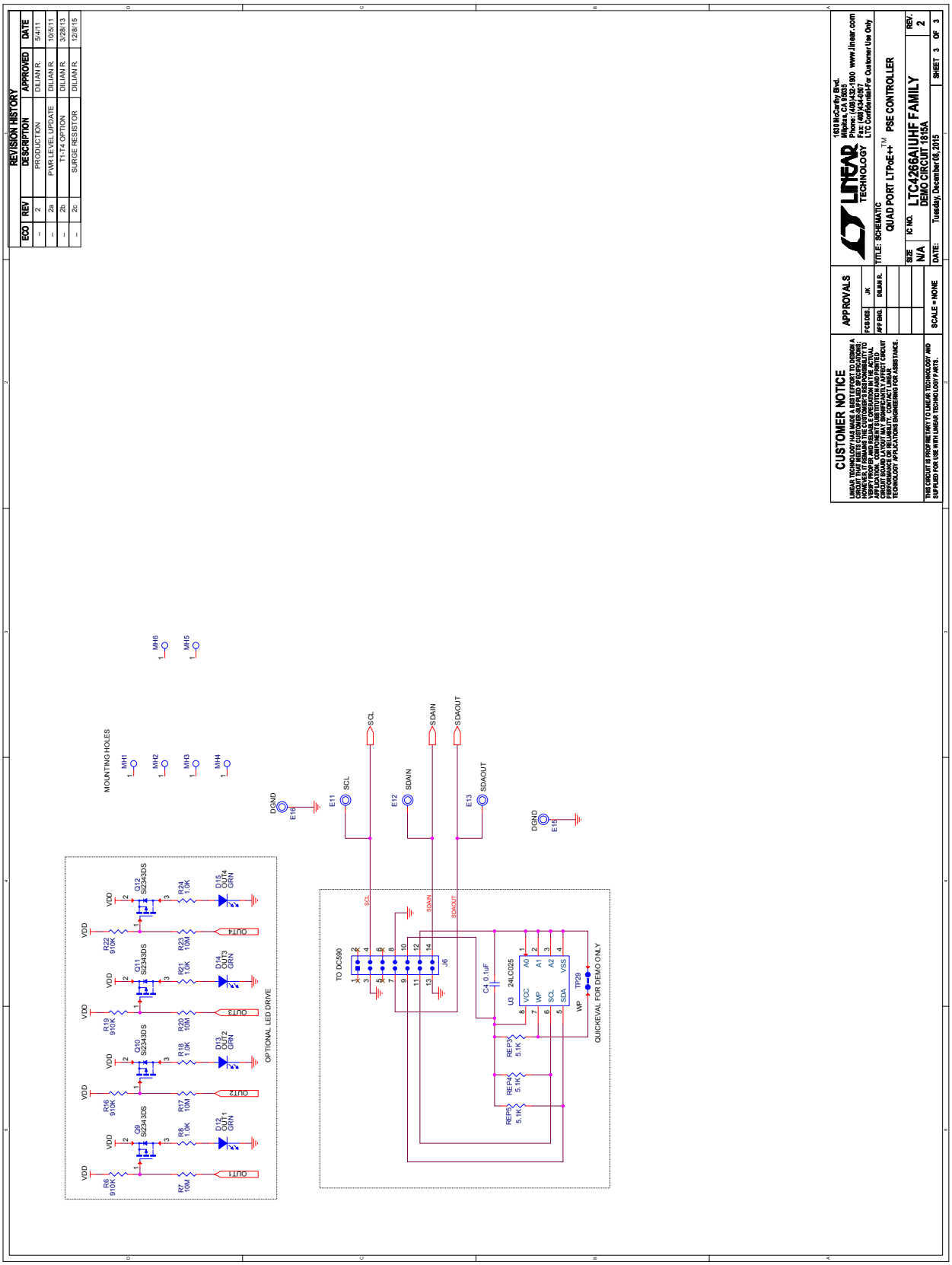
SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035