ISL54233

Wideband Differential 3:1 Multiplexer

FN7918
Rev.1.00
Dec 12, 2018

The ISL54233 is a single supply differential 3 to 1 multiplexer that operates from a single supply in the range of 2.7V to 4.6V. It was designed to multiplex between three different differential data sources, allowing the multiplexing of USB 2.0 high speed data signals, UART data signals and digital video through a common headphone connector in Personal Media Players and other portable battery powered devices.

The switch channels have low ON capacitance and high bandwidth (1.6GHz) to pass USB high speed signals (480Mbps) and digital video signals with minimal edge and phase distortion and can swing rail-to-rail to pass UART and full-speed USB signals.

All channels of the multiplexer can be turned OFF (disabled) by driving the C0 and C1 logic pins to the low state.

The ISL54233 is available in a tiny 12 Ld 2.2mmx1.4mm ultra-thin QFN and 12 Ld 3mmx3mm TQFN package. It operates over a temperature range of -40°C to +85°C.

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0 on All Ports
- Digital Video Transmission
- COM Pins Allow Negative Swings to -2V
- All Switches OFF Mode
- Power OFF Protection
- COM Pins Overvoltage Tolerant to 5.5V
- Low ON Capacitance @ 240MHz 2.8pF
- -3dB Frequency. 1.6GHz
- Single Supply Operation (V_{DD}) . . . . . 2.7V to 4.6V
- Available 12 Ld UTQFN and 12 Ld TQFN Packages
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components
- Pb-Free (RoHS Compliant)

Applications

- MP4 and Other Personal Media Players
- Mobile Phone/Smart Phone
- Tablets, Readers, GPS and MHL

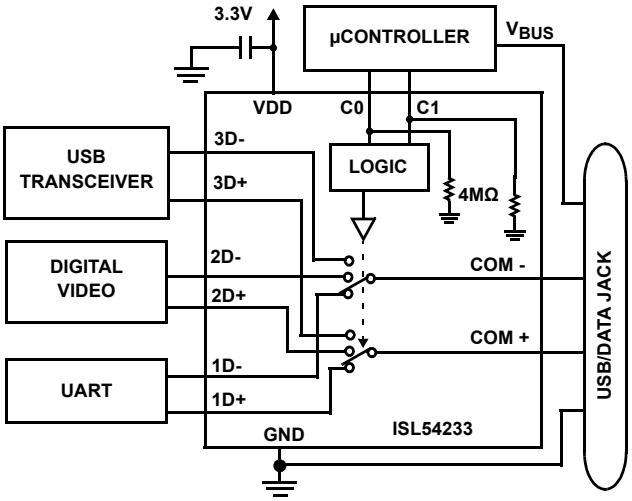


FIGURE 1. TYPICAL APPLICATION

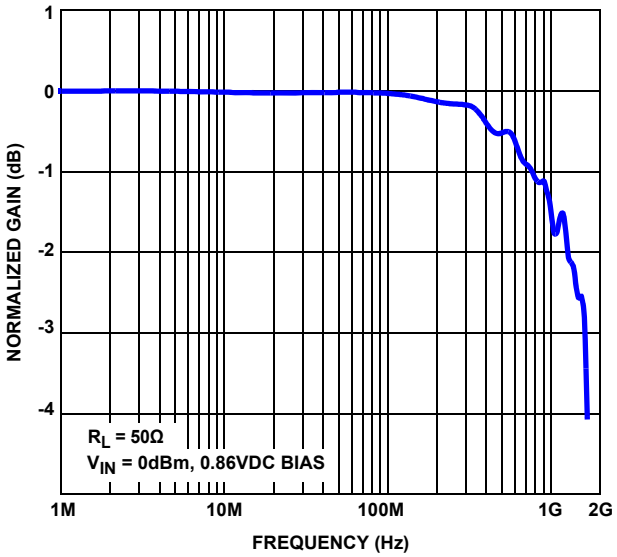
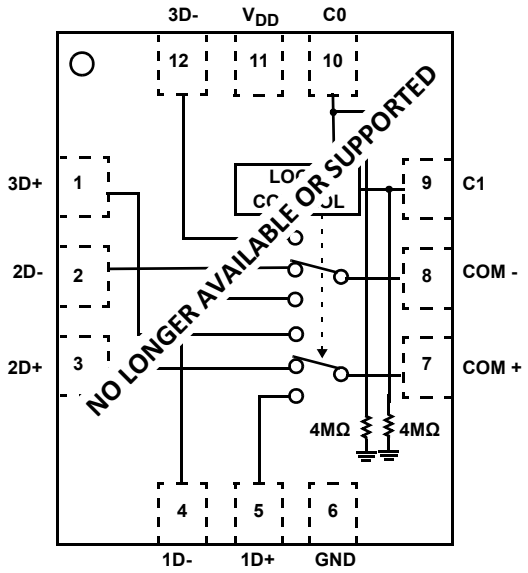


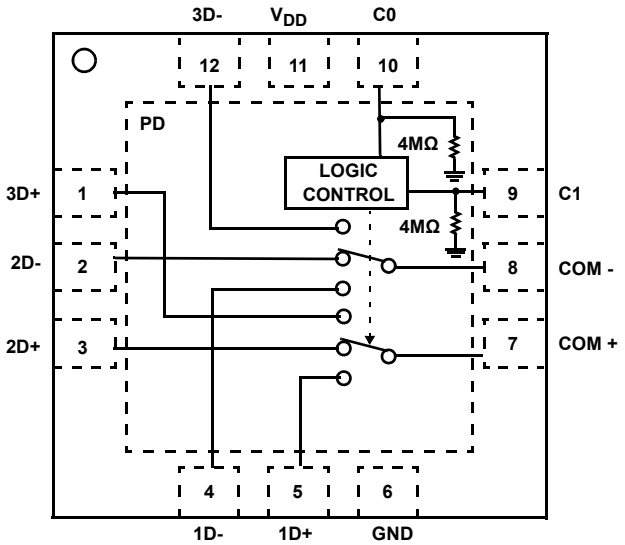
FIGURE 2. BANDWIDTH CHARACTERISTICS CURVE

Pin Configuration

12 LD 2.2X1.4 UTQFN
TOP VIEW



12 LD 3x3 TQFN
TOP VIEW



NOTE:
1. ISL54233 switches shown for C1 = Logic “1” and C0 = Logic “0”.

Pin Descriptions

UTQFN	TQFN	NAME	FUNCTION
1	1	3D+	USB3/DV Differential Input
2	2	2D-	USB2/DV Differential Input
3	3	2D+	USB2/DV Differential Input
4	4	1D-	USB1/DV Differential Input
5	5	1D+	USB1/DV Differential Input
6	6	GND	Ground Connection
7	7	COM+	Data Common Pin
8	8	COM-	Data Common Pin
9	9	C1	Digital Control Input
10	10	C0	Digital Control Input
11	11	V_{DD}	Power Supply
12	12	3D-	USB3/DV Differential Input
-	PAD	PAD	Thermal Pad. Tie to Ground or Float

Truth Table

C1	C0	MODE	COMMENTS
0	0	Wired-OR Audio	All switches open
0	1	USB/DV #1	1D- and 1D+ ON
1	0	USB/DV #2	2D- and 2D+ ON
1	1	USB/DV #3	3D- and 3D+ ON

C0, C1: Logic “0” when ≤ 0.5V or float, Logic “1” when ≥ 1.4V with V_{DD} in range of 2.7V to 3.6V.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54233IRUZ-T (Notes 2, 3) **(No longer available or supported)**	HM	-40 to +85	12 Ld 2.2mmx1.4mm UTQFN (Tape and Reel)	L12.2.2x1.4A
ISL54233IRTZ (Note 4)	4233	-40 to +85	12 Ld 3mmx3mm TQFN	L12.3x3A
ISL54233IRTZ-T (Note 2, 4)	4233	-40 to +85	12 Ld 3mmx3mm TQFN (Tape and Reel)	L12.3x3A

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54233. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to 5.5V
Input Voltages
  1D+, 1D-, 2D+, 2D-, 3D+, 3D- . . . . . -2V to 5.5V
  C0, C1 (Note 6) . . . . . -0.3V to 5.5V
Output Voltages
  COM-, COM+ . . . . . -2V to 5.5V
Continuous Current (1D-, 1D+, 2D-, 2D+, 3D-, 3D+). . . . . ±40mA
Peak Current (1D-, 1D+, 2D-, 2D+, 3D-, 3D+)
  (Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
  Human Body Model (Tested per JESD22-A114F) . . . . . >5kV
  Machine Model (Tested per JESD22-A115B) . . . . . >400V
  Charged Device Model (Tested per JESD22-C110D) . . . . . >2kV
Latch-up (Tested per JESD-78B; Class 2, Level A) . . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
12 Ld UTQFN Package (Notes 7, 10)	155	90
12 Ld TQFN Package (Notes 8, 9)	58	1.0

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range . . . . . 2.7V to 4.6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on C1 and C0 exceeding GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
9. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
10. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L} = 0.5V, (Note 11), **Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	V_{DD} = 2.7V to 4.6V	Full	**-1**	-	**V_{DD}**	V
ON-Resistance, r_{ON}	V_{DD} = 2.7V, I_{COMx} = 17mA, V_{D+} or V_{D-} = 0V to 400mV (see Figure 5, Note 15)	25	-	6	8	Ω
		Full	-	-	**10**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 2.7V, I_{COMx} = 17mA, V_{D+} or V_{D-} = Voltage at max r_{ON}, (Notes 15, 16)	25	-	0.07	0.5	Ω
		Full	-	-	**0.55**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 2.7V, I_{COMx} = 17mA, V_{D+} or V_{D-} = 0V to 400mV, (Notes 14, 15)	25	-	0.32	0.8	Ω
		Full	-	-	**1.2**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, I_{COMx} = 17mA, V_{D+} or V_{D-} = 3.3V (see Figure 5, Note 15)	+25	-	9.5	15	Ω
		Full	-	-	**20**	Ω
OFF Leakage Current, $I_{XD+(OFF)}$ or $I_{XD-(OFF)}$, $I_{COMX(OFF)}$	V_{DD} = 4.6V, All OFF Mode (C0 = 0.5V, C1 = 0.5V), V_{COM-} or V_{COM+} = 0.3V, 3.3V, V_{XD+} or V_{XD-} = 3.3V, 0.3V	25	-15	-	15	nA
		Full	**-20**	-	**20**	nA
ON Leakage Current, $I_{XD+(ON)}$ or $I_{XD-(ON)}$, $I_{COMX(ON)}$	V_{DD} = 4.6V, V_{XD+} or V_{XD-} = 0.3V, 3.3V, V_{COM-} or V_{COM+} = 0.3V, 3.3V	25	-20	-	20	nA
		Full	**-25**	-	**25**	nA
DPDT DYNAMIC CHARACTERISTICS						
All OFF to ON or ON to All OFF Address Transition Time, t_{TRANS}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (see Figure 3)	25	-	125	-	ns
Data Channel to Data Channel Address Transition Time, t_{TRANS}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (see Figure 3)	25	-	125	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.6V, R_L = 50Ω, C_L = 10pF, (see Figure 4)	25	-	30	-	ns
Skew, ($t_{SKEWOUT}$ - t_{SKEWIN})	V_{DD} = 3.0V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps, (Duty Cycle = 50%) (see Figure 8)	25	-	75	-	ps
Total Jitter, t_J	V_{DD} = 3.0V, R_L = 50Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps	25	-	210	-	ps

Electrical Specifications - 2.7V to 3.6V Supply

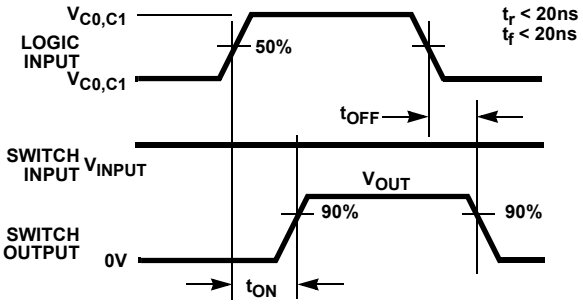
Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L} = 0.5V, (Note 11), **Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Rise/Fall Degradation (Propagation Delay), t_{PD}	V_{DD} = 3.0V, R_L = 45Ω, C_L = 10pF, (see Figure 8)	25	-	250	-	ps
Crosstalk	V_{DD} = 3.0V, R_L = 50Ω, f = 240MHz	25	-	-36	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 240MHz	25	-	-32	-	dB
-3dB Bandwidth	Signal = 0dBm, 0.2VDC offset, R_L = 50Ω	25	-	1.6	-	GHz
OFF Capacitance, C_{XD+OFF}, C_{XD-OFF}	f = 1MHz, V_{DD} = 3.0V (see Figure 6)	25	-	3	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.0V (see Figure 6)	25	-	6	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 240MHz, V_{DD} = 3.0V	25	-	2.8	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**		**4.6**	V
Positive Supply Current, I_{DD} (ALL OFF Mode)	V_{DD} = 3.6V, C1 = GND, C0 = GND	25	-	6.5	8	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (USB1 Mode)	V_{DD} = 3.6V, C1 = GND, C0 = V_{DD}	25	-	6.5	8	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (USB2 Mode)	V_{DD} = 3.6V, C1 = V_{DD}, C0 = GND	25	-	6.5	8	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (USB3 Mode)	V_{DD} = 3.6V, C0 = C1 = V_{DD}	25	-	6.5	8	µA
		Full	-	-	**15**	µA
Power OFF COMx Current, I_{COMx}	V_{DD} = 0V, C0 = C1 = Float, COMx = 5.25V	25	-	-	1	µA
Power OFF Logic Current, I_{C0}, I_{C1}	V_{DD} = 0V, C0 = C1 = 5.25V	25	-	11	-	µA
Power OFF D+/D- Current, I_{XD+}, I_{XD-}	V_{DD} = 0V, C0 = C1 = Float, XD- = XD+ = 5.25V	25	-	5	-	µA
DIGITAL INPUT CHARACTERISTICS						
C0, C1 Voltage Low, V_{C0L}, V_{C1L}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
C0, C1 Voltage High, V_{C0H}, V_{C1H}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	**5.25**	V
C0, C1 Input Current, I_{C0L}, I_{C1L}	V_{DD} = 3.6V, C0 = C1 = 0V or Float	Full	**-50**	6.2	**50**	nA
C0, C1 Input Current, I_{C0H}, I_{C1H}	V_{DD} = 3.6V, C0 = C1 = 3.6V	Full	**-2**	1.6	**2**	µA
C0, C1 Pull-Down Resistor, R_{Cx}	V_{DD} = 3.6V, C0 = C1 = 3.6V, Measure current into C0 or C1 pin and calculate resistance value.	Full	-	4	-	MΩ

NOTES:

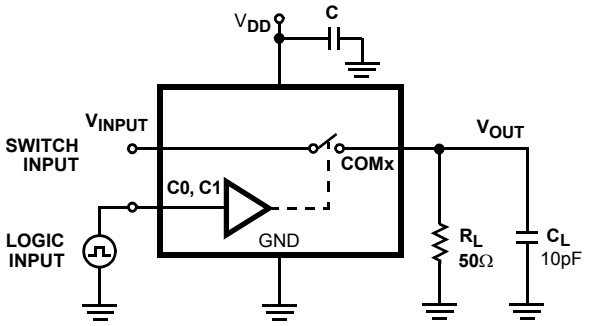
11. V_{logic} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
15. Limits established by characterization and are not production tested.
16. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between 1D+ and 1D- or between 2D+ and 2D- or between 3D+ and 3D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 3A. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 3B. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 3. SWITCHING TIMES

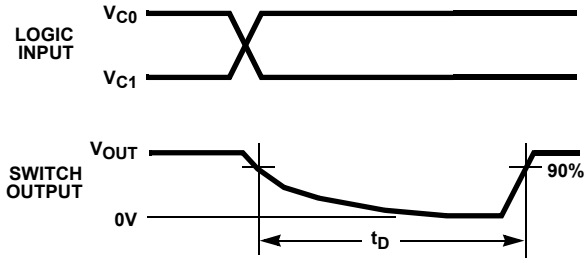
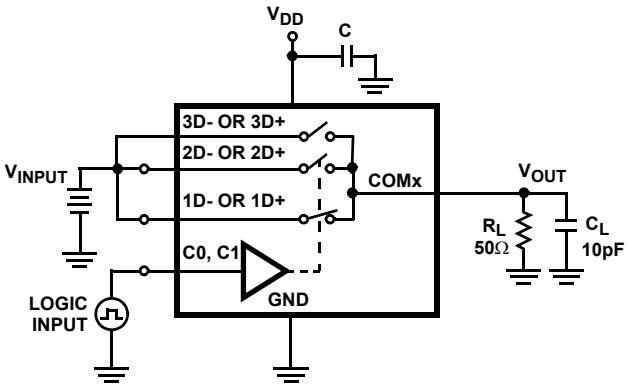


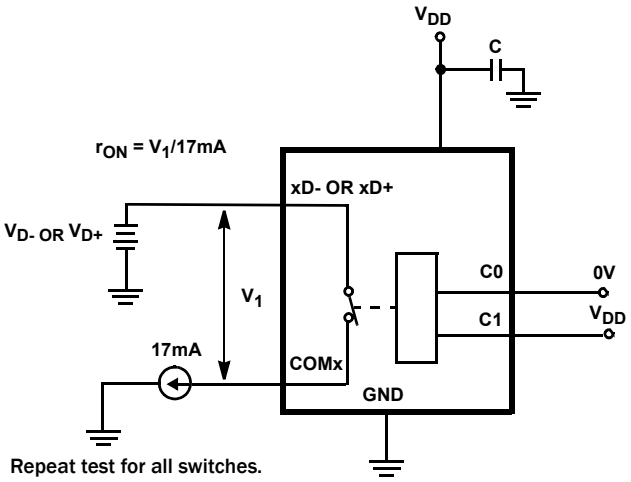
FIGURE 4A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

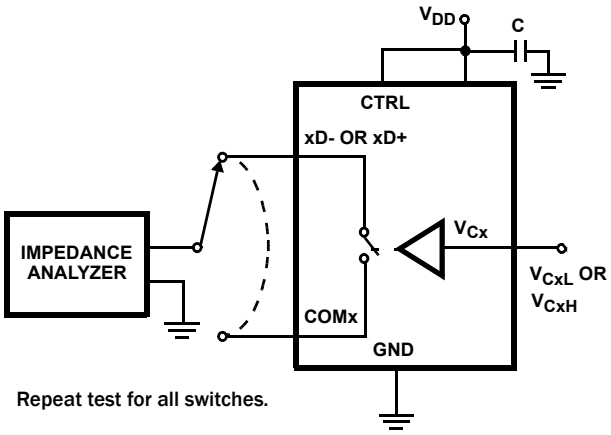
FIGURE 4B. TEST CIRCUIT

FIGURE 4. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

FIGURE 5. r_{ON} TEST CIRCUIT



Repeat test for all switches.

FIGURE 6. CAPACITANCE TEST CIRCUIT

Test Circuits and Waveforms (Continued)

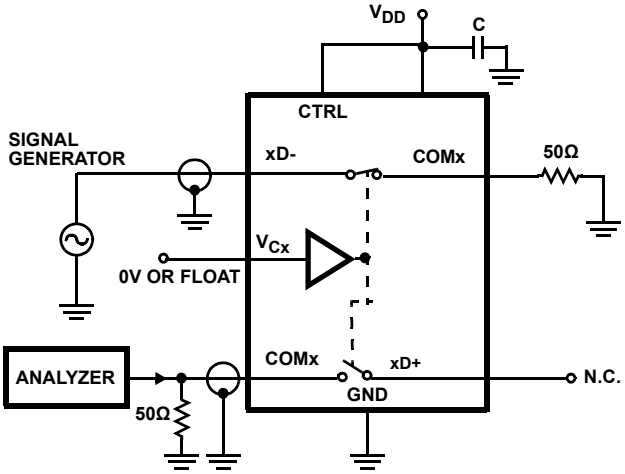


FIGURE 7. CROSSTALK TEST CIRCUIT

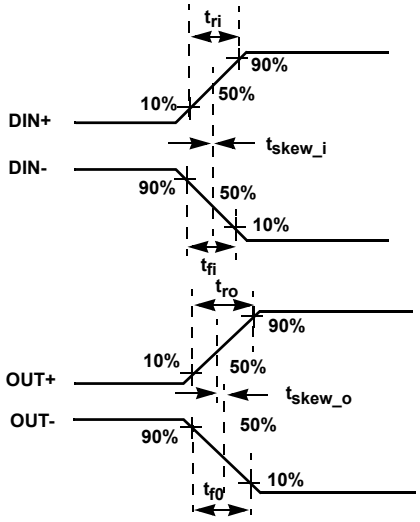
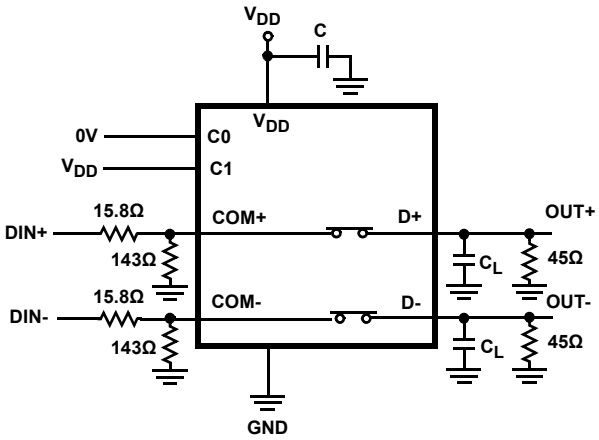


FIGURE 8A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

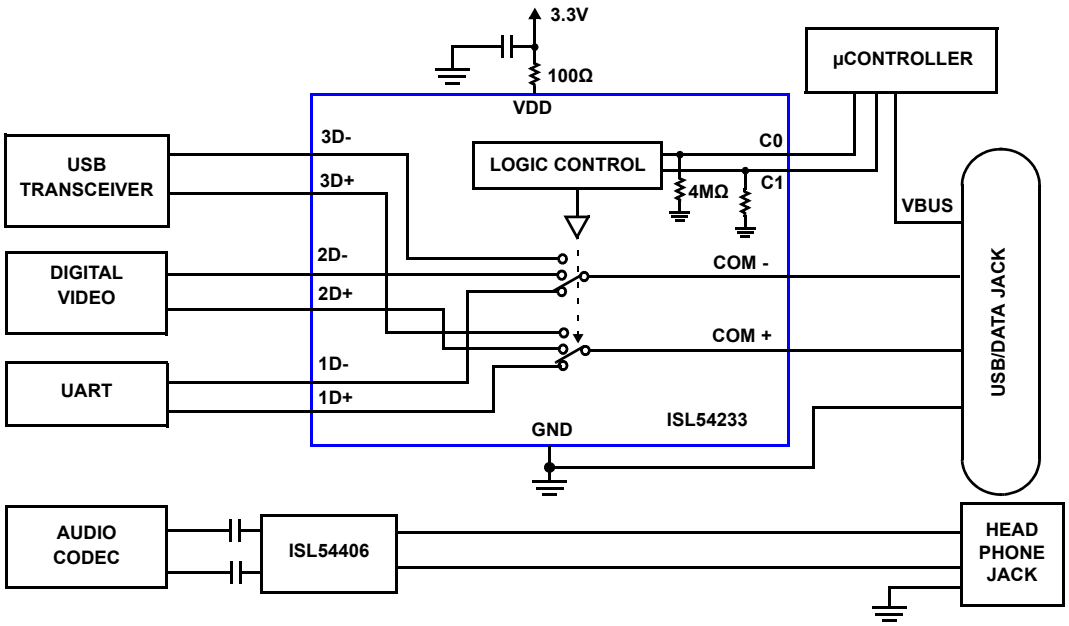
|tskew_0| Change in Skew through the Switch for Output Signals

|tskew_i| Change in Skew through the Switch for Input Signals

FIGURE 8B. TEST CIRCUIT

FIGURE 8. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54233 device consists of dual SP3T (single pole/triple throw) analog switches. It operates from a single DC power supply in the range of 2.7V to 4.6V. It was designed to function as a differential 3 to 1 multiplexer to select between three different differential data signals. It is offered in tiny UTQFN and TQFN packages for use in MP3 players, PDAs, cellphones, and other personal media players.

The device consists of six 6Ω data switches. It was designed to pass high-speed USB differential data and digital video signals with minimal edge and phase distortion. It can swing rail-to-rail to pass UART and full-speed USB signals.

The COM pins can accept signals that swing below ground by as much as -2V. This allows an audio source to be wired-OR connected at the COM pins.

The ISL54233 was specifically designed for MP3 players, personal media players and cellphone applications that need to combine three differential data channels into a single shared connector, thereby saving space and component cost. This functionality is shown in the Typical Application Block Diagram on page 1.

A detailed description of the switches is provided in the following sections.

Data Switches

The six data switches (1D+, 1D-, 2D+, 2D-, 3D+, 3D-) are 6Ω bidirectional switches that were specifically designed to pass high-speed USB differential data signals in the range of 0V to 400mV. The switches have low capacitance and high bandwidth to pass USB high-speed signals (480Mbps) with minimum edge and phase distortion to meet USB 2.0 signal quality specifications. See Figures 15 and 16 for high-speed Eye Pattern taken with the switch in the signal path.

These switches can also swing rail-to-rail and pass USB full-speed (12Mbps) and UART signals with minimal distortion. See Figure 17 for USB full-speed Eye Pattern taken with the switch in the signal path.

The maximum normal operating signal range for the USB switches is from -1V to V_{DD}. The signal voltage at D- and D+ should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1V for normal operation.

Fault Protection and Power-Off Protection

However, in the event that the USB 5.25V V_{BUS} voltage were shorted to one or both of the COM pins, the ISL54233 has fault protection circuitry to prevent damage to the ISL54233 part. The fault circuitry allows the signal pins (COM-, COM+, 1D-, 1D+, 2D-, 2D+, 3D-, 3D+) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 4.6V. This fault condition causes no stress to the IC.

In addition, when V_{DD} is at 0V (ground) all switches are OFF and the fault voltage is isolated from the other side of the switch (Power-Off Protection).

When V_{DD} is in the range of 2.7V to 4.6V, the fault voltage will pass through to the output of an active switch channel.
Note: During the fault condition, normal operation is not guaranteed until the fault condition is removed.

ISL54233 Operation

The discussion that follows will discuss using the ISL54233 in the “Application Block Diagram” on page 8.

POWER

The power supply connected at V_{DD} (pin 11) provides power to the ISL54233 part. Its voltage should be kept in the range of 2.7V to 4.6V. In a typical application, V_{DD} will be in the range of 2.7V to 4.3V and will be connected to the battery or LDO of the MP3 player or cellphone.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the V_{DD} pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the V_{DD} pin as possible.

LOGIC CONTROL

The state of the ISL54233 device is determined by the voltage at the C1 pin (pin 9) and the C0 pin (pin 10). Refer to the "Truth Table" on page 2.

The C1 pin and C0 pin are internally pulled low through 4MΩ resistors to ground and can be tri-stated or left floating.

The C1 pin and C0 pin can be driven with a voltage that is higher than the V_{DD} supply voltage. They can be driven up to 5.25V with the V_{DD} supply in the range of 2.7V to 4.6V. Driving the logic higher than the supply rail will cause the logic current to increase. With V_{DD} = 2.7V and V_{LOGIC} = 5.25V, I_{LOGIC} current is approximately 5.5µA.

Logic Control Voltage Levels

With V_{DD} in the range of 2.7V to 3.6V the logic levels are: C1, C0 = Logic "0" (Low) when ≤ 0.5V or Floating. C1, C0 = Logic "1" (High) when ≥ 1.4V.

ALL SWITCHES OFF Mode

If the C1 pin = Logic "0" and C0 pin = Logic "0" the part will be in the ALL SWITCHES OFF mode. In this mode, the 3D- and 3D+ data switches, the 2D- and 2D+ data switches, and the 1D- and 1D+ data switches will be OFF (high impedance).

The COM pins can accommodate signals that swing below ground by as much as -2V. This allows an audio CODEC to be connected to the COM pins when the device is in the all off state.

USB/DV 1 Mode

If the C1 pin = Logic "0" and C0 pin = Logic "1" the part will go into USB/DV1 mode. The 1D- and 1D+ switches are ON and the 2D- and 2D+ switches and 3D- and 3D+ will be OFF (high impedance).

USB/DV 2 Mode

If the C1 = Logic "1" and C0 pin = Logic "0" the part will be in the USB/DV2 mode. The 2D- and 2D+ switches will be ON and the 1D- and 1D+ switches and the 3D- and 3D+ will be OFF (high impedance).

USB/DV 3 Mode

If the C1 pin = Logic "1" and C0 pin = Logic "1" the part will be in the USB/DV3 mode. The 3D- and 3D+ switches are ON, and the 1D- and 1D+ switches and 2D- and 2D+ switches will be OFF (high impedance).

Printed Circuit Board Design for High Frequency Performance

In 50Ω systems, the ISL54233 has a -3dB bandwidth of 1.6GHz (see Figure 19).

To achieve this high bandwidth requires careful design and layout of the PCB board. Signal traces must be designed to minimize reflections and reduce parasitic resistance, inductance and capacitance that degrade the frequency response performance.

Figure 9 shows a picture of the engineering board used to measure the frequency response of the ISL54233 part. The board was specifically design for taking high frequency bandwidth measurements. The board was made with special materials and was carefully layed out using RF board techniques to maximize it for high frequency operation.

The next section, "Board Layout Guidelines", will provide a list of the PCB board requirements needed to get the maximum bandwidth from the ISL54233 part when tested with a 50Ω Network Analyzer.

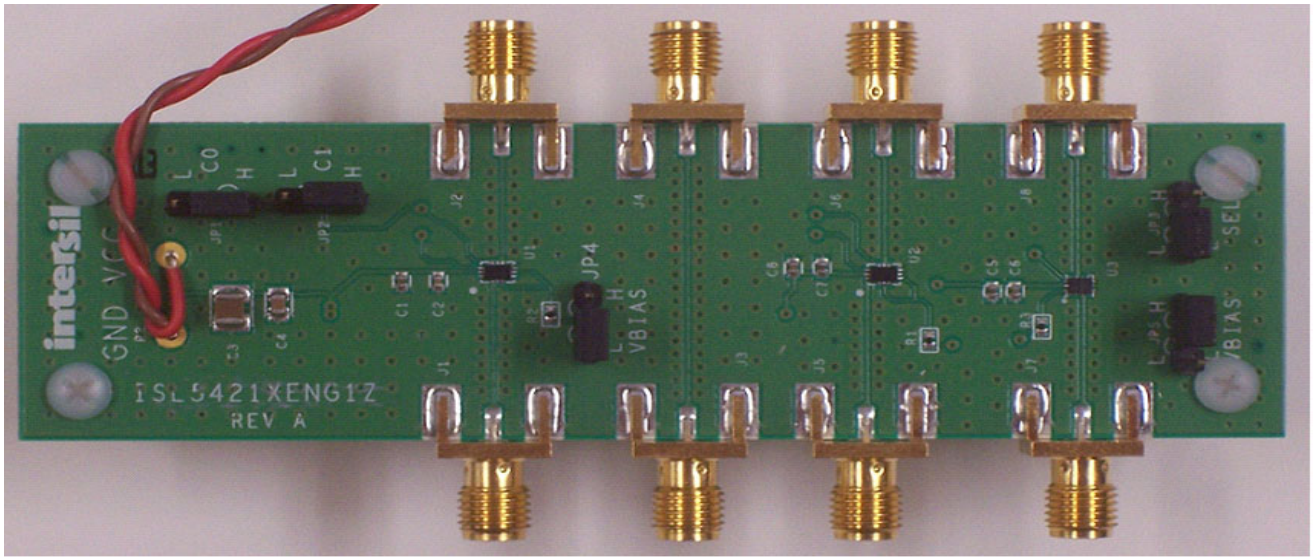


FIGURE 9. RF HIGH FREQUENCY BOARD

BOARD LAYOUT GUIDELINES

- The ISL54233 device must be soldered directly onto the PCB board. No IC sockets can be used. Their parasitic impedance will degrade the frequency performance.
- The signal traces (1D+, 1D-, 2D+, 2D-, 3D+, 3D-, COM- and COM+) must have a controlled (characteristic) impedance of 50Ω ±5%. Tight control on trace width and dielectric thickness must be followed to get 50Ω lines. Impedance tests results for controlled lines should be requested from the board fabrication house.
- A four layer PCB board: Signal (top) layer), Thin-Dielectric, GND (2nd layer), Thick-Dielectric, GND (3rd layer), Thin-Dielectric, Signal (Bottom layer) is required to achieve 50Ω traces. The top and bottom thin-dielectric are Nelco 4000-13 or Rogers 4350 core type material. The center thick-dielectric is FR4 pre-preg material.
  Figure 10 illustrates the material and sequencing of the layers. The dimensions called out are those required to achieve 50Ω microstrip for the signal traces.

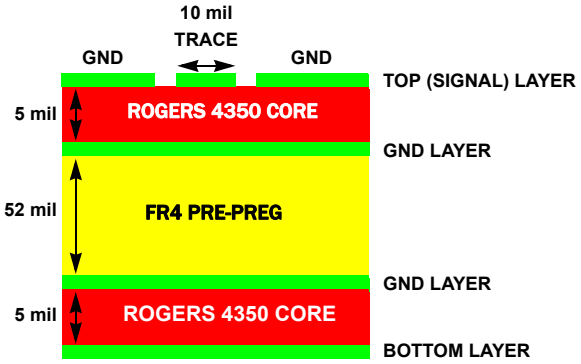


FIGURE 10. FOUR LAYER BOARD STACK-UP

- Route all controlled impedance signal lines on the top (signal) layer with no vias or through holes. Vias or through holes make it difficult to maintain a controlled impedance and tend to generate reflections.
- The signal trace lengths should be as short (<1 inch from SMA connector to the switch pin) and straight as possible. If it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Use Edge - Launch SMA connectors for all signal lines. The SMA connector terminal should be tapered to the signal trace.
- Ground stitching should be done along signal traces and around SMA ground connectors. This helps to isolate the trace in a ground conduit. This reduces capacitive coupling between traces and provides a good return path for the signal.
- Use dry film solder mask. Clear the solder mask from signal trace.
- Power and/or logic lines can be run on the bottom layer. Logic lines should be routed away from the signal lines. This will minimize capacitive coupling from the logic lines.
- A 4.7µF capacitor is placed from V_{CC} to GND where the power is brought onto the board. It keeps any low frequency noise from getting on the board. Since a bulk capacitor will look inductive at higher frequencies, an additional 0.1µF capacitor is placed across the supply lines. A 0.01µF decoupling capacitor needs to be connected from the V_{DD} pin to ground of the ISL54233 part to filter out any power supply noise from entering the part. The capacitor should be a RF type chip capacitor and should be located as close to the V_{DD} pin as possible. Note: RF type capacitors have a smaller foot-print than regular capacitors.

Typical Performance Curves

T_A = +25°C, Unless Otherwise Specified.

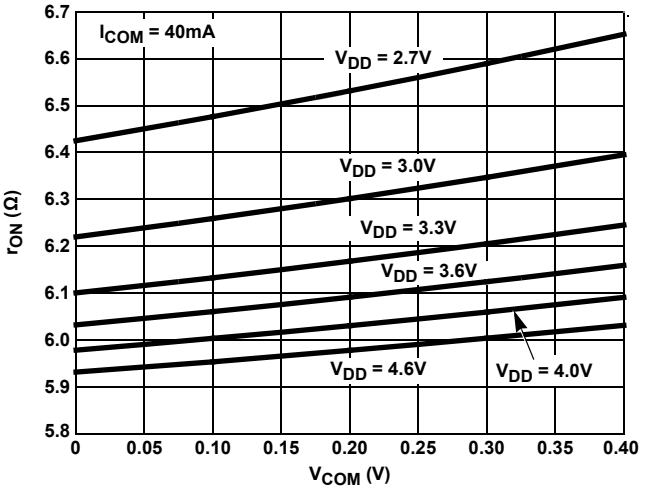


FIGURE 11. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

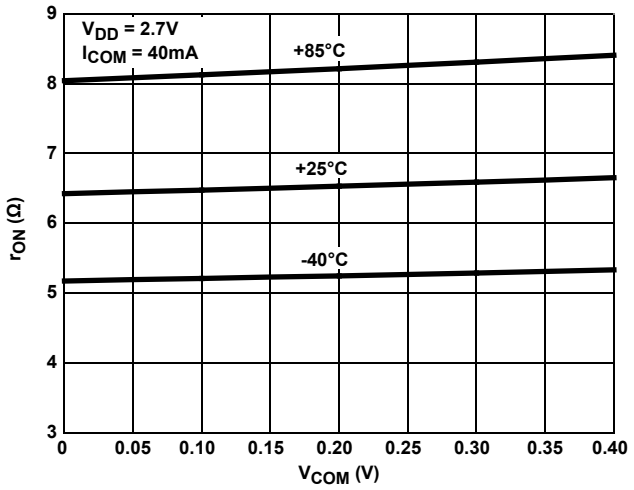


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

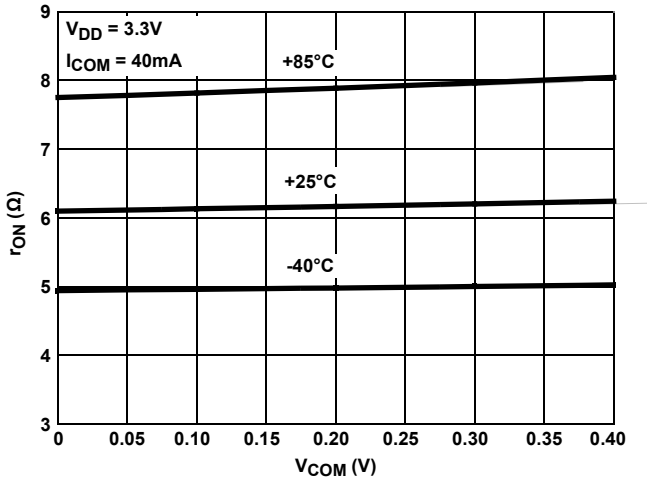


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

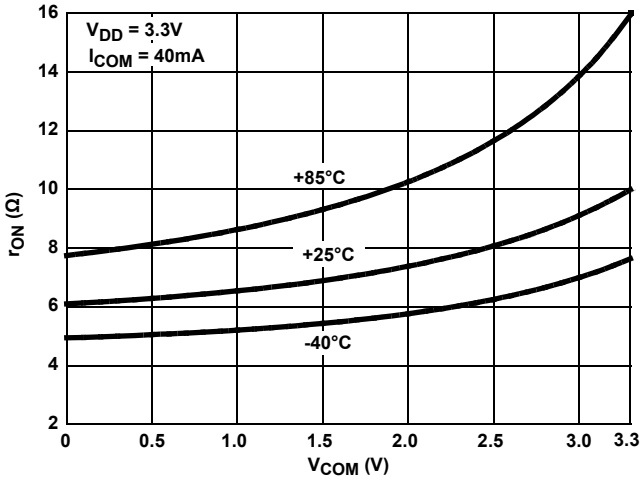


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

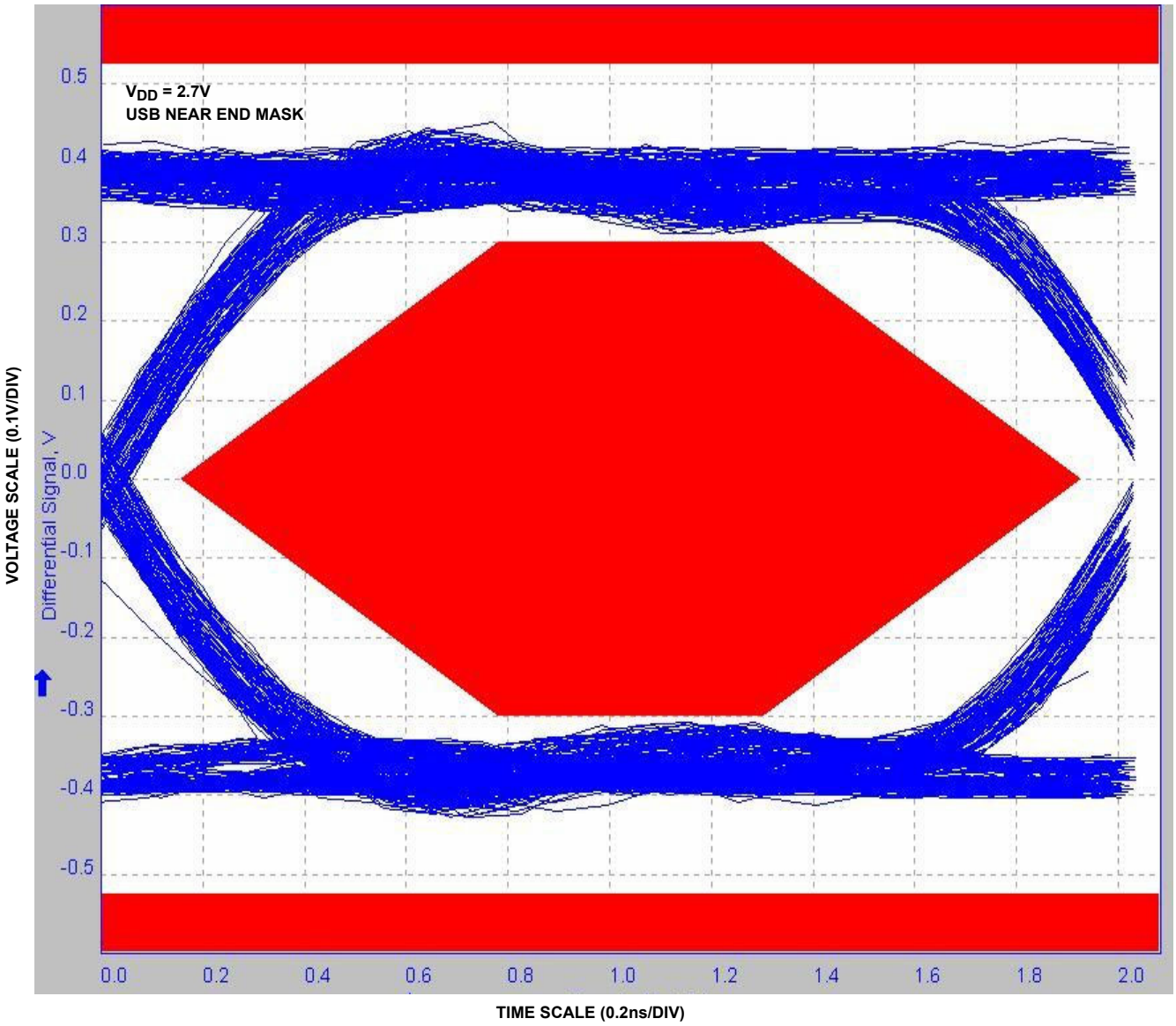


FIGURE 15. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

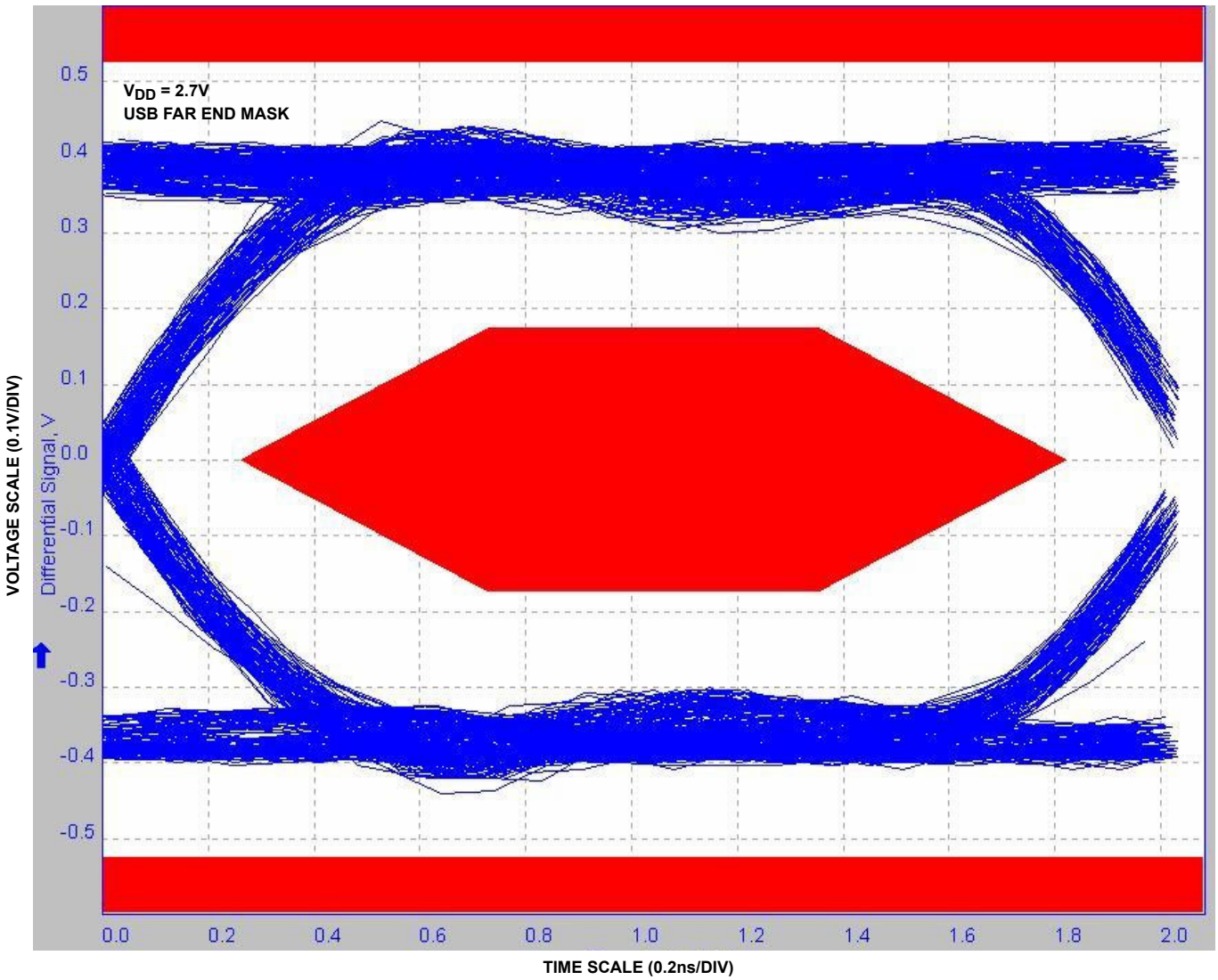


FIGURE 16. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

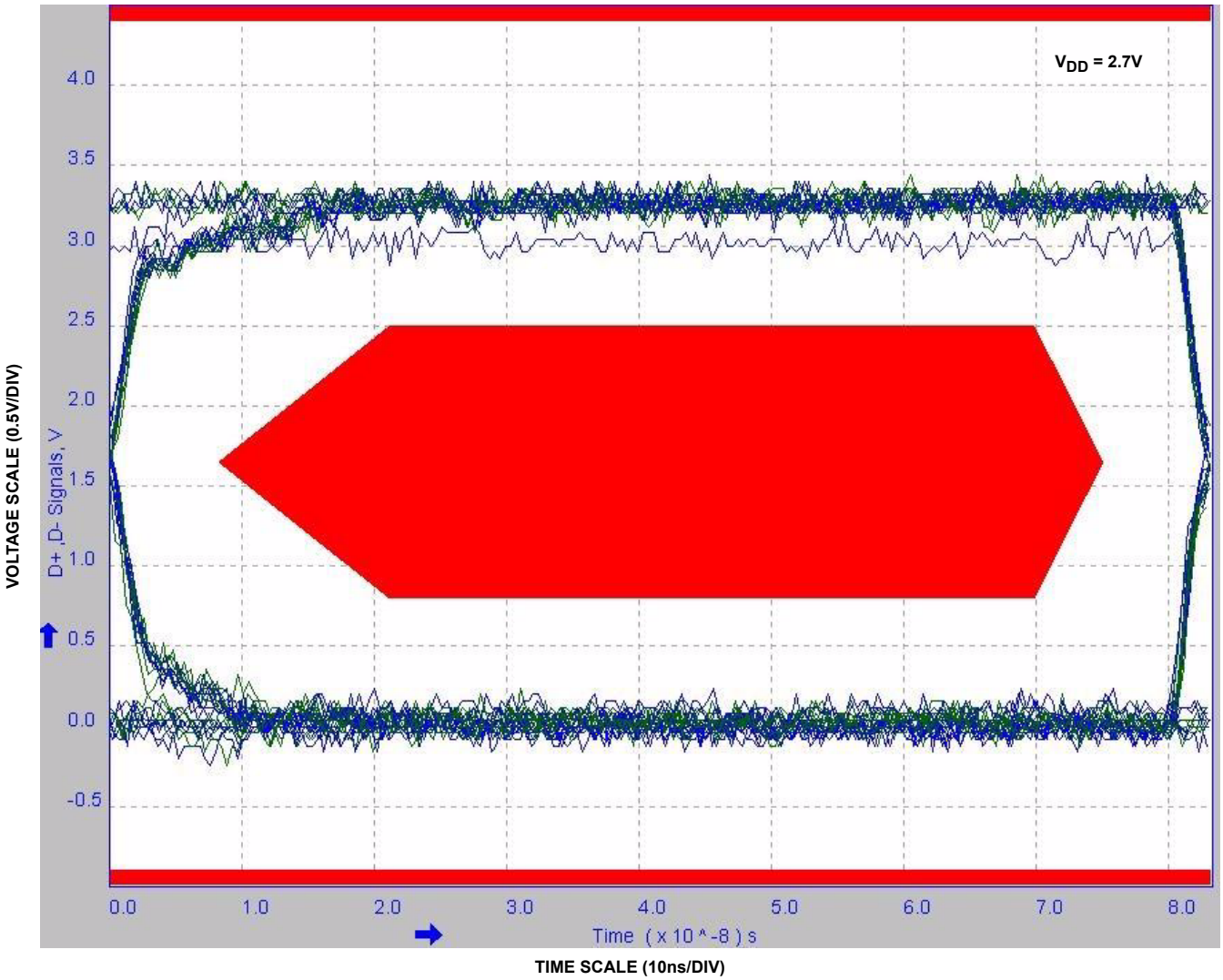


FIGURE 17. EYE PATTERN: 12Mbps USB SIGNAL WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

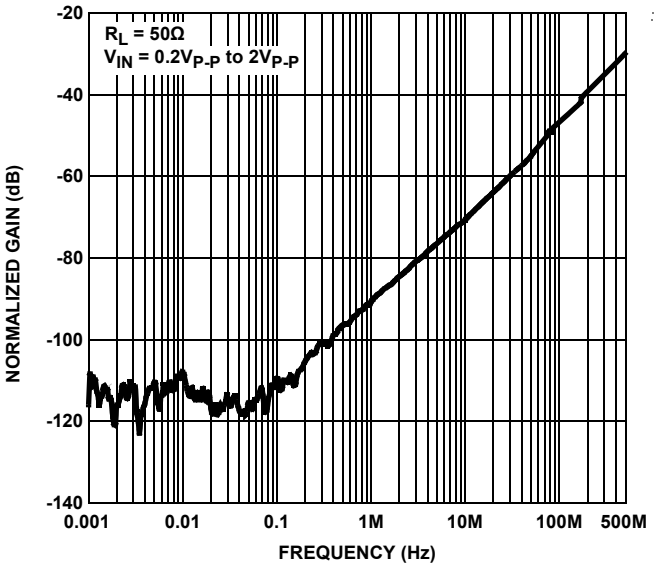


FIGURE 18. OFF-ISOLATION USB SWITCHES

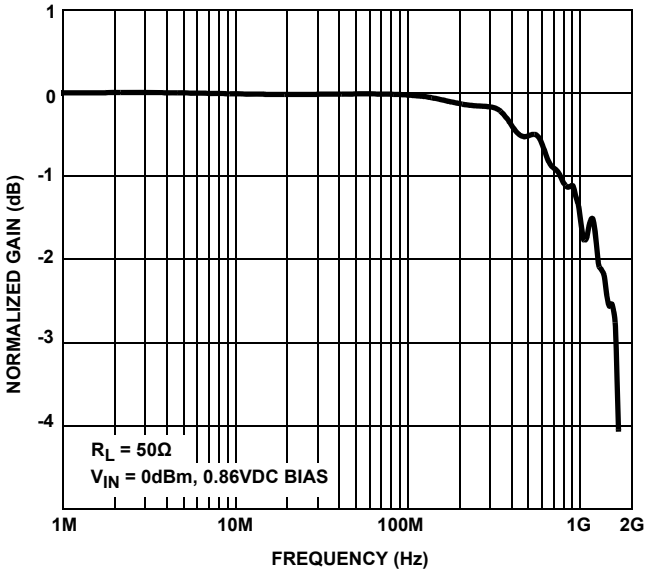


FIGURE 19. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE AND TQFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

837

PROCESS:

Submicron CMOS

Revision History

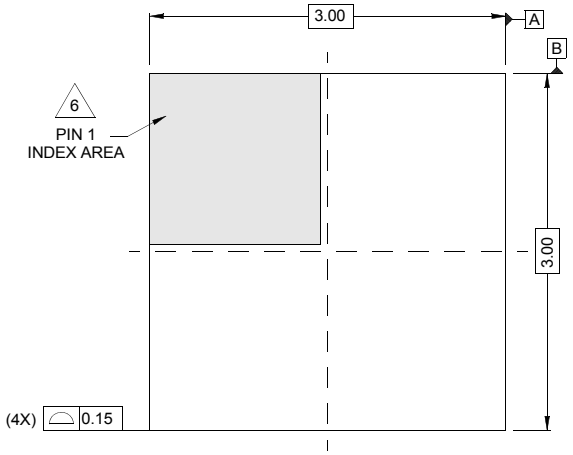
DATE	REVISION	CHANGE
Dec 12, 2018	FN7918.1	Updated ordering information table. Removed Products section. Updated disclaimer.
Dec 21, 2011	FN7918.0	Initial Release.

Package Outline Drawings

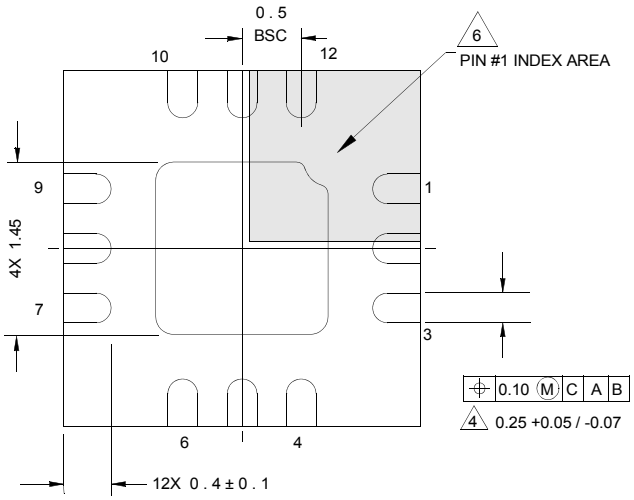
For the most recent package outline drawing, see L12.3x3A.

L12.3x3A

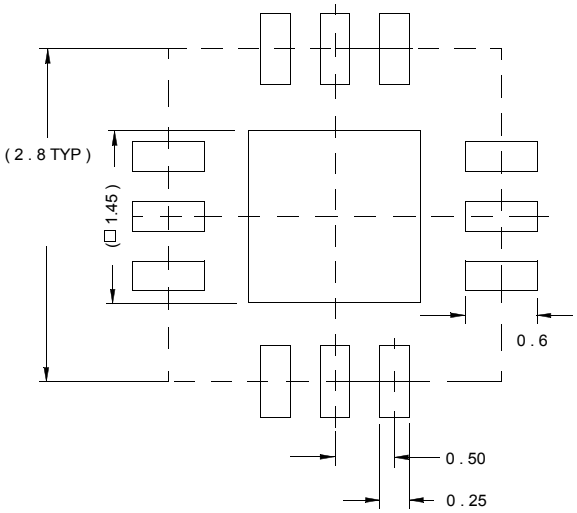
12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE
Rev 0, 09/07



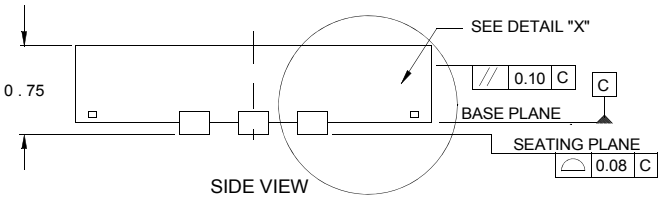
TOP VIEW



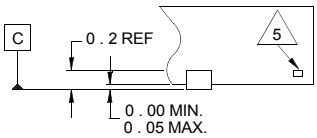
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

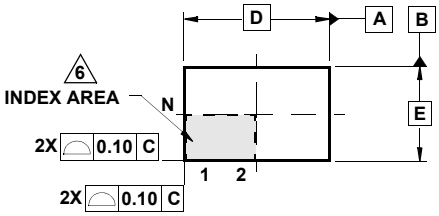
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

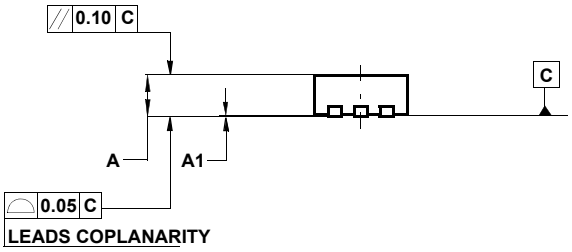
For the most recent package outline drawing, see L12.2.2x1.4A.

L12.2.2x1.4A

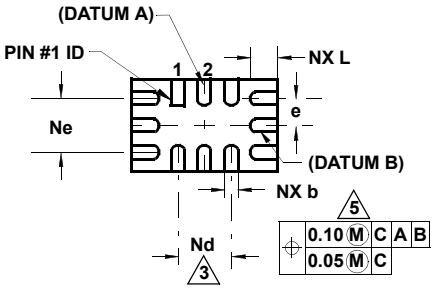
12 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (UTQFN)



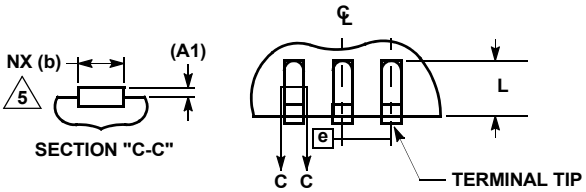
TOP VIEW



SIDE VIEW



BOTTOM VIEW

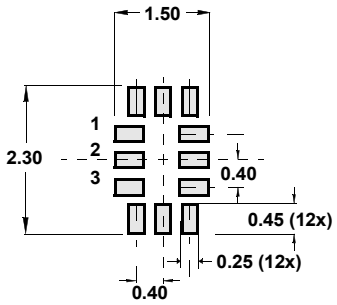


SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.15	2.20	2.25	-
E	1.35	1.40	1.45	-
e		0.40 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		12		2
Nd		3		3
Ne		3		3
θ	0	-	12	4

Rev. 0 12/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



TYPICAL RECOMMENDED LAND PATTERN 10

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(Rev.4.0-1 November 2017)

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