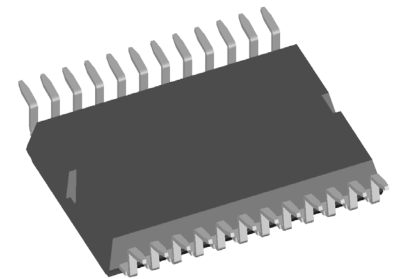
# Three phase full Bridge

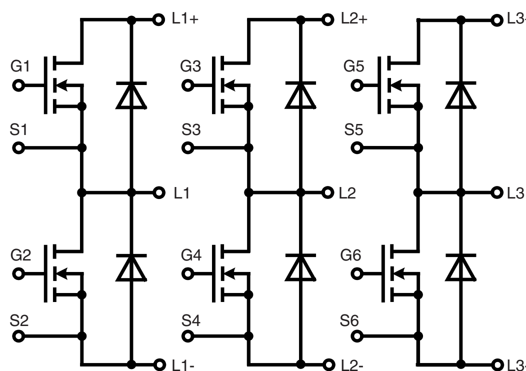
with Trench MOSFETs
in DCB-isolated high-current package

$V_{DSS}$ = 100 V
$I_{D25}$ = 190 A
$R_{DSon\ typ.}$ = 1.7 mΩ

**Part number**
MTI145WX100GD



Surface Mount Device




**Features / Advantages:**

- MOSFETs in trench technology:
  - low $R_{DSon}$
  - optimized intrinsic reverse diode
- Package:
  - high level of integration
  - high current capability
  - aux. terminals for MOSFET control
  - terminals for soldering or welding connections
  - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings

**Applications:**

AC drives
- in automobiles
  - electric power steering
  - starter generator
- in industrial vehicles
  - propulsion drives
  - fork lift drives
- in battery supplied equipment

**Package:** ISOPLUS-DIL®

- High level of integration
- RoHS compliant
- High current capability
- Aux. Terminals for MOSFET control
- Terminals for soldering or welding connections
- Space and weight savings

**Terms & Conditions of usage**
The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office.
Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office.
Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend
- to perform joint risk and quality assessments;
- the conclusion of quality agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

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| MOSFETs | | | | Ratings | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Definitions** | **Conditions** | | **min.** | **typ.** | **max.** | **Unit** |
| $V_{DSS}$ | *drain source breakdown voltage* | | $T_{VJ}$ = 25°C to 150°C | | | 100 | V |
| $V_{GS}$<br>$V_{GSM}$ | *gate source voltage*<br>*max. transient gate source voltage* | | | | | ±15<br>±20 | V<br>V |
| $I_{D25}$<br>$I_{D90}$ | *continuous drain current* | | $T_C$ = 25°C<br>$T_C$ = 90°C | | | 190<br>145 | A<br>A |
| $R_{DS(on)}$ [1)] | *static drain source on resistance* | on chip level at<br>$I_D$ = 100 A; $V_{GS}$ = 10 V | $T_{VJ}$ = 25°C<br>$T_{VJ}$ = 125°C | | 1.7<br>2.9 | 2.2 | mΩ<br>mΩ |
| $V_{GS(th)}$ | *gate threshold voltage* | $I_D$ = 275 µA; $V_{DS}$ = $V_{GS}$ | $T_{VJ}$ = 25°C | 2.0 | 2.7 | 3.5 | V |
| $I_{DSS}$ | *drain source leakage current* | $V_{DS}$ = $V_{DSS}$; $V_{GS}$ = 0 V | $T_{VJ}$ = 25°C<br>$T_{VJ}$ = 125°C | | <br>10 | 1<br>100 | µA<br>µA |
| $I_{GSS}$ | *gate source leakage current* | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | | | | 500 | nA |
| $R_G$ | *gate resistance* | on chip level | | | 1.9 | | Ω |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | *input capacitance*<br>*output capacitance*<br>*reverse transfer capacitance* | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; f = 1 Mhz | | | 11.1<br>1.94<br>70 | | nF<br>nF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | *total gate charge*<br>*gate source charge*<br>*gate drain (Miller) charge* | $V_{GS}$ = 10 V; $V_{DS}$ = 50 V; $I_D$ = 100 A | | | 155<br>48<br>27 | | nC<br>nC<br>nC |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$<br>$E_{on}$<br>$E_{off}$<br>$E_{rec(off)}$ | *turn-on delay time*<br>*current rise time*<br>*turn-off delay time*<br>*current fall time*<br>*turn-on energy per pulse*<br>*turn-off energy per pulse*<br>*turn-off reverse recovery losses* | inductive load<br>$V_{GS}$ = 10 V; $V_{DS}$ = 50 V<br>$I_D$ = 100 A; $R_G$ = 27 Ω | $T_{VJ}$ = 125°C | | 135<br>75<br>600<br>40<br>200<br>600<br>36 | | ns<br>ns<br>ns<br>ns<br>µJ<br>µJ<br>µJ |
| $R_{thJC}$ | *thermal resistance junction to case* | | | | | 0.85 | K/W |
| $R_{thJH}$ | *thermal resistance junction to heatsink* | with heat transfer paste (IXYS test setup) | | | 1.1 | 1.4 | K/W |
| | | 1) $V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{Pin\ to\ Chip})$ | | | | | |
| **Source-Drain Diode** | | | | | | | |
| $I_{F25}$<br>$I_{F90}$ | *forward current* | | $T_C$ = 25°C<br>$T_C$ = 90°C | | | 180<br>105 | A<br>A |
| $V_{SD}$ | *source drain voltage* | $I_F$ = 100 A; $V_{GS}$ = 0 V | $T_{VJ}$ = 25°C | | 0.9 | 1.2 | V |
| $Q_{RM}$<br>$I_{RM}$<br>$t_{rr}$ | *reverse recovery charge*<br>*max. reverse recovery current*<br>*reverse recovery time* | $V_R$ = 50 V; $I_F$ = 100 A<br>$R_G$ = 27 Ω (di/dt = 1700 A/µs) | $T_{VJ}$ = 125°C | | 2<br>54<br>60 | | µC<br>A<br>ns |

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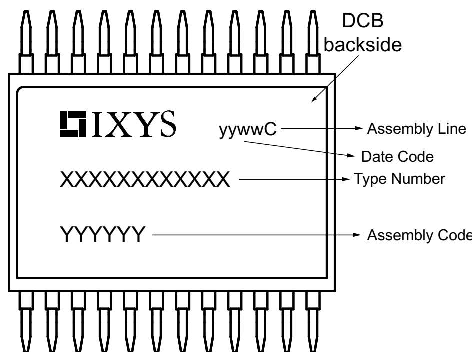
| Package ISOPLUS-DIL® | | | | Ratings | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Definitions** | **Conditions** | | **min.** | **typ.** | **max.** | **Unit** |
| $I_{RMS}$ | *RMS current* | per pin in main current paths (L1+...L3+, L1-...L3-, L1...L3) may be additionally limited by external connections (PCB tracks) 2 pins for output L1, L2, L3 | | | | 75 | A |
| $T_{stg}$ | *storage temperature* | | | -55 | | 125 | °C |
| $T_{op}$ | *operation temperature* | | | -55 | | 150 | °C |
| $T_{VJ}$ | *virtual junction temperature* | | | -55 | | 175 | °C |
| **Weight** | | | | | 13 | | g |
| $F_C$ | *mounting force with clip* | | | 50 | | 250 | N |
| $V_{ISOL}$ | *isolation voltage* | t = 1 second | 50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA | 1200 | | | V |
| | | t = 1 minute | | 1000 | | | V |
| $R_{pin-chip}$ | *resistance terminal to chip* | $V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{pin\ to\ chip})$ | | | 0.5 | | mΩ |
| $C_P$ | *coupling capacity* | between shorted pins and back side metallization | | | 160 | | pF |




**Part number**

M = MOSFET
T = Trench
I = Infineon Trench
145 = Current Rating [A]
WX = 6-Pack with separated Phase Legs
100 = Reverse Voltage [V]
GD = ISOPLUS-DIL

| Ordering | Part Name | Marking on Product | Delivering Mode | Base Qty | Ordering Code |
|---|---|---|---|---|---|
| Standard | MTI145WX100GD-SMD | MTI145WX100GD | Tube | 13 | 518023 |

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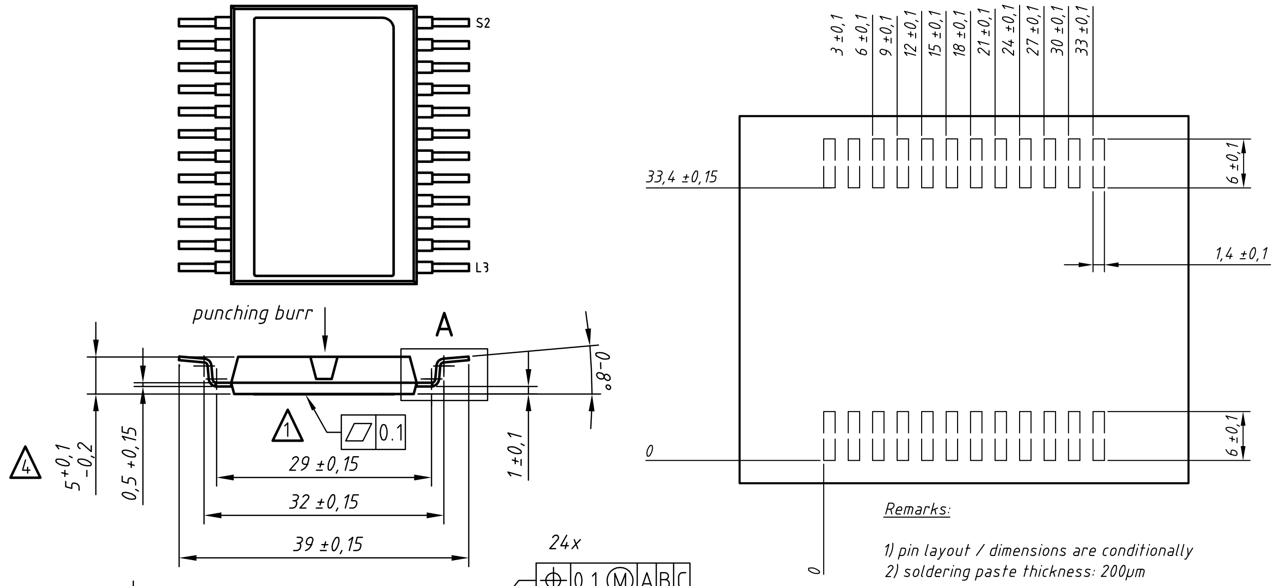
## Outlines ISOPLUS-DIL®




0.1 Ⓜ A B C

G5 L3
S5 L3
L3+ G6
L3- S6
G3 L2
S3 L2
L2+ G4
L2- S4
G1 L1
S1 L1
L1+ G2
L1- S2

37,5 ±0,25 · 22x 3 ±0,1 · 2,25 ±0,1 · 1,5 · 1 ±0,15 · 1.6 · 25 ±0,25 · B · C

Detail A

SEATING PLANE · A · 3,5 ±0,02 (2) · 3,55 +0,02/−0,15 (3)

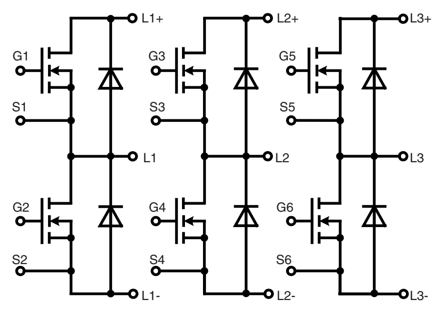
(1) Convex bow of substrate, typ. 10-40 µm longitudinal and 5-15 µm transversal

(2) Distance between pin and case bottom side.

(3) Distance between pin and contact surface.

(4) Distance between parallel planes aligned to top and bottom sides of the package

contact pin:
- galv. tin plating, per pin side: Sn 10...25 µm, undercoating Ni 0,2...1 µm
- stamping edges may be free of tin
- puching burr: ≤ 0,05mm

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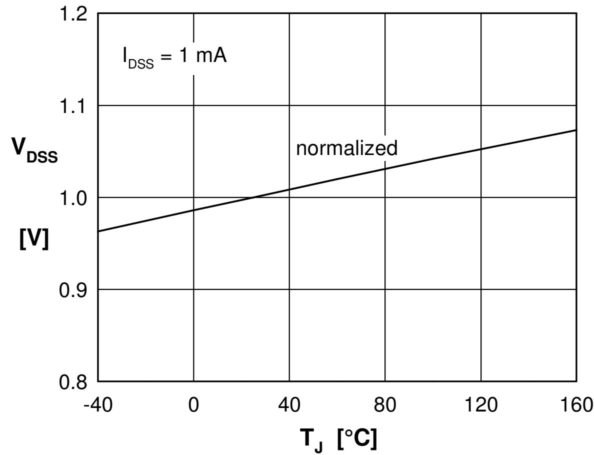


Fig.1 Drain source breakdown voltage $V_{DSS}$ vs. junction temperature $T_{VJ}$

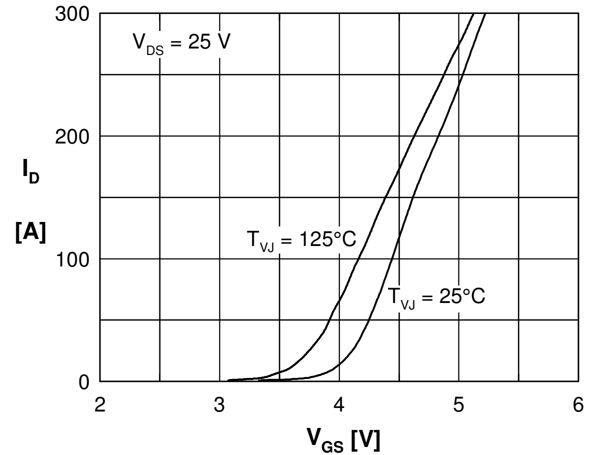


Fig. 2 Typ. transfer characteristics

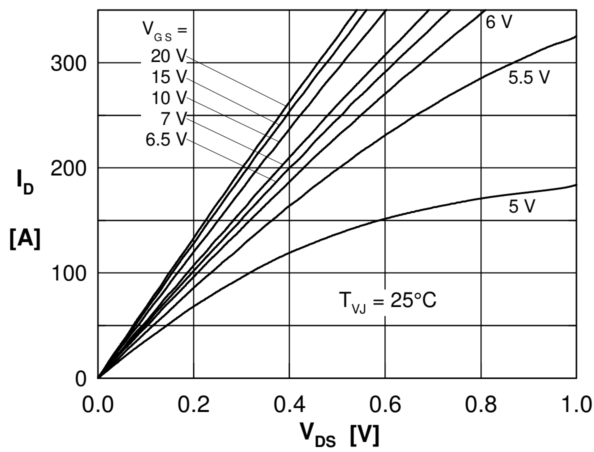


Fig. 3 Typ. output characteristics on die level

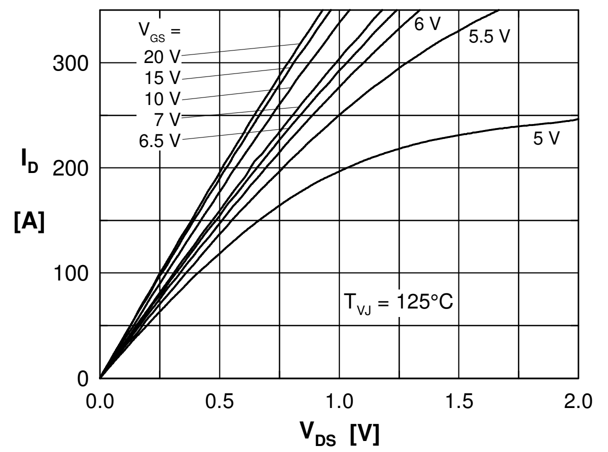


Fig. 4 Typ. output characteristics on die level

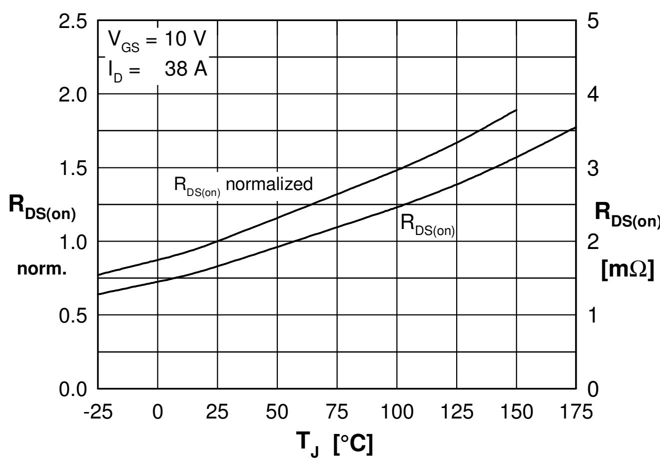


Fig.5 Drain source on-state resistance $R_{DS(on)}$ vs. junction temperature $T_{VJ}$, on die level

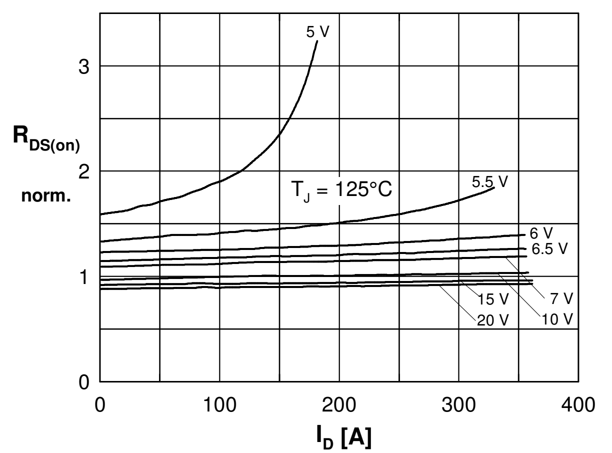


Fig. 6 Drain source on-state resistance $R_{DS(on)}$ versus $I_D$, on die level

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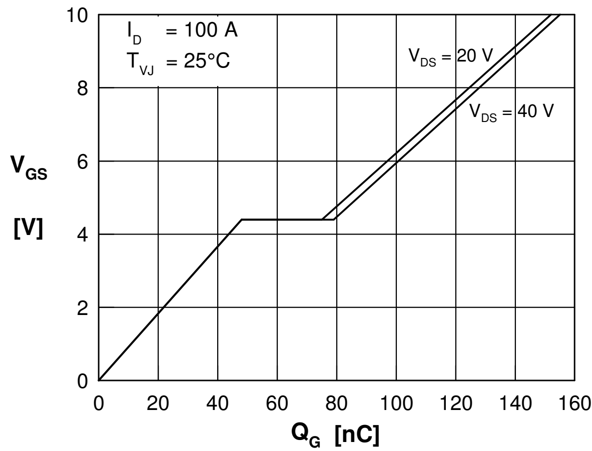


Fig.7 Typical turn on gate charge

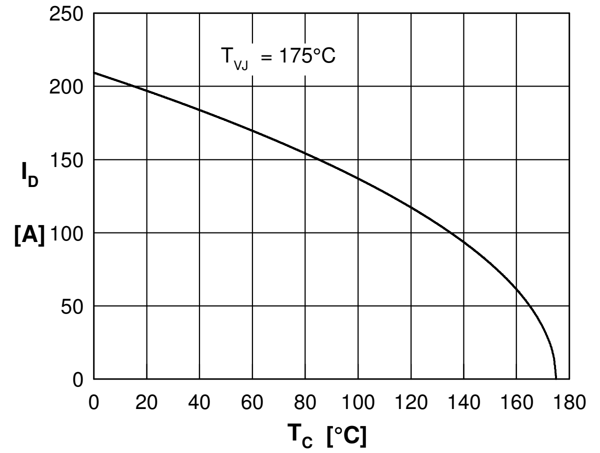


Fig. 8 Drain current $I_D$ vs. case temperature $T_C$ (Chip capability)

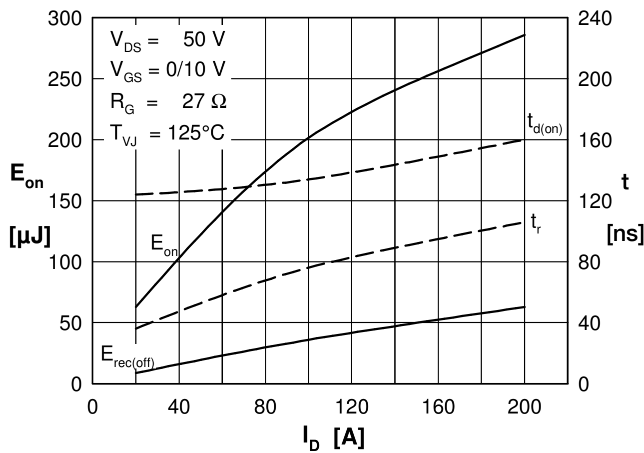


Fig. 9 Typ. turn-on energy and switching times versus drain current, inductive switching

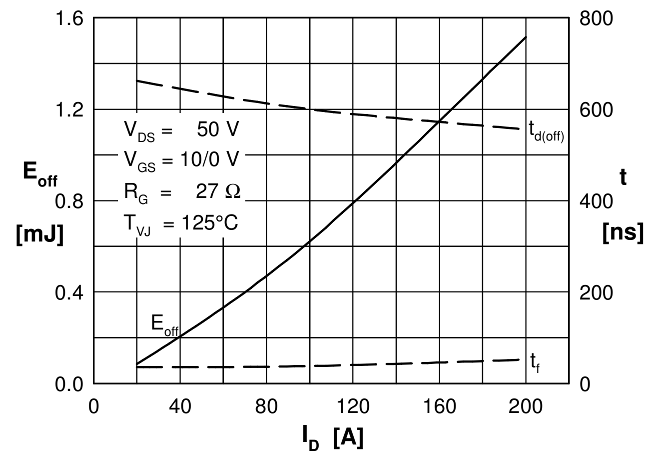


Fig. 10 Typ. turn-off energy and switching times versus drain-current, inductive switching

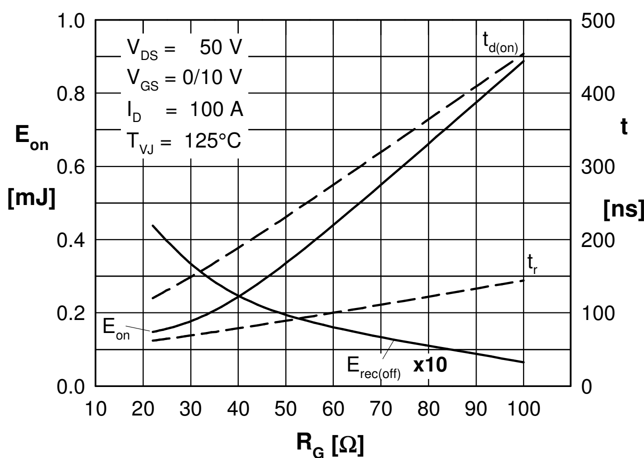


Fig. 11 Typ. turn-on energy and switching times versus gate resistor, inductive switching

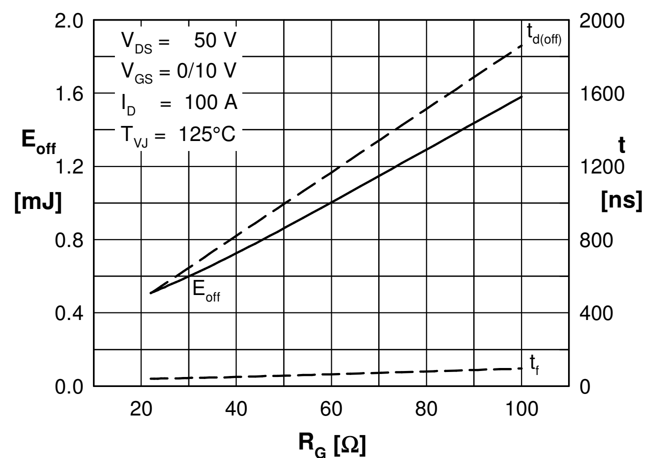


Fig. 12 Typ. turn-off energy and switching times versus gate resistor, inductive switching

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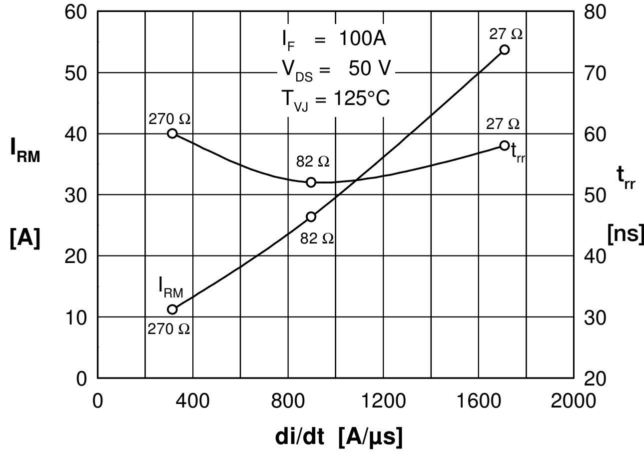


Fig. 13 Typ. reverse recovery characteristics

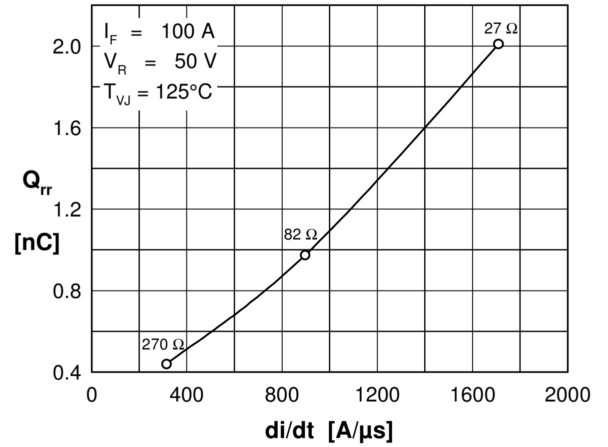


Fig. 14 Typ. reverse recovery characteristics

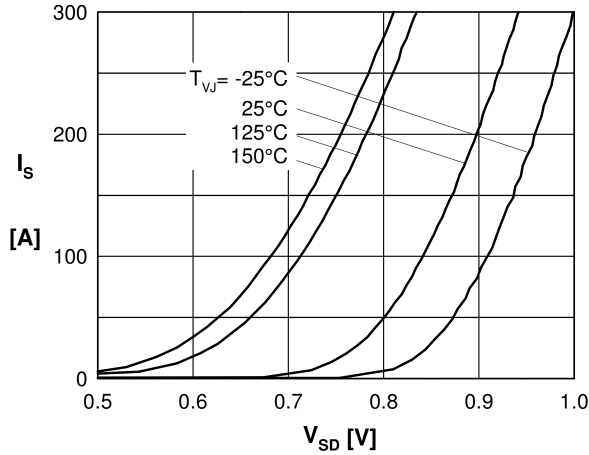


Fig.15 Source current $I_S$ vs. source drain voltage $V_{SD}$ (body diode) on die level

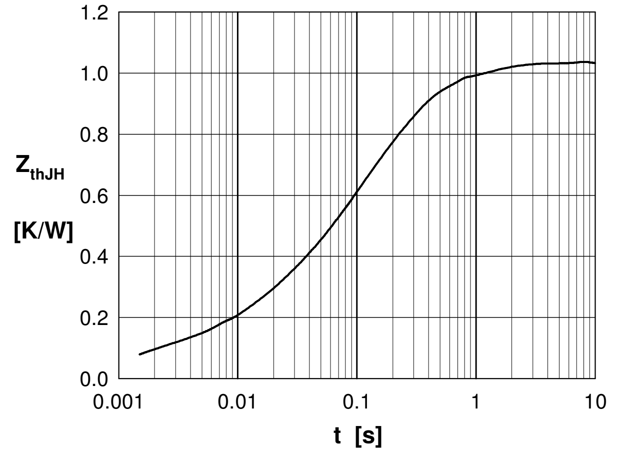


Fig. 16 Typ. thermal impedance junction to heatsink $Z_{thJH}$ with heat transfer paste (IXYS test setup)

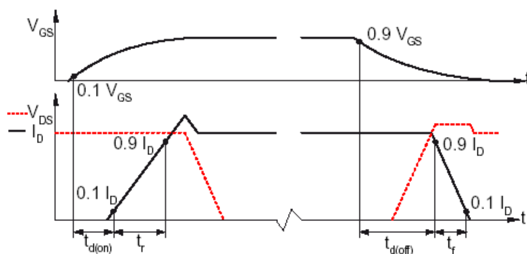


Fig. 17 Definition of switching times

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