

## Description

The F0424 is a 600MHz to 4200MHz SiGe High-Gain Broadband RF Amplifier. The combination of low noise figure (NF) and high linearity performance allows the device to be used in both receiver and transmitter applications.

The F0424 is designed to operate with a single 5V or 3.3V power supply using a nominal 70mA of  $I_{CC}$ . With a supply voltage of 5V, the F0424 provides 17.3dB gain with +40dBm OIP3 and 2.3dB noise figure at 2600MHz.

The device is packaged in a  $2 \times 2$  mm, 8-pin Thin DFN with 50Ω single-ended RF input and output impedances for ease of integration into the signal path.

## Competitive Advantage

- High Gain
- Broadband
- STBY Feature
- Superior Reliability versus GaAs

## Typical Applications

- 4G TDD and FDD Base Stations
- 2G/3G Base Stations
- Repeaters and DAS
- Point-to-Point Infrastructure
- Public Safety Infrastructure
- Military Handhelds

**Table 1. Typical Values**

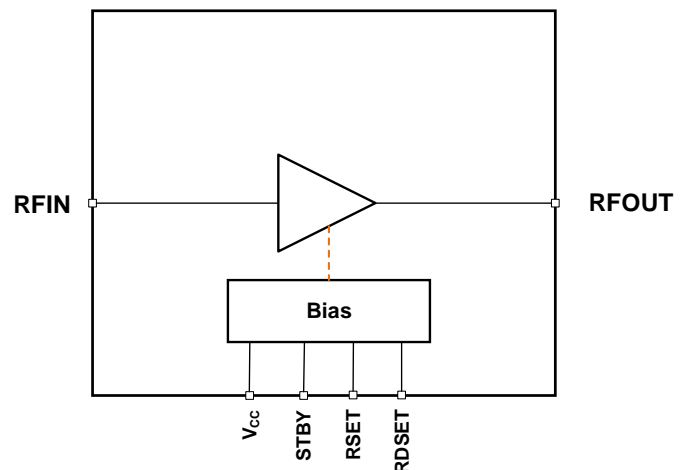
Part Number	Frequency (MHz)	Gain (dB)	NF (dB)	OIP3 (dBm)
F0424	600 to 4200	17.3	2.3	+40

## Features

- RF Range: 600MHz to 4200MHz
- Noise Figure = 2.3dB at 2600MHz
- Gain = 17.3dB at 2600MHz
- OIP3 = +40dBm at 2600MHz
- Output P1dB = +21dBm at 2600MHz
- Near-Constant Gain versus Temperature
- 3.3V or 5V Power Supply
- $I_{CC} = 70$ mA
- 2mA Standby Current
- 350mW Typical DC Power at 5V Supply
- 50Ω Input and Output Impedances
- Operating Temperature ( $T_{EPAD}$ ) Range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- $2 \times 2$  mm, 8-DFN Package

## Block Diagram

**Figure 1. Block Diagram**



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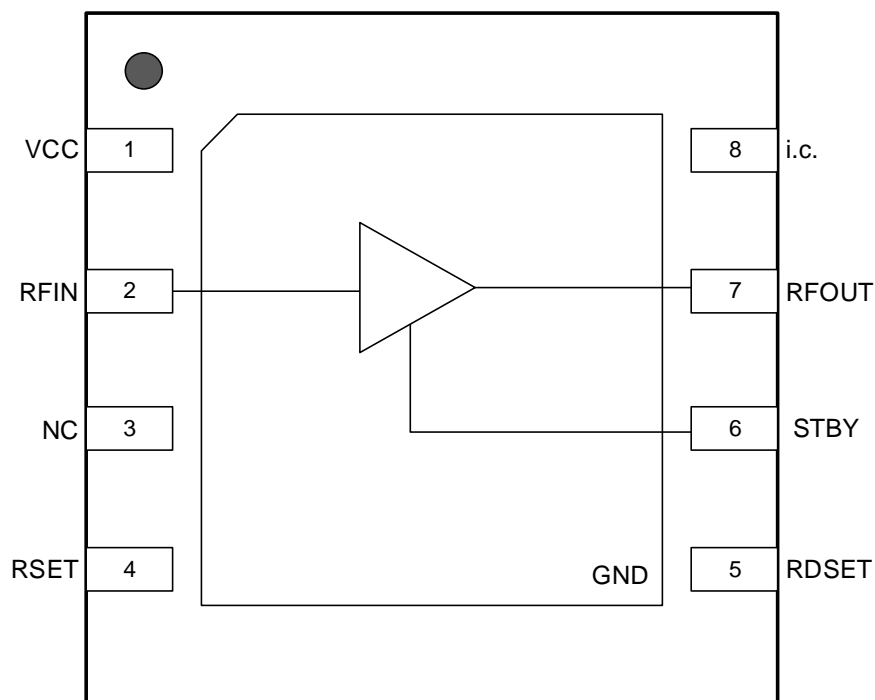
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## Pin Assignments

**Figure 2. Pin Assignments for 2 × 2 × 0.75 mm 8-DFN Package – Top View**



## Pin Descriptions

**Table 2. Pin Descriptions**

Number	Name	Description
1	VCC	Power supply. The bypass capacitor must be as close to the pin as possible.
2	RFIN	RF input internally matched to 50Ω. An external DC block is required.
3	NC	No connection. This pin can be left unconnected, connected to VCC, or connected to GND. IDT recommends connecting it to GND.
4	RSET	Main amplifier current bias setting resistor. Connect to GND.
5	RDSET	Distortion amplifier current bias setting resistor. Connect to GND.
6	STBY	Standby. If this pin is not connected or is logic LOW, the device will operate under its normal operating condition. If this pin is logic HIGH, the F0424 will be in STBY Mode.
7	RFOUT	RF output internally matched to 50Ω. An external DC block is required.
8	i.c.	Connect this pin directly to ground.
	EPAD	Exposed pad. This pad is internally connected to GND. Solder this exposed pad to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F0424 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Units
V <sub>CC</sub> to GND	V <sub>CC</sub>	-0.3	+5.5	V
STBY	V <sub>STBY</sub>	-0.3	+3.6	V
STBY Minus VCC Voltage (voltage difference)	V <sub>STBY-VCC</sub>		0.3	V
RFIN Externally Applied DC Current	I <sub>RFIN</sub>	-1	+1	mA
RFOUT Externally Applied DC Voltage	V <sub>RFOUT</sub>	V <sub>CC</sub> - 0.15	V <sub>CC</sub> + 0.15	V
RSET Pin Maximum DC Current	I <sub>PIN4</sub>	-1	+1	mA
RDSET Pin Maximum DC Current	I <sub>PIN5</sub>	-1	+1	mA
RF Input Power (RFOUT) Present for 24 Hours Maximum [a]	P <sub>MAX_IN</sub>		+20	dBm
Continuous Power Dissipation	P <sub>DISS</sub>		0.6	W
Junction Temperature	T <sub>JMAX</sub>		140	°C
Storage Temperature Range	T <sub>STOR</sub>	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)			1000 (Class C3)	V

[a] Exposure to these maximum RF levels can result in significant V<sub>CC</sub> current draw due to overdriving the amplifier stages.

## Recommended Operating Conditions

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Power Supply Voltage	V <sub>CC</sub>	V <sub>CC</sub> pins	3.15		5.25	V
Operating Temperature Range	T <sub>EPAD</sub>	Exposed paddle temperature	-40		+105	°C
RF Frequency Range	f <sub>RF</sub>	Operating range	600		4200	MHz
RFIN Source Impedance	Z <sub>RFIN</sub>	Single-ended		50		Ω
RFOUT Load Impedance	Z <sub>RFOUT</sub>	Single-ended		50		Ω

## Electrical Characteristics

See the F0424 Typical Application Circuit in Figure 42. Specifications apply when operated with  $V_{CC} = +5.0V$ ,  $R_5 = 2.49k\Omega$ ,  $R_6 = 160\Omega$ ,  $T_{EPAD} = +25^\circ C$ ,  $f_{RF} = 2.6GHz$ ,  $STBY = LOW$ ,  $Z_S = Z_L = 50\Omega$  single-ended, and output power = 0dBm/tone, unless stated otherwise. EVKit trace and connector losses are de-embedded (see the F0424EVBK Evaluation Kit in Figure 40).

**Table 5. Electrical Characteristics – 5V Supply Voltage**

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	$V_{IH}$		<b>1.07</b> [a]			V
Logic Input Low Threshold	$V_{IL}$				<b>0.8</b>	V
Logic Current	$I_{IH}, I_{IL}$	Applied STBY voltage = 3.6V	<b>-10</b>		<b>+100</b>	$\mu A$
Supply Current	$I_{CC}$			70	<b>80</b>	mA
Pull-down Resistor on STBY pin	$R_{STBY}$			50		$k\Omega$
Standby Current	$I_{CC\_STBY}$			2	<b>3</b>	mA
Settling Time	$t_{SETTLE}$	50% STBY control to within $\pm 0.5dB$ of final power level		0.25		$\mu s$
RF Input Return Loss	$RL_{IN}$			13		dB
RF Output Return Loss	$RL_{OUT}$			12		dB
Gain	G	$f_{RF} = 600MHz$		17.2		dB
		$f_{RF} = 1900MHz$		17.6		
		$f_{RF} = 2600MHz$	<b>16</b>	17.3		
		$f_{RF} = 3500MHz$		16.7		
		$f_{RF} = 4200MHz$		16.1		
Gain Flatness (amplitude)	$G_{VAR}$	$f_{RF} = 700MHz, \pm 100MHz$		$\pm 0.15$		dB
		$f_{RF} = 1900MHz, \pm 100MHz$		$\pm 0.1$		
		$f_{RF} = 2600MHz, \pm 100MHz$		$\pm 0.1$		
		$f_{RF} = 3500MHz, \pm 100MHz$		$\pm 0.1$		
		$f_{RF} = 4100MHz, \pm 100MHz$		$\pm 0.15$		
Gain Variation over Temperature	$G_{TEMP}$	$T_{EPAD} = -40^\circ C$ to $+105^\circ C$		$\pm 0.2$		dB
Noise Figure	NF	$f_{RF} = 2600MHz$		2.3	2.7	dB
		$f_{RF} = 3500MHz$		2.7		dB
Noise Figure Variation over Temperature	$NF_{TEMP}$	$T_{EPAD} = -40^\circ C$ to $+105^\circ C$		$\pm 0.4$		dB
Output Third-Order Intercept Point	OIP3	$f_{RF} = 2600MHz$ 5MHz tone separation	<b>35</b>	40		dBm
		$f_{RF} = 3500MHz$ 5MHz tone separation		40		
Output Third-Order Intercept Point Variation over Temperature	$OIP3_{VAR}$	$f_{RF} = 2600MHz$ 5MHz tone separation $T_{EPAD} = -40^\circ C$ to $+105^\circ C$		-1.2/+0.26		dB
Output P1dB compression	$OP_{1dB}$	$f_{RF} = 2600MHz$	<b>20</b>	21		dBm
		$f_{RF} = 3500MHz$		20		
Reverse Isolation	$REV_{ISO}$			24		dB

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

## Electrical Characteristics

See the F0424 Typical Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $R_5 = 2.49k\Omega$ ,  $R_6 = 160\Omega$ ,  $T_{EPAD} = +25^\circ C$ ,  $f_{RF} = 2.6GHz$ ,  $STBY = LOW$ ,  $Z_S = Z_L = 50\Omega$  single-ended, and output power = 0dBm/tone, unless stated otherwise. EVKit trace and connector losses are de-embedded.

**Table 6. Electrical Characteristics – 3.3V Supply Voltage**

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	$V_{IH}$		<b><i>1.07</i></b> [a]			V
Logic Input Low Threshold	$V_{IL}$				<b><i>0.8</i></b>	V
Logic Current	$I_{IH}, I_{IL}$	Applied STBY voltage = 3.6V	<b><i>-10</i></b>		<b><i>+100</i></b>	$\mu A$
Supply Current	$I_{CC}$			70		mA
Pull-Down Resistor on STBY Pin	$R_{STBY}$			50		$k\Omega$
Standby Current	$I_{CC\_STBY}$			2		mA
Settling Time	$t_{SETTLE}$	50% STBY control to within $\pm 0.5dB$ of final power level		0.25		$\mu s$
RF Input Return Loss	$RL_{IN}$			13		dB
RF Output Return Loss	$RL_{OUT}$			12		dB
Gain	G	$f_{RF} = 600MHz$		17.2		dB
		$f_{RF} = 1900MHz$		17.6		
		$f_{RF} = 2600MHz$		17.3		
		$f_{RF} = 3500MHz$		16.7		
		$f_{RF} = 4200MHz$		16.1		
Gain Flatness (amplitude)	$G_{VAR}$	$f_{RF} = 700MHz, \pm 100MHz$		$\pm 0.15$		dB
		$f_{RF} = 1900MHz, \pm 100MHz$		$\pm 0.1$		
		$f_{RF} = 2600MHz, \pm 100MHz$		$\pm 0.1$		
		$f_{RF} = 3500MHz, \pm 100MHz$		$\pm 0.2$		
		$f_{RF} = 4100MHz, \pm 100MHz$		$\pm 0.15$		
Gain Variation over Temperature	$G_{TEMP}$	$T_{EPAD} = -40^\circ C$ to $+105^\circ C$		$\pm 0.2$		dB
Noise Figure	NF	$f_{RF} = 2600MHz$		2.3		dB
		$f_{RF} = 3500MHz$		2.7		dB
Noise Figure Variation over Temperature	$NF_{TEMP}$	$T_{EPAD} = -40^\circ C$ to $+105^\circ C$		$+0.5/-0.4$		dB
Output Third Order Intercept Point	OIP3	$f_{RF} = 2600MHz$ 5MHz tone separation		33		dBm
		$f_{RF} = 3500MHz$ 5MHz tone separation		31		
Output P1dB compression	OP <sub>1dB</sub>	$f_{RF} = 2600MHz$		16.4		dBm
		$f_{RF} = 3500MHz$		15.5		
Reverse Isolation	REV <sub>ISO</sub>			24		dB

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.



## Thermal Characteristics

**Table 7. Package Thermal Characteristics**

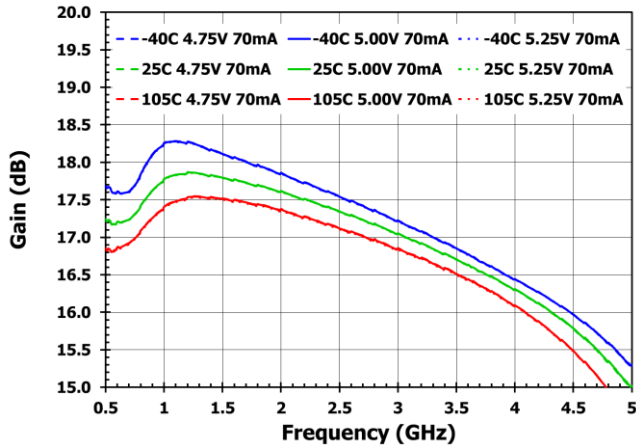
Parameter	Symbol	Value	Units
Junction-to-Ambient Thermal Resistance.	$\theta_{JA}$	93	°C/W
Junction-to-Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC-BOT}$	27	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL-1	

## Typical Operating Conditions (TOC)

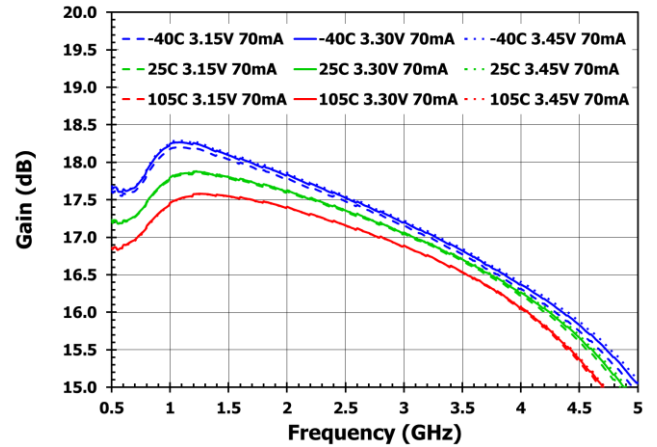
- Evaluation kit connector and trace losses de-embedded
- $V_{CC} = 5.0V$  (plots also taken with  $V_{CC} = 3.3V$ )
- $T_{EPAD} = +25^{\circ}C$
- STBY = not connected (internally pulled logic low)
- RSET (R5) = 2.49K unless otherwise noted
- Small signal parameters measured with  $P_{OUT} = 0dBm$
- Two tone tests  $P_{OUT} = 0dBm$ /tone with 5MHz tone spacing
- $Z_L = Z_S = 50\Omega$ , single-ended

## Typical Performance Characteristics

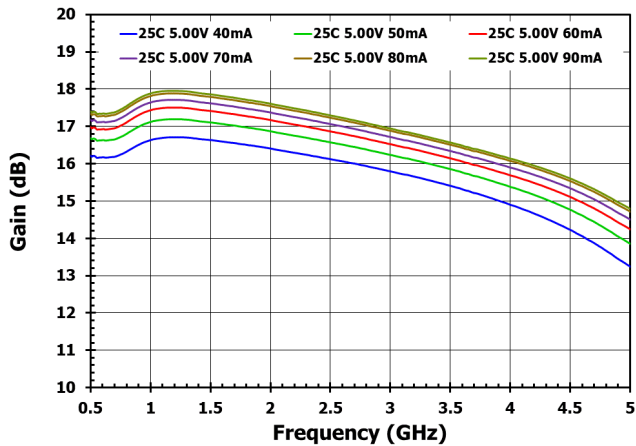
**Figure 3. Gain versus Temperature (5V Variation)**



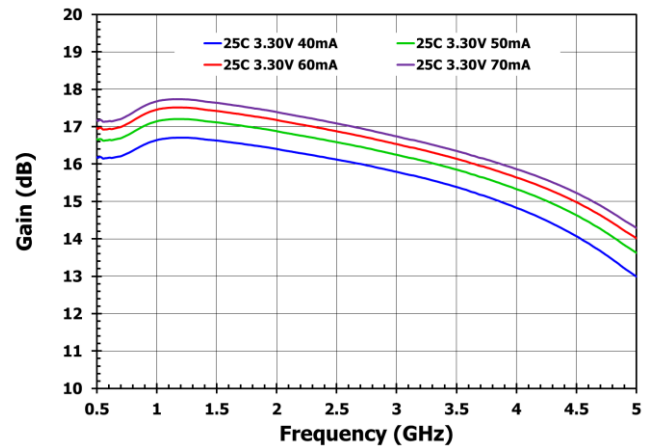
**Figure 4. Gain versus Temperature (3.3V Variation)**



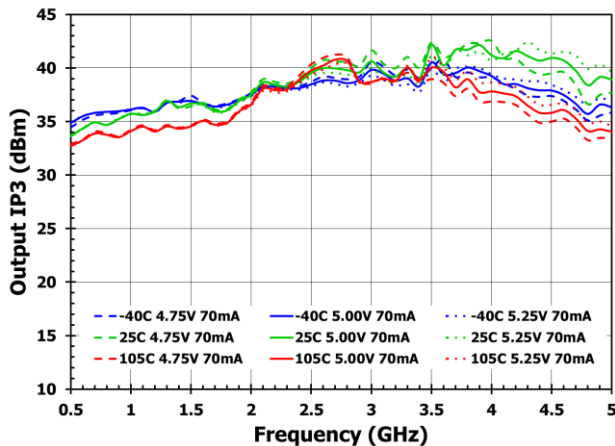
**Figure 5. Gain versus Bias Current (5.0V)**



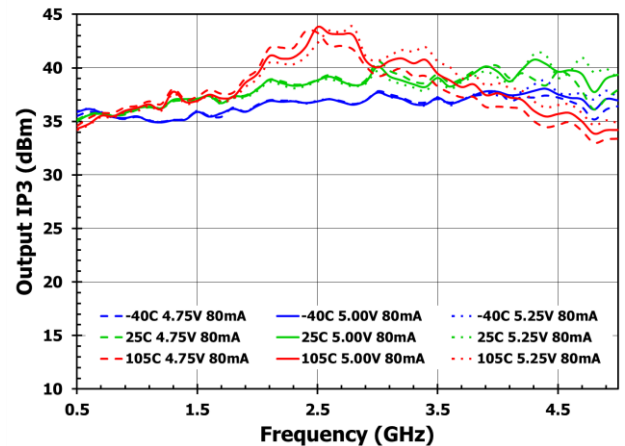
**Figure 6. Gain versus Bias Current (3.3V)**



**Figure 7. Output IP3 versus Temperature (5V Variation, 70mA)**

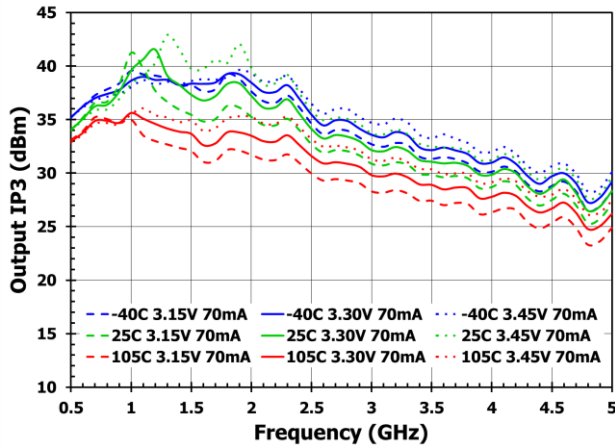


**Figure 8. Output IP3 versus Temperature (5V Variation, 80mA)**

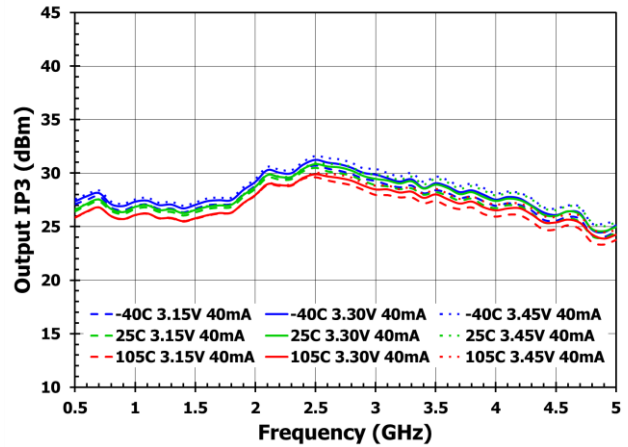


## Typical Performance Characteristics

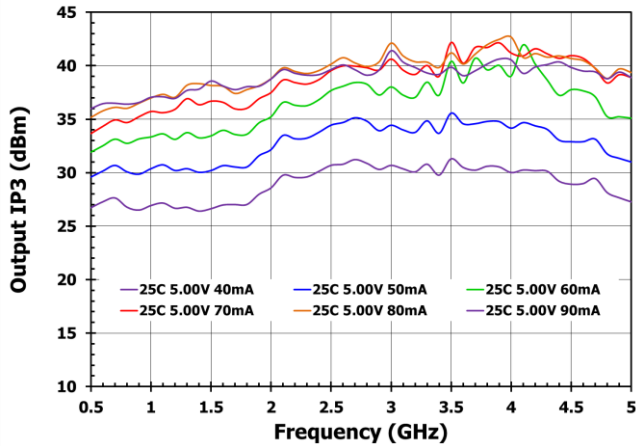
**Figure 9. Output IP3 versus Temperature (3.3V Variation, 70mA)**



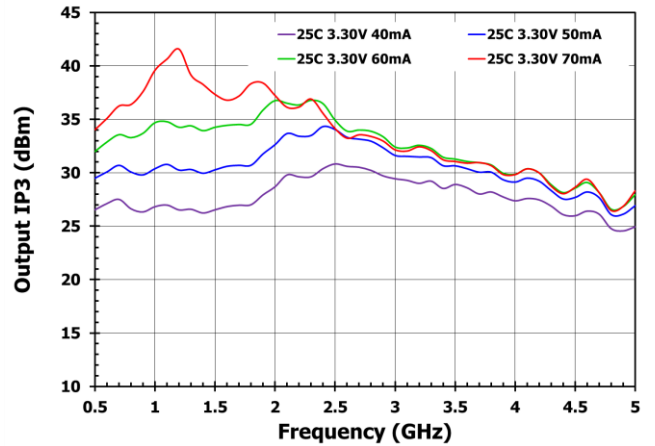
**Figure 10. Output IP3 versus Temperature (3.3V Variation, 40mA)**



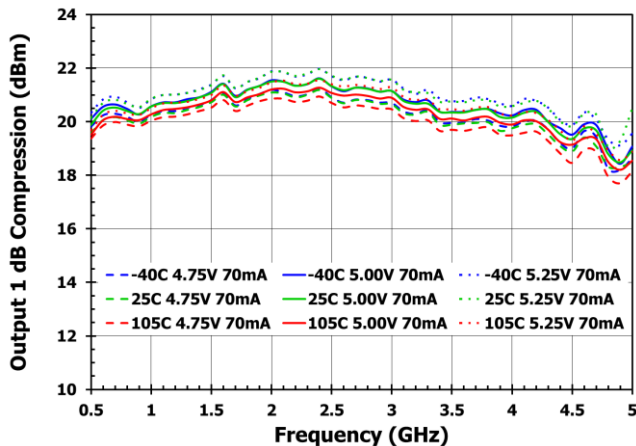
**Figure 11. Output IP3 versus Bias Current (5.0V)**



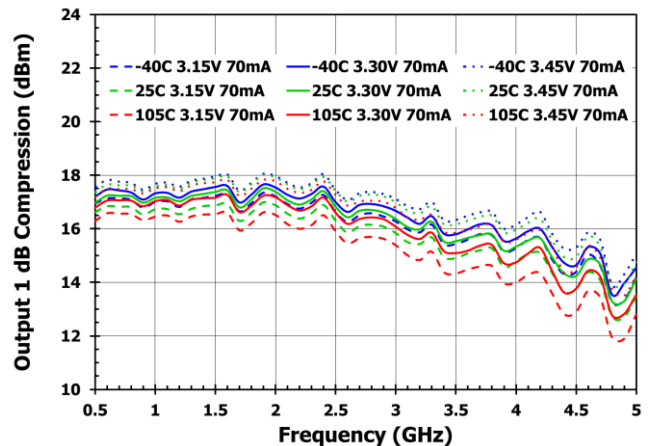
**Figure 12. Output IP3 versus Bias Current (3.3V)**



**Figure 13. Output 1dB Compression versus Temperature (5V Variation, 70mA)**

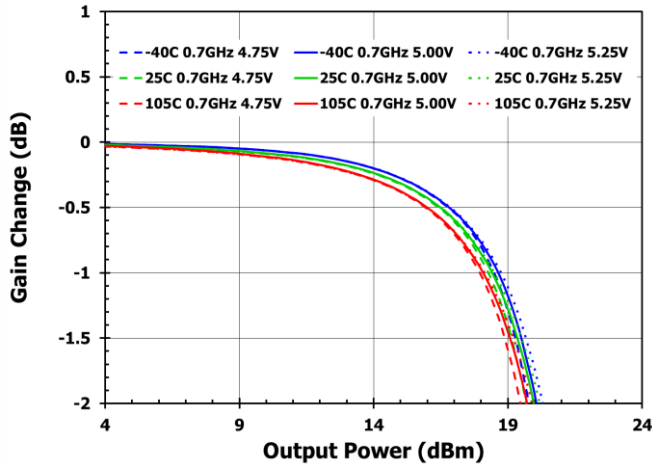


**Figure 14. Output 1dB Compression versus Temperature (3.3V Variation, 70mA)**

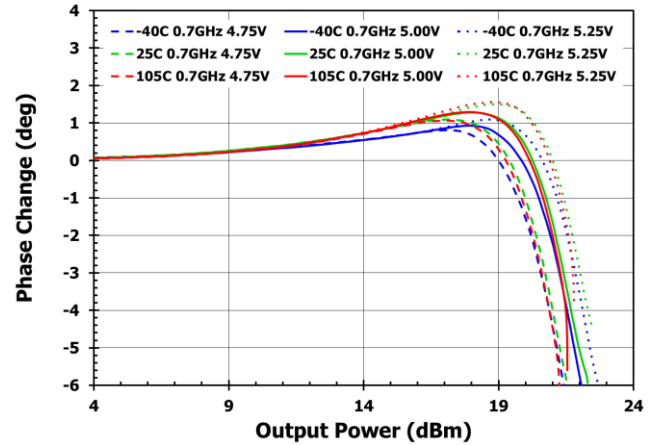


## Typical Performance Characteristics

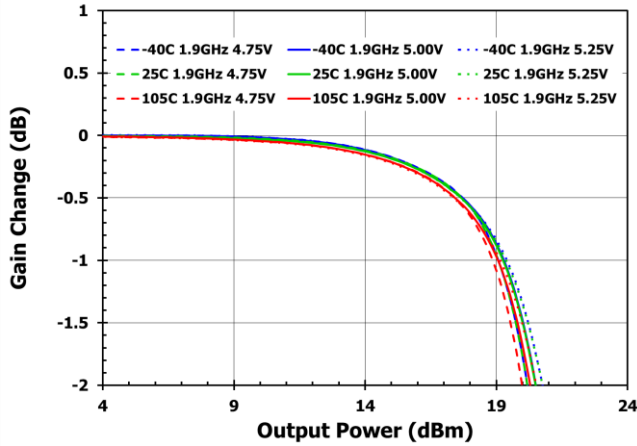
**Figure 15. Gain Compression versus Temperature (5V, 0.7GHz, 70mA)**



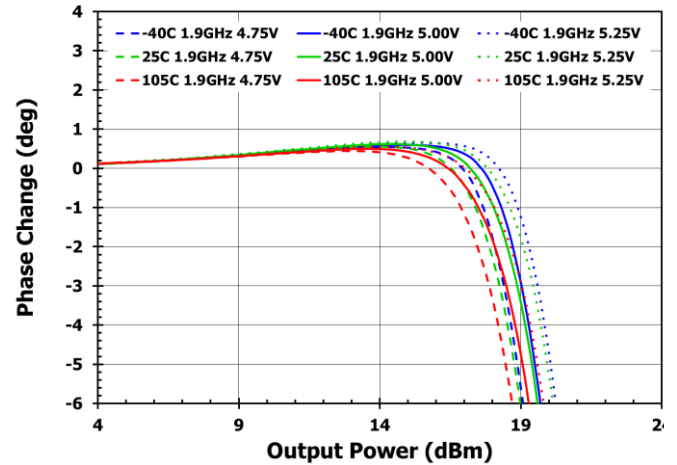
**Figure 16. Phase Compression versus Temperature (5V, 0.7GHz, 70mA)**



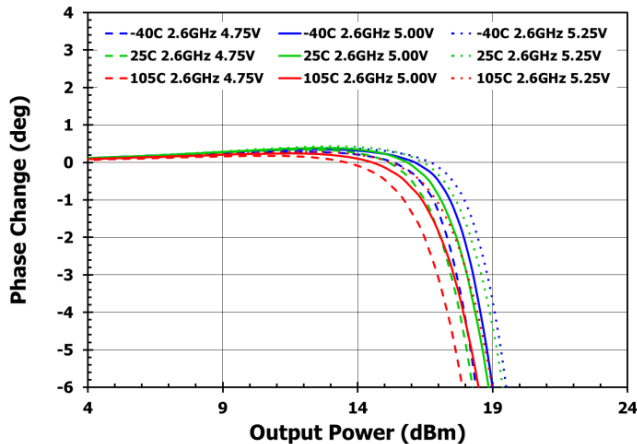
**Figure 17. Gain Compression versus Temperature (5V, 1.9GHz, 70mA)**



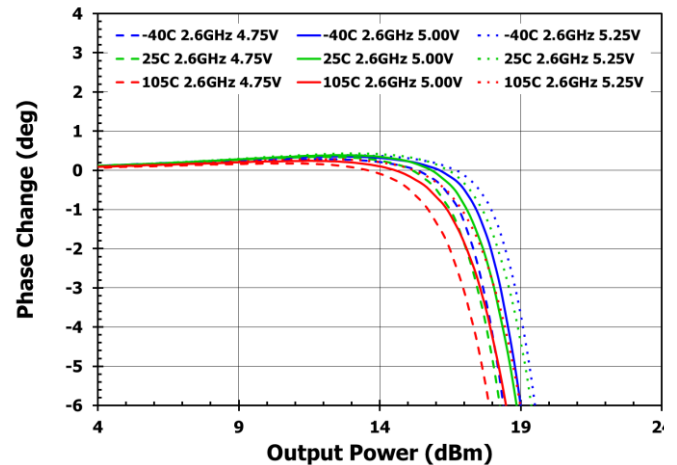
**Figure 18. Phase Compression versus Temperature (5V, 1.9GHz, 70mA)**



**Figure 19. Gain Compression versus Temperature (5V, 2.6GHz, 70mA)**

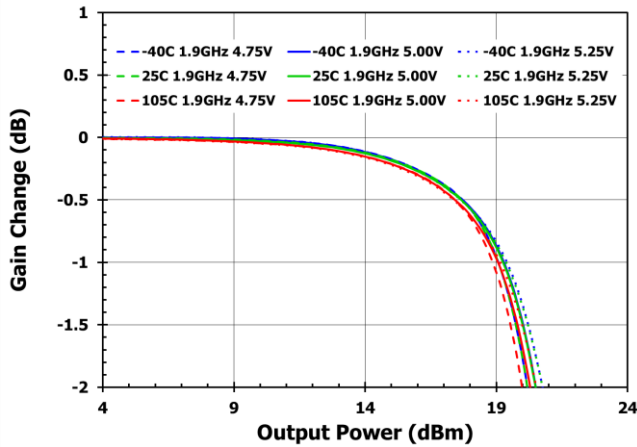


**Figure 20. Phase Compression versus Temperature (5V, 2.6GHz, 70mA)**

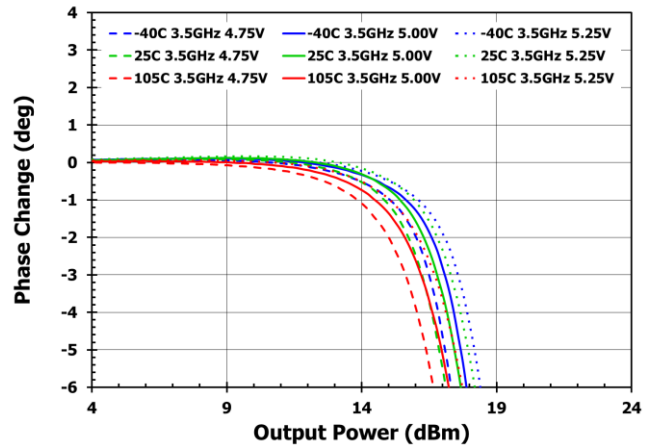


## Typical Performance Characteristics

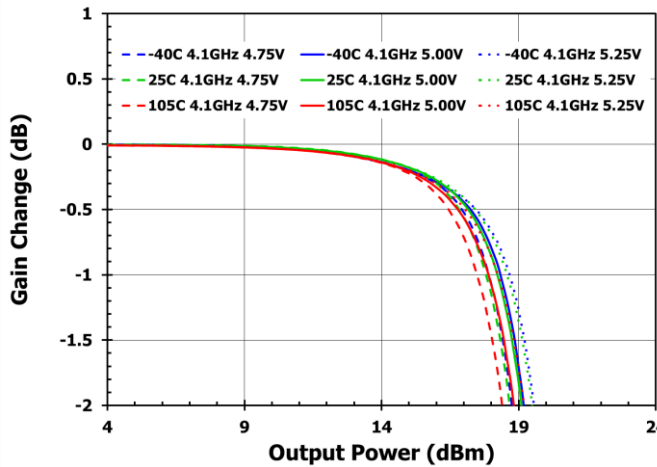
**Figure 21. Gain Compression versus Temperature (5V, 3.5GHz, 70mA)**



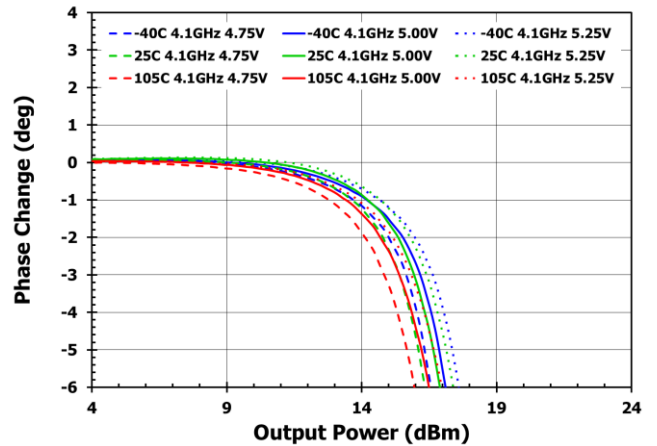
**Figure 22. Phase Compression versus Temperature (5V, 3.5GHz, 70mA)**



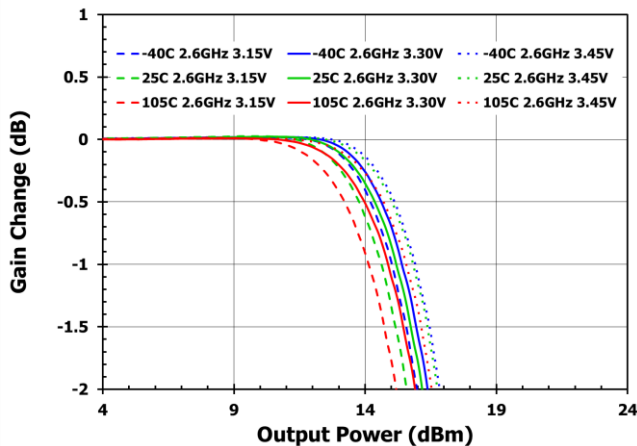
**Figure 23. Gain Compression versus Temperature (5V, 4.1GHz, 70mA)**



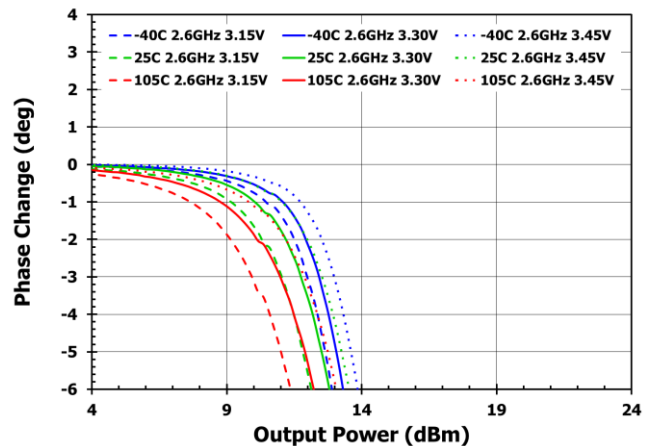
**Figure 24. Phase Compression versus Temperature (5V, 4.1GHz, 70mA)**



**Figure 25. Gain Compression versus Temperature (3.3V, 2.6GHz, 70mA)**

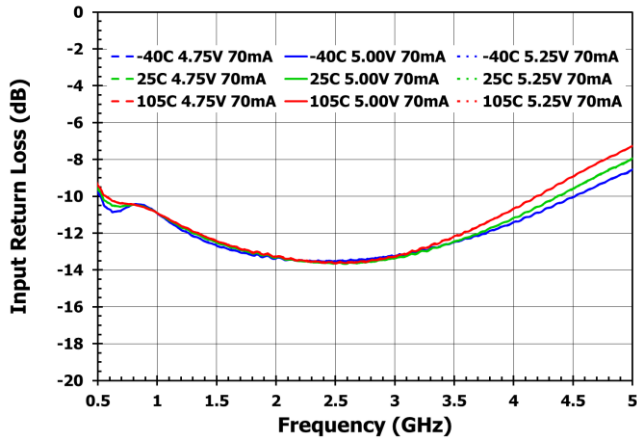


**Figure 26. Phase Compression versus Temperature (3.3V, 2.6GHz, 70mA)**

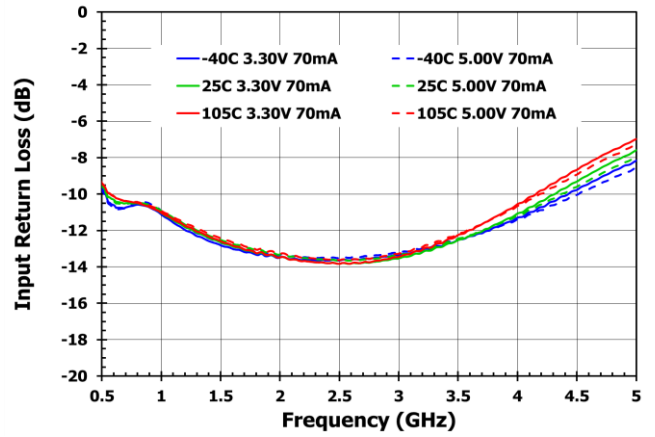


## Typical Performance Characteristics

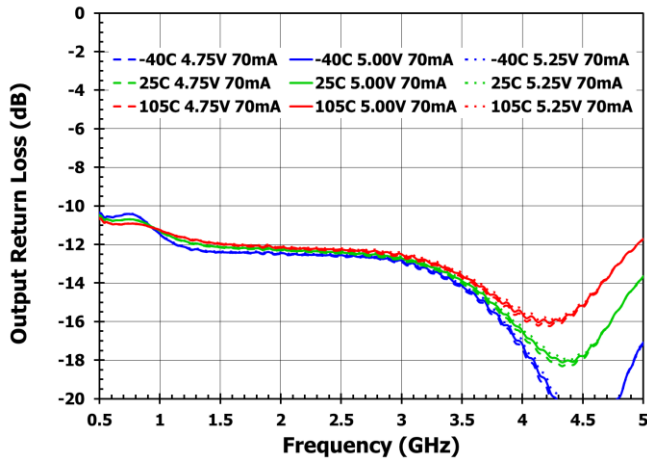
**Figure 27. RFIN Return Loss versus Temperature (5V Variation)**



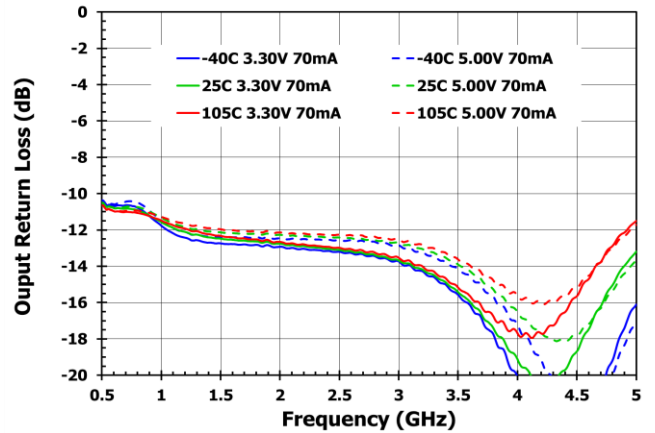
**Figure 28. RFIN Return Loss versus Temperature (3.3V Variation)**



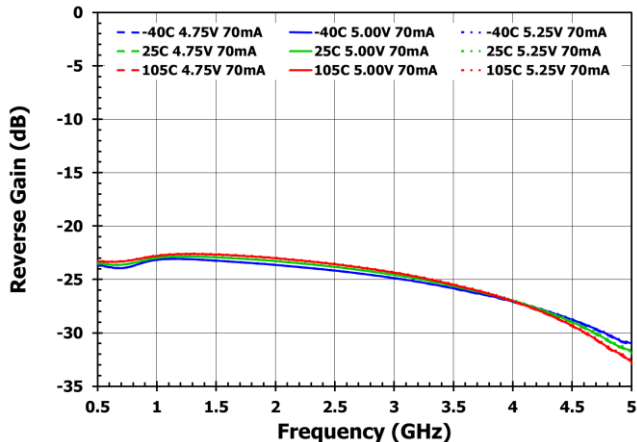
**Figure 29. RFOUT Return Loss versus Temperature (5V Variation)**



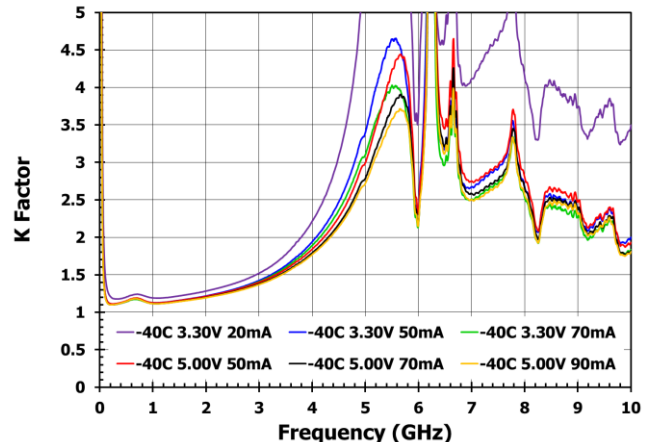
**Figure 30. RFOUT Return Loss versus Temperature (3.3V Variation)**



**Figure 31. Reverse Gain versus Temperature (5V Variation)**

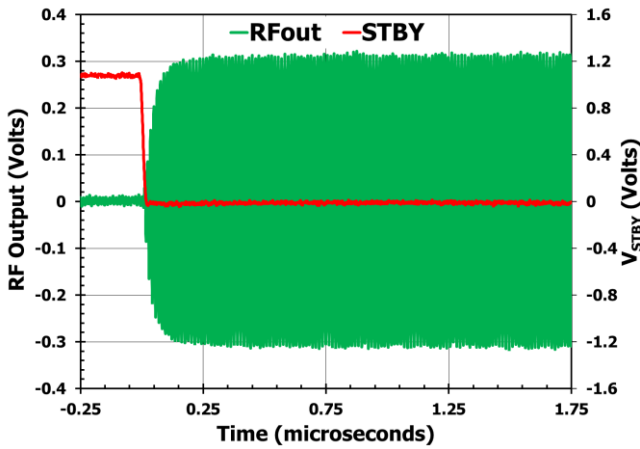


**Figure 32. Stability Factor for Various Currents (3.3V, 5.0V, -40°C, R8=1K)**

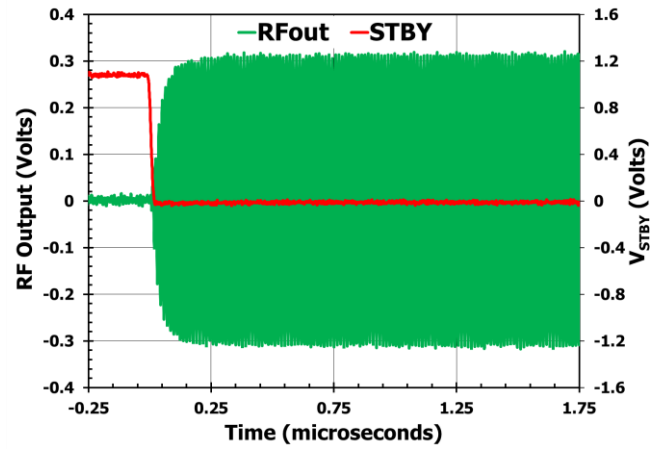


# Typical Performance Characteristics

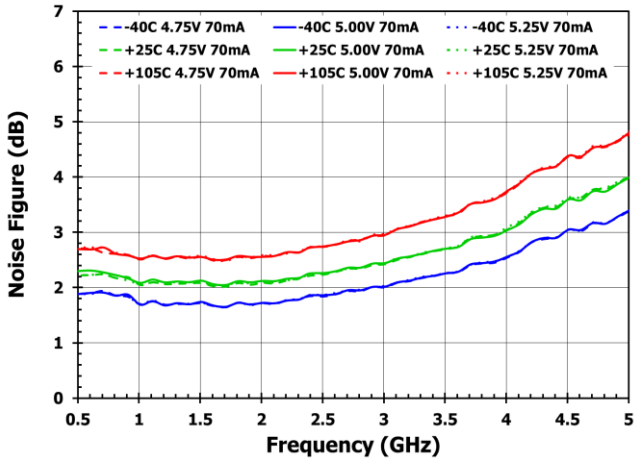
**Figure 33. Turn-on Time (3.3V)**



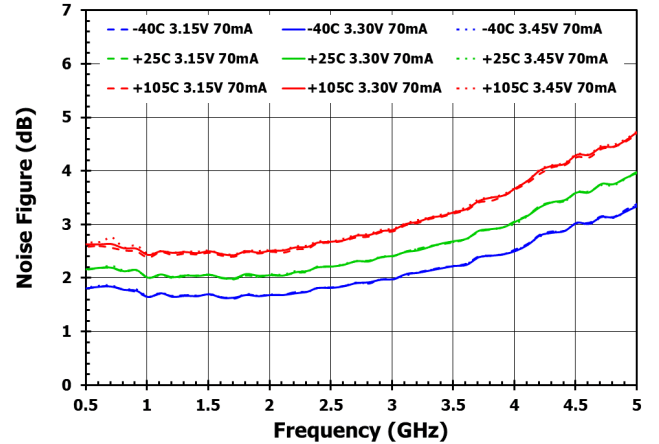
**Figure 34. Turn-on Time (5.0V)**



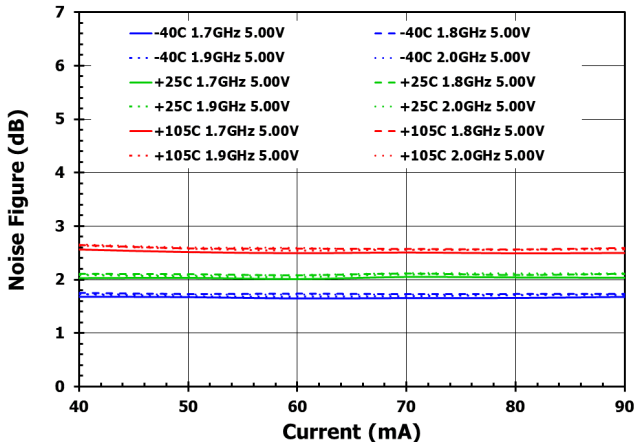
**Figure 35. Noise Figure versus Temperature (5.0V Variation)**



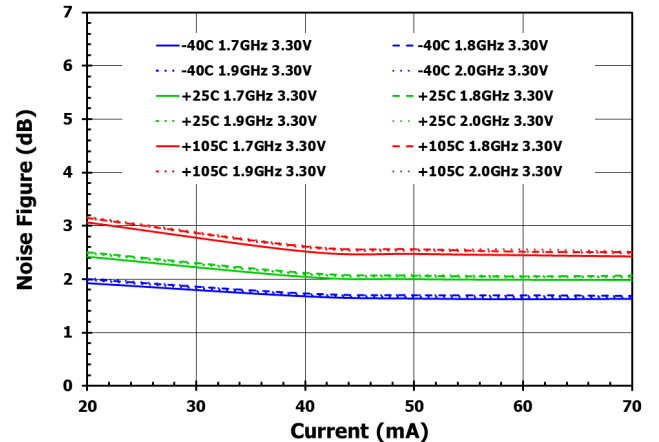
**Figure 36. Noise Figure versus Temperature (3.3V Variation)**



**Figure 37. Noise Figure versus Current (5.0V Variation)**



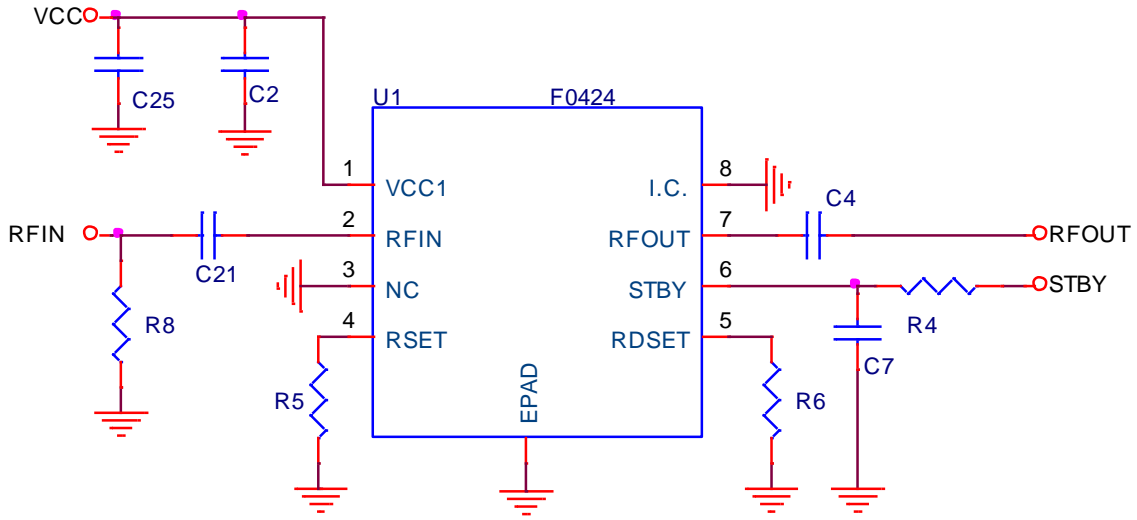
**Figure 38. Noise Figure versus Current (3.3V Variation)**



## Typical Application Circuit

Figure 39 is a typical circuit (minimum components) that can be use in a design for the F0424 by the customer.

**Figure 39. Electrical Schematic**





## Evaluation Kit Picture

Figure 40. Evaluation Kit – Top View

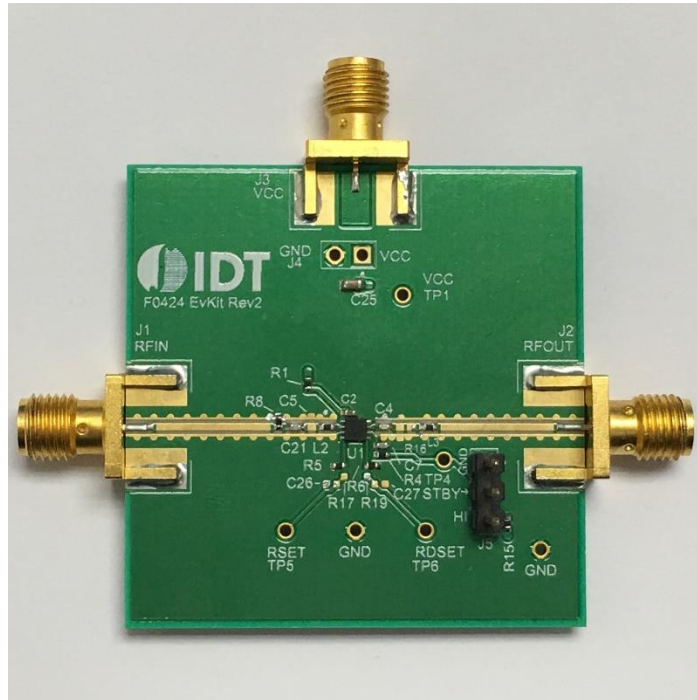
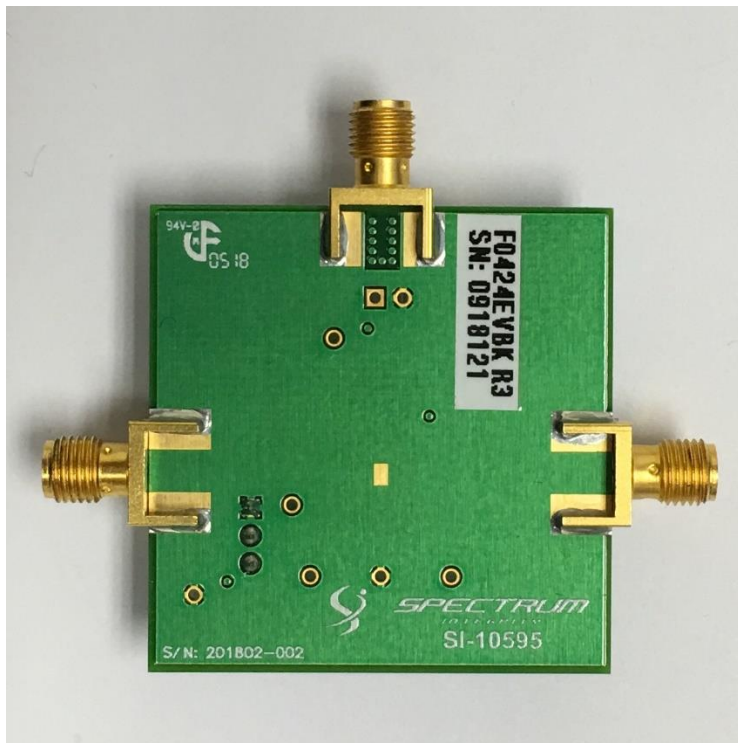
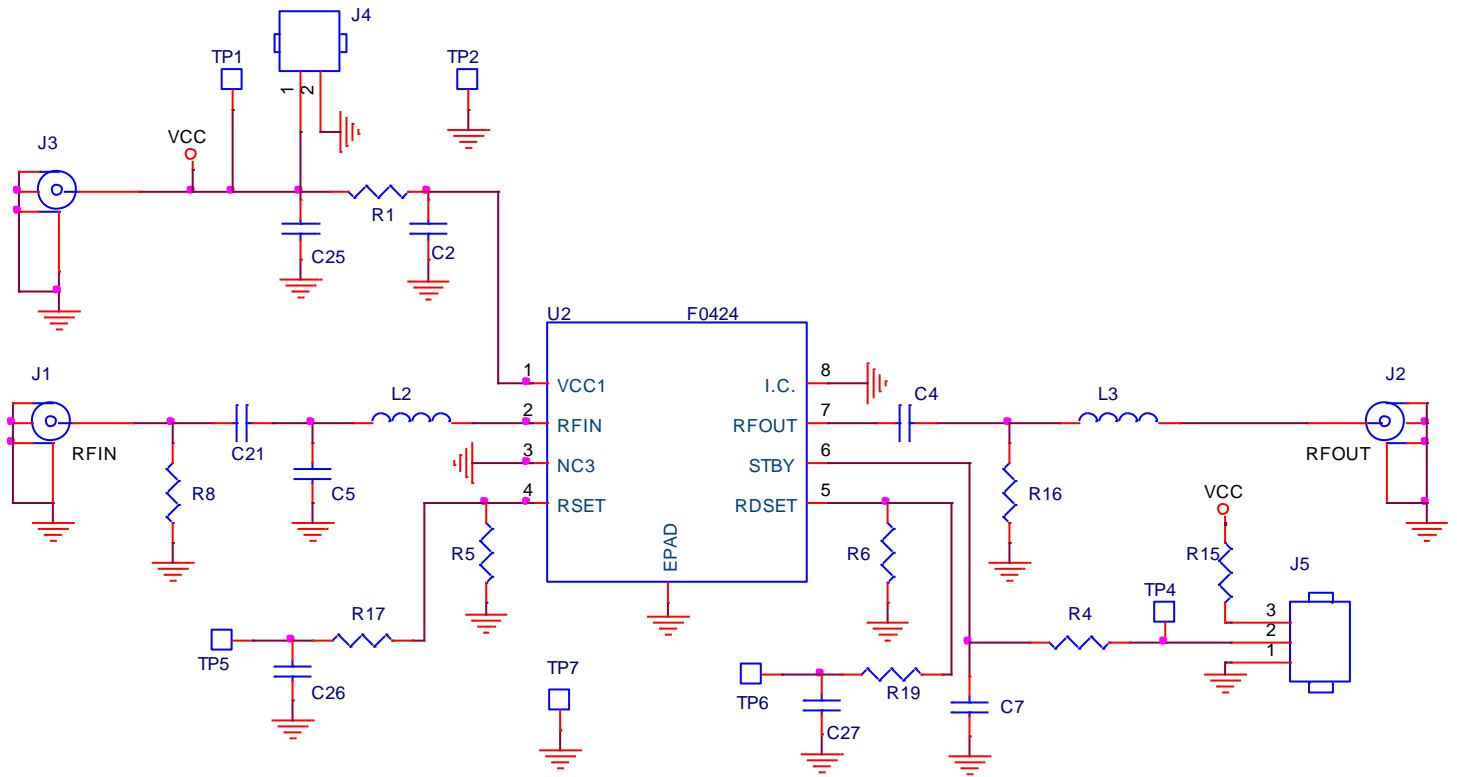


Figure 41. Evaluation Kit – Bottom View



## Evaluation Kit / Applications Circuit

Figure 42. Electrical Schematic for Evaluation Board



**Table 8. Bill of Material (BOM)**

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C2	1	10nF $\pm 5\%$ 50V X7R Ceramic Capacitor (0402)	GRM155R71H103J	Murata
C4, C21	2	22pF $\pm 5\%$ , 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H220J	Murata
C7	1	2pF $\pm 0.1\text{pF}$ 100V C0G, Ceramic Capacitor (0402)	GRM1555C1H2R0B	Murata
C25	1	1 $\mu\text{F}$ $\pm 10\%$ 16V X7R Ceramic Capacitor (0603)	GRM188R71C105K	Murata
L2, L3, R1, R15	4	0 $\Omega$ 1/10W Resistors (0402)	ERJ-2GE0R00X	Panasonic
R4, R8	1	1k $\Omega$ $\pm 1\%$ 1/10W Resistor (0402)	ERJ-3EKF1001X	Panasonic
R5	1	2.49k $\Omega$ $\pm 1\%$ 1/10W Resistor (0402) see Table 9 for resistor value versus operating current	ERJ-2RKF2491X	Panasonic
R6	1	160 $\Omega$ $\pm 1\%$ 1/10W Resistor (0402)	ERJ-2RKF1600X	Panasonic
J1, J2, J3	3	Edge Launch SMA (0.375 inch pitch ground tab)	142-0701-851	Emerson Johnson
J4	0	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J5	1	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
TP1	1	TEST POINT PC MINI .040"D RED	Keystone5000	Keystone
TP2	1	TEST POINT PC MINI .040"D BLACK	Keystone5001	Keystone
TP4, TP5, TP6, TP7	0	DNP		
U1	1	High Gain Broadband RF Amplifier	F0424	IDT
C5, C26, C27, R16, R17, R19	NA	These components are not populated		

**Table 9. RSET Biasing Resistor for Various Bias Currents (5V, 3.3V Supply)**

Operating $I_{cc}$	RSET Resistor (R5)
40mA	6.19k $\Omega$
50mA	4.22k $\Omega$
60mA	3.16k $\Omega$
70mA	2.49k $\Omega$
80mA	2.00k $\Omega$
90mA	1.74k $\Omega$

NOTE: 1% Resistors can be substituted with 5% equivalents.

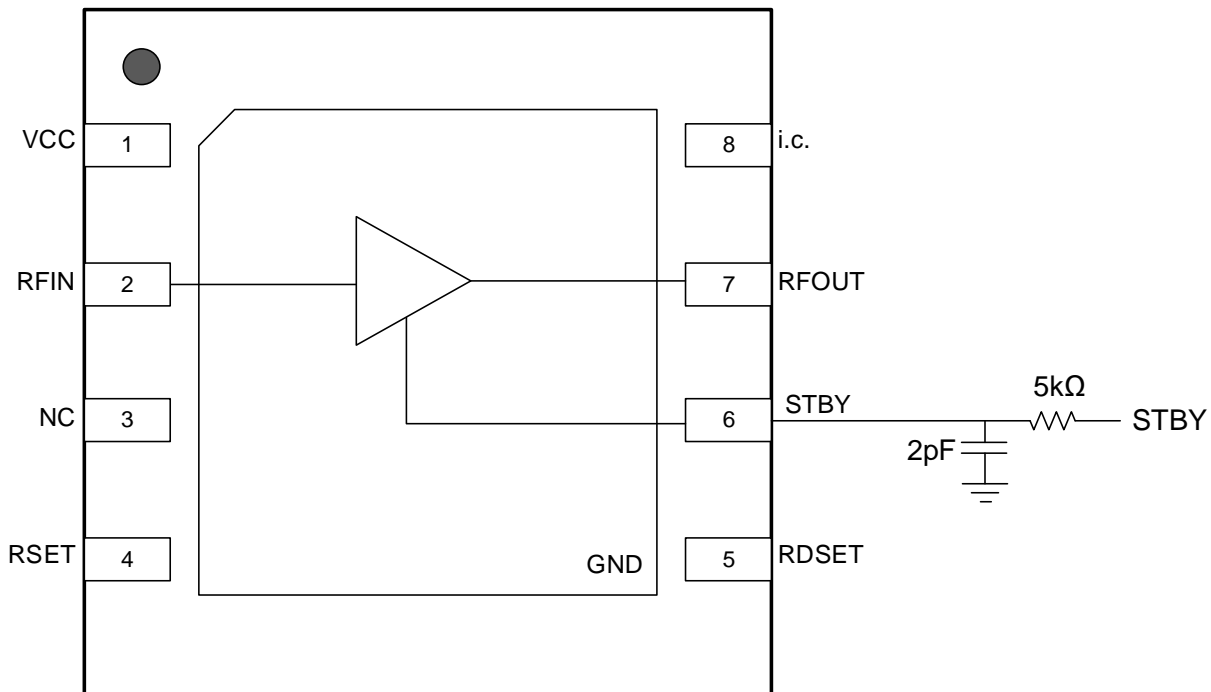
## Applications Information

### Power Supplies

A common  $V_{CC}$  power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V/20\mu S$ . In addition, all control pins should remain at  $0V (\pm 0.3V)$  while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of the STBY control pin is recommended. This applies to the STBY pin as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

**Figure 43. Control Pin Interface for Signal Integrity**

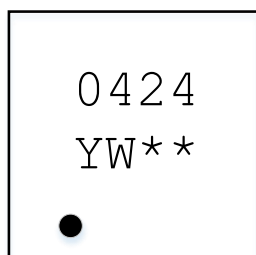


## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

<https://www.idt.com/document/psc/8-dfn-package-outline-drawing-20-x-20-x-075-mm-body-05mm-pitch-epad-08-x-160-mm-ntg8p2>

## Marking Diagram



Line 1 – 0424 = abbreviated the part number.

Line 2 – Y = Year code, last digit of production year (“8” would correspond to 2018).

Line 2 – W = Work week code (“W” corresponds to week 30).

Line 2 - \*\* = Sequential alphanumeric for lot traceability.

## Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
F0424NTGK	F0424 High-Gain Broadband RF Amplifier, 2.0 × 2.0 × 0.75 mm 8-DFN (NTG8P2)	1	Tray	-40°C to +105°C
F0424NTGK8	F0424 High-Gain Broadband RF Amplifier, 2.0 × 2.0 × 0.75 mm 8-DFN (NTG8P2)	1	Reel	-40°C to +105°C
F0424EVBK	Evaluation Board			

## Revision History

Revision Date	Description of Change
March 7, 2019	<ul style="list-style-type: none"> <li>▪ Added simplified application circuit.</li> <li>▪ Updated datasheet format</li> </ul>
May 5, 2018	Initial release.



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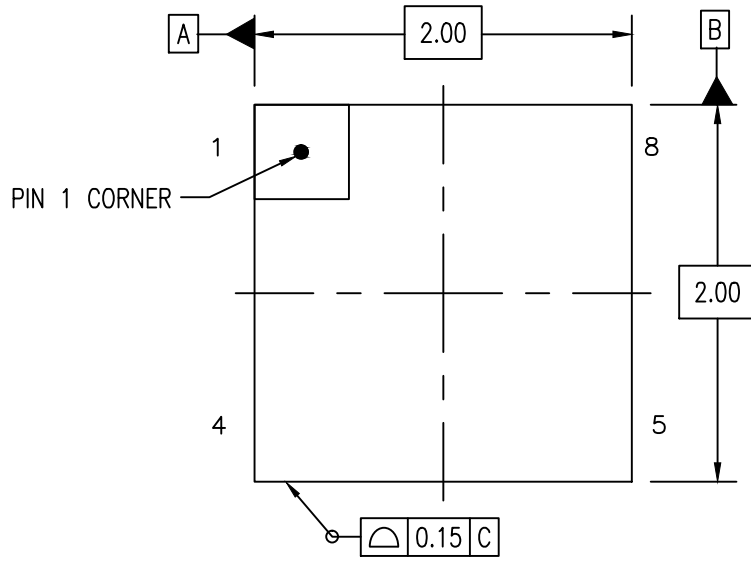
### Tech Support

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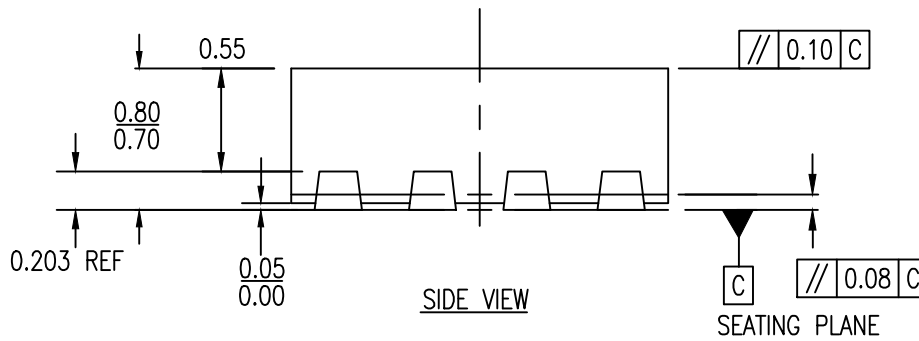
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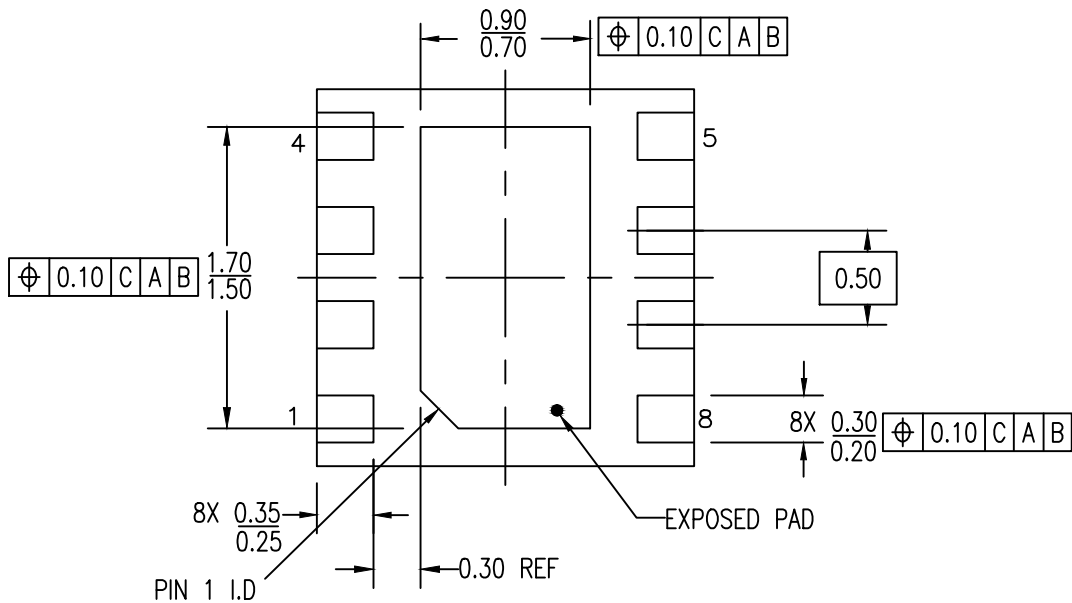
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TOP VIEW



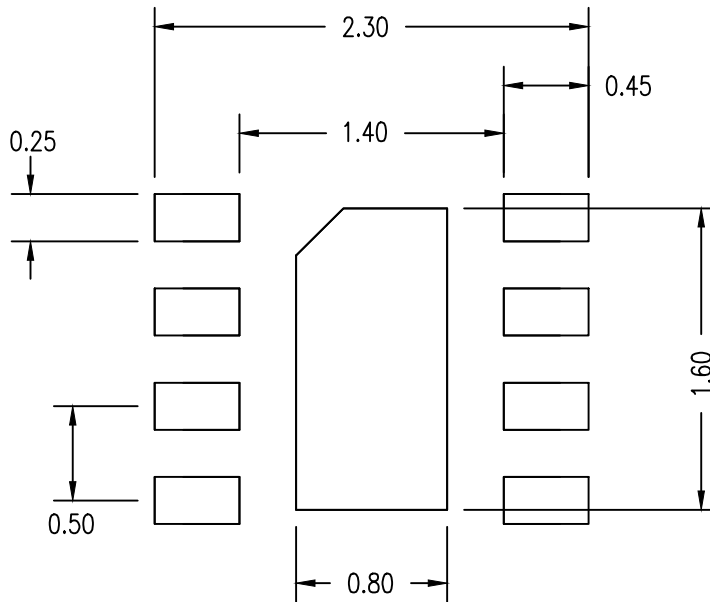
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994



### RECOMMENDED LAND PATTERN DIMENSION

#### NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Feb 12, 2018	Rev 01.	New Format, Change QFN to VFQFPN
April 12, 2018	Rev 02	Change "VFQFPN" to "DFN"