Dual Low Power PLL Frequency Synthesizer

Data Sheet

ADF4212L

FEATURES

- I_{DD} total: 7.5 mA
- Bandwidth RF/IF: 2.4 GHz/1.0 GHz
- 2.7 V to 3.3 V power supply
- Separate V_P allows extended tuning voltage
- Programmable dual modulus prescaler
  - RF and IF: 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- 3-wire serial interface
- Analog and digital lock detect
- Fastlock mode
- Power-down mode
- 20-lead TSSOP and 20-lead LFCSP packages

APPLICATIONS

- Wireless handsets (GSM, PCS, DCS, DSC1800, CDMA, WCDMA)
- Base stations for wireless Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANS
- Cable TV tuners (CATV)
- Communications test equipment

GENERAL DESCRIPTION

The ADF4212L is a dual frequency synthesizer that can be used to implement local oscillators (LO) in the up-conversion and down-conversion sections of wireless receivers and transmitters. It can provide the LO for both the RF and IF sections. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual modulus prescaler (P/P + 1). The A (6-bit) and B (12-bit) counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 15-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with external loop filters and voltage controlled oscillators (VCOs).

Control of all the on-chip registers is via a simple 3-wire interface with 1.8 V compatibility. The devices operate with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

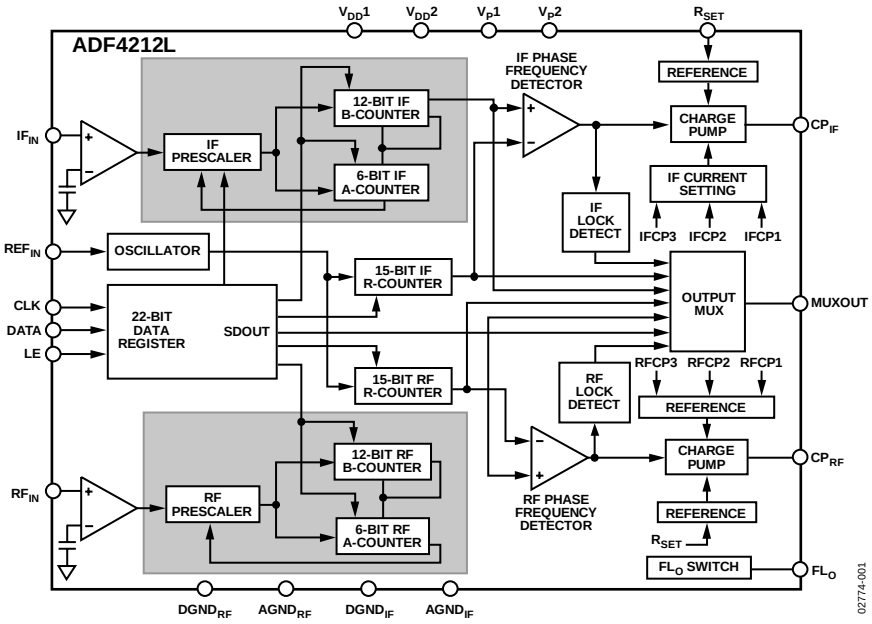

Figure 1.

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SPECIFICATIONS

$V_{DD}1 = V_{DD}2 = 2.7$ V to 3.3 V; V_P1, $V_P2 = V_{DD}$ to 5.5 V; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0$ V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 1.

Parameter[1]	B Version	B Chips[2]	Unit	Test Conditions/Comments
RF/IF CHARACTERISTICS				
RF Input Frequency (RF_{IN})	0.2/2.4	0.2/2.4	GHz min/max	For lower frequencies, ensure that slew rate (SR) > 140 V/µs
RF Input Sensitivity	−10/0	−10/0	dBm min/max	V_{DD} = 3 V
IF Input Frequency (IF_{IN})	100/1000	100/1000	MHz min/max	
IF Input Sensitivity	−10/0	−10/0	dBm min/max	V_{DD} = 3 V
MAXIMUM ALLOWABLE				
Prescaler Output Frequency[3]	188	188	MHz max	
REF_{IN} CHARACTERISTICS				See Figure 26 for input circuit
REF_{IN} Input Frequency	10/150	10/150	MHz min/max	
REF_{IN} Input Sensitivity	500 mV/V_{DD}	500 mV/V_{DD}	V p-p min/max	AC-coupled; when dc-coupled, 0 V to V_{DD} maximum (CMOS compatible)
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[4]	75	75	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable, see Table 10
High Value	5	5	mA typ	With R_{SET} = 2.7 kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2	2	% typ	With R_{SET} = 2.7 kΩ
R_{SET} Range	1.5/5.6	1.5/5.6	kΩ min/max	
I_{CP} Three-State Leakage Current	1	1	nA max	
Sink and Source Current Matching	6	6	% typ	0.5 V < V_{CP} < V_P − 0.5 V
I_{CP} vs. V_{CP}	2	2	% typ	0.5 V < V_{CP} < V_P − 0.5 V
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	1.4	1.4	V min	
V_{INL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	1.4	1.4	V min	Open-drain 1 kΩ pull-up to 1.8 V
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
$V_{DD}1$	2.7/3.3	2.7/3.3	V min/max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$	V min/max	
V_P1, V_P2	$V_{DD}1$/5.5	$V_{DD}1$/5.5	V min/max	
I_{DD} (RF and IF)[5]	7.5/10	7.5/10	mA typ/max	
RF Only	5.0/6	5.0/6	mA typ/max	
IF Only	2.5/4	2.5/4	mA typ/max	
I_P (I_P1 + I_P2)	0.6	0.6	mA typ	
Low Power Sleep Mode	1	1	µA typ	

[1] Operating temperature range is as follows: B version: −40°C to +85°C.
[2] The B chip specifications are given as typical values.
[3] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency less than this value.
[4] Guaranteed by design. Sample tested to ensure compliance.
[5] T_A = 25°C. RF = 1 GHz; prescaler = 32/33. IF = 500 MHz; prescaler = 16/17.

$V_{DD}1 = V_{DD}2 = 2.7$ V to 3.3 V; V_P1, $V_P2 = V_{DD}$ to 5.5 V; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0$ V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; dBm referred to 50 V.

Table 2.

Parameter[1]	B Version	B Chips[2]	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
RF Phase Noise Floor[3]	−170	−170	dBc/Hz typ	25 kHz PFD frequency
	−162	−162	dBc/Hz typ	200 kHz PFD frequency
Phase Noise Performance[4]				VCO output
IF: 540 MHz Output[5]	−89	−89	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
IF: 900 MHz Output[6]	−87	−87	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
RF: 900 MHz Output[6]	−89	−89	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
RF: 1750 MHz Output[7]	−84	−84	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
RF: 2400 MHz Output[8]	−87	−87	dBc/Hz typ	1 kHz Offset and 1 MHz PFD frequency
Spurious Signals				
IF: 540 MHz Output[5]	−88/−90	−88/−90	dB typ	200 kHz/400 kHz and 200 kHz PFD frequency
IF: 900 MHz Output[6]	−90/−94	−90/−94	dB typ	200 kHz/400 kHz and 200 kHz PFD frequency
RF: 900 MHz Output[6]	−90/−94	−90/−94	dB typ	200 kHz/400 kHz and 200 kHz PFD frequency
RF: 1750 MHz Output[7]	−80/−82	−80/−82	dB typ	200 kHz/400 kHz and 200 kHz PFD frequency
RF: 2400 MHz Output[8]	−80/−82	−80/−82	dB typ	200 kHz/400 kHz and 200 kHz PFD frequency

[1] Operating temperature range is as follows: B version: −40°C to +85°C.
[2] The B Chip specifications are given as typical values.
[3] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value). See Figure 9.
[4] The phase noise is measured with the EVAL-ADF4212EB and the HP8562E spectrum analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz at 0 dBm).
[5] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{IF} = 540 MHz; N = 2700; loop B/W = 20 kHz
[6] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; loop B/W = 20 kHz
[7] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; loop B/W = 20 kHz
[8] f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; offset frequency = 1 kHz; f_{RF} = 2400 MHz; N = 9800; loop B/W = 20 kHz

TIMING CHARACTERISTICS

$V_{DD}1 = V_{DD}2 = 2.6$ V to 3.3 V; V_P1, $V_P2 = V_{DD}$ to 5.5 V; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0$ V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 3.

Parameter[1]	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	Data to clock setup time
t_3	10	ns min	Data to clock hold time
t_4	25	ns min	Clock high duration
t_5	25	ns min	Clock low duration
t_6	10	ns min	Clock to LE setup time
t_7	20	ns min	LE pulse width

[1] Guaranteed by design but not production tested.

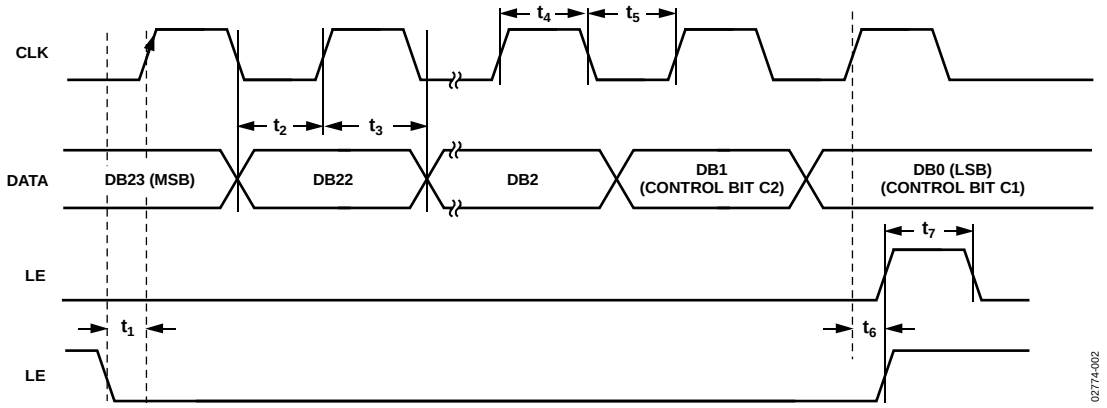

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter[1, 2]	Rating
$V_{DD}1$ to GND	−0.3 V to +3.6 V
$V_{DD}1$ to $V_{DD}2$	−0.3 V to +0.3 V
V_P1, V_P2 to GND	−0.3 V to +5.8 V
V_P1, V_P2 to $V_{DD}1$, $V_{DD}2$	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN}, IF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	122°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Not Soldered)	216°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and is ESD sensitive. Proper precautions should be taken for handling and assembly.
[2] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

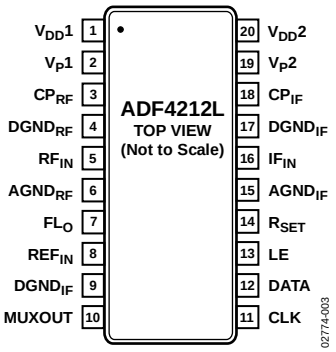

Figure 3. TSSOP Pin Configuration

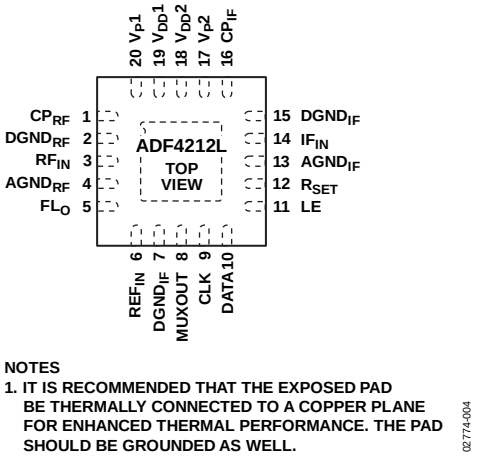

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Mnemonic	Pin No. TSSOP	Pin No. LFCSP	Description
CP_{RF}	3	1	RF Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external RF loop filter, which in turn drives the external RF VCO.
$DGND_{RF}$	4	2	Digital Ground Pin for the RF Digital Circuitry.
RF_{IN}	5	3	Input to the RF Prescaler. This small signal input is normally ac-coupled from the RF VCO.
$AGND_{RF}$	6	4	Ground Pin for the RF Analog Circuitry.
FL_O	7	5	Multiplexed Output of RF/IF Programmable or Reference Dividers, RF/IF Fastlock Mode. CMOS output.
REF_{IN}	8	6	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. See Figure 26. This input can be driven from a TTL or CMOS crystal oscillator, or can be ac-coupled.
$DGND_{IF}$	9, 17	7, 15	Digital Ground Pin for the IF Digital, Interface, and Control Circuitry.
MUXOUT	10	8	This multiplexer output allows either the IF/RF lock detect, the scaled RF, the scaled IF, or the scaled reference frequency to be accessed externally.
CLK	11	9	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	12	10	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	13	11	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, with the latch selected using the control bits.
R_{SET}	14	12	Connecting a resistor between this pin and ground sets the maximum RF and IF charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is, therefore, $$I_{CP\ MAX} = \frac{13.5}{R_{SET}}$$ where R_{SET} = 2.7 kΩ and $I_{CP\ MAX}$ = 5 mA for both the RF and IF charge pumps.
$AGND_{IF}$	15	13	Ground Pin for the IF Analog Circuitry.
IF_{IN}	16	14	Input to the IF Prescaler. This small signal input is normally ac-coupled from the IF VCO.
CP_{IF}	18	16	Output from the IF Charge Pump. This is normally connected to a loop filter that drives the input to an external VCO.
V_P2	19	17	Power Supply for the IF Charge Pump. This should be greater than or equal to $V_{DD}2$. In systems where $V_{DD}2$ is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range up to 5.5 V.

Mnemonic	Pin No. TSSOP	Pin No. LFCSP	Description
$V_{DD}2$	20	18	Power Supply for the IF, Digital, and Interface Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}2$ should have a value of between 2.6 V and 3.3 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.
$V_{DD}1$	1	19	Power Supply for the RF Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}1$ should have a value of between 2.6 V and 3.3 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
V_P1	2	20	Power Supply for the RF Charge Pump. This should be greater than or equal to $V_{DD}1$. In systems where $V_{DD}1$ is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range up to 5.5 V.
EP		Exposed Pad	It is recommended that the exposed pad be thermally connected to a copper plane for enhanced thermal performance. The pad should be grounded as well.

TYPICAL PERFORMANCE CHARACTERISTICS

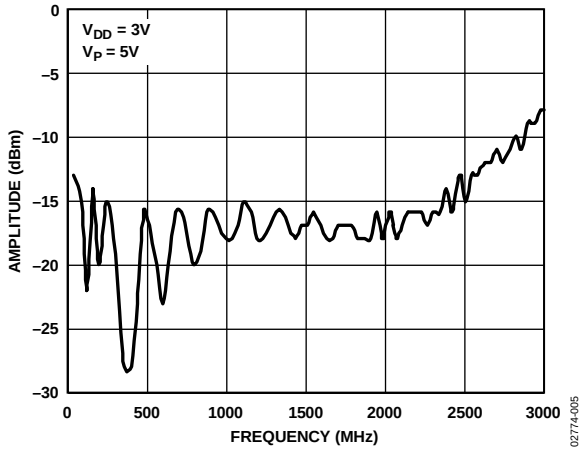

Figure 5. Input Sensitivity (RF Input)

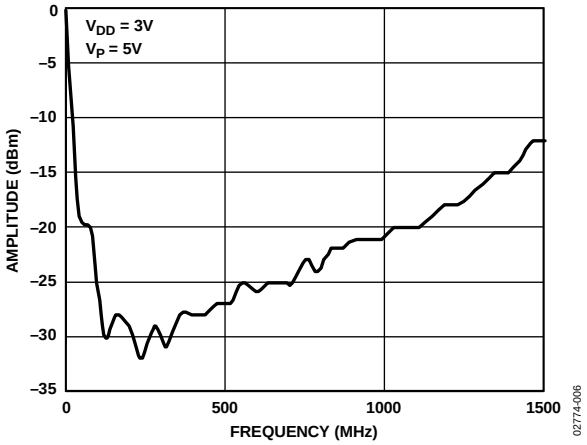

Figure 6. Input Sensitivity (IF Input)

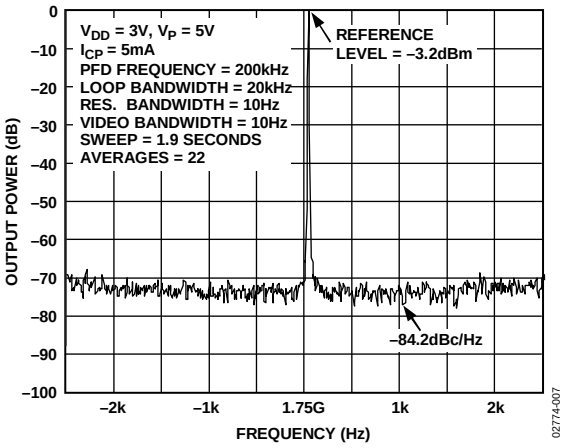

Figure 7. Phase Noise, RF Side (1750 MHz, 200 kHz, 20 kHz)

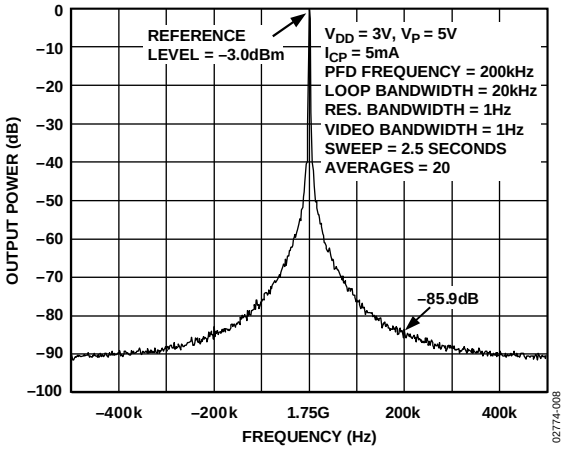

Figure 8. Reference Spurs, RF Side (1750 MHz, 200 kHz, 20 kHz)

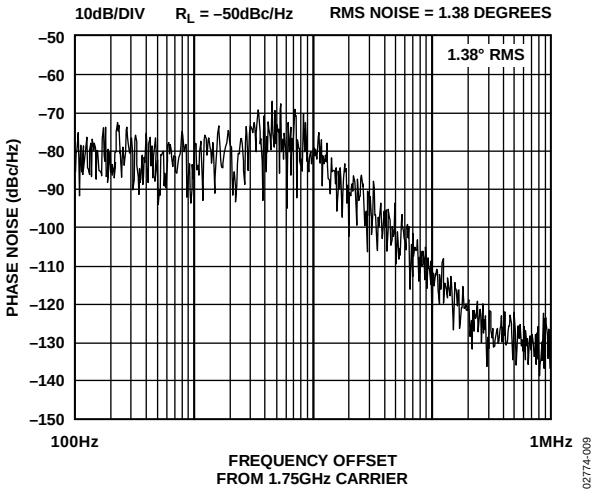

Figure 9. Integrated Phase Noise (1750 MHz, 200 kHz/20 kHz)

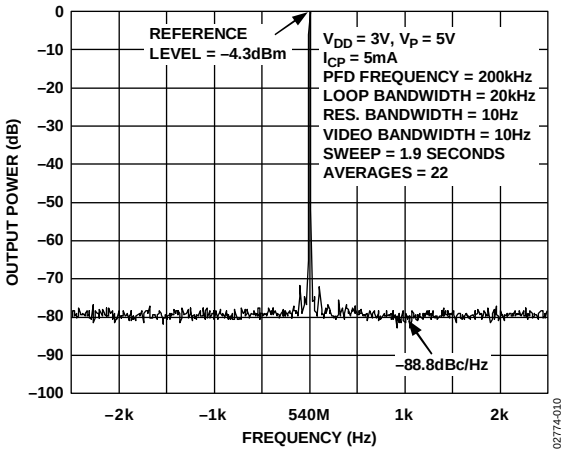

Figure 10. Phase Noise, IF Side (540 MHz, 200 kHz/20 kHz)

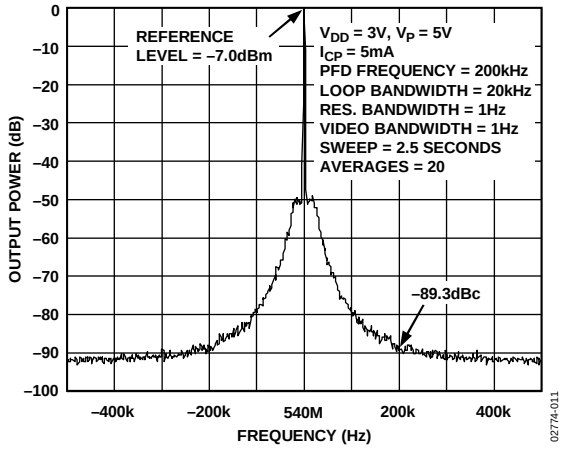

Figure 11. Reference Spurs, IF Side (540 MHz, 200 kHz, 20 kHz)

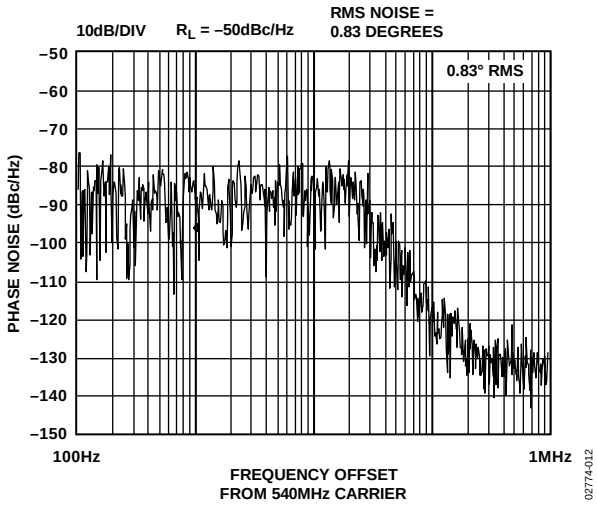

Figure 12. Integrated Phase Noise (540 MHz, 200 kHz/20 kHz)

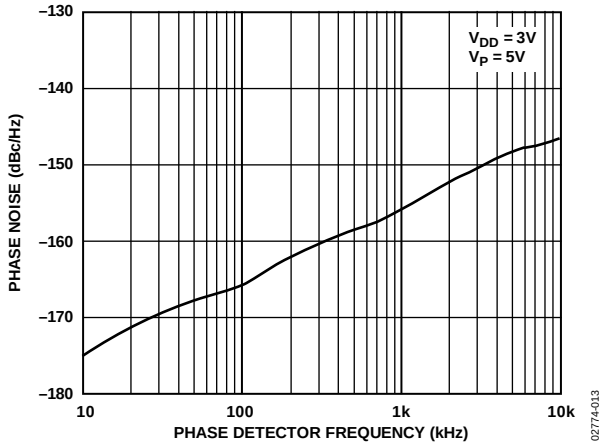

Figure 13. Phase Noise Referred to CP Output vs. PFD Frequency, RF Side

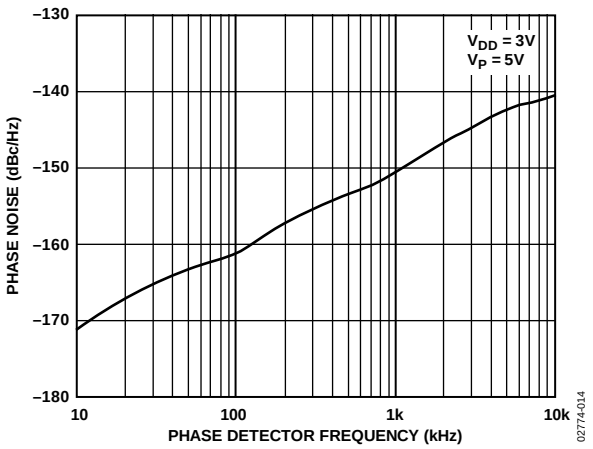

Figure 14. Phase Noise Referred to CP Output vs. PFD Frequency, IF Side

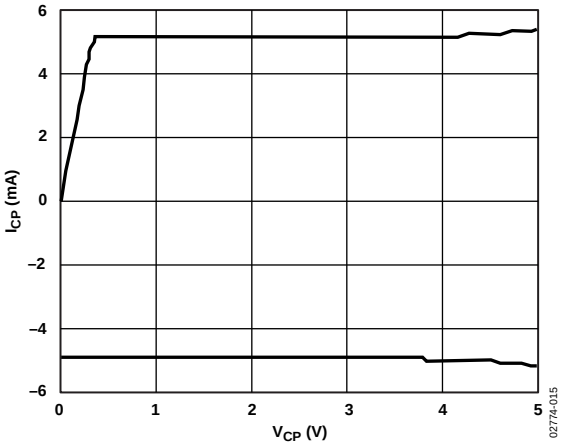

Figure 15. RF Charge Pump Output Characteristics

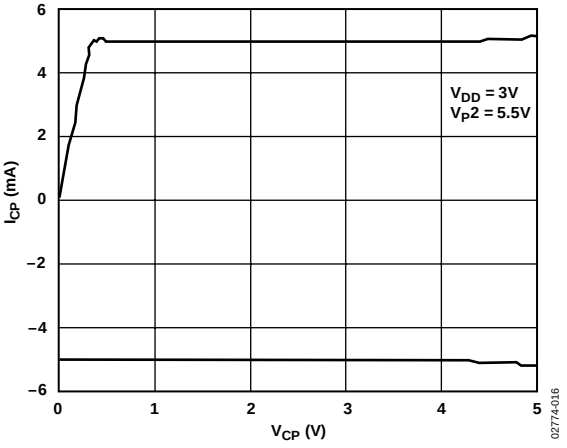

Figure 16. IF Charge Pump Output Characteristics

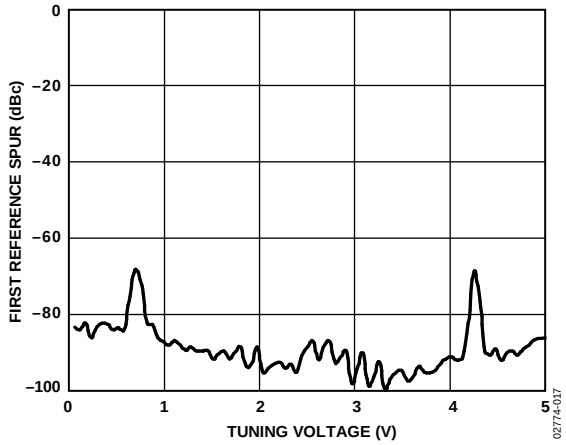

Figure 17. RF Reference Spurs (200 kHz) vs. V_{TUNE} (1750 MHz, 200 kHz, 20 kHz)

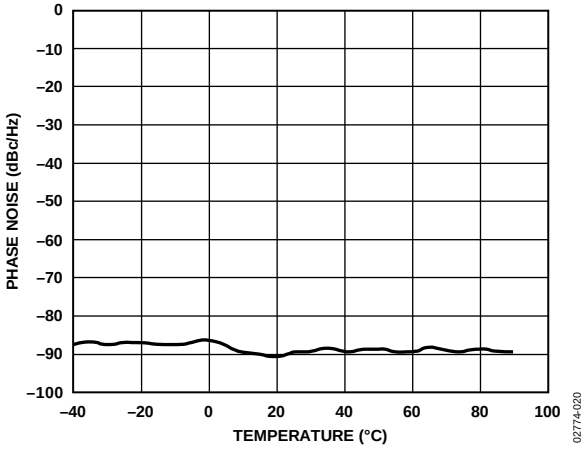

Figure 20. IF Phase Noise vs. Temperature (540 MHz, 200 kHz, 20 kHz)

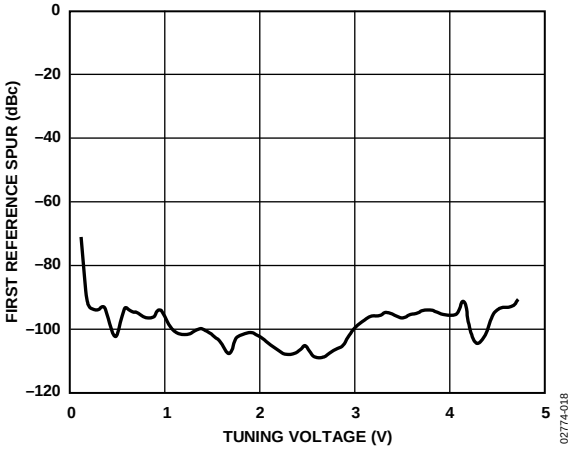

Figure 18. IF Reference Spurs (200 kHz) vs. V_{TUNE} (1750 MHz, 200 kHz, 20 kHz)

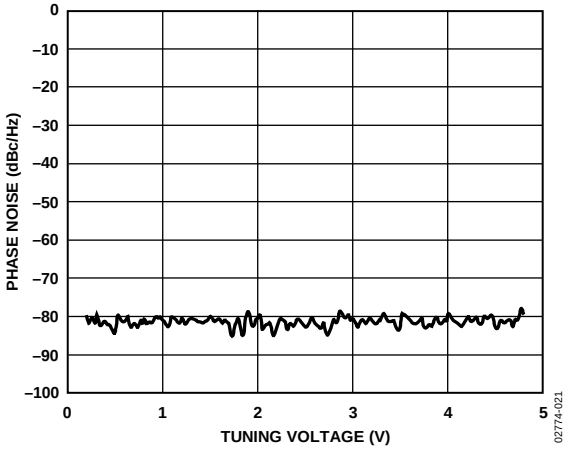

Figure 21. RF Noise vs. V_{TUNE}

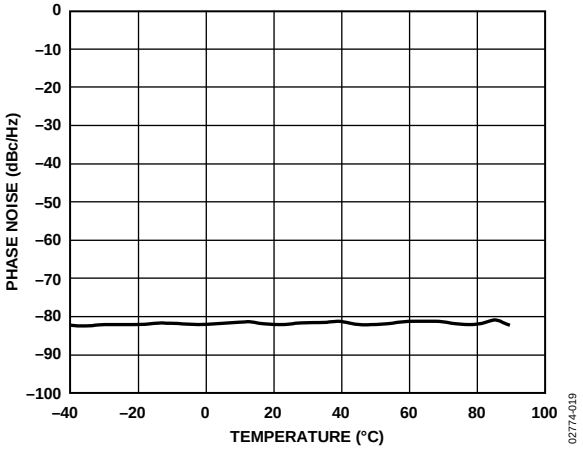

Figure 19. RF Phase Noise vs. Temperature (1750 MHz, 200 kHz, 20 kHz)

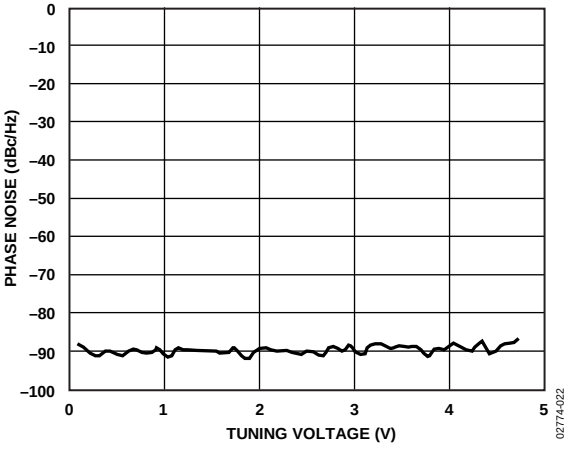

Figure 22. IF Noise vs. V_{TUNE}

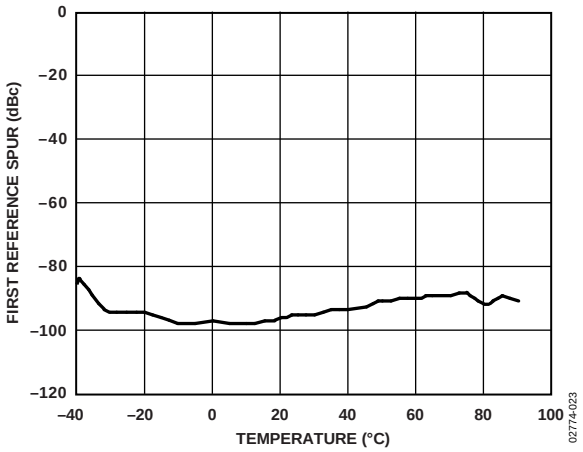

Figure 23. RF Spurs vs. Temperature

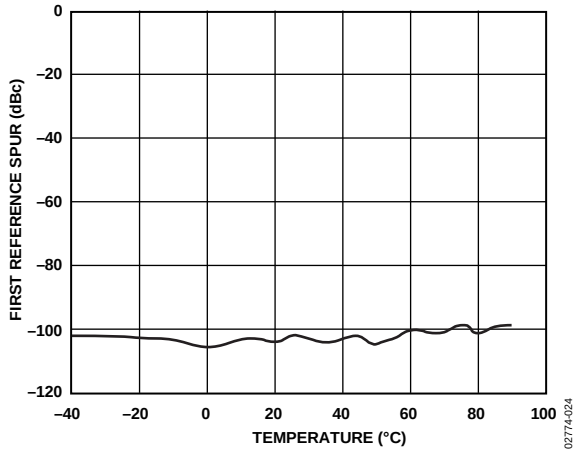

Figure 24. IF Spurs vs. Temperature

FREQUENCY (MHz)	s11.REAL	s11.IMAG	FREQUENCY (MHz)	s11.REAL	s11.IMAG
50	0.97692	–0.021077	1550	0.561872	–0.646879
150	0.942115	–0.110459	1650	0.529742	–0.668172
250	0.961217	–0.085802	1750	0.514244	–0.702192
350	0.920667	–0.185830	1850	0.405754	–0.714541
450	0.897441	–0.245482	1950	0.379354	–0.703593
550	0.888164	–0.282399	2050	0.312959	–0.802878
650	0.850012	–0.305457	2150	0.322646	–0.803970
750	0.760189	–0.358884	2250	0.288881	–0.807055
850	0.767363	–0.541032	2350	0.199294	–0.758619
950	0.779511	–0.585687	2450	0.206914	–0.725029
1050	0.761034	–0.482539	2550	0.168344	–0.770837
1150	0.624825	–0.530106	2650	0.092764	–0.776619
1250	0.635364	–0.590526	2750	0.036125	–0.706197
1350	0.630242	–0.592498	2850	0.037007	–0.716939
1450	0.634506	–0.655932	2950	–0.053842	–0.736527

02774-025

Figure 25. S Parameter Data for the RF Input

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 26. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

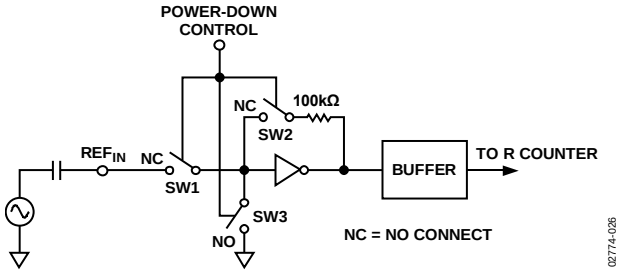

Figure 26. Reference Input Stage

RF/IF INPUT STAGE

The RF/IF input stage is shown in Figure 27. It is followed by a two-stage limiting amplifier to generate the current mode logic (CML) clock levels needed for the prescaler.

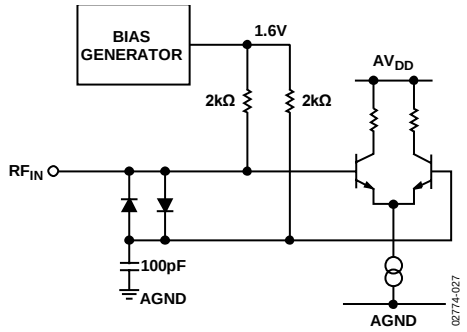

Figure 27. RF/IF Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = PB + A). The dual modulus prescaler, operating at CML levels, takes the clock from the RF/IF input stage and divides it down to a manageable frequency for the A and B CMOS counters in the RF and IF sections. The prescaler in both sections is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65 (see Table 9 and Table 10). It is based on a synchronous 4/5 core.

RF/IF A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 188 MHz or less. Thus, with an RF input frequency of 2.5 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

PULSE SWALLOW FUNCTION

The A and B CMOS counters, in conjunction with the dual modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).

P is the preset modulus of the dual modulus prescaler (8/9, 16/17, and so on).

B is the preset divide ratio of the binary 12-bit counter (3 to 4095).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference oscillator frequency.

R is the preset divide ratio of the binary 15-bit programmable reference counter (1 to 32,767).

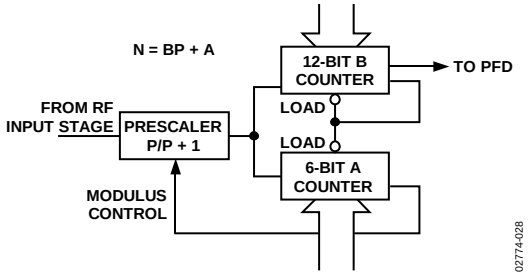

Figure 28. RF/IF A and B Counters

RF/IF R COUNTER

The 15-bit RF/IF R counter allows the input reference frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 29 is a simplified schematic. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

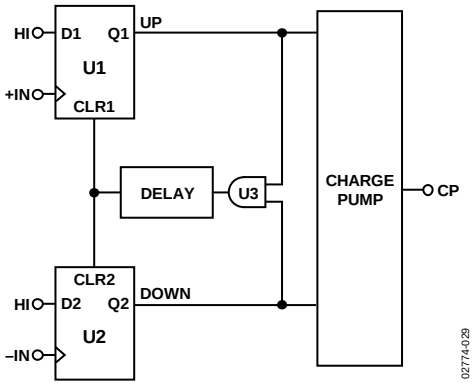

Figure 29. RF/IF PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4212L allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11, and P12 (see Table 8 and Table 10). Figure 30 shows the MUXOUT section in block diagram form.

LOCK DETECT

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect. Digital lock detect is active high. It is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, it is high with narrow, low-going pulses.

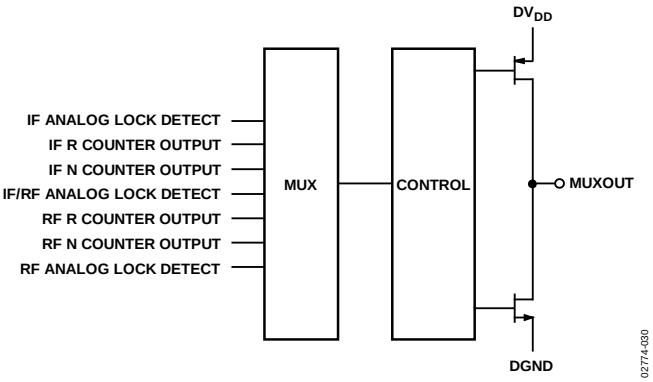

Figure 30. MUXOUT Schematic

RF/IF INPUT SHIFT REGISTER

The ADF4212L digital section includes a 24-bit input shift register, a 15-bit IF R counter, and an 18-bit IF N counter (comprising a 6-bit IF A counter and a 12-bit IF B counter). Also present is a 15-bit RF R counter and an 18-bit RF N counter (comprising a 6-bit RF A counter and a 12-bit RF B counter). Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 6.

Table 7 shows a summary of how the latches are programmed.

Table 6. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	IF R counter
0	1	IF N counter (A and B)
1	0	RF R counter
1	1	RF N counter (A and B)

Table 7. Latch Summary

IF R COUNTER LATCH

IF CP CURRENT SETTING			IF F_O	LOCK DETECT PRECISION	THREE-STATE CP	IF PD POLARITY	15-BIT REFERENCE COUNTER										CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IFCP2	IFCP1	IFCP0	P4	P3	P2	P1	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF N COUNTER LATCH

IF CP GAIN	IF POWER-DOWN	IF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P8	P7	P6	P5	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF R COUNTER LATCH

RF CP CURRENT SETTING			RF F_O	RF LOCK DETECT	THREE-STATE CP	RF PD POLARITY	15-BIT RF REFERENCE COUNTER										CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RFCP2	RFCP1	RFCP0	P12	P11	P10	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF N COUNTER LATCH

RF C GAIN	RF POWER-DOWN	RF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P17	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

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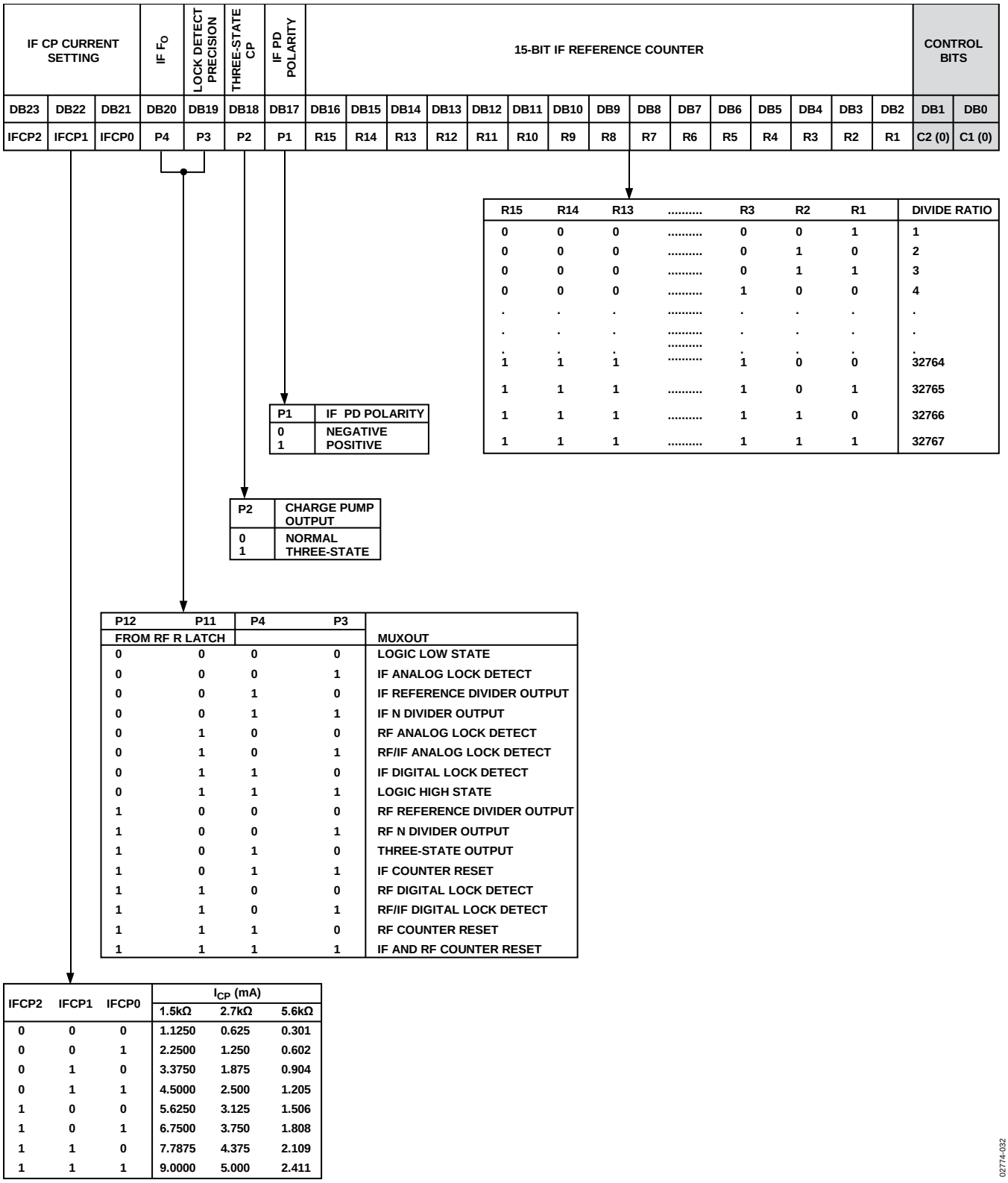
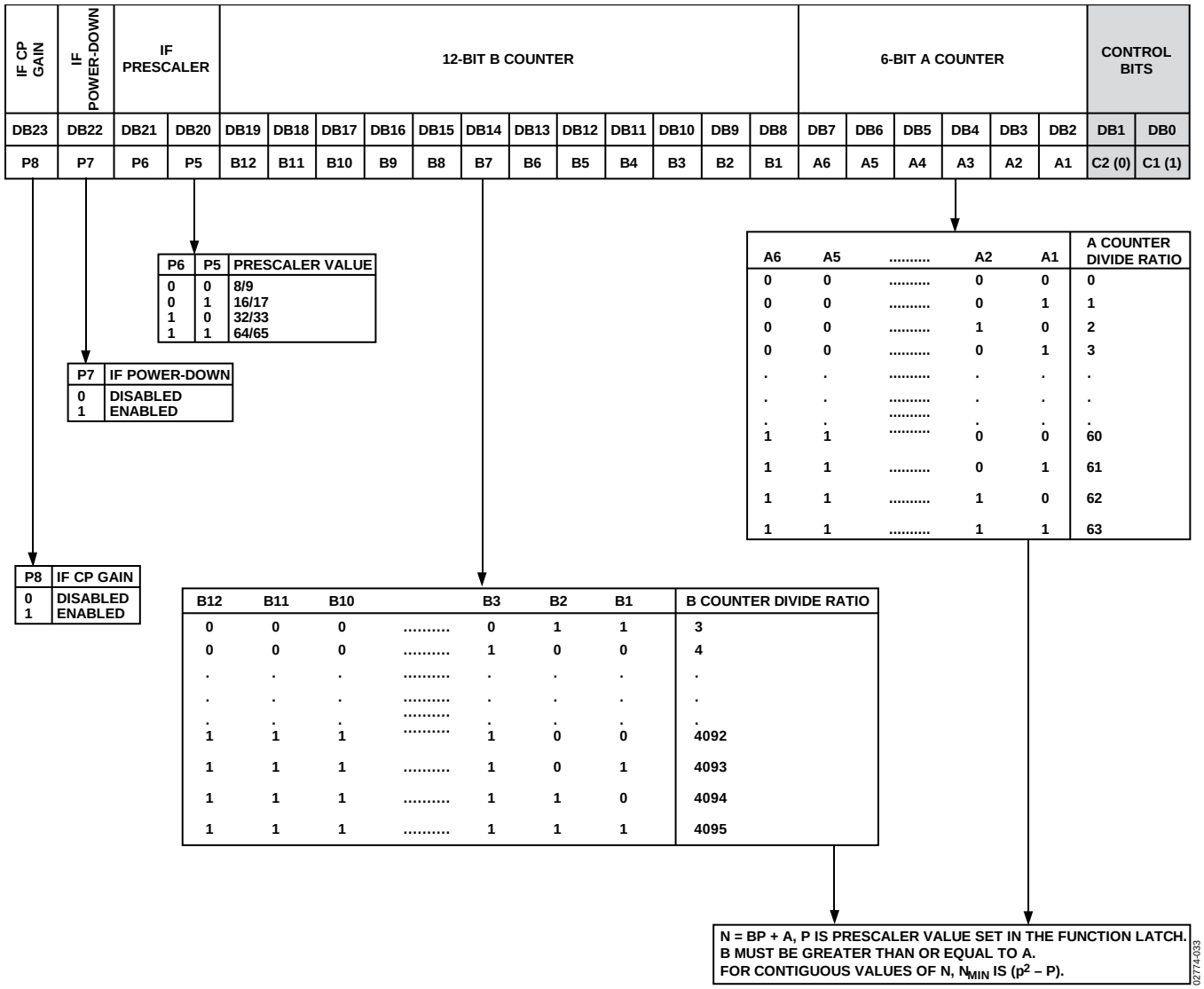
IF R COUNTER LATCH

Table 8. IF R Counter Latch Map



IF N COUNTER LATCH

Table 9. IF N Counter Latch Map



RF R COUNTER LATCH

Table 10. RF R Counter Latch Map

RF CP CURRENT SETTING			RF F_O	RF LOCK DETECT	THREE-STATE CP	RF PD POLARITY	15-BIT RF REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RFCP2	RFCP1	RFCP0	P12	P11	P10	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R15	R14	R13	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	32764
1	1	1	.....	1	0	1	32765
1	1	1	.....	1	1	0	32766
1	1	1	.....	1	1	1	32767

P9	RF PD POLARITY
0	NEGATIVE
1	POSITIVE

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	P4	P3	MUXOUT
		FROM IF R LATCH		
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	0	1	0	IF REFERENCE DIVIDER OUTPUT
0	0	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
0	1	1	0	IF DIGITAL LOCK DETECT
0	1	1	1	LOGIC HIGH STATE
1	0	0	0	RF REFERENCE DIVIDER OUTPUT
1	0	0	1	RF N DIVIDER OUTPUT
1	0	1	0	THREE-STATE OUTPUT
1	0	1	1	IF COUNTER RESET
1	1	0	0	RF DIGITAL LOCK DETECT
1	1	0	1	RF/IF DIGITAL LOCK DETECT
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

RFCP2	RFCP1	RFCP0	I_{CP} (mA)		
			1.5kΩ	2.7kΩ	5.6kΩ
0	0	0	1.1250	0.625	0.301
0	0	1	2.2500	1.250	0.602
0	1	0	3.3750	1.875	0.904
0	1	1	4.5000	2.500	1.205
1	0	0	5.6250	3.125	1.506
1	0	1	6.7500	3.750	1.808
1	1	0	7.7875	4.375	2.109
1	1	1	9.0000	5.000	2.411

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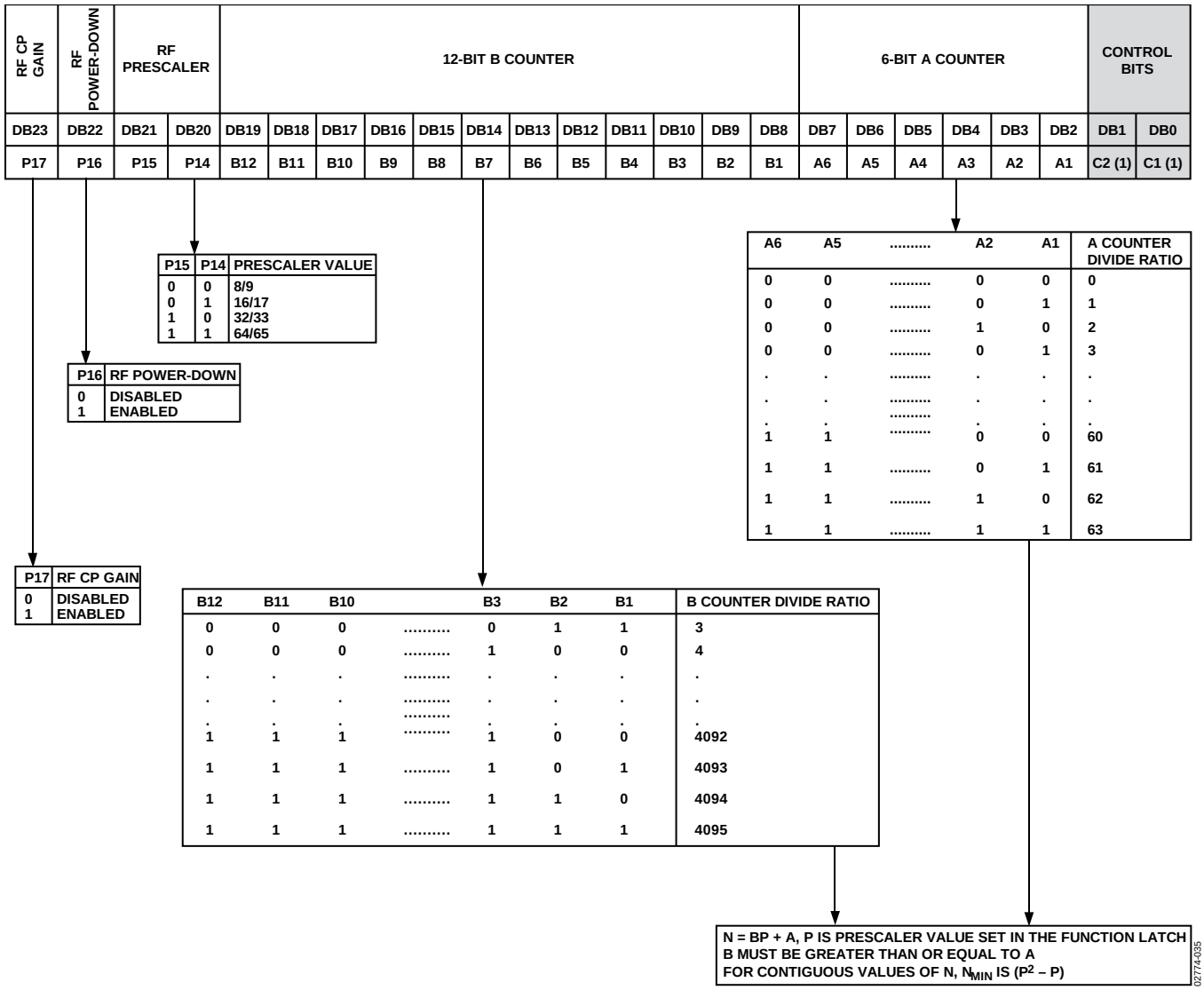
RF N COUNTER LATCH

Table 11. RF N Counter Latch Map



PROGRAM MODES

Table 8 and Table 10 show how to set up the program modes in the ADF4212L. The following should be noted:

- IF and RF analog lock detect indicate when the PLL is in lock. When the loop is locked and either IF or RF analog lock detect is selected, the MUXOUT pin shows a logic high with narrow, low-going pulses. When the IF/RF analog lock detect is chosen, the locked condition is indicated only when both IF and RF loops are locked.
- The IF counter reset mode resets the R, A, and B counters in the IF section and puts the IF charge pump into three-state mode. The RF counter reset mode resets the R, A, and B counters in the RF section and puts the RF charge pump into three-state. The IF and RF counter reset mode does both of the above. Upon removal of the reset bits, the A and B counters resume counting in close alignment with the R counter. (Maximum error is one prescaler output cycle.)
- The fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during fastlock operation. Activation of fastlock occurs whenever RF CP gain in the RF reference counter is set to 1.

IF AND RF POWER-DOWN

It is possible to program the ADF4210 family for either synchronous or asynchronous power-down on either the IF or RF side.

Synchronous IF Power-Down

Programming a 1 to P7 of the ADF4212L initiates a power-down. If P2 of the ADF4212L has been set to 0 (normal operation), a synchronous power-down is conducted. The device automatically puts the charge pump into three-state mode and completes the power-down.

Asynchronous IF Power-Down

If P2 of the ADF4212L has been set to 1 (the IF charge pump in three-state mode) and P7 is subsequently set to 1, an asynchronous power-down is conducted. The device goes into power-down on the rising edge of LE, which latches the 1 to the IF power-down bit (P7).

Synchronous RF Power-Down

Programming a 1 to P16 of the ADF4212L initiates a power-down. If P10 of the ADF4212L has been set to 0 (normal operation), a synchronous power-down is conducted. The device automatically puts the charge pump into three-state mode and then completes the power-down.

Asynchronous RF Power-Down

If P10 of the ADF4212L has been set to 1 (the RF charge pump in three-state mode) and P16 is subsequently set to 1, an asynchronous power-down is conducted. The device goes into power-down on the rising edge of LE, which latches the 1 to the RF power-down bit (P16).

Activation of either synchronous or asynchronous power-down forces the IF/RF loop's R and A/B dividers to their load state conditions, and the IF/RF input section is debiased to a high impedance state.

The REF_{IN} oscillator circuit is disabled only if both the IF and RF power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all power-down modes.

The IF/RF section of the device returns to normal powered-up operation immediately upon LE latching a 0 to the appropriate power-down bit.

IF SECTION

Programmable IF Reference (R) Counter

If Control Bits[C2:C1] = 00, the data is transferred from the input shift register to the 15-bit IF R counter. Table 8 shows the input shift register data format for the IF R counter and the divide ratios that are possible.

IF Phase Detector Polarity

P1 sets the IF phase detector polarity. When the IF VCO characteristics are positive, P1 should be set to 1. When the IF VCO characteristics are negative, it should be set to 0. See Table 8.

IF Charge Pump Three-State

P2 puts the IF charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation. See Table 8.

IF Program Modes

Table 8 shows how to set up the program modes in the ADF4212L.

IF Charge Pump Currents

IFCP2, IFCP1, and IFCP0 program the current setting for the IF charge pump. See Table 8.

Programmable IF N Counter

If Control Bits[C2:C1] = 01, the data in the input register is used to program the IF N (A + B) counter. The N counter consists of a 6-bit swallow counter (A counter) and 12-bit programmable counter (B counter). Table 9 shows the input register data format for programming the IF A and B counters and the divide ratios possible.

IF Prescaler Value

P5 and P6 in the IF N counter latch set the IF prescaler values. See Table 9.

IF Power-Down

Table 9 shows the power-down bits in the ADF4212L.

IF Fastlock

The IF CP gain bit (P8) of the IF N counter latch register in the ADF4212L is the fastlock enable bit. Only when P8 is set to 1 is IF fastlock enabled. When fastlock is enabled, the IF CP current is set to the maximum value. Also, an extra loop filter damping resistor to ground is switched in using the FL_O pin, thus compensating for the change in loop characteristics while in fastlock. Because the IF CP gain bit is contained in the IF N counter, only one write is needed to both program a new output frequency and initiate fastlock. To come out of fastlock, the IF CP gain bit on the IF N counter latch register must be set to 0 (see Table 9).

RF SECTION

Programmable RF Reference (R) Counter

If Control Bits[C2: C1] = 10, the data is transferred from the input shift register to the 15-bit RF R counter. Table 10 shows the input shift register data format for the RF R counter and the divide ratios possible.

RF Phase Detector Polarity

P9 sets the IF phase detector polarity. When the RF VCO characteristics are positive, P9 should be set to 1. When they are negative, it should be set to 0 (see Table 10).

RF Charge Pump Three-State

P10 puts the RF charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation (see Table 10).

RF Program Modes

Table 10 shows how to set up the program modes in the ADF4212L.

RF Charge Pump Currents

RFCP2, RFCP1, and RFCP0 program the current setting for the RF charge pump. See Table 10.

Programmable RF N Counter

If Control Bits[C2:C1] = 11, the data in the input register is used to program the RF N (A + B) counter. The N counter consists of a 6-bit swallow counter (A counter) and a 12-bit programmable counter (B counter). Table 11 shows the input register data format for programming the RF N counter and the divide ratios that are possible.

RF Prescaler Value

P14 and P15 in the RF N counter latch set the RF prescaler values. See Table 11.

RF Power-Down

Table 11 shows the power-down bits in the ADF4212L.

RF Fastlock

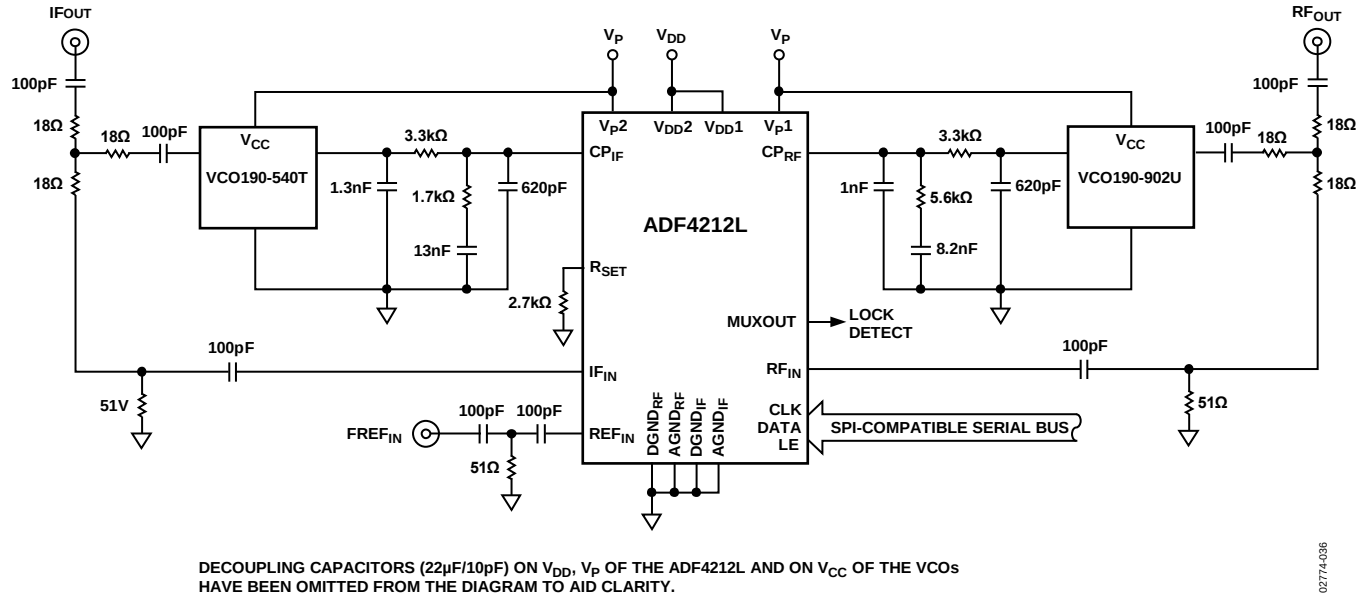
The RF CP gain bit (P17) of the RF N counter latch register in the ADF4212L is the fastlock enable bit. Only when P17 is set to 1 is IF fastlock enabled. When fastlock is enabled, the RF CP current is set to the maximum value. Also, an extra loop filter damping resistor to ground is switched in using the FL_O pin, thus compensating for the change in loop characteristics while in fastlock. Because the RF CP gain bit is contained in the RF N counter, only one write is needed to both program a new output frequency and initiate fastlock. To come out of fastlock, the RF CP gain bit on the RF N counter latch register must be set to 0. See Table 11.

APPLICATIONS INFORMATION

LOCAL OSCILLATOR FOR GSM HANDSET RECEIVER

Figure 31 shows the ADF4212L being used with a VCO to produce the required LOs for a GSM base station transmitter or receiver. The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. Typical GSM systems have a 13 MHz TCXO driving the reference input without any 50 Ω termination. To have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference.

The RF output frequency range is 880 MHz to 915 MHz. The loop filter is designed to give a 20 kHz loop bandwidth. The filter is set up for a 5 mA charge pump current, and the VCO sensitivity is 12 MHz/V. The IF output is fixed at 540 MHz. The filter is again designed to have a bandwidth of 20 kHz, and the system is programmed to give channel steps of 200 kHz.



DECOUPLING CAPACITORS (22µF/10pF) ON V_{DD}, V_P OF THE ADF4212L AND ON V_{CC} OF THE VCOs HAVE BEEN OMITTED FROM THE DIAGRAM TO AID CLARITY.

Figure 31. GSM Handset Receiver Local Oscillator Using the ADF4212L

WIDEBAND PLL

Many of the wireless applications for synthesizers and VCOs in PLLs are narrow band in nature. These applications include the various wireless standards such as GSM, DSC1800, CDMA, or WCDMA. In each of these cases, the total tuning range for the LO is less than 100 MHz. However, there are also wideband applications where the LO can have up to an octave tuning range. For example, cable television tuners have a total range of about 400 MHz. Figure 32 shows an application where the ADF4212L is used to control and program the Micronetics M3500-1324. The loop filter was designed for an RF output of 2100 MHz, a loop bandwidth of 40 kHz, a PFD frequency of 1 MHz, I_{CP} of 10 mA (2.5 mA synthesizer I_{CP} multiplied by the gain factor of 4), VCO K_D of 80 MHz/V (sensitivity of the M3500-1324 at an output of 2100 MHz), and a phase margin of 45 degrees.

In narrow-band applications, there is generally a small variation in output frequency (generally less than 10%) and a small variation in VCO sensitivity over the range (typically <10%). However, in wideband applications, both of these parameters have a much greater variation, which changes the loop bandwidth. This, in turn, can affect stability and lock time. By changing the programmable I_{CP}, it is possible to obtain compensation for these varying loop conditions and to ensure that the loop is always operating close to optimal conditions.

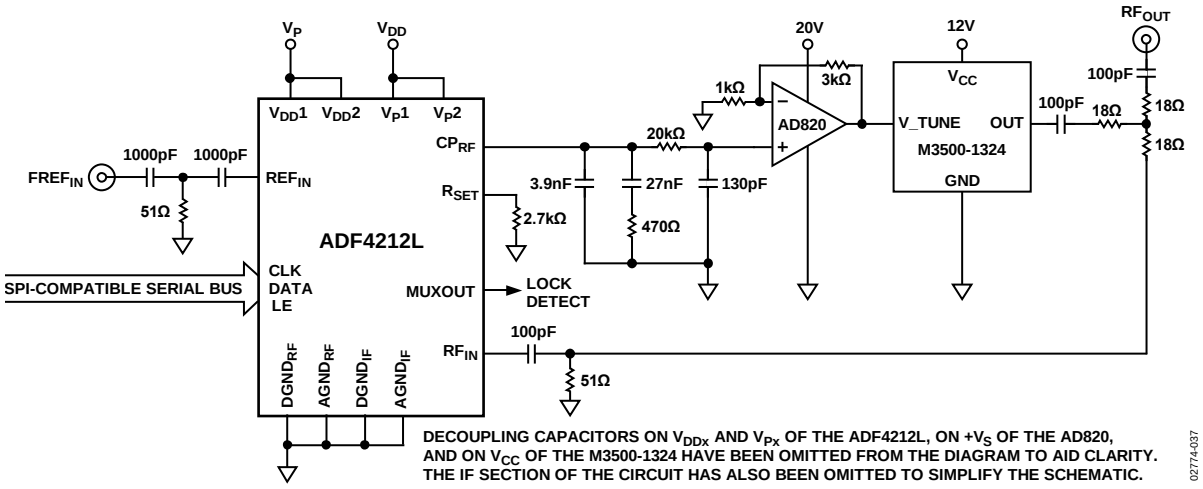


Figure 32. Wideband PLL Circuit

INTERFACING

The ADF4212L has a simple SPI-compatible interface for writing to the device. CLK, DATA, and LE control the data transfer. When latch enable (LE) goes high, the 22 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 µs, which is more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 33 shows the interface between the ADF4212L and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI (serial port interface) master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4212L needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

When first applying power to the ADF4212L, four writes (one each to the R counter latch and the N counter latch for both the IF and RF sides) are required for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 180 kHz.

ADSP-2181 Interface

Figure 34 shows the interface between the ADF4212L and the ADSP-21xx digital signal processor. As previously described, the ADF4212L needs a 24-bit serial word for each latch write. The easiest way to accomplish this with the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

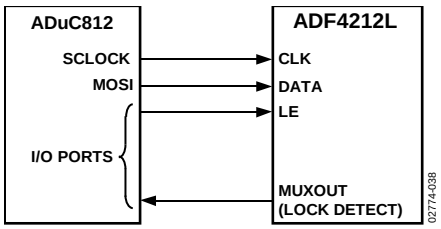


Figure 33. ADuC812 to ADF4212L Interface

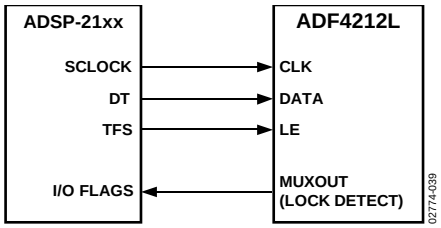


Figure 34. ADSP-21xx to ADF4212L Interface

PCB DESIGN GUIDELINES FOR LEAD FRAME CHIP SCALE PACKAGE

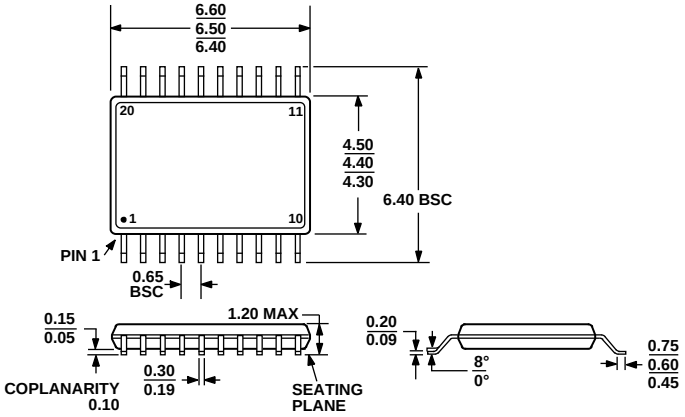
The lands on the LFCSP (CP-20-6) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

The thermal pad on the PCB should be at least as large as the exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz copper to plug the via.

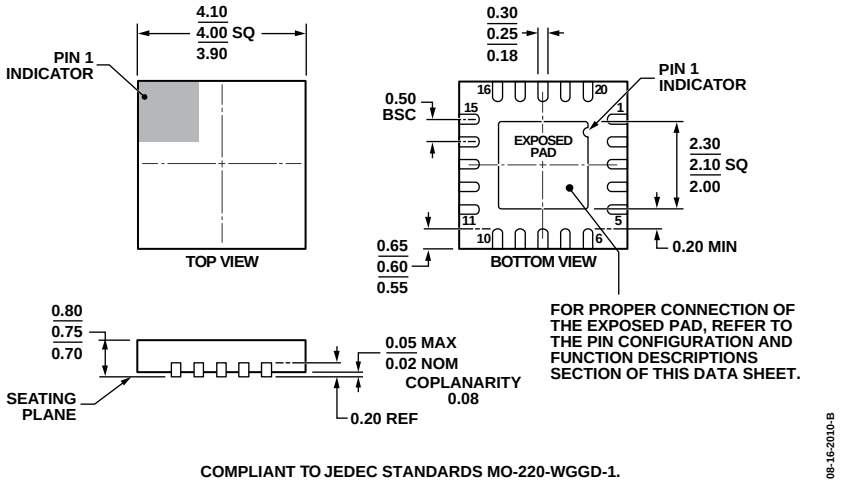
The user should connect the PCB thermal pad to PCB ground.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 35. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 36. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADF4212LBRUZ	−40°C to +85°C	20-Lead TSSOP	RU-20
ADF4212LBRUZ-RL	−40°C to +85°C	20-Lead TSSOP	RU-20
ADF4212LBRUZ-RL7	−40°C to +85°C	20-Lead TSSOP	RU-20
ADF4212LBCPZ	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6
ADF4212LBCPZ-RL	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6
ADF4212LBCPZ-RL7	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6

[1] Z = RoHS Compliant Part.
[2] CP-20-6 package was formerly CP-20-1 package.

NOTES

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