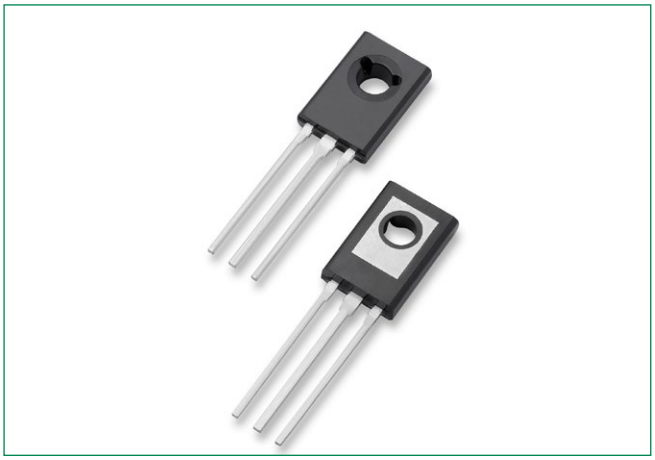
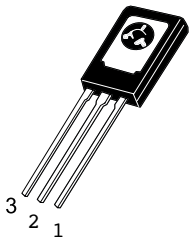
2N6071A/B Series



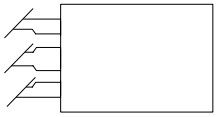
Pin Out



REAR VIEW
SHOW TAB

TO-225
CASE 077
STYLE 5

1. Cathode
2. Anode
3. Gate



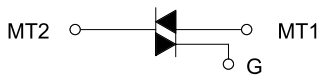
Description

Designed primarily for full-wave AC control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

Features

- Sensitive Gate Triggering Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering: 4 Mode - 2N6071A, B; 2N6073A, B; 2N6075A, B
- Blocking Voltages to 600 V
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Device Marking: Device Type, e.g., 2N6071A, Date Code

Functional Diagram



Additional Information

Datasheet | Resources | Samples

Revised: 06/05/19

Maximum Ratings and Thermal Characteristics (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (Note 1) (T_J = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N6071A,B 2N6073A,B 2N6075A,B	V_{DRM}, V_{RRM}	200 400 600	-
*On-State RMS Current (T_C = 85°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	4.0	A
*Peak Non-repetitive Surge Current (One Full cycle, 60 Hz, T_J = +110°C)	I_{TSM}	30	A
Circuit Fusing Considerations (t = 8.3 ms)	I_{2t}	3.7	A2s
*Peak Gate Power (Pulse Width "1.0 µs, T_C = 85°C)	P_{GM}	10	W
*Average Gate Power (t = 8.3 ms, T_C = 85°C)	$P_{G(AV)}$	0.5	W
*Peak Gate Voltage (Pulse Width "1.0 µs, T_C = 85°C)	V_{GM}	5.0	V
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw) (Note 2)	_	8.0	in. lb.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
2. Torque rating applies with use of a compression washer. Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

Thermal Characteristics

Rating	Symbol	Value	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

*Indicates JEDEC Registered Data.

Electrical Characteristics - OFF (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Repetitive Blocking Current TJ = 25°C (VD = VDRM = VRRM; Gate Open) TJ = 110°C	TJ = 25°C	IDRM, IRRM	-	-	10	µA
	TJ = 110°C		-	-	2	mA

Electrical Characteristics - ON (TC = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak On-State Voltage (Note 3) (I_{TM} = ±6.0 A Peak)		C	-	-	2	V
*Gate Trigger Voltage (Continuous DC), All Quadrants (Main Terminal Voltage = 12 Vdc, R_L = 100 Ω, T_J = -40 °C)		VGT	-	1.4	2.5	V
Gate Non-Trigger Voltage, All Quadrants (Main Terminal Voltage = 12 Vdc, RL = 100 Ω, TJ = 110°C)		VGD	.02	-	-	V
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = ±1 Adc)	T_J = -40°C	IH	-	-	30	mA
	T_J = 25°C		-	-	15	
Turn-On Time (I_{TM} = 14 Adc, I_{GT} = 100 mAdc)		tgt	-	1.5	-	µs

			QUADRANT (Maximum Value)			
Gate Trigger Current (Continuous DC) (Main Terminal Voltage = 12 Vdc, RL = 100 Ω)	Type	IGT @ TJ	I mA	II mA	III mA	IV mA
	2N6071A 2N6073A 2N6075A	+25°C	5	5	5	10
		-40°C	20	20	20	30
	2N6071B 2N6073B 2N6075B	+25°C	3	3	3	5
		-40°C	15	15	15	20

3. Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

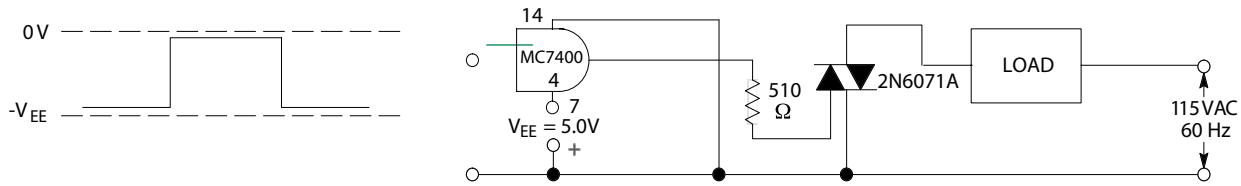
*Indicates JEDEC Registered Data.

Revised: 06/05/19

Dynamic Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Commutation Voltage @ V_{DRM}, T_J = 85°C, Gate Open, I_{TM} = 5.7 A, Exponential Waveform, Commutating di/dt = 2.0 A/ms	dv/dt(c)	-	5	10	V/µs

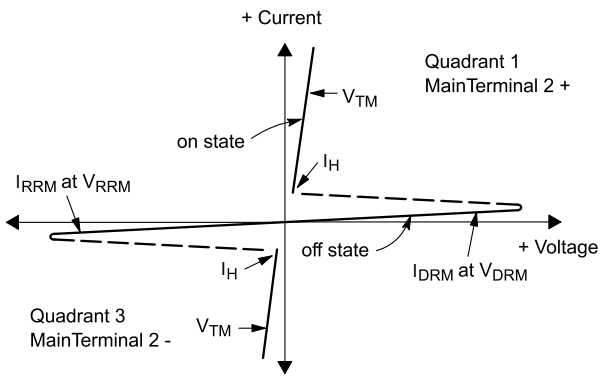
SAMPLE APPLICATION: TTL-Sensitive Gate 4 Ampere Triac Triggers in Modes II and III



Trigger devices are recommended for gating on Triacs. They provide:
1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current

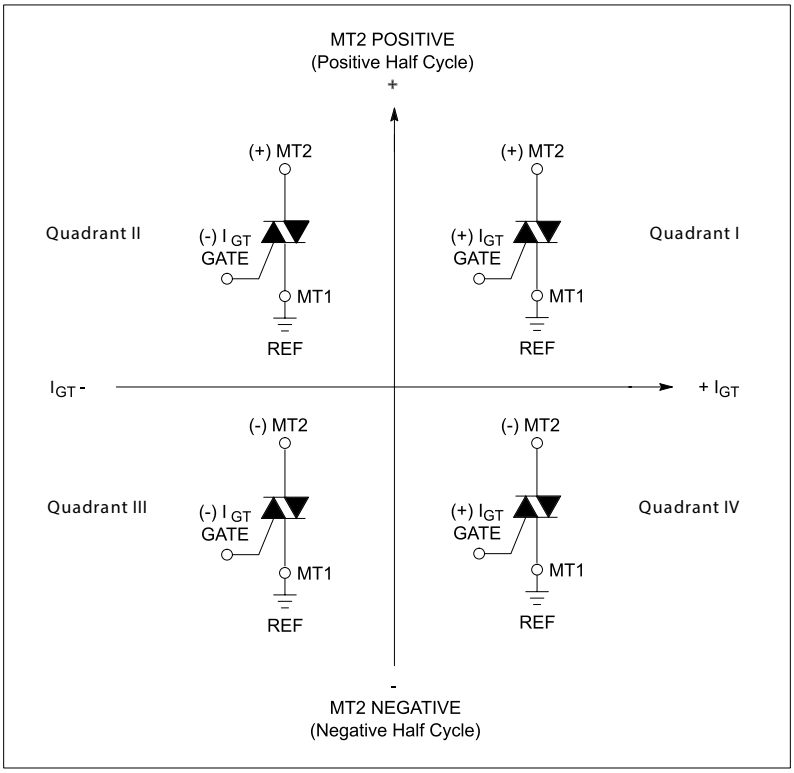


Sensitive Gate Logic Reference

IC Logic Functions	Firing Quadrant			
	I	II	III	IV
TTL	_	2N6071A Series	2N6071A Series	_
HTL	_	2N6071A Series	2N6071A Series	_
CMOS (NAND)	2N6071B Series	_	_	2N6071B Series
CMOS (Buffer)	_	2N6071B Series	2N6071B Series	_
Operational Amplifier	2N6071A Series	_	_	2N6071A Series
Zero Voltage Switch	_	2N6071A Series	2N6071A Series	_

Revised: 06/05/19

Quadrant Definitions for a Triac



Ratings and Characteristic Curves

Figure 1. Average Current Derating

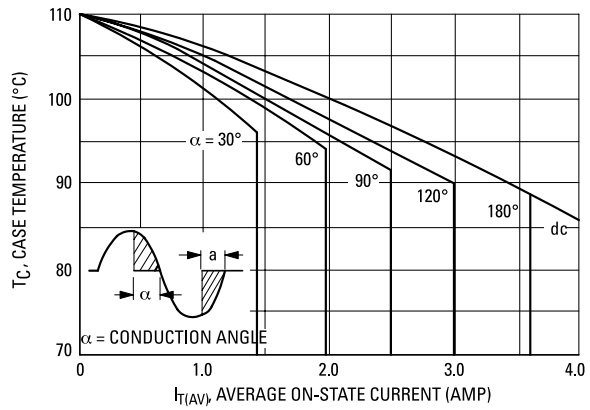


Figure 2. RMS Current Derating

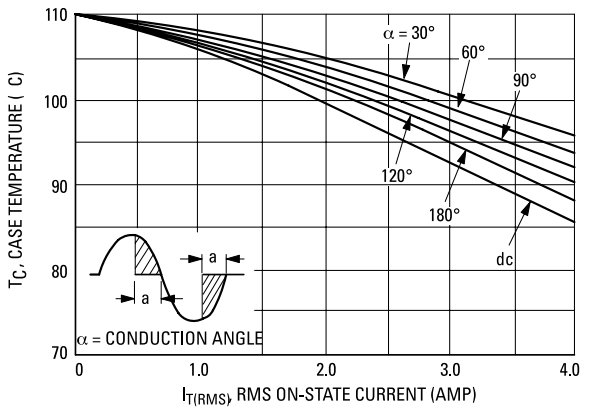


Figure 3. Power Dissipation

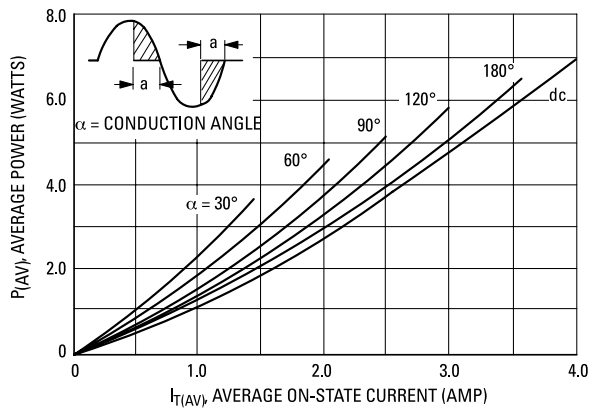


Figure 4. Power Dissipation

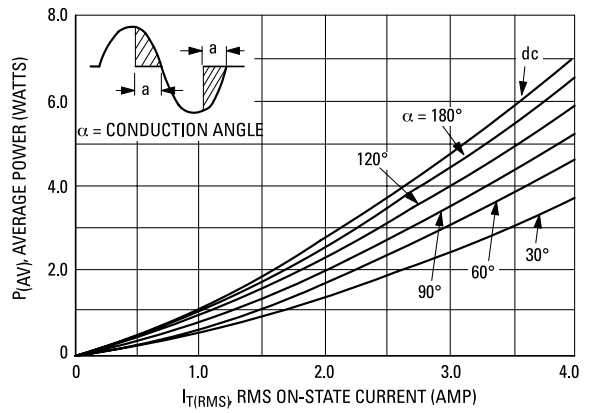


Figure 5. Typical Gate-Trigger Voltage

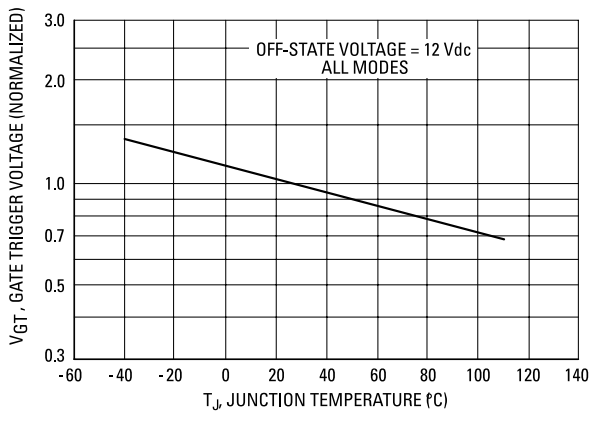


Figure 6. Typical Gate-Trigger Current

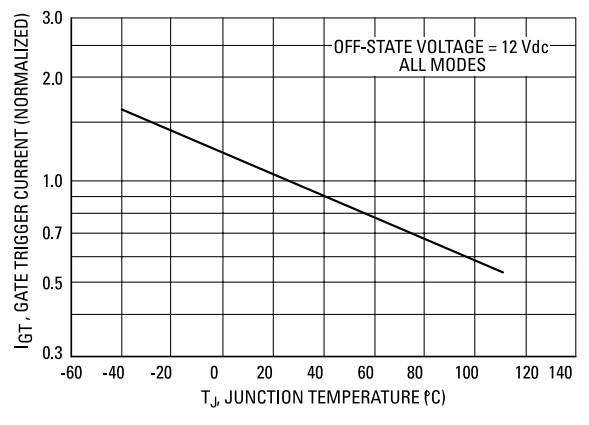


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Figure 7. Maximum On-State Characteristics

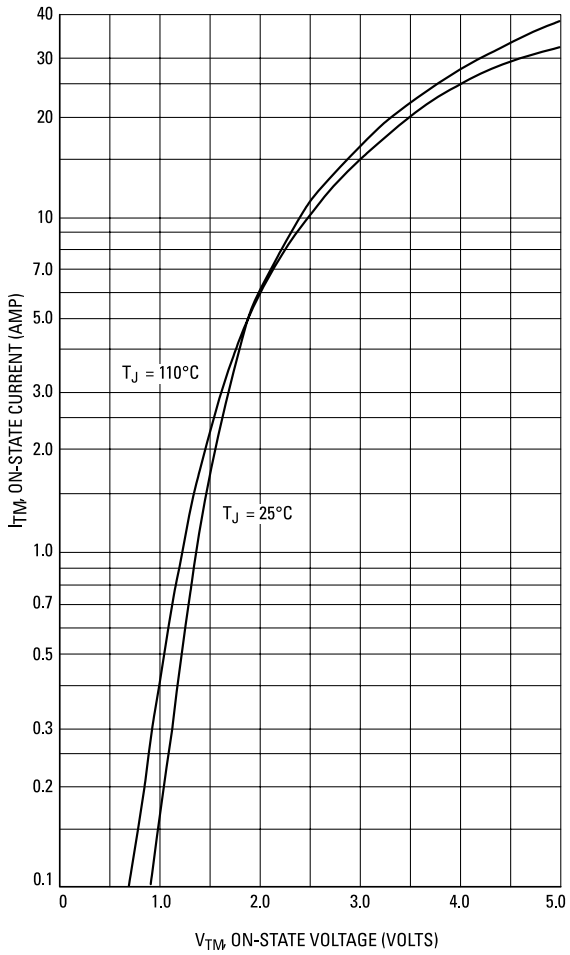


Figure 8. Typical Holding Current

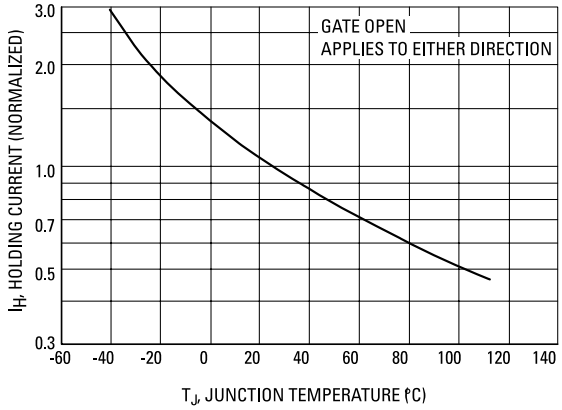


Figure 9. Maximum Allowable Surge Current

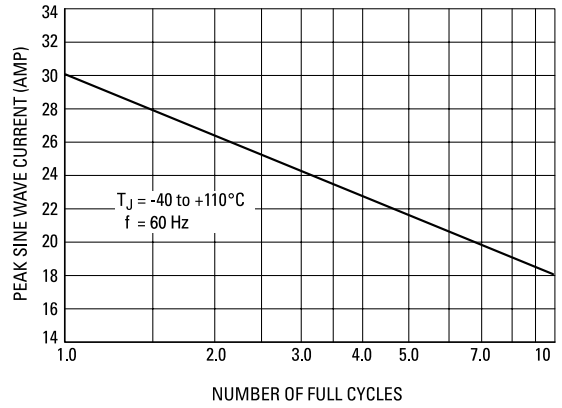
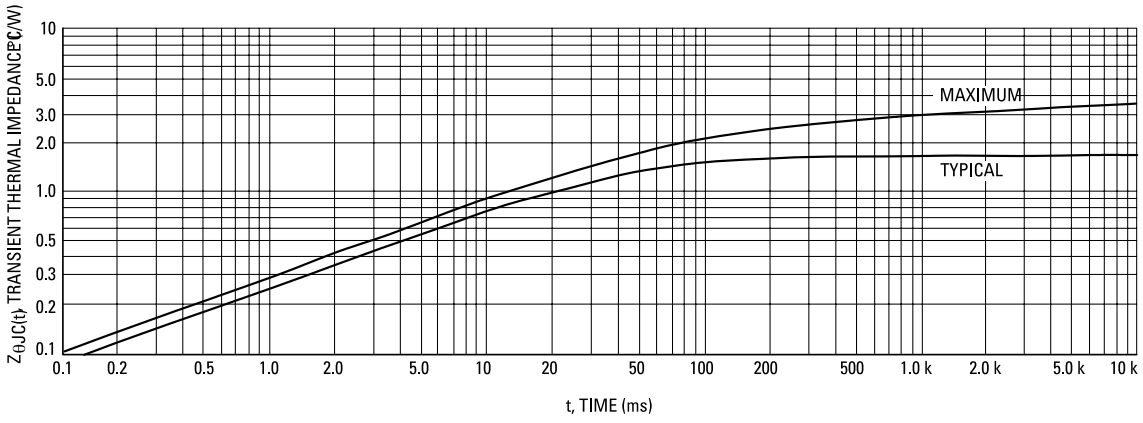


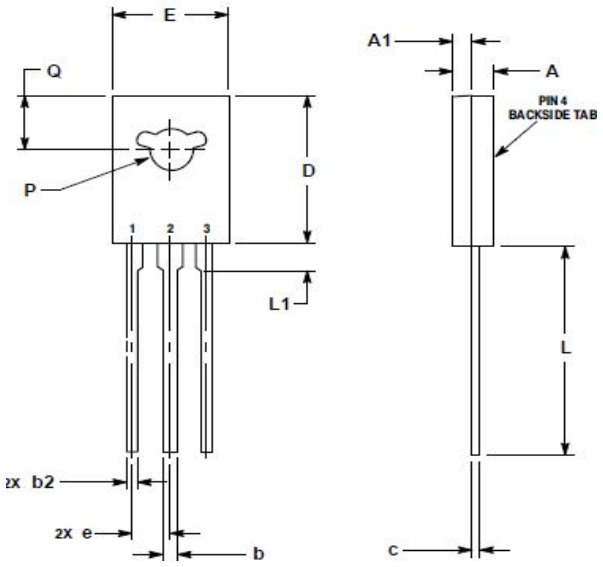
Figure 10. Thermal Response



Revised: 06/05/19

Thyristors
Surface Mount – 200V-600W > 2N6071A/B Series

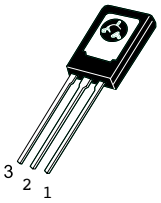
Dimensions



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.102	0.110	2.60	2.80
A1	0.047	0.055	1.20	1.40
b	0.028	0.034	0.70	0.86
b2	0.028	0.034	0.70	0.86
c	0.019	0.022	0.49	0.57
D	0.417	0.449	10.60	11.40
E	0.291	0.323	7.40	8.20
e	0.090 TYP		2.29 TYP	
L	0.551	0.630	14.00	16.00
L1	0.091	0.106	2.30	2.70
P	0.118	0.134	3.00	3.40
Q	0.142	0.157	3.60	4.00

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077-01 THRU -08 OBSOLETE, NEW STANDARD 077-09.

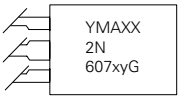
Part Marking System



REAR VIEW
SHOW TAB

1. Cathode
2. Anode
3. Gate

TO-225
CASE 077
STYLE 5



x =1,3,5
y =A,B
Y =Year
M =Month
A =Assembly Site
XX =Lot Serial Code

Ordering Information

Device	Package	Shipping†
2N6071A	TO-225	2500 Units / Box
2N6071AG	TO-225 (Pb-Free)	
2N6071AT	TO-225	50 Units / Tube 1920 Units / Box
2N6071ATG	TO-225 (Pb-Free)	
2N6071B	TO-225	2500 Units / Box
2N6071BG	TO-225 (Pb-Free)	
2N6071BT	TO-225	50 Units / Tube 1920 Units / Box
2N6071BTG	TO-225 (Pb-Free)	
2N6073A	TO-225	2500 Units / Box
2N6073AG	TO-225 (Pb-Free)	
2N6073B	TO-225	
2N6073BG	TO-225 (Pb-Free)	
2N6075A	TO-225	
2N6075AG	TO-225 (Pb-Free)	
2N6075B	TO-225	
2N6075BG	TO-225 (Pb-Free)	

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