Very Low Noise Single-Ended SAR ADC Driver with True Zero Output

FEATURES

- **Output Swings to True Zero on Single Supply**
- **2.3nV/√Hz Noise Density**
- **Fast Settling Time: 150ns, 16-Bit, 4V Step**
- 110dB SNR in 3MHz Bandwidth
- Low Distortion, HD_2 = –103dBc and HD_3 = –109dBc for $4V_{P-P}$ Output at 40kHz
- Low Offset Voltage: 250µV Max
- Low Power Shutdown: 350µA Max
- 3mm × 3mm 8-Pin DFN and 8-lead MSOP Packages

APPLICATIONS

- 16-Bit and 18-Bit SAR ADC Driver
- High Speed Buffer Amplifiers
- Low Noise Signal Processing

DESCRIPTION

The LTC®6360 is a very low noise, high precision, high speed amplifier suitable for driving SAR ADCs. The LTC6360 features a total output noise of 2.3nV/√Hz combined with 150ns settling time to 16-bit levels (A_V = 1).

While powered from a single 5V supply, the amplifier output can swing to 0V while maintaining high linearity. This is made possible with the inclusion of a very low noise on-chip charge pump that generates a negative voltage to bias the output stage of the amplifier, increasing the allowable negative voltage swing.

The LTC6360 is available in a compact 3mm × 3mm, 8-pin leadless DFN package and an 8-pin MSOP package with exposed pad and operates over a –40°C to 125°C temperature range.

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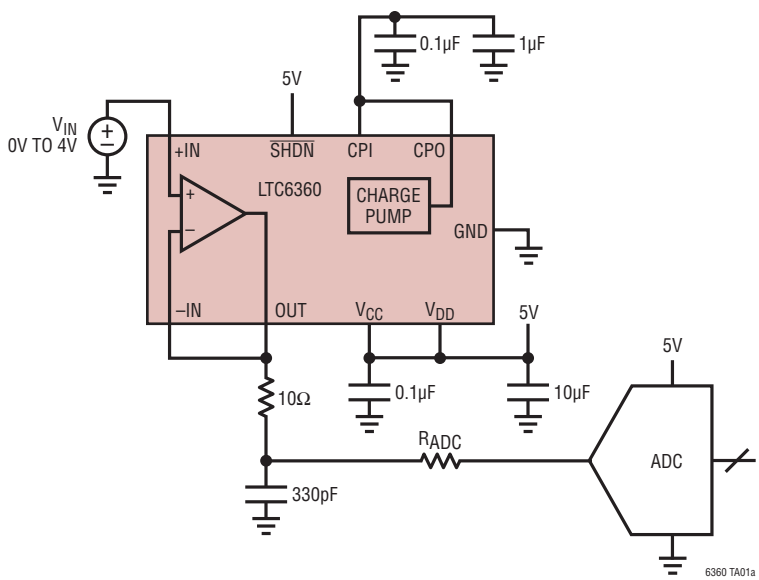
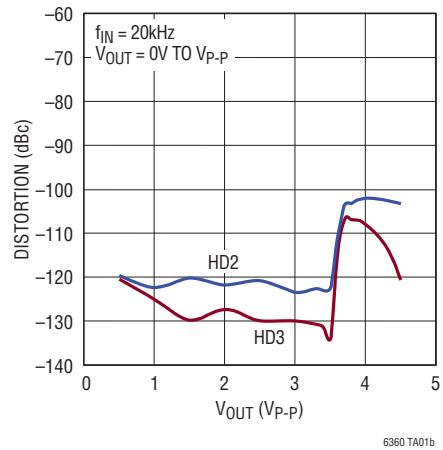
TYPICAL APPLICATION

ADC Driver



Harmonic Distortion vs Output Amplitude

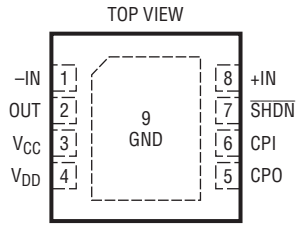


ABSOLUTE MAXIMUM RATINGS

(Note 1)

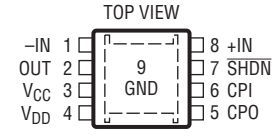
Total Supply Voltage
(V_{CC}/V_{DD} – GND) 5.5V
Input Current (Note 2) ..... ±10mA
Output Short Circuit Duration (Note 3) ..... Indefinite
Operating Ambient Temperature Range
(Note 4) ..... –40°C to 125°C
Specified Temperature Range (Note 5) .... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) MS8E Only ..... 300°C

PIN CONFIGURATION



DD-8 PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION TO GND



MS8E PACKAGE
8-LEAD PLASTIC MSOP WITH EXPOSED PAD

T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6360CDD#PBF	LTC6360CDD#TRPBF	LFQT	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6360IDD#PBF	LTC6360IDD#TRPBF	LFQT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6360HDD#PBF	LTC6360HDD#TRPBF	LFQT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6360CMS8E#PBF	LTC6360CMS8E#TRPBF	LTFQS	8-Lead Plastic MSOP	0°C to 70°C
LTC6360IMS8E#PBF	LTC6360IMS8E#TRPBF	LTFQS	8-Lead Plastic MSOP	–40°C to 85°C
LTC6360HMS8E#PBF	LTC6360HMS8E#TRPBF	LTFQS	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless noted otherwise, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, $V_{\overline{SHDN}}$ = 5V. See Figure 1 for circuit configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (MS8E)	V_{+IN} = 0V	 ●		30	250 600	µV µV
		V_{+IN} = 2V	 ●		30	250 600	µV µV
		V_{+IN} = 4.25V	 ●		40	300 700	µV µV
V_{OS}	Input Offset Voltage (DD8)	V_{+IN} = 0V	 ●		90	400 900	µV µV
		V_{+IN} = 2V	 ●		90	400 900	µV µV
		V_{+IN} = 4.25V	 ●		170	600 1200	µV µV
$V_{OS}/\Delta T$	Offset Voltage Drift		●		1.3		µV/°C
I_B	Input Bias Current (at +IN, –IN)	V_{+IN} = 0V	 ●	–30 –39	–17		µA µA
		V_{+IN} = 2V	 ●	–28 –36	–15		µA µA
		V_{+IN} = 4.25V	 ●	–26 –31	–13.5		µA µA
I_{OS}	Input Offset Current (at +IN, –IN)	V_{+IN} = 0V V_{+IN} = 2V V_{+IN} = 4.25V	● ● ●		0.1 0.1 0.1	1.0 1.0 1.0	µA µA µA
e_n	Input Voltage Noise Density	f = 1MHz			2.3		$nV/\sqrt{Hz}$
i_n	Input Current Noise Density	f = 1MHz			3		$pA/\sqrt{Hz}$
SNR	Signal to Noise Ratio	V_{OUT} = $4V_{P-P}$, 3MHz Noise Bandwidth			110		dB
V_{CMR}	Input Common Mode Voltage Range	Guaranteed by CMRR	●	0		4.25	V
R_{IN}	Input Resistance	Differential Mode Common Mode			8 940		kΩ kΩ
C_{IN}	Input Capacitance	+IN, –IN			2		pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = 0V to 4.5V	 ●	235 200	1000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{+IN} = $V_{–IN}$ = 0V to 3V	●	83	114		dB
		V_{+IN} = $V_{–IN}$ = 0V to 4.25V (MS8E)	●	78	111		dB
		V_{+IN} = $V_{–IN}$ = 0V to 4.25V (DD8)	●	75	96		dB
PSRR	Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OS}$)	V_{CC} = 4.75V to 5.25V			99		dB
V_S	Supply Voltage	V_{CC} = V_{DD}	●	4.75	5	5.25	V
INL	DC Linearity (Note 6)	V_{+IN} = 0V to 4.25V			40		µV
V_{OH}	Output Voltage High	No Load Sourcing 1mA	● ●	4.80 4.75	4.91 4.89		V V
V_{OL}	Output Voltage Low	No Load Sinking 1mA	● ●		–0.48 –0.47	–0.20 –0.15	V V
I_{SC}	Output Short Circuit Current	Sourcing, Output Shorted to GND, V_{+IN} – $V_{–IN}$ = 200mV	 ●	18 16	45		mA mA
		Sinking, Output Shorted to V_{CC}, V_{+IN} – $V_{–IN}$ = –200mV	 ●	4.1 3.2	5.8		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless noted otherwise, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, V_{SHDN} = 5V. See Figure 1 for circuit configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_L	$\overline{SHDN}$ Pin Input Voltage, Logic Low		●			0.8	V
V_H	$\overline{SHDN}$ Pin Input Voltage, Logic High		●	2.0			V
I_{SHDNH}	$\overline{SHDN}$ Pin Current, Logic High	$V_{\overline{SHDN}}$ = 5V	●			100	nA
I_{SHDNL}	$\overline{SHDN}$ Pin Current, Logic Low	$V_{\overline{SHDN}}$ = 0V	●	–15	–9.5		µA
I_{CC}	V_{CC} Supply Current	$V_{\overline{SHDN}}$ = 2.0V	 ●		6.6	8 9	mA mA
I_{DD}	V_{DD} Supply Current	$V_{\overline{SHDN}}$ = 2.0V	 ●		7.0	9.5 10	mA mA
I_{TOT}	Total Supply Current I_{CC} + I_{DD}	$V_{\overline{SHDN}}$ = 2.0V	 ●		13.6	17.5 19	mA mA
I_{CC}(SHDN)	V_{CC} Supply Current in Shutdown	$V_{\overline{SHDN}}$ = 0.8V	●		110	200	µA
I_{DD}(SHDN)	V_{DD} Supply Current in Shutdown	$V_{\overline{SHDN}}$ = 0.8V	●		80	150	µA
I_{TOT} (SHDN)	Total Supply Current I_{CC} + I_{DD} in Shutdown	$V_{\overline{SHDN}}$ = 0.8V	●		190	350	µA
GBW	Gain-Bandwidth Product	Noninverting, f = 1MHz			1		GHz
BW	Closed Loop –3dB Bandwidth	V_{OUT} = 50mV_{P-P}, A_V = 1		150	250		MHz
FPBW	Full Power Bandwidth (Note 7)	V_{OUT} = 0V to 4V			2.7		MHz
SR	Slew Rate	A_V = –1 Rising Falling			 135 95		 V/µs V/µs
HD2/HD3	Harmonic Distortion	V_{OUT} = 0V to 2V f_{IN} = 10kHz f_{IN} = 40kHz f_{IN} = 1MHz			 –121/–130 –121/–123 –96/–116		 dBc dBc dBc
HD2/HD3	Harmonic Distortion	V_{OUT} = 0V to 4V f_{IN} = 10kHz f_{IN} = 40kHz f_{IN} = 1MHz			 –101/–110 –103/–109 –87/–105		 dBc dBc dBc
t_S	Settling Time	4V Step 0.25% 0.025% 0.0015% (±1LSB, 16-Bit, Falling Edge)			 45 110 150		 ns ns ns
t_{OVDR}	Overdrive Recovery Time	V_{+IN} to GND and V_{CC}			30		ns
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0V to 5V			1		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 5V to 0V			0.3		µs
V_{CPO}	CPO Output Voltage		●	–0.8	–0.6	–0.3	V
$V_{CPORIPPLE}$	CPO Ripple Voltage	No External CPO/CPI Capacitors, 100MHz Measurement Bandwidth			1.5		mV_{RMS}
$V_{OUTRIPPLE}$	Output Ripple Voltage	No External CPO/CPI Capacitors, 50MHz Measurement Bandwidth			11.5		$µV_{RMS}$
f_{RIPPLE}	Ripple Frequency		 ●	9.5 9.25	10	10.5 10.75	MHz MHz
$I_{CPO(MAX)}$	Maximum Continuous CPO Output Current	V_{CPO} ≤ –0.4V (Note 8)		3.5	4.5		mA
R_{CPO}	CPO DC Output Impedance	I_{CPO} = 0 to 3.5mA (Note 8)	●		30	65	Ω

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by back-to-back diodes and diodes to each supply. If the inputs are taken beyond the supplies or the differential input voltage exceeds 0.7V, the input current must be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6360C/LTC6360I/LTC6360H are guaranteed functional over the temperature range –40°C to 125°C.

Note 5: The LTC6360C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6360C is designed, characterized and expected to meet specified performance from –40°C to 125°C, but are not tested or QA sampled at these temperatures. The LTC6360I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6360H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: DC linearity is calculated by measuring the output vs input voltage and calculating the maximum deviation from the least squares best fit line at 100mV increments.

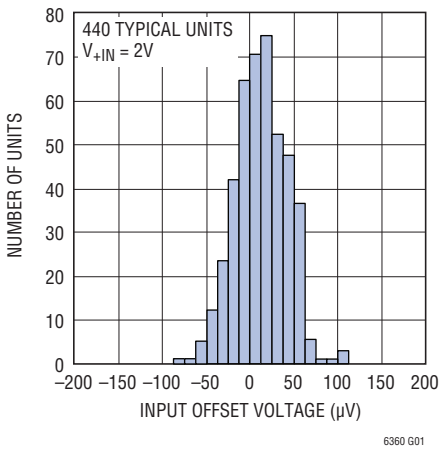
Note 7: FPBW is determined from distortion performance with HD2, HD3 < –70dBc as the criteria for a valid output. FPBW is limited by the charge pump current sinking capability. See text for details.

Note 8: $I_{CPO(MAX)}$ and R_{CPO} are measured with CPO disconnected from CPI and CPI driven by external –0.7V source.

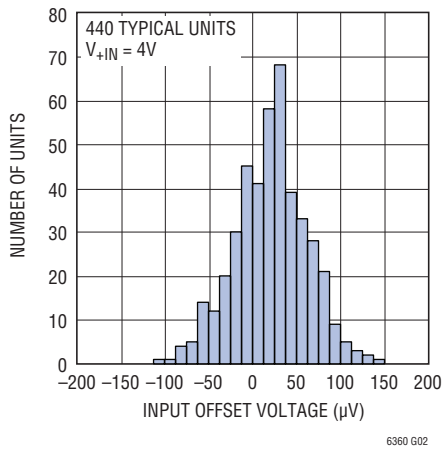
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, $V_{\overline{SHDN}}$ = 5V, see Figure 1 for circuit configuration.

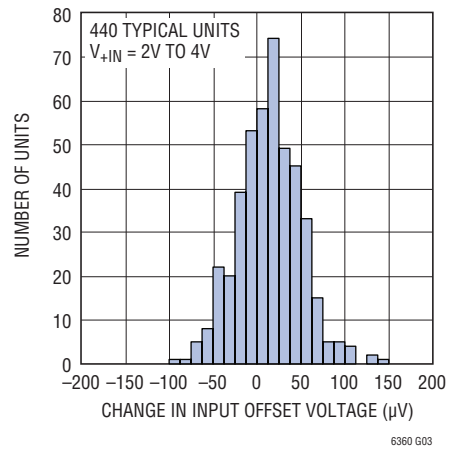
V_{OS} Distribution, MS8E (PNP Stage)



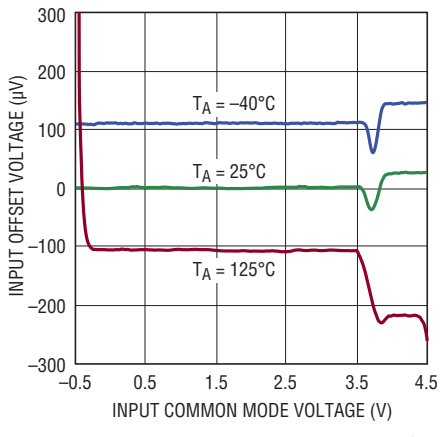
V_{OS} Distribution, MS8E (NPN Stage)



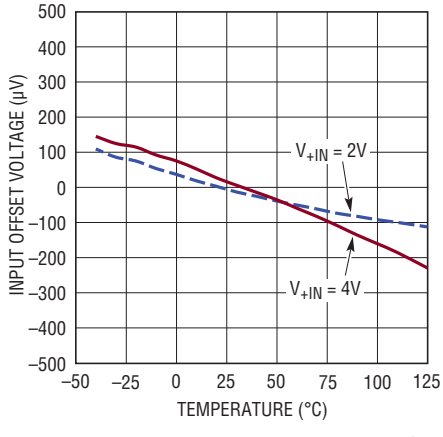
ΔV_{OS} Distribution, MS8E (PNP to NPN Stage)



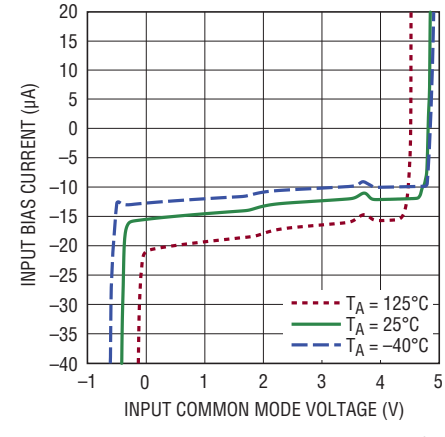
Offset Voltage vs Input Common Mode Voltage



V_{OS} vs Temperature



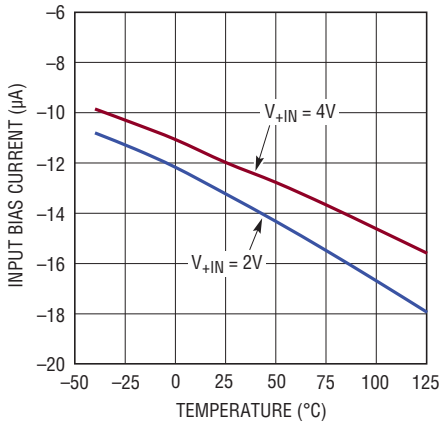
Input Bias Current vs Input Common Mode Voltage



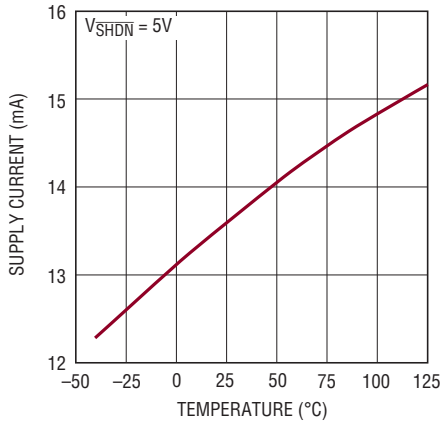
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, $V_{\overline{SHDN}}$ = 5V, see Figure 1 for circuit configuration.

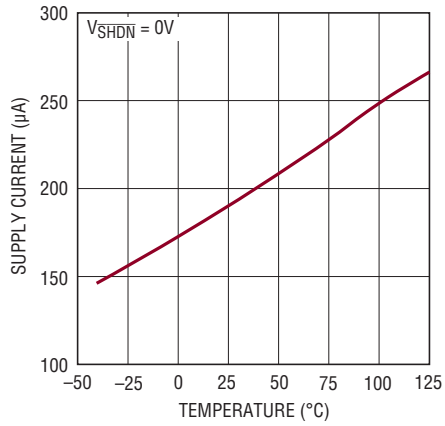
Input Bias Current vs Temperature



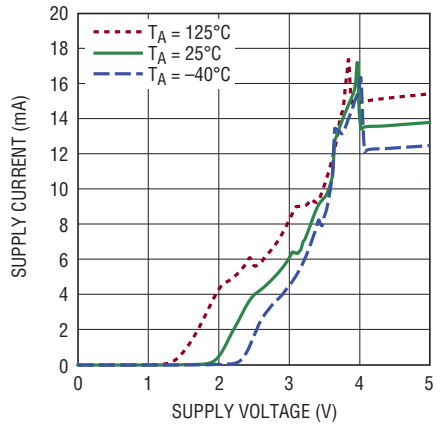
Total Supply Current vs Temperature



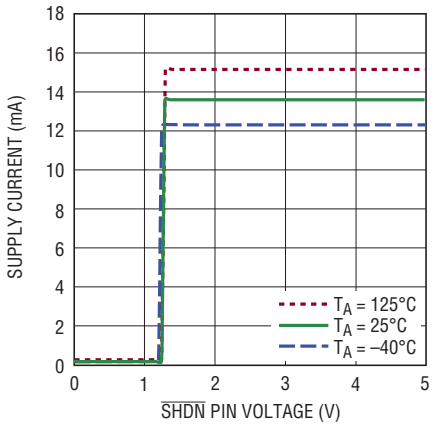
Total Supply Current in Shutdown vs Temperature



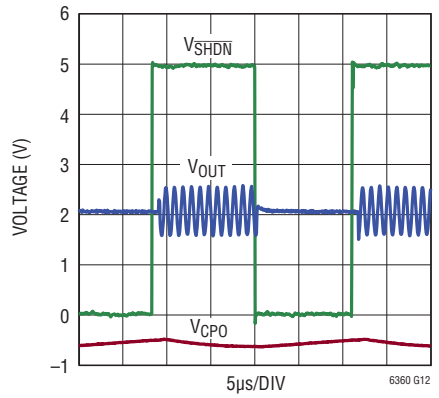
Total Supply Currents vs Supply Voltage



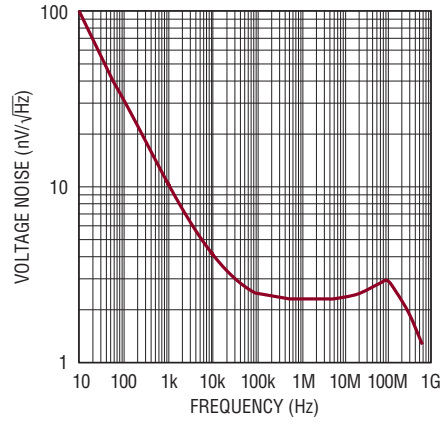
Total Supply Currents vs $\overline{SHDN}$ Voltage



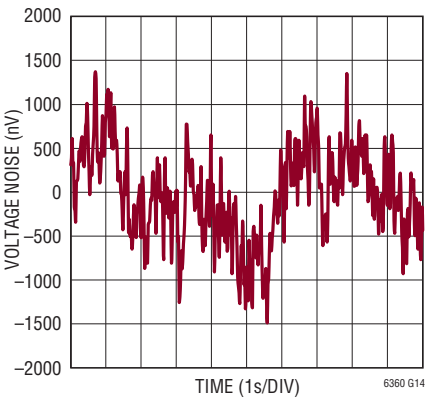
Turn-On and Turn-Off Transient Response



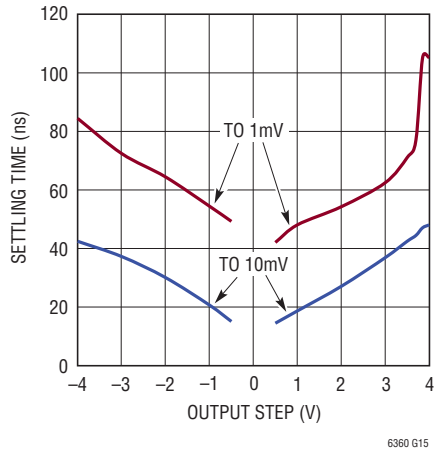
Input Voltage Noise vs Frequency



0.1Hz to 10Hz Voltage Noise



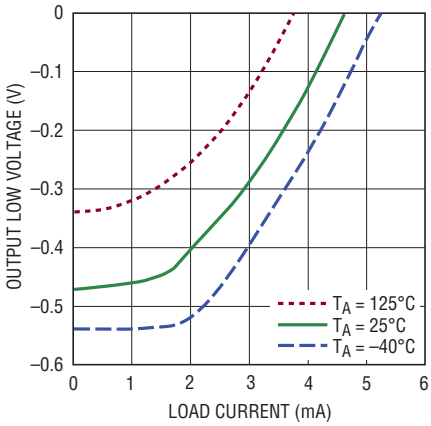
Output Settling Time vs Output Step



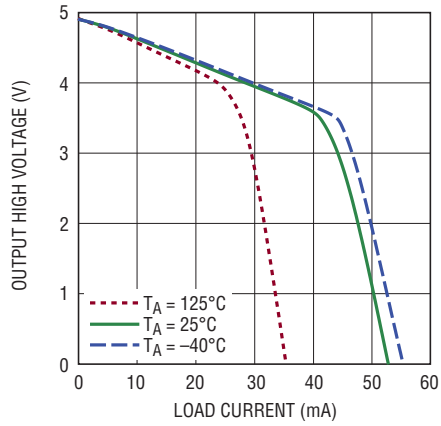
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, $V_{\overline{SHDN}}$ = 5V, see Figure 1 for circuit configuration.

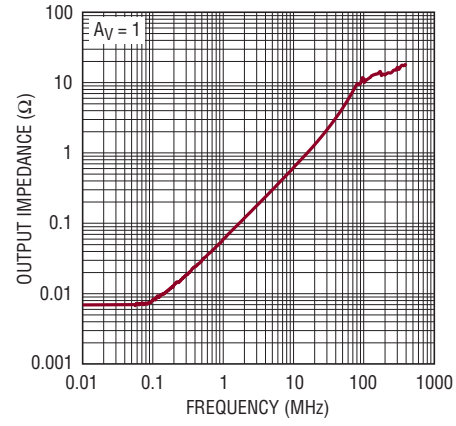
Output Low Voltage vs Load Current



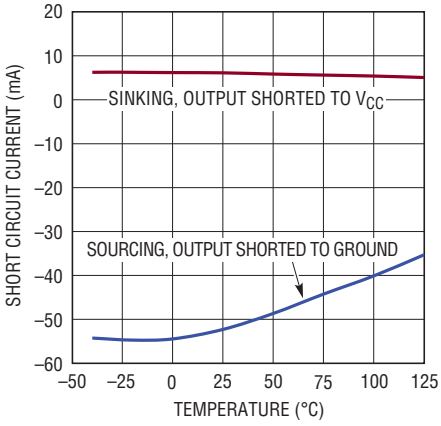
Output High Voltage vs Load Current



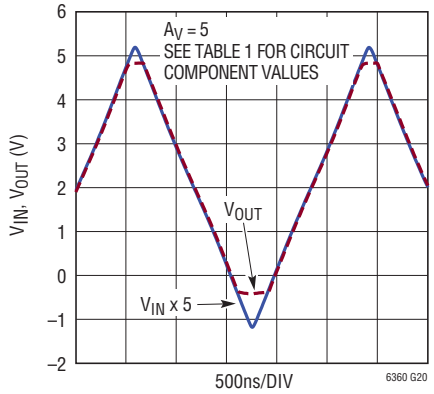
Output Impedance vs Frequency



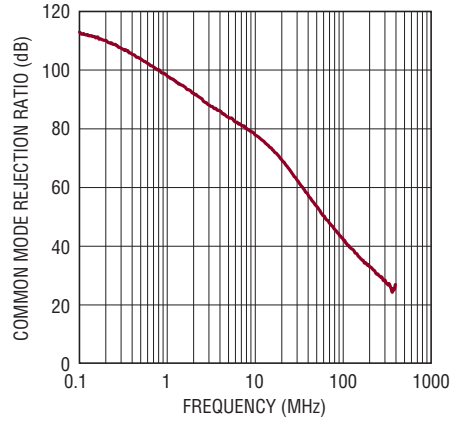
Output Short Circuit Current vs Temperature



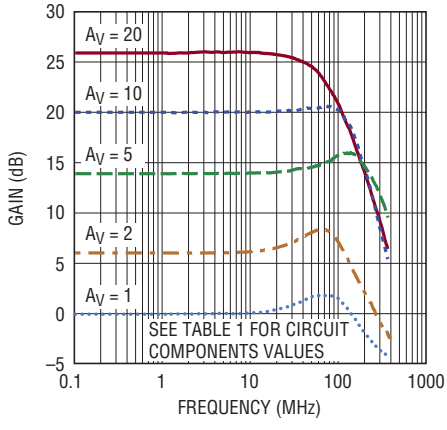
Output Overdrive Recovery



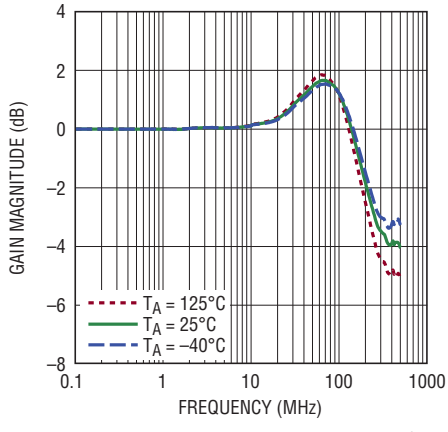
Common Mode Rejection Ratio vs Frequency



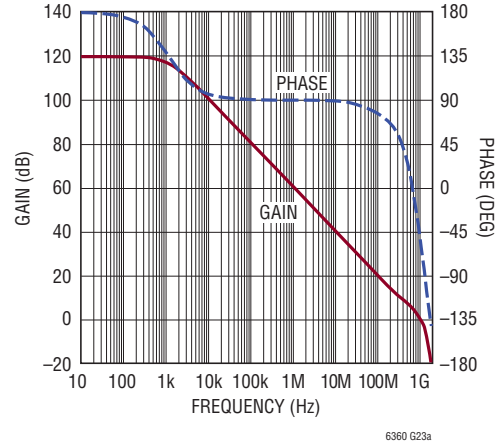
Frequency Response vs Gain



Frequency Response vs Temperature



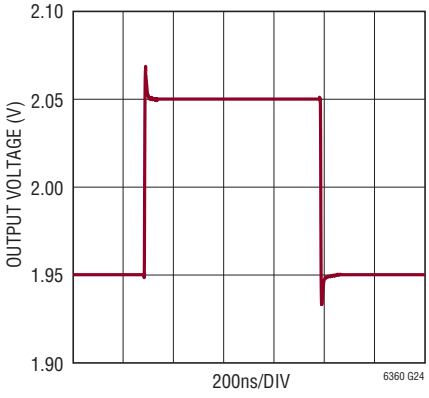
Open Loop Gain and Phase vs Frequency



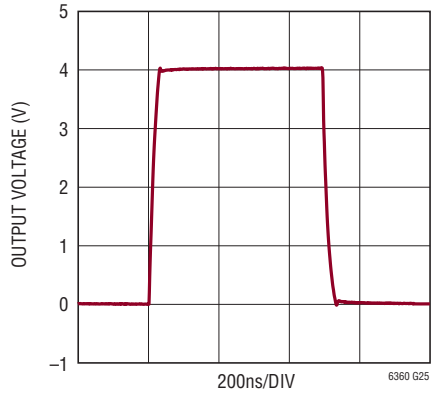
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = V_{DD} = 5V, V_{+IN} = 2V, $V_{\overline{SHDN}}$ = 5V, see Figure 1 for circuit configuration.

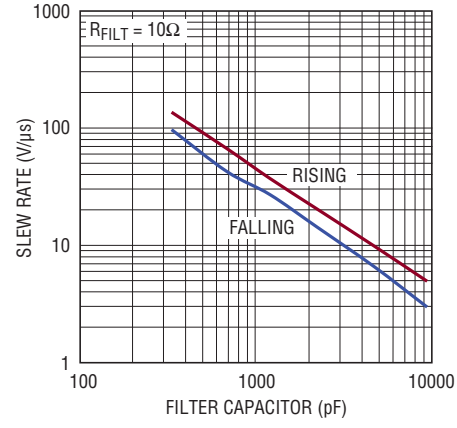
Small Signal Step Response



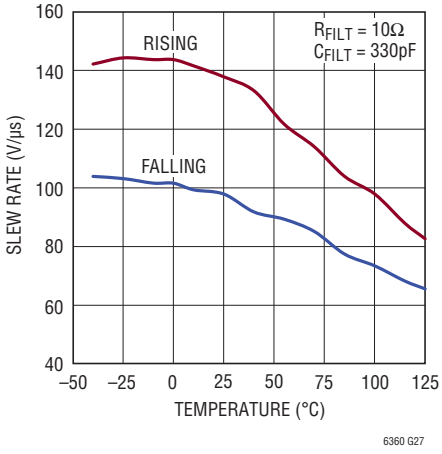
Large Signal Step Response



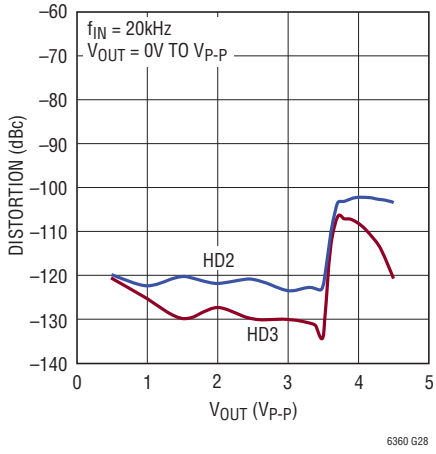
Slew Rate vs Filter Capacitor



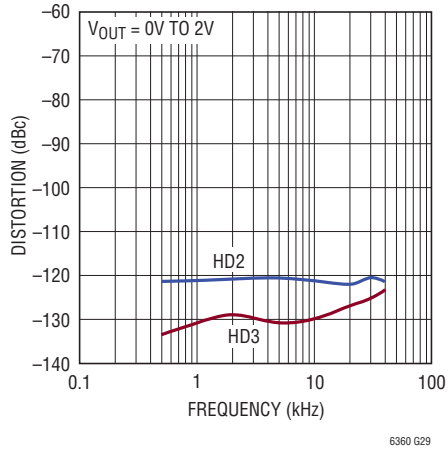
Slew Rate vs Temperature



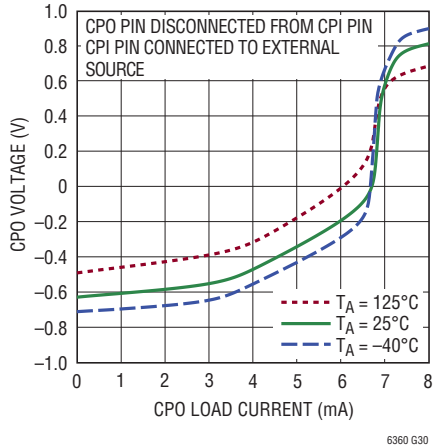
Harmonic Distortion vs Output Amplitude



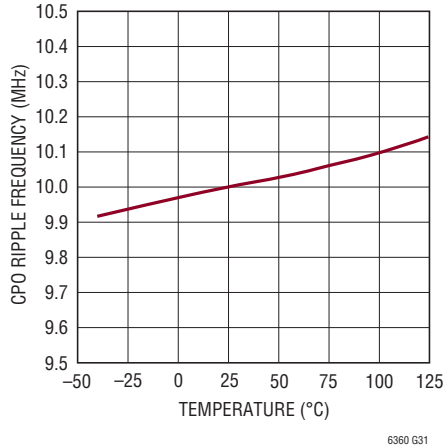
Harmonic Distortion vs Frequency



CPO Voltage vs CPO Load Current



CPO Ripple Frequency vs Temperature



PIN FUNCTIONS

–IN (Pin 1): Inverting Amplifier Input.

OUT (Pin 2): Output of Amplifier.

V_{CC} (Pin 3): Analog Power Supply. Normally connected to a 5V supply.

V_{DD} (Pin 4): Digital Power Supply. Normally connected to V_{CC}.

CPO (Pin 5): Output of Charge Pump. This pin is internally biased at –0.6V below GND.

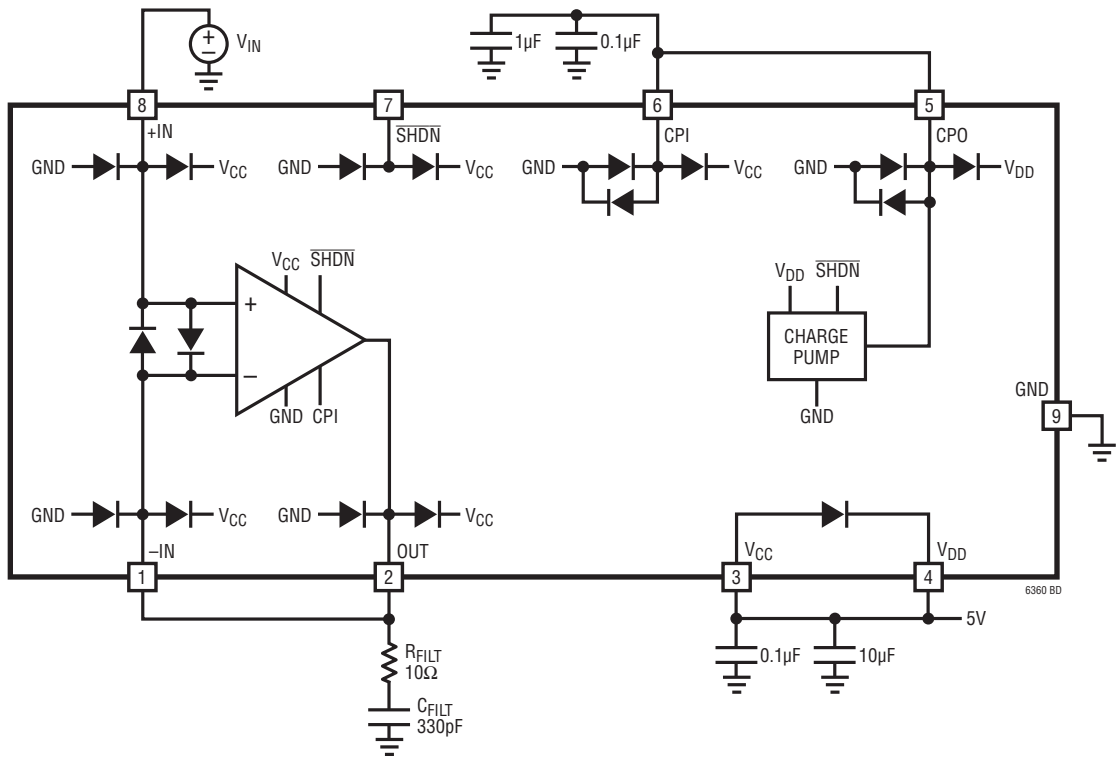
CPI (Pin 6): Input for Amplifier Negative Rail. Normally connected to CPO.

$\overline{SHDN}$ (Pin 7): Shutdown Pin. If tied high or left floating, the part is enabled. If tied low, the part is disabled and draws less than 350µA of supply current.

+IN (Pin 8): Noninverting Amplifier Input. Provides a high impedance input.

GND (Exposed Pad Pin 9): Ground Pin. Normally connected to ground.

BLOCK DIAGRAM



TEST CIRCUIT

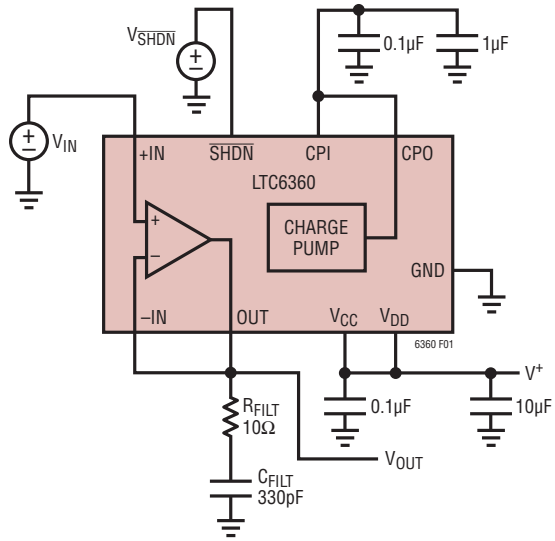


Figure 1. Test Circuit

OPERATION

The LTC6360 is a low noise amplifier suitable for driving single-ended high performance successive approximation register (SAR) ADCs. The LTC6360 uses a single amplifier with negative charge pump topology as shown in the Block Diagram.

The output can swing from –0.48V to 4.91V. The amplifier is designed to drive a series 10Ω resistor and 330pF capacitor filter network to ground, although larger load capacitances can be driven.

An on-chip low noise charge pump generates a small negative voltage (typically –0.6V) at the CPO pin. This negative voltage is normally connected to the amplifier's output stage via the CPI pin, allowing the output to swing to true zero on a single 5V supply. Compared to typical rail-to-rail output amplifiers that can only swing to within a few hundred millivolts of ground, the LTC6360 provides improved linearity and increased functionality for applications that benefit from a true zero output swing.

The LTC6360 features a low noise amplifier that can support a signal-to-noise ratio of 110dB over a 3MHz noise bandwidth.

Basic Connections

Shown in Figure 2 is a typical application for the LTC6360 as a unity gain driver. The amplifier's two inputs (+IN and –IN) can accommodate a voltage range of 0V to 4.25V on a single 5V rail. This provides a simple interface for 5V ADCs with a 4.096V full-scale range.

Noninverting gain (shown in Figure 3) and inverting gain (shown in Figure 4) configurations are also possible. For best DC precision, R_S should be made equal to the parallel combination of R_F and R_G. R_S can be bypassed with a capacitor to reduce its noise contribution.

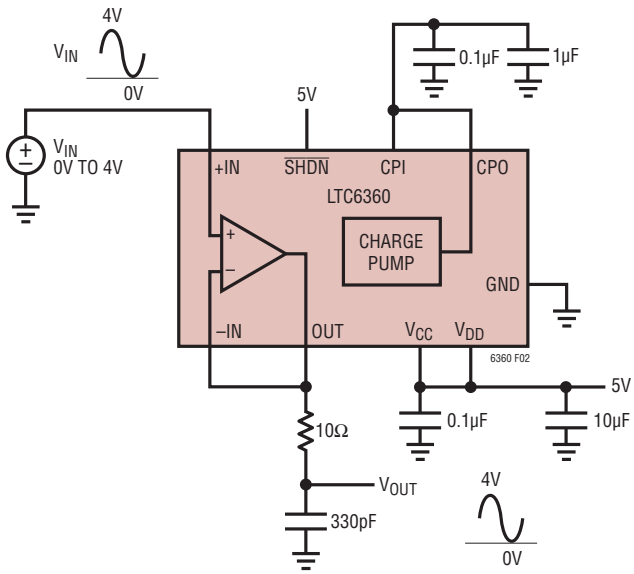


Figure 2. Unity Gain Driver.

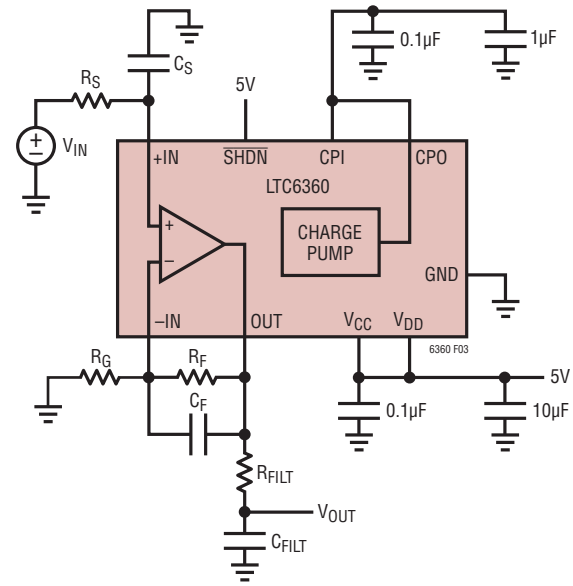


Figure 3. Noninverting Gain Configuration.

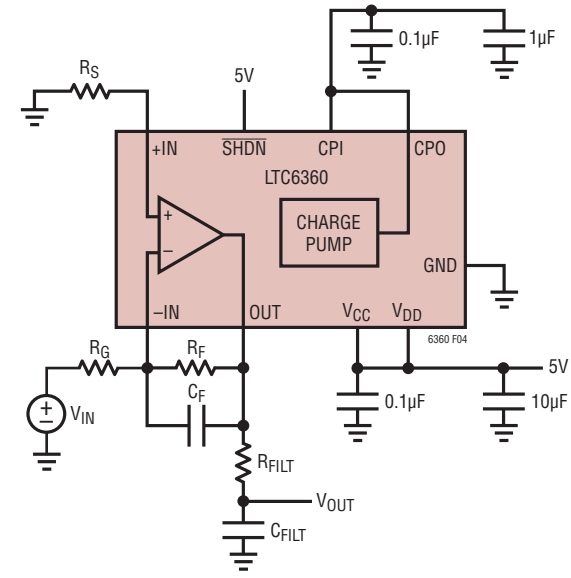


Figure 4. Inverting Gain Configuration

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Amplifier Characteristics

Figure 5 shows a simplified schematic of the LTC6360's amplifier. The input stage has NPN and PNP differential pairs operating in parallel. This topology allows the inputs to swing all the way from the negative rail to within 0.75V of the positive supply rail. The PNP differential pair is the primary input differential pair and is active when the common mode voltage is less than 1.5V from the positive rail. When the common mode voltage exceeds V_{CC} – 1.5V, the NPN pair is activated and the PNP is deactivated. The input stage transconductance, gm, is maintained nearly constant during the handover from PNP pair to NPN pair. Additionally, a precision two-point trim algorithm is used to maintain near constant offset voltage over the entire input common mode range.

Input bias current flows out of the +IN and –IN inputs. The magnitude of this current is regulated via an input current compensation circuit which eliminates the discontinuity and polarity reversal of input bias current that would otherwise occur when transitioning from one input pair to the other. Typical total change in input bias current over the entire input common mode range is approximately 3.5µA.

Amplifier Feedback Components

When feedback resistors are used to set gain, care should be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input, –IN, does not degrade stability. For instance, to set the LTC6360 in a gain of +2, R_F and R_G of Figure 3 could be set to 2k. If the total capacitance at –IN (LTC6360 plus PC board) were 2pF, a new pole would be formed in the loop response at 80MHz, which could lead to instability or ringing in the step response. A capacitor connected across the feedback resistor and having the same value as the total –IN parasitic capacitance will eliminate any ringing or oscillation. Special care should be taken during layout, including using the shortest possible trace lengths and removing the ground plane under the –IN pin, to minimize the parasitic capacitance.

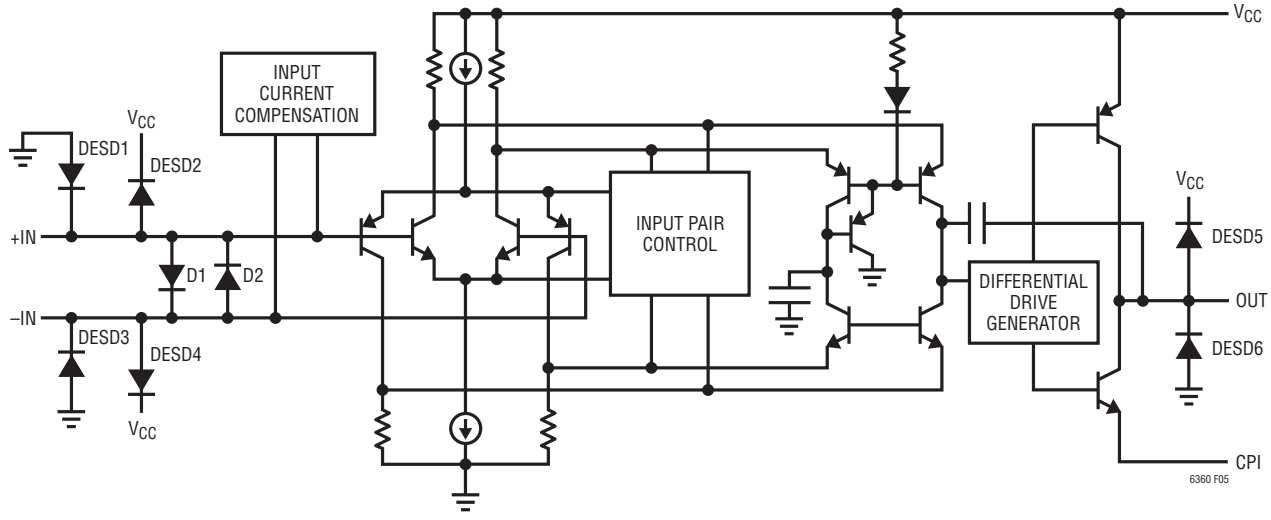

Figure 5. Amplifier Simplified Schematic

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Input bias current induced DC voltage offsets can be minimized by matching the parallel impedance of R_F and R_G to the source impedance, R_S. For example, in the typical application when the amplifier is configured as a unity gain buffer, choosing R_F equal to R_S will minimize the offset. Since nonzero values of R_F will contribute to the total output noise, R_F may be bypassed with a capacitor to reduce the noise bandwidth.

Input Protection

Back-to-back diodes (D1 and D2 in Figure 5) are included between +IN and –IN to protect the input devices. The inputs do not have internal resistors in series with the input transistors, a technique often used to protect the input transistors from excessive current flow during an overdrive condition. Adding series input resistors would significantly degrade the low noise performance. Therefore, if the voltage across the amplifier's inputs is allowed to exceed ±0.7V, steady state current conducted through the protection diodes should be externally limited to ±10mA. The input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive or momentary clipping without protection resistors.

Driving the input signal sufficiently beyond the specified input common mode voltage range will cause the input transistors to saturate. When saturation occurs, the amplifier loses a stage of phase inversion and the output will begin to invert. Diode D1 or D2 (Figure 5) forward biases and holds the output within a diode drop of the input signal. To avoid this inversion, limit the input drive to within the specified input common mode range.

ESD

The LTC6360 has ESD protection diodes on all inputs and outputs. The diodes are reverse biased during normal operation. If the input pins are driven beyond either supply, large currents will flow through these diodes. If the current is transient and limited to 10mA or less, no damage to the device will occur.

On-Chip Charge Pump

A low noise on-chip charge pump generates a small negative voltage that is used to bias the output stage of the amplifier, enabling output swing below 0V. The charge pump output voltage is typically –0.6V. Several design techniques have been used to lower the ripple present at OUT due to the switching action of the charge pump. The charge pump output is made available via the CPO pin, and the amplifier's charge pump input at the CPI pin. This allows additional external filtering via a capacitor connected from CPI to GND.

The charge pump operates at a nominal frequency of 10MHz. The output voltage at CPO will have small frequency components at multiples of 5MHz. These components are further reduced by the PSRR of the amplifier's output stage. The amplitude of the fundamental component at the OUT pin is typically $1\mu V_{RMS}$ with a 0.1µF bypass capacitor at CPI.

Conventionally, a two chip solution is chosen to provide output swing to true zero on a single supply: one amplifier and an inverting charge pump to provide a negative rail. Compared to a two chip solution, the LTC6360 offers several advantages: a more compact layout with lower part count, lower output ripple, less EMI and lower power.

Figure 6 shows the ripple voltage spectrum at the output, V_{OUT}, with a 0.1µF external CPI bypass capacitor.

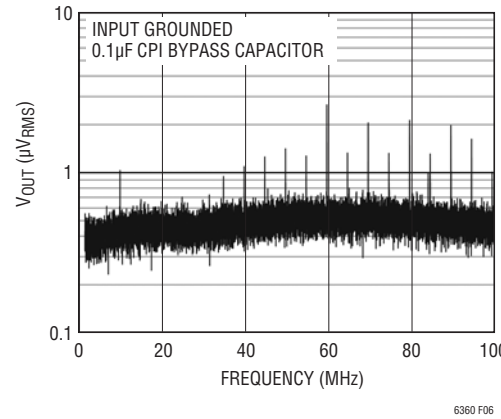

Figure 6. Output Ripple Voltage

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The charge pump is capable of sinking up to 4.5mA of DC current with a typical DC output impedance of 30Ω. If more current is demanded of the charge pump, the voltage at CPO will collapse towards 0V. A diode connected from CPO to GND limits the CPO node from being pulled above ground by more than one diode drop.

Transient currents are absorbed by the filter capacitors from CPO/CPI to GND. Care should be taken in selecting the filter capacitors such that there is minimum ripple voltage and droop during peak transient current demand. Using multiple small surface mount capacitors is advised, with each capacitor covering a portion of the total frequency range.

Slew Rate and Full Power Bandwidth

Additional consideration needs to be paid to the current demanded of the charge pump. When driving a capacitive load, the LTC6360 will exhibit a clipped distortion characteristic at a lower frequency than where slew rate limited distortion would occur. In contrast to a traditional amplifier, where the full power bandwidth is determined from the amplifier's slew rate, when driving capacitive loads, the full power bandwidth of the LTC6360 will be limited by the charge pump sinking capability.

The average current sunk by the charge pump when driving a capacitive load can be approximated as:

$$I_{CP(AVG)} = 2V_P \bullet C_{FILT} \bullet f + 1mA \quad (1)$$

where V_P and f are the amplitude and frequency of the driven signal respectively.

The maximum frequency that the charge pump can support while maintaining the CPO pin below –0.4V is:

$$f_{FPBW} = (I_{CP(MAX)} - 1mA)/(2V_P \bullet C_{FILT}) \quad (2)$$

where $I_{CP(MAX)}$ is given in the specification table. Full-scale signals beyond this frequency will cause the charge pump to collapse towards 0V, limiting the output amplitude and causing distortion.

Output Compensation

The LTC6360 is internally compensated to be gain of 5 stable. Lower gains require an external RC network at the output to provide compensation. The amplifier has been decompensated to provide the highest possible gain-bandwidth with a typical RC load of 10Ω in series with 330pF. The extra gain-bandwidth obtained serves to reduce distortion over a wider bandwidth. Since an external RC filter network is desired in most ADC applications, the decompensation is transparent in these cases and actually serves to improve distortion performance.

The RC network at the output contributes a pole-zero pair that reduces the loop gain above the pole frequency. The simplified circuit model at high frequencies is shown in Figure 7. At high frequencies, the open-loop output impedance of the amplifier can be represented by an equivalent resistor, ro, of 45Ω.

The pole frequency is:

$$f_P = 1/(2\pi(R_{FILT} + ro)C_{FILT}) \quad (3)$$

The zero frequency is:

$$f_Z = 1/(2\pi R_{FILT}C_{FILT}) \quad (4)$$

which is also the –3dB bandwidth of the filter formed by R_{FILT} and C_{FILT}. The zero-pole ratio is given by:

$$f_Z/f_P = 1 + ro/R_{FILT} \quad (5)$$

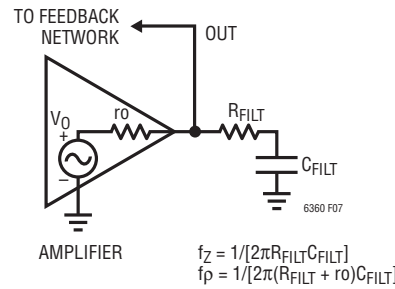

Figure 7. Pole-Zero Introduced by RC Network at Output

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The amount that the loop gain and subsequent bandwidth will be reduced is equal to this zero-pole ratio. For example, for 20dB of loop gain reduction (one decade bandwidth reduction), R_{FILT} should be made equal to 5Ω.

Figure 8 shows the open loop gain without compensation and with a 10Ω/330pF RC compensation network. The pole-zero can be seen to reduce the open loop gain above 10MHz, stabilizing the amplifier for unity gain applications.

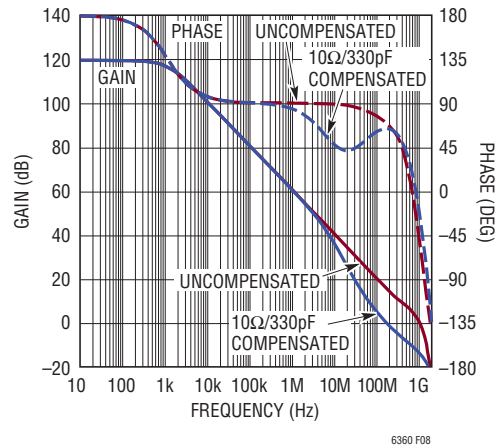

Figure 8. Open Loop Gain and Phase with and without Output Compensation

The following is a guideline for designing the RC filter to ensure stability with a circuit gain less than five:

1. In order to sufficiently reduce the gain prior to the unity loop gain crossover point, f_C, the zero-pole ratio should be greater than 5/NG, where NG is the circuit noise gain. For example, based on Equation 5, a unity gain configuration allows a maximum R_{FILT} value of 11.25Ω.

2. The zero should be located below to the unity gain crossover frequency, f_C. Once the RC network is introduced, f_C will occur at a lower frequency given by:

$$f_C = f_{C(AMP)}/(f_Z / f_P \bullet NG) \quad (6)$$

where $f_{C(AMP)}$ is the unity gain-bandwidth of the amplifier without the RC network. Thus, the following condition should be met:

$$f_Z < f_{C(AMP)}/(f_Z / f_P \bullet NG) \quad (7)$$

where $f_{C(AMP)}$ is approximately 1GHz.

This sets a lower limit on CL of:

$$C_{FILT} > (f_Z / f_P \bullet NG)/(2\pi R_{FILT} f_{C(AMP)}) \quad (8)$$

Note that for large zero-pole ratios, additional margin may be needed. In this case, setting f_Z equal to f_C yields a phase margin of at best 45°. In practice, the amplifier's higher order poles will further reduce the phase margin below 45°. Therefore, f_Z should be made lower than f_C in order to ensure adequate phase margin. Phase margin in the case of large pole-zero ratios case can be estimated as $\tan^{-1}(f_C/f_Z)$.

Likewise for small zero-pole ratios, the pole will not have contributed a full 90° of lagging phase prior to the zero contributing leading phase. The requirement for f_Z being lower than f_C can be relaxed in these cases.

3. Select R_{FILT} and C_{FILT} to yield the desired filter bandwidth while meeting the two constraints listed above.

The layout of the filter RC network is critical to the stability of the part and care should be taken to minimize parasitic inductance in this path.

Table 1 lists suggested RC filter values for some common circuit gains. Note that longer filter time constants can be implemented by increasing the C_{FILT} value beyond what is shown in Table 1 without degrading stability. For large C_{FILT} values, it may be necessary to use multiple high quality surface mount capacitors to reduce ESR and maintain a high self resonant frequency.

Table 1. Component Values for Various Circuit Gains

Noise Gain (NG)	R_F	C_F	R_G	R_{FILT}	C_{FILT}
1	0	DNI	DNI	10	330pF
2	2k	2pF	2k	25	150pF
5	2k	0.2pF	500	DNI	DNI
10	2k	DNI	222	DNI	DNI
20	2k	DNI	181	DNI	DNI

DNI – Do Not Install

Interfacing the LTC6360 to A/D Converters

When driving an ADC, a single-pole RC filter between the output of the LTC6360 and the input of the ADC can improve system performance. The sampling process of ADCs creates a charge transient at the ADC input

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caused by the switching of the ADC sampling capacitor. This momentarily disturbs the output of the amplifier as charge is transferred between amplifier and ADC. The amplifier must recover and settle from this load transient before the acquisition period ends. An RC network at the output of the LTC6360 helps decouple the sampling transient of the ADC from the amplifier, reducing the demands on the amplifier's output stage (see Figure 9). The resistor at the input of the ADC minimizes the sampling transients that discharge the RC filter capacitor.

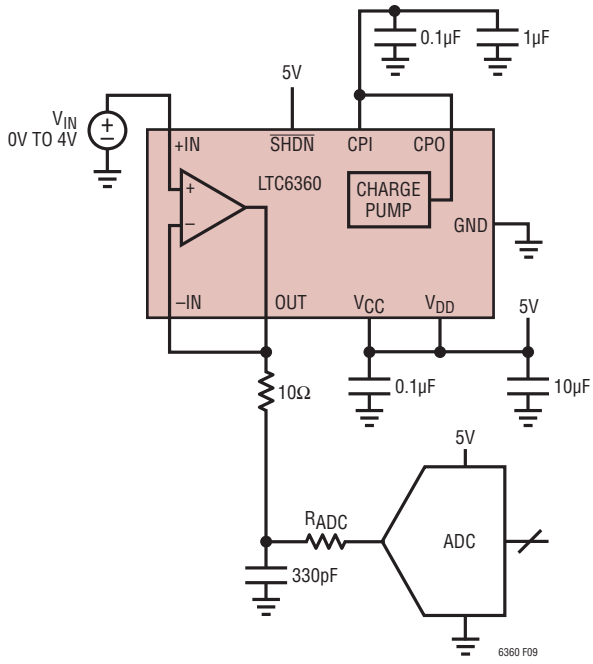

Figure 9. Driving an ADC

The filter capacitor serves to provide the bulk of the charge during the sampling process, while the filter resistor dampens and attenuates any charge injected by the ADC. The RC filter has the additional benefit of band limiting broadband output noise.

The selection of the RC time constant depends on the application; but generally, longer time constants will improve SNR at the expense of longer settling time. Excessive settling time can introduce gain errors and distortion if the filter components are not perfectly linear. 16-bit applications typically require a minimum settling time of eleven RC time constants of a first order filter. Note also that too small a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling.

High quality resistors and capacitors should be used for the RC filter network since these components stabilize the internal amplifier and can also contribute their own distortion. For lowest distortion, choose capacitors with a high quality dielectric, such as a C0G multilayer ceramic capacitor. Metal film surface mount resistors are more linear than carbon types.

$\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin is 5V TTL or 3.6V CMOS level compatible. If the $\overline{\text{SHDN}}$ pin (Pin 7) is pulled low, below 0.8V, the LTC6360 will power down. If the pin is left open or pulled high, above 2.0V, the part will enter normal active operation. The turn-on time between the shutdown and active states is typically 1µs, and turn-off time is typically 0.3µs.

In shutdown, the output pin (OUT) appears as an open collector with a nonlinear capacitor to ground and steering diodes to V_{CC} and ground. Because of the nonlinear capacitance, the output will still have the ability to sink and source small amounts of transient current if exposed to significant voltage transients. The input protection diodes between +IN and –IN can still conduct if voltage transients at the input exceed 700mV.

Noise Considerations

The LTC6360 has a low noise density e_n of 2.3nV/$\sqrt{\text{Hz}}$. This is equivalent to the voltage noise of a 320Ω resistor at the +IN input. For source resistors larger than 320Ω, voltage noise due to the source resistance will start to dominate. The current noise density is 3pA/$\sqrt{\text{Hz}}$, thus source resistors larger than about 770Ω will interact with the input current noise and result in output noise that is amplifier current noise dominant.

Note that the parallel combination of gain setting resistors R_F and R_G behaves like the source resistance, R_S, in noise calculations.

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Lower value gain and feedback resistors, R_G and R_F, will result in lower output noise at the expense of increased distortion due to increased loading of the amplifier. External loading should not be less than 2kΩ to avoid degrading distortion performance. When using R_S equal to $R_F||R_G$, wideband noise can be substantially reduced by bypassing with a small capacitor across R_F.

Using a single pole passive RC filter network at the output of the LTC6360 reduces the output noise bandwidth and thereby increases the signal to noise ratio of the system.

For example, in a typical system with an output signal of $4V_{P-P}$, an RC output filter with R_{FILT} = 10Ω and C_{FILT} = 330pF will reduce the total integrated noise from 57μV (250MHz –3dB bandwidth at OUT) to 27μV (48MHz –3dB bandwidth) and improve the SNR from 90dB to 97dB.

Keep in mind that long RC time constants in the output filter can increase the settling time at the inputs of the ADC. Incomplete settling can cause gain errors or increase apparent crosstalk in multiplexed systems.

Board Layout and Bypass Capacitors/DC1639A Demoboard

It is recommended that a high quality X5R or X7R, 0.1μF bypass capacitor be placed directly between the V_{CC} and the GND pin; the GND pin (exposed pad) should be tied directly to a low impedance ground plane with minimal routing. The CPI pin can be filtered with several high quality X5R or X7R capacitors returned to GND with minimal trace routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best with the LTC6360.

Stray parasitic capacitance at the –IN pin should be kept to a minimum to prevent degraded stability response resulting in excessive ringing or oscillations. Traces at –IN should be kept as short as possible, and any ground plane should be stripped from under the pin and trace.

The RC filter network at the output serves both as a filter and compensation network. Parasitic trace inductance in this path will tend to destabilize the amplifier. The RC filter network at the output should return directly to a low impedance ground plane and trace routing should be minimized in this path. A high quality COG/NPO surface mount capacitor should be used to optimize distortion performance and reduce destabilizing series resistance and inductance. When large filter capacitor values are required, multiple surface mount capacitors may be necessary with the smallest-valued capacitor placed closest to the output.

The DC1639A demoboard has been designed for the evaluation of the LTC6360 following the above layout practices. Its schematic and layout are shown in Figures 10 and 11.

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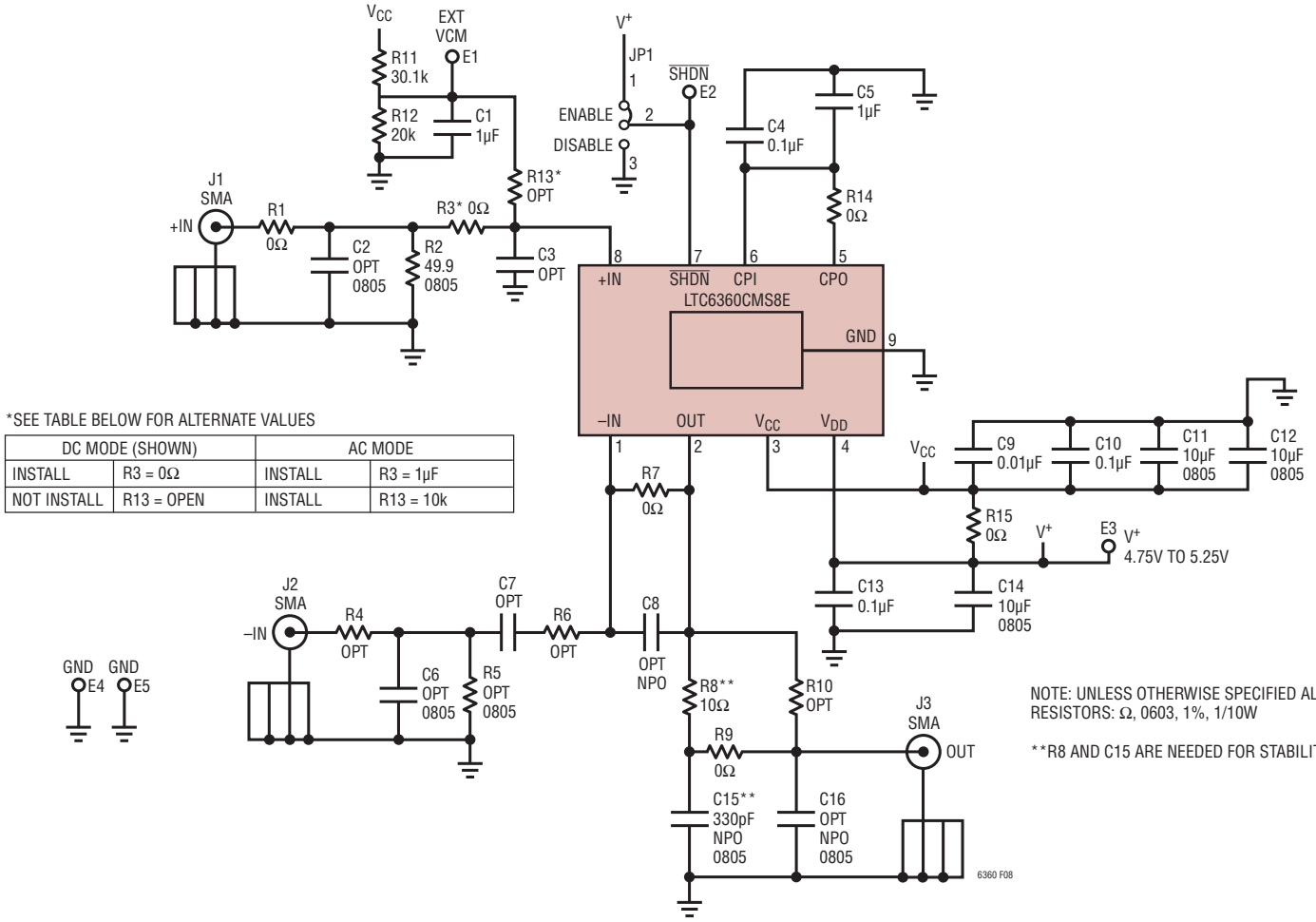


*SEE TABLE BELOW FOR ALTERNATE VALUES

DC MODE (SHOWN)		AC MODE	
INSTALL	R3 = 0Ω	INSTALL	R3 = 1µF
NOT INSTALL	R13 = OPEN	INSTALL	R13 = 10k

NOTE: UNLESS OTHERWISE SPECIFIED ALL RESISTORS: Ω, 0603, 1%, 1/10W

**R8 AND C15 ARE NEEDED FOR STABILITY

Figure 10. DC1639A Demoboard Schematic

APPLICATIONS INFORMATION

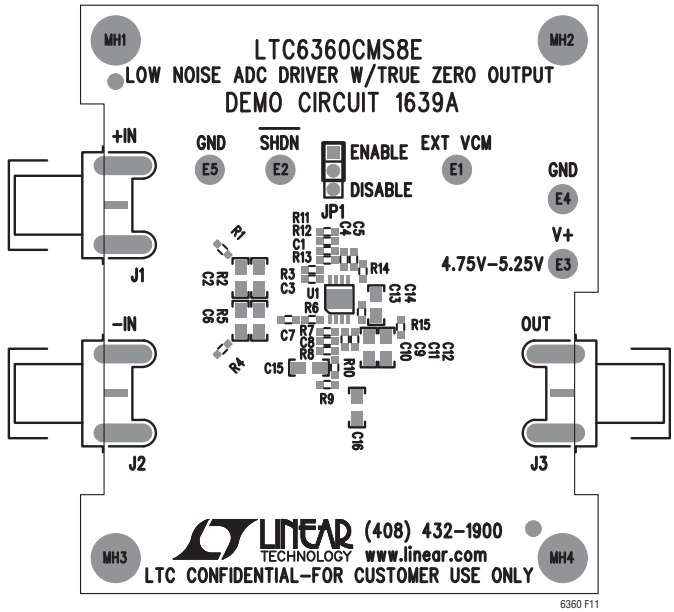


Figure 11. DC1639A Demoboard Layout

APPLICATIONS INFORMATION

Interfacing to High Voltage Signals

Using the amplifier in the inverting configuration, with a fixed input common mode voltage, allows the input signal to traverse a swing beyond the LTC6360 supply rails.

A practical application for the inverting gain configuration is translating a high voltage signal to a range suitable for a low voltage SAR ADC. For a clean interface, two conditions must be met:

1. The gain is selected so that full-scale signals at HV_{IN} are translated at the output of the LTC6360 to the appropriate full-scale range for the ADC.
2. $V_{OUT} = V_{FS}/2$ when HV_{IN} is centered at HV_{NOM}, where V_{FS} is the ADC full-scale input voltage and HV_{NOM} is the average level of the input voltage.

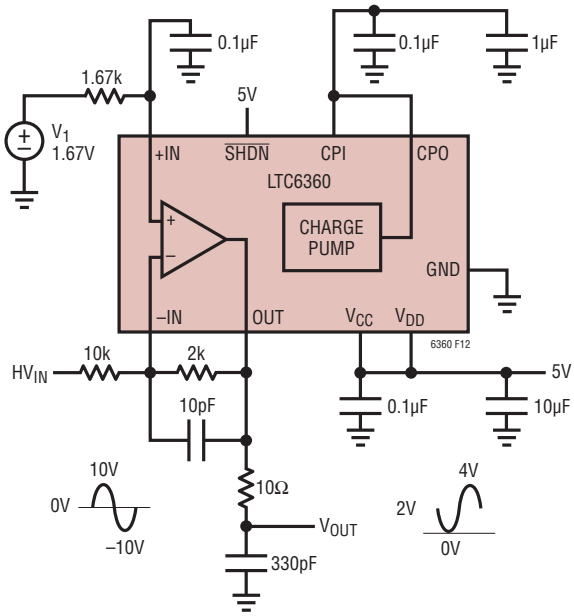


Figure 12. Interfacing a ±10V Input Signal to a 5V ADC

Applying the above constraints to the design equations gives values for R_F/R_G and V1:

$$R_F / R_G = \frac{[V_{OUT(MAX)} - V_{OUT(MIN)}]}{[HV_{IN(MAX)} - HV_{IN(MIN)}]} \quad (9)$$

$$V_1 = [V_{FS}/2 + R_F/R_G \bullet HV_{NOM}]/(1 + R_F/R_G) \quad (10)$$

Applying these formulas to the case where ±10V input signal is to be translated to a 0V to 4V full-scale range yields the values shown in Figure 12.

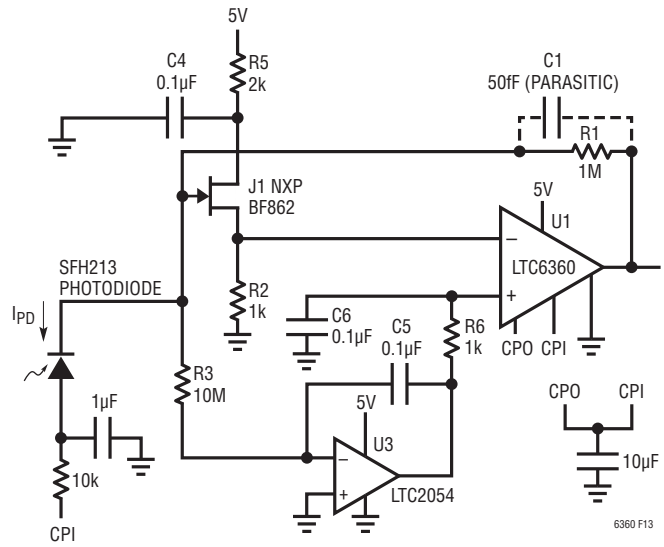


Figure 13. Low Noise, True Zero 1MΩ DC Precise Photodiode Transimpedance Amplifier

APPLICATIONS INFORMATION

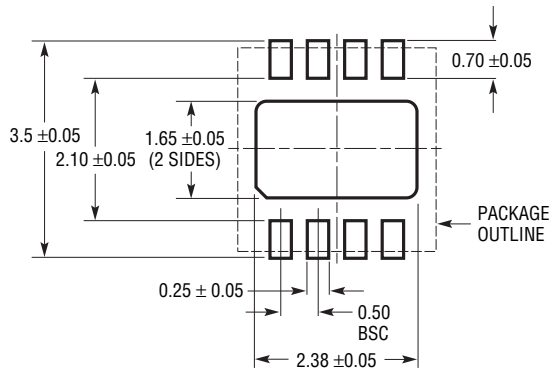
Low Noise, True Zero 1MΩ Photodiode Transimpedance Amplifier

Figure 13 shows the LTC6360 applied as a transimpedance amplifier. The LTC6360 charge pump drives the anode of the photodiode. The BF862 ultra low noise JFET (J1) acts as a source follower, buffering the input of the LTC6360 and making it suitable for the high impedance feedback element R1. The BF862 has a minimum I_{DSS} of 10mA and a pinchoff voltage between –0.3V and –1.2V. The LTC2054 chopper stabilized op amp acts to servo the DC voltage at the JFET gate to 0V, which allows the output of the LTC6360 to swing to 0V when there is no photo diode current.

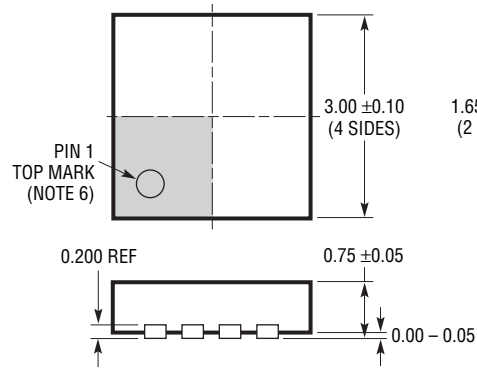
Amplifier output noise density is dominated by the 130nV/$\sqrt{Hz}$ of the feedback resistor at low frequency, rising to 320nV/$\sqrt{Hz}$ at 1MHz. Note that because the JFET has a g_m of approximately 1/100Ω, its attenuation looking into R2 is only about 10%. The closed loop bandwidth using a SFH213 photodiode was measured at approximately 3.2MHz.

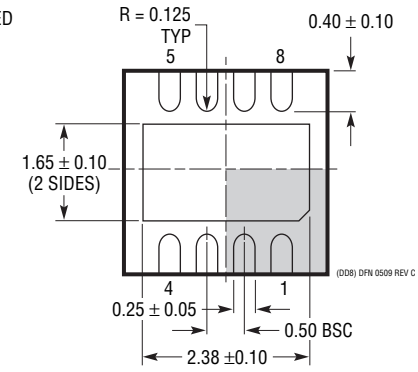
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



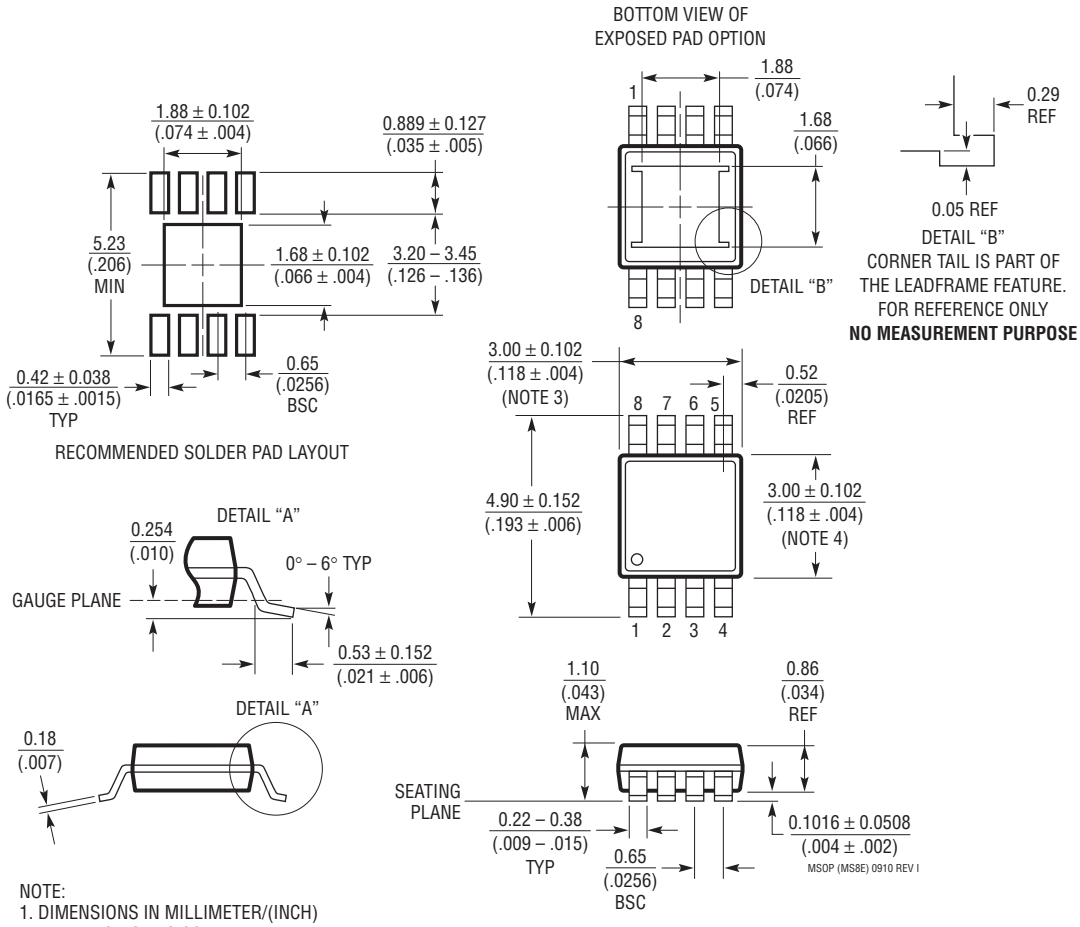


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev I)

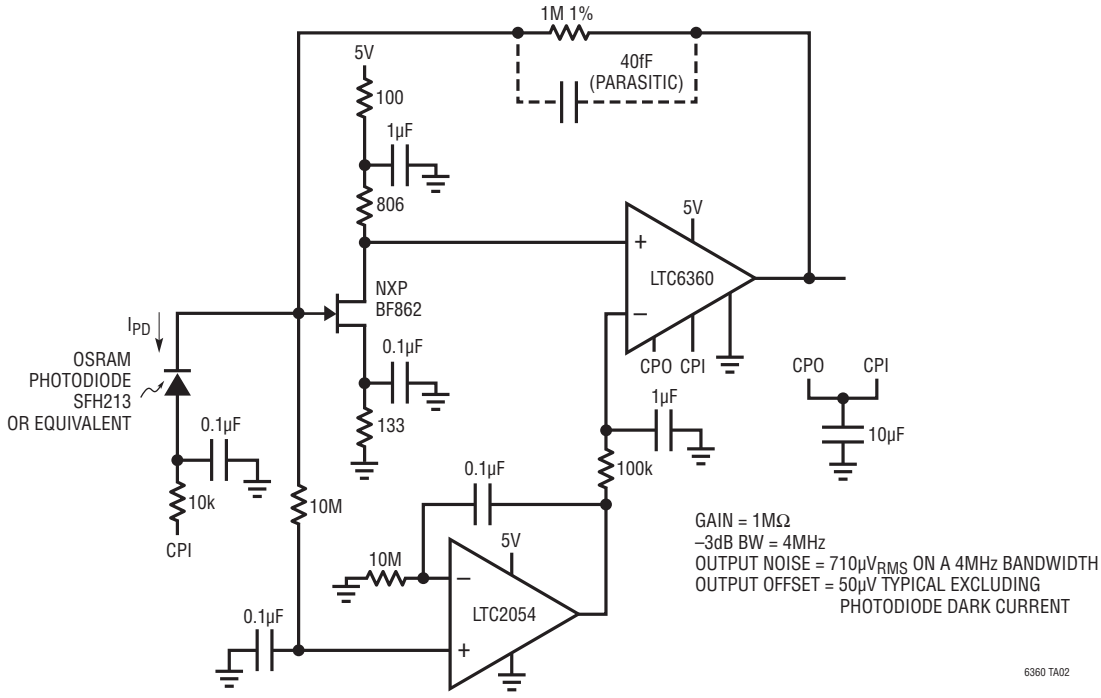


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Precision Ultralow Noise True Zero Photodiode Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT6350	Low Noise Single-Ended to Differential Converter/ADC Driver	1.9nV/√Hz, 2.7V to 12V Operation, 240ns 0.01% Settling Time
LTC6253	720MHz, 3.5mA Dual Power Efficient Rail-to-Rail I/O Op Amps	720MHz, 3.3mA, 2.75nV/√Hz, 280V/µs, 350µV, –77dBc at 4MHz
LT1818/LT1819	Single/Dual Wide Bandwidth, High Slew Rate Low Noise and Distortion Op Amps	400MHz, 9mA, 6nV/√Hz, 2500V/µs, 1.5mV, –85dBc at 5MHz
LT1806/LT1807	Single/Dual Low Noise Rail-to-Rail I/O Op Amps	325MHz, 13mA, 3.5nV/√Hz, 140V/µs, 550µV, 85mA Output Drive

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