## 1. General description

Double NPN switching transistor in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

### 2. Features and benefits

- Leadless ultra small SMD plastic package
- · Reduces component count
- · Reduces pick and place costs
- Low package height of 0.5 mm

## 3. Applications

· General-purpose switching and amplification

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	40	V
I <sub>C</sub>	collector current			-	-	200	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 1 V; I <sub>C</sub> = 10 mA		100	180	300	



40 V, 200 mA double NPN switching transistor

# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1		C1 B2 E2
2	B1	base TR1	$\begin{bmatrix} 1 \\ 7 \end{bmatrix}$	
3	C2	collector TR2	2 5	(TR1) TR2)
4	E2	emitter TR2		
5	B2	base TR2	3   8   4	E1 B1 C2
6	C1	collector TR1		sym020
7	C1	collector TR1	Transparent top view	
8	C2	collector TR2	DFN1412-6 (SOT1268)	

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package					
	Name	Description	Version			
PMBT3904RA		plastic, thermal enhanced ultra thin small outline package; no leads; 6 terminals; 1.4 mm x 1.2 mm x 0.47 mm body	SOT1268			

# 7. Marking

#### Table 4. Marking codes

Type number	Marking code
PMBT3904RA	C6

40 V, 200 mA double NPN switching transistor

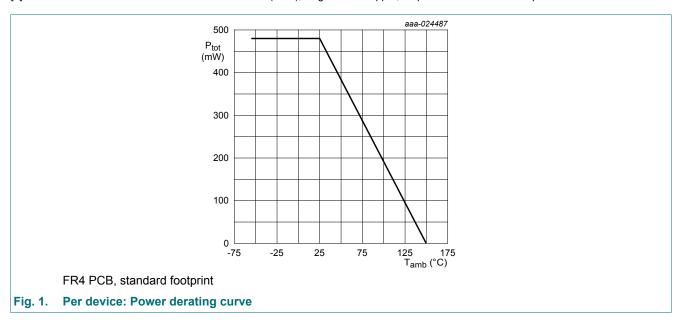
# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transist	or		•			
V <sub>CBO</sub>	collector-base voltage	open emitter		-	60	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	40	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	6	V
I <sub>C</sub>	collector current			-	200	mA
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms		-	200	mA
I <sub>BM</sub>	peak base current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	325	mW
Per device						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	480	mW
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



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### 9. Thermal characteristics

#### **Table 6. Thermal characteristics**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

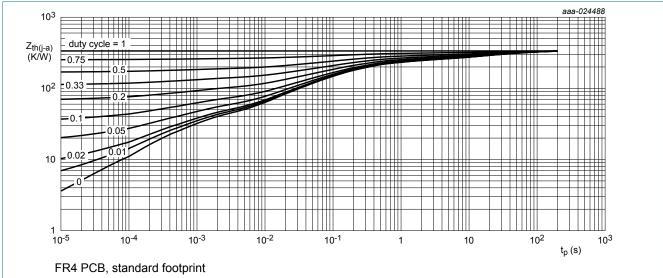


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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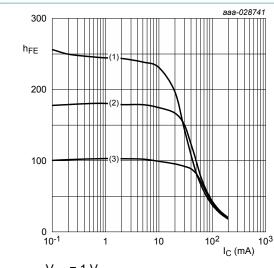
## 10. Characteristics

#### **Table 7. Characteristics**

 $T_{amb}$  = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transist	or					
V <sub>(BR)CBO</sub>	collector-base breakdown voltage	I <sub>C</sub> = 100 μA; I <sub>E</sub> = 0 A	60	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I <sub>C</sub> = 1 mA; I <sub>B</sub> = 0 A	40	-	-	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I <sub>C</sub> = 0 A; I <sub>E</sub> = 100 μA	6	-	-	V
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 30 V; I <sub>E</sub> = 0 A	-	-	50	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 6 V; I <sub>C</sub> = 0 A	-	-	50	nA
h <sub>FE</sub> DC curre	DC current gain	V <sub>CE</sub> = 1 V; I <sub>C</sub> = 100 μA	60	180	-	
		V <sub>CE</sub> = 1 V; I <sub>C</sub> = 1 mA	80	180	-	
		V <sub>CE</sub> = 1 V; I <sub>C</sub> = 10 mA	100	180	300	
		V <sub>CE</sub> = 1 V; I <sub>C</sub> = 50 mA	60	105	-	
		$V_{CE}$ = 1 V; $I_{C}$ = 100 mA; pulsed; $t_{p} \le$ 300 μs; $\delta \le$ 0.02	30	50	-	
V <sub>CEsat</sub> collector-	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 1 mA	-	75	200	mV
		I <sub>C</sub> = 50 mA; I <sub>B</sub> = 5 mA	-	120	300	mV
V <sub>BEsat</sub>	base-emitter saturation	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 1 mA	650	750	850	mV
	voltage	I <sub>C</sub> = 50 mA; I <sub>B</sub> = 5 mA	-	850	950	mV
t <sub>d</sub>	delay time	I <sub>C</sub> = 10 mA; I <sub>Bon</sub> = 1 mA; I <sub>Boff</sub> = -1 mA	-	-	35	ns
t <sub>r</sub>	rise time		-	-	35	ns
t <sub>on</sub>	turn-on time		-	-	70	ns
t <sub>s</sub>	storage time		-	-	200	ns
t <sub>f</sub>	fall time		-	-	50	ns
t <sub>off</sub>	turn-off time		-	-	250	ns
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 5 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz	-	-	4	pF
C <sub>e</sub>	emitter capacitance	V <sub>EB</sub> = 0.5 V; I <sub>C</sub> = 0 A; i <sub>c</sub> = 0 A; f = 1 MHz	-	-	8	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = 20 V; I <sub>C</sub> = 10 mA; f = 100 MHz	300	-	-	MHz

#### 40 V, 200 mA double NPN switching transistor

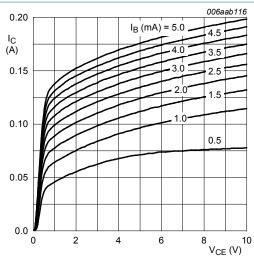


$$V_{CE} = 1 V$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

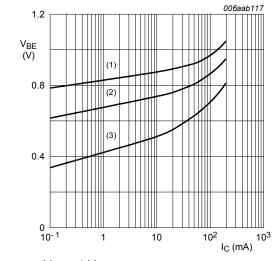
$$(3) T_{amb} = -55 °C$$

Fig. 3. DC current gain as a function of collector current; typical values



 $T_{amb}$  = 25 °C

Fig. 4. Collector current as a function of collectoremitter voltage; typical values



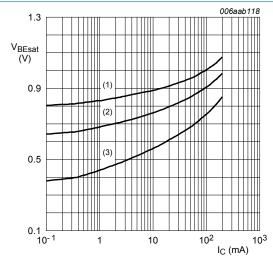
 $V_{CE} = 1 V$ 

(1) 
$$T_{amb} = -55 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3) 
$$T_{amb} = 150 \, ^{\circ}C$$

Fig. 5. Base-emitter voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 10$$

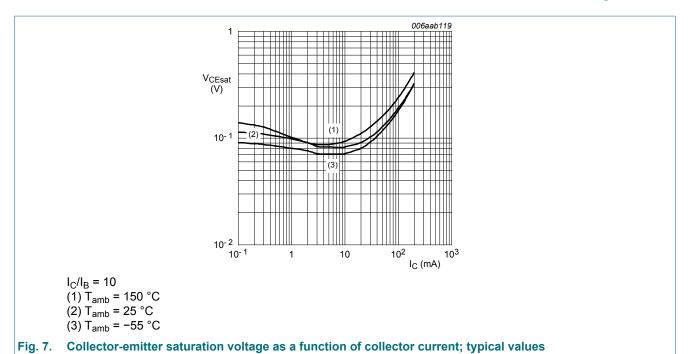
(1) 
$$T_{amb} = -55 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

$$(3) T_{amb} = 150 °C$$

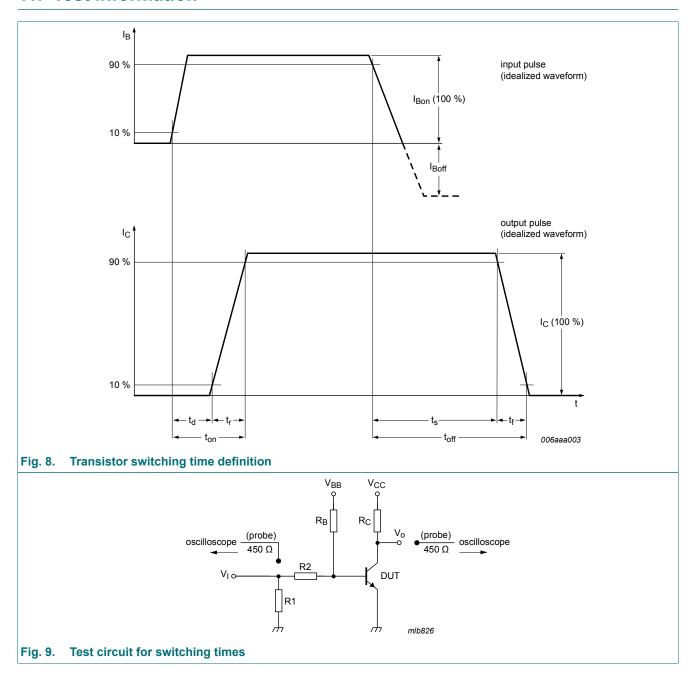
Fig. 6. Base-emitter saturation voltage as a function of collector current; typical values

### 40 V, 200 mA double NPN switching transistor



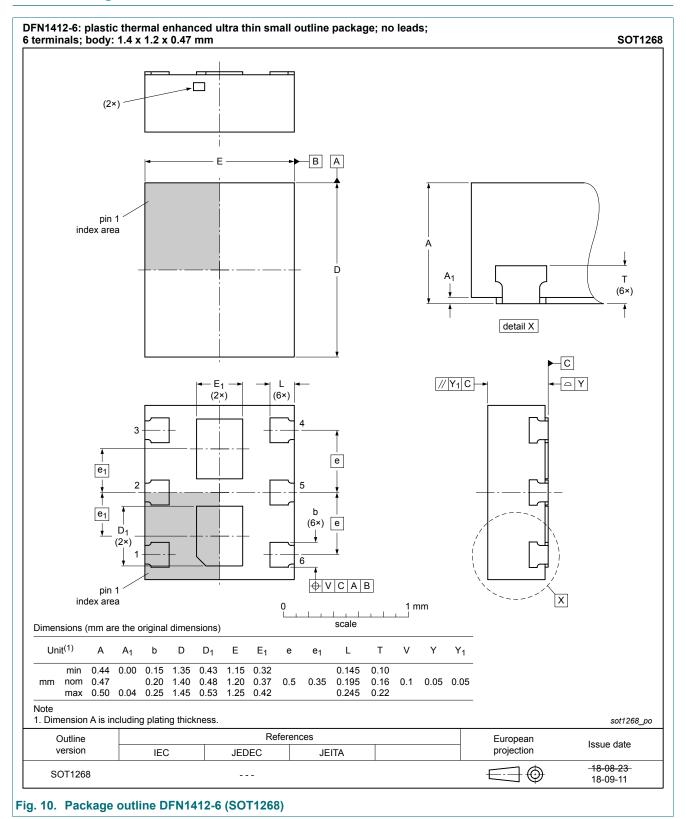
### 40 V, 200 mA double NPN switching transistor

## 11. Test information



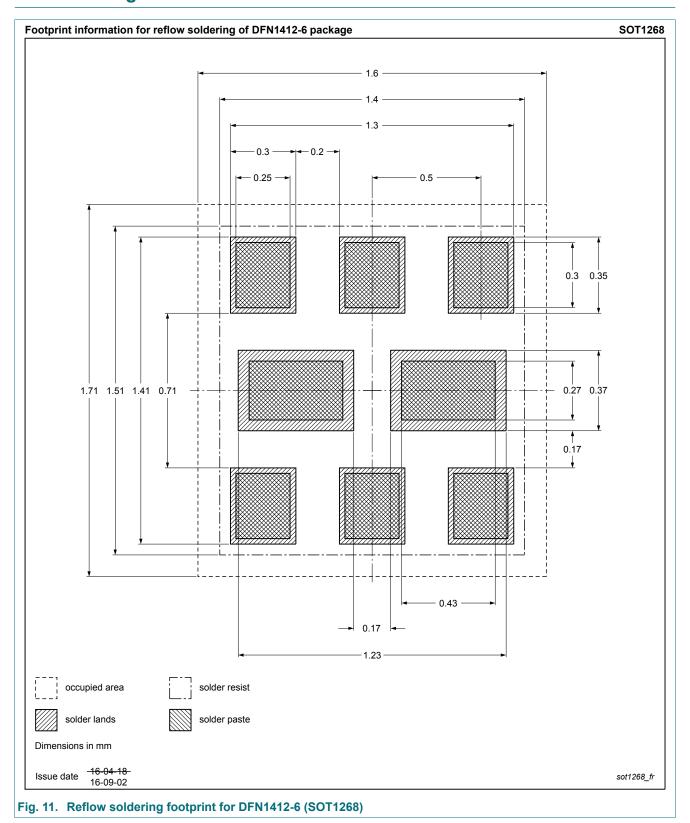
40 V, 200 mA double NPN switching transistor

# 12. Package outline



40 V, 200 mA double NPN switching transistor

# 13. Soldering



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# 14. Revision history

### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMBT3904RA v.1	20180913	Product data sheet	-	-

## 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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### 40 V, 200 mA double NPN switching transistor

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