



# PCA9672

Remote 8-bit I/O expander for Fm+ I<sup>2</sup>C-bus with interrupt and reset

Rev. 3 — 27 May 2013

Product data sheet

## 1. General description

The PCA9672 provides general-purpose remote I/O expansion via the two-wire bidirectional I<sup>2</sup>C-bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 1 MHz 30 mA drive I<sup>2</sup>C-bus interface, three hardware address inputs and a reset input operating between 2.3 V and 5.5 V. 1 MHz I<sup>2</sup>C-bus Fast-mode Plus (Fm+) can support PWM dimming of LEDs, and higher I<sup>2</sup>C-bus drive 30 mA allows more devices to be on the bus without the need for bus buffers. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. The system master can read from the input port or write to the output port through a single register.

The low current consumption of 2.5  $\mu$ A (typical, static) is great for mobile applications and the latched output ports have 25 mA high current sink drive capability for directly driving LEDs.

The PCA9672 has two hardware address pins, allowing sixteen of each device to be on the same I<sup>2</sup>C-bus without the need for bus buffers, so there can be supporting up to 128 I/Os (for example, 128 LEDs).

The active LOW open-drain interrupt output ( $\overline{\text{INT}}$ ) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I<sup>2</sup>C-bus.

The internal Power-On Reset (POR) and active LOW hardware reset pin ( $\overline{\text{RESET}}$ ) initialize the I/Os as inputs with a weak internal pull-up 100  $\mu$ A current source.

## 2. Features and benefits

- I<sup>2</sup>C-bus to parallel port expander
- 1 MHz I<sup>2</sup>C-bus interface (Fast-mode Plus I<sup>2</sup>C-bus)
- Operating supply voltage 2.3 V to 5.5 V with 5.5 V tolerant I/Os held to  $V_{DD}$  with 100  $\mu$ A current source
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability directly drive LEDs
- Total package sink capability of 200 mA
- Active LOW reset input
- Active LOW open-drain interrupt output



- Sixteen programmable slave addresses using two address pins
- Readable device ID (manufacturer, device type, and revision)
- Software reset
- Low standby current (2.5  $\mu$ A typical)
- $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16 and HVQFN16

### 3. Applications

- LED signs and displays
- Servers
- Keypads
- Industrial control
- Medical equipment
- PLCs
- Cellular telephones
- Mobile devices
- Gaming machines
- Instrumentation and test measurement

### 4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9672BS	672	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body $3 \times 3 \times 0.85$ mm	SOT758-1
PCA9672D	PCA9672D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9672PW	PCA9672	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9672BS	PCA9672BS,118	HVQFN16	Reel 13" Q1/T1 *standard mark SMD	6000	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
PCA9672D	PCA9672D,512	SO16	Standard marking * tube dry pack	1920	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
	PCA9672D,518	SO16	Reel 13" Q1/T1 *standard mark SMD dry pack	1000	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
PCA9672PW	PCA9672PW,112	TSSOP16	Standard marking * IC's tube - DSC dry pack	2400	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
	PCA9672PW,118	TSSOP16	Reel 13" Q1/T1 *standard mark SMD	2500	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

5. Block diagram

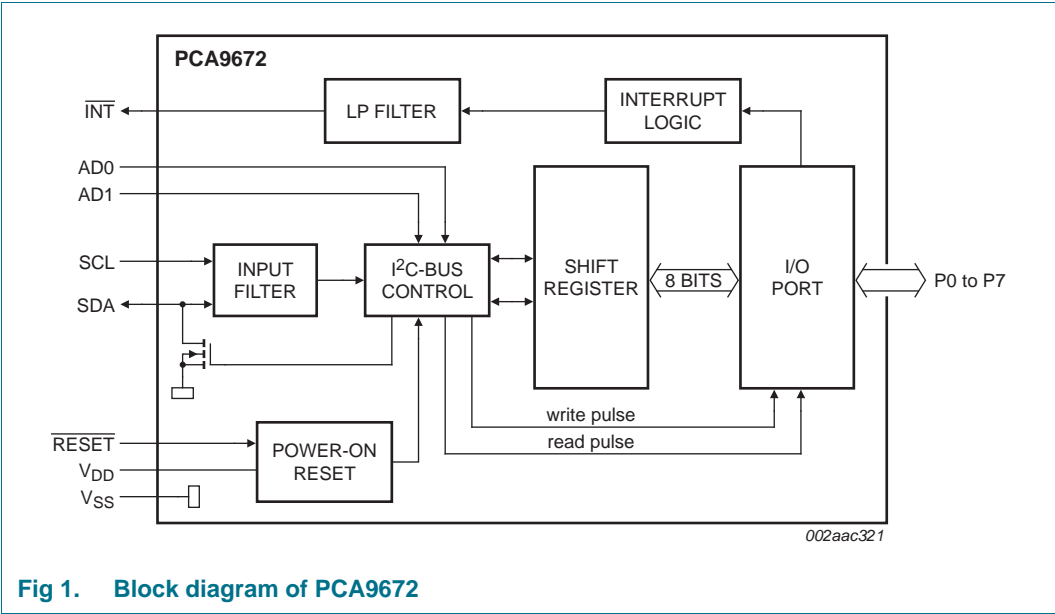


Fig 1. Block diagram of PCA9672

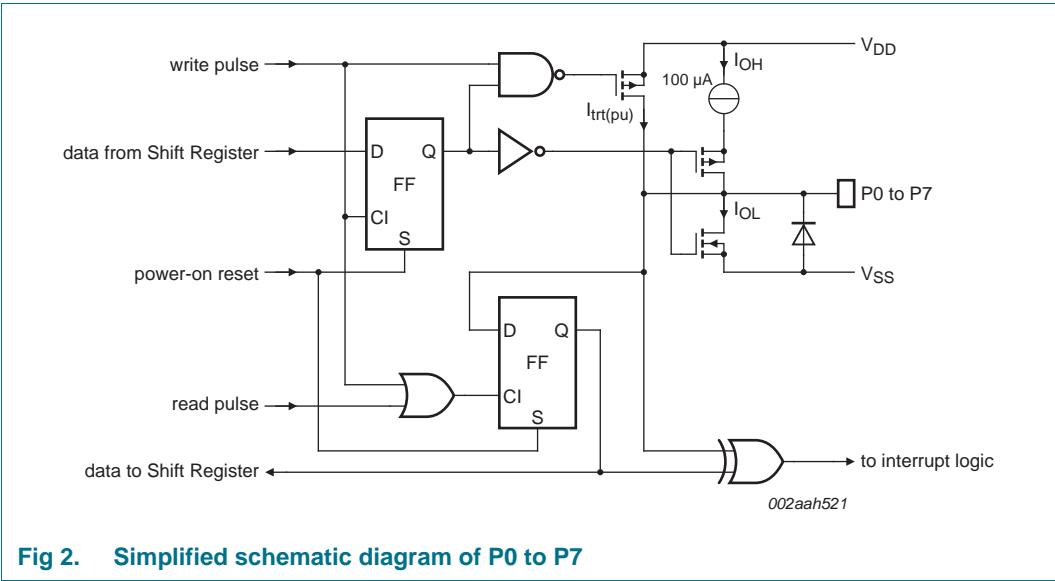
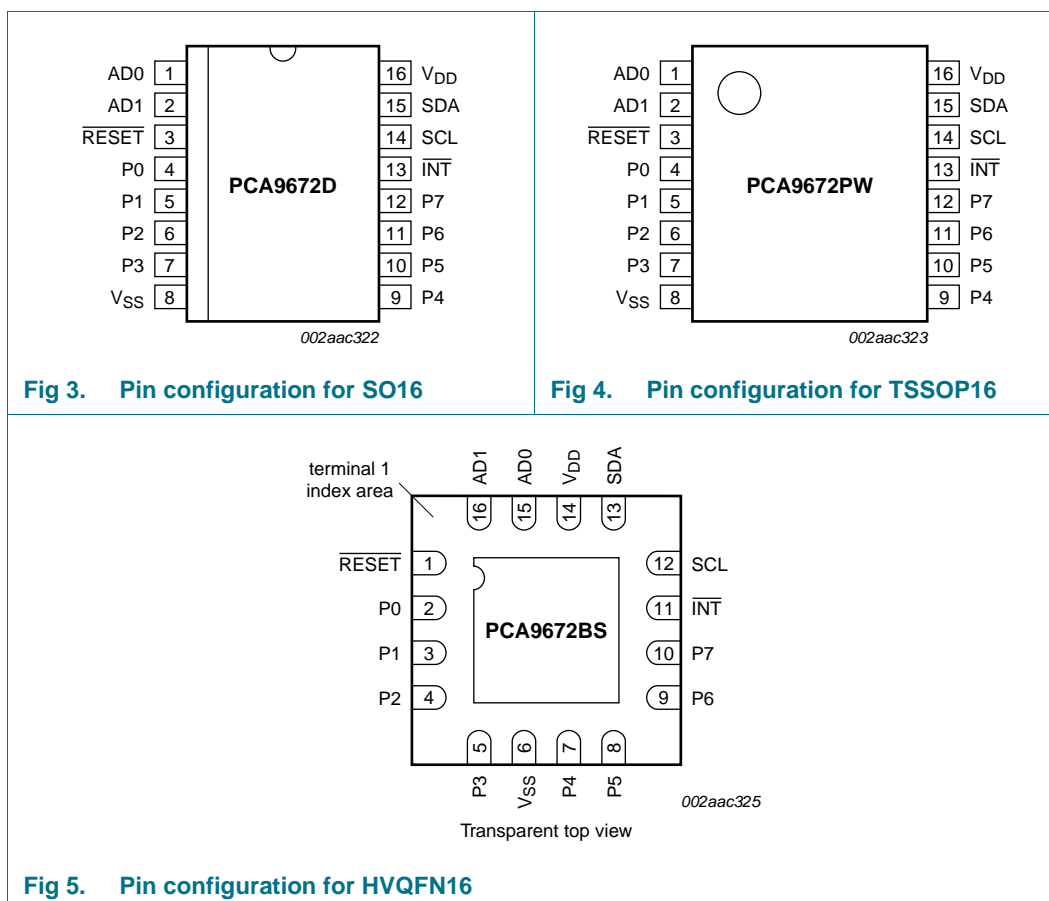


Fig 2. Simplified schematic diagram of P0 to P7

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
AD0	1	15	address input 0
AD1	2	16	address input 1
$\overline{\text{RESET}}$	3	1	reset input (active LOW)
P0	4	2	quasi-bidirectional I/O 0
P1	5	3	quasi-bidirectional I/O 1
P2	6	4	quasi-bidirectional I/O 2
P3	7	5	quasi-bidirectional I/O 3
V <sub>SS</sub>	8	6	supply ground
P4	9	7	quasi-bidirectional I/O 4
P5	10	8	quasi-bidirectional I/O 5
P6	11	9	quasi-bidirectional I/O 6

Table 3. Pin description ...continued

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
P7	12	10	quasi-bidirectional I/O 7
INT	13	11	interrupt output (active LOW)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V <sub>DD</sub>	16	14	supply voltage

- [1] HVQFN16 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCA9672”](#).

### 7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address format of the PCA9672 is shown in [Figure 6](#). Slave address pins AD1 and AD0 are used to choose one of 16 slave addresses. These devices can monitor the change in SDA or SCL in addition to the static levels of V<sub>DD</sub> or V<sub>SS</sub> to decode four states allowing a larger address range. To conserve power, no internal pull-up resistors are incorporated on AD1 or AD0, so they must be externally connected to V<sub>DD</sub>, V<sub>SS</sub> directly or through resistors, or to SCL or SDA directly. Address values depending on AD1 and AD0 can be found in [Table 4 “PCA9672 address map”](#).

**Remark:** When using the PCA9672 reserved I<sup>2</sup>C-bus addresses must be used with caution since they can interfere with:

- “reserved for future use” I<sup>2</sup>C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

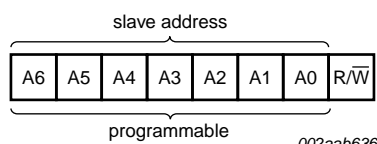


Fig 6. PCA9672 address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When AD1 and AD0 are held to V<sub>DD</sub> or V<sub>SS</sub>, the same address as the PCF8574 or the newer PCA8574 with A2 held to V<sub>SS</sub> is applied.

### 7.1.1 Address map

Table 4. PCA9672 address map

Pin connectivity		Address of PCA9672								Address byte value		7-bit hexadecimal address without R/W
AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
SCL	V <sub>SS</sub>	0	0	1	0	0	0	0	-	20h	21h	10h
SCL	V <sub>DD</sub>	0	0	1	0	0	0	1	-	22h	23h	11h
SDA	V <sub>SS</sub>	0	0	1	0	0	1	0	-	24h	25h	12h
SDA	V <sub>DD</sub>	0	0	1	0	0	1	1	-	26h	27h	13h
SCL	SCL	0	0	1	1	0	0	0	-	30h	31h	18h
SCL	SDA	0	0	1	1	0	0	1	-	32h	33h	19h
SDA	SCL	0	0	1	1	0	1	0	-	34h	35h	1Ah
SDA	SDA	0	0	1	1	0	1	1	-	36h	37h	1Bh
V <sub>SS</sub>	V <sub>SS</sub>	0	1	0	0	0	0	0	-	40h	41h	20h
V <sub>SS</sub>	V <sub>DD</sub>	0	1	0	0	0	0	1	-	42h	43h	21h
V <sub>DD</sub>	V <sub>SS</sub>	0	1	0	0	0	1	0	-	44h	45h	22h
V <sub>DD</sub>	V <sub>DD</sub>	0	1	0	0	0	1	1	-	46h	47h	23h
V <sub>SS</sub>	SCL	0	1	0	1	0	0	0	-	50h	51h	28h
V <sub>SS</sub>	SDA	0	1	0	1	0	0	1	-	52h	53h	29h
V <sub>DD</sub>	SCL	0	1	0	1	0	1	0	-	54h	55h	2Ah
V <sub>DD</sub>	SDA	0	1	0	1	0	1	1	-	56h	57h	2Bh

## 7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the PCA9672.

- General Call address: allows to reset the PCA9672 through the I<sup>2</sup>C-bus upon reception of the right I<sup>2</sup>C-bus sequence. See [Section 7.2.1 “Software Reset”](#) for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See [Section 7.2.2 “Device ID \(PCA9672 ID field\)”](#) for more information.

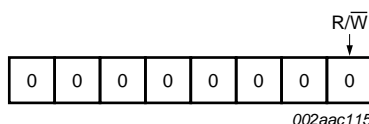


Fig 7. General Call address

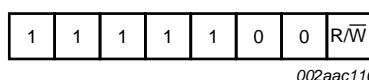


Fig 8. Device ID address

### 7.2.1 Software Reset

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

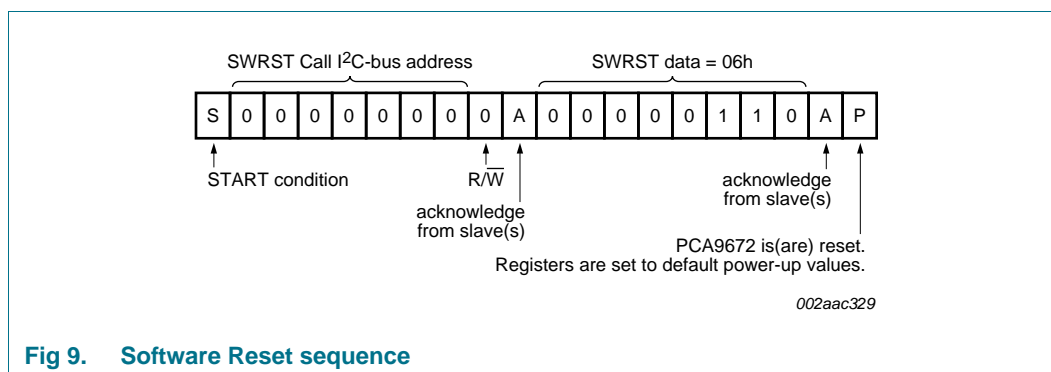
1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The PCA9672 device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
  - a. The PCA9672 acknowledges this value only. If the byte is not equal to 06h, the PCA9672 does not acknowledge it.

If more than 1 byte of data is sent, the PCA9672 does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9672 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the PCA9672 (at any time) as a 'Software Reset Abort'. The PCA9672 does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in [Figure 9](#).



Simple code for Software Reset:

<S> <00h> <ACK> <06h> <ACK> <P>

7.2.2 Device ID (PCA9672 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I<sup>2</sup>C-bus address ‘1111 100’ with the R/W bit set to 0 (write).
3. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
4. The master sends a Re-START command.

**Remark:** A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed.

**Remark:** A STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID read cannot be performed.

5. The master sends the Reserved Device ID I<sup>2</sup>C-bus address ‘1111 100’ with the R/W bit set to 1 (read).
6. The device ID read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits and then the 3 die revision bits (3 LSB of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

**Remark:** The reading of the Device ID can be stopped anytime by sending a NACK command.

**Remark:** If the master continues to ACK the bytes after the third byte, the PCA9672 rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9672, the Device ID is as shown in [Figure 10](#).

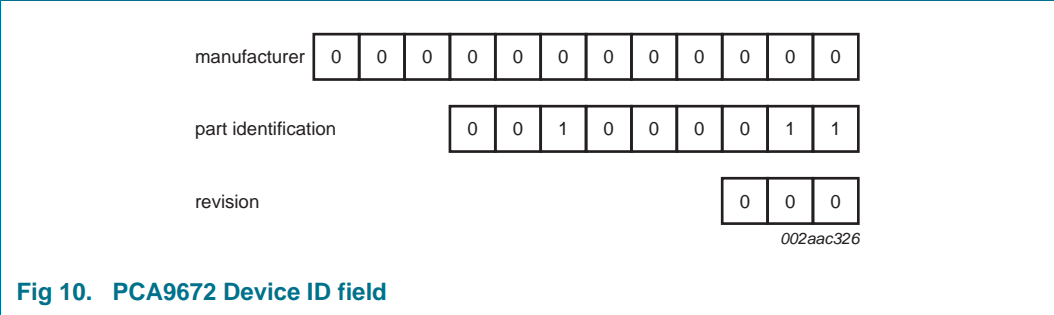
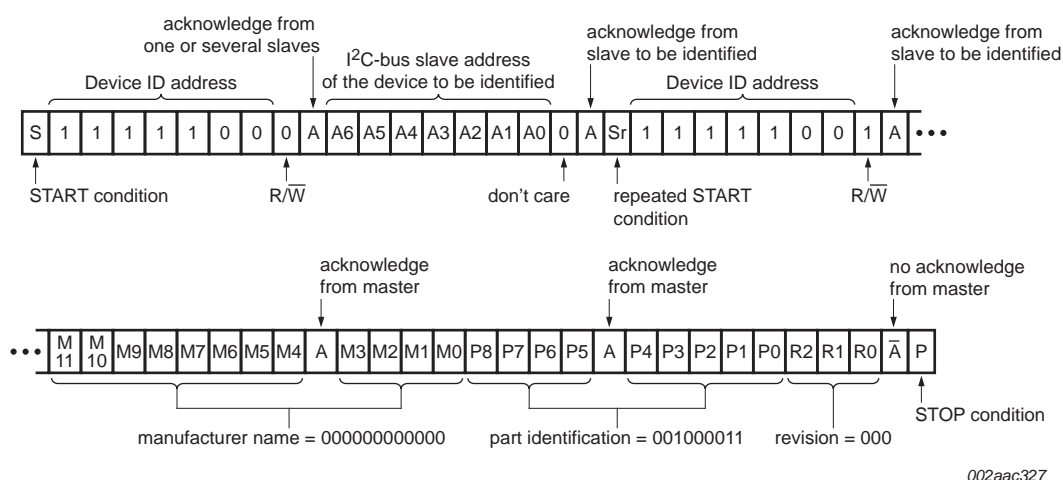


Fig 10. PCA9672 Device ID field





If more than 2 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 11. Device ID field reading PCA9672

Simple code for reading Device ID:

```
<S> <F8h> <ACK> <slave address> <ACK> <Sr> <F9h> <ACK> <DATA1>
<ACK> <DATA2> <ACK> <DATA3> <NACK> <P>
```

## 8. I/O programming

### 8.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power-on, all the ports are HIGH with a weak 100  $\mu$ A internal pull-up to  $V_{DD}$ , but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the p-channel (transistor to  $V_{DD}$ ) is small, which saves die size and therefore cost. LED drive only requires an internal transistor to ground, while the LED is connected to  $V_{DD}$  through a current-limiting resistor. Totem pole I/O have both n-channel and p-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor — good for logic levels.
- Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.
- Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

**Input HIGH:** The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to  $V_{DD}$  or drives logic 1, then the master will read the value of 1.

**Input LOW:** The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to  $V_{SS}$  or drives logic 0, which sinks the weak 100  $\mu A$  current source, then the master will read the value of 0.

**Output HIGH:** The master writes 1 to the register. There is an additional 'accelerator' or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port's 100  $\mu A$  current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to  $V_{SS}$ /driving the port with logic 0 at the same time. After the half clock cycle there is only the 100  $\mu A$  current source to hold the port HIGH.

**Output LOW:** The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

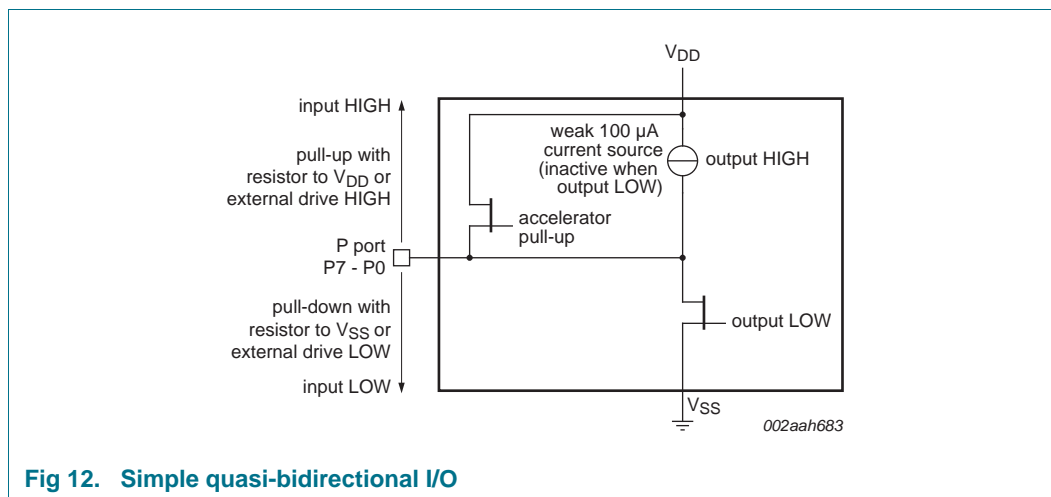
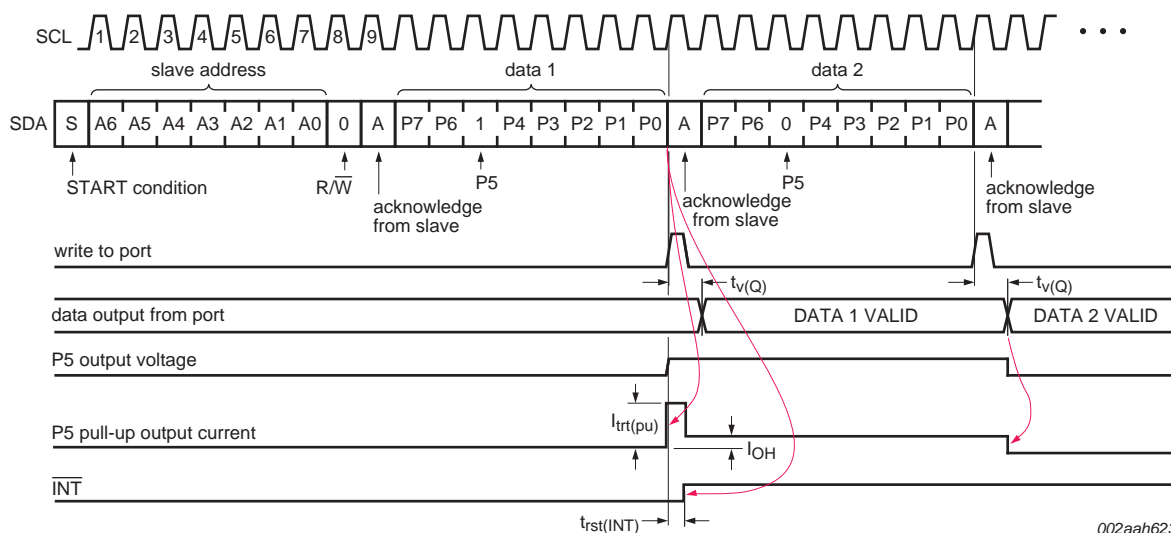


Fig 12. Simple quasi-bidirectional I/O

## 8.2 Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PCA9672 acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PCA9672. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for  $\frac{1}{2}$  of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.



002aah623

Fig 13. Write mode (output)

Simple code for Write cycle:

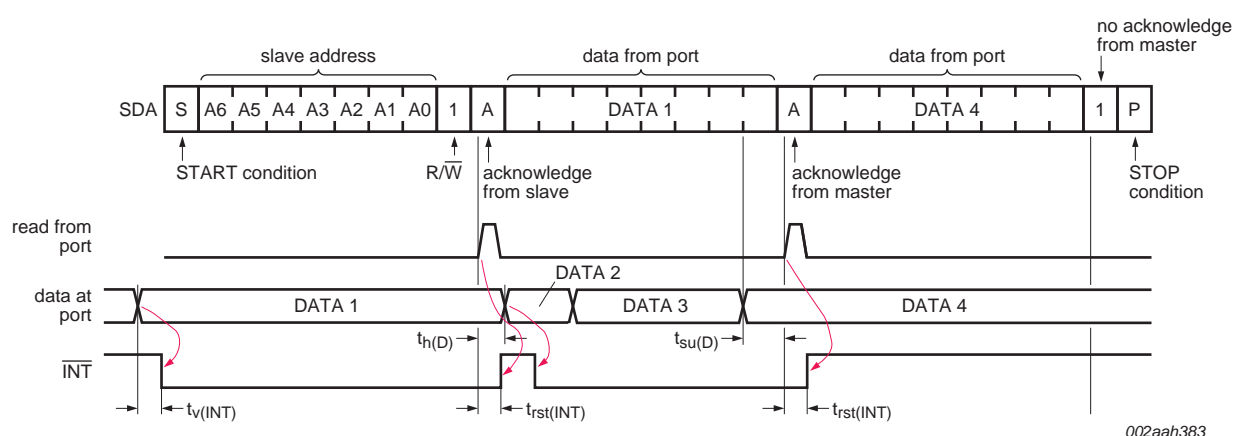
```
<S> <slave address + W> <ACK> <DATA1> <ACK> <DATA2> <ACK> <DATA1> ...  
<DATAAn> <ACK> <P>
```

### 8.3 Reading from a port (Input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset or hardware reset or software reset. To enter the Read mode, the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the input pin.

If the data on the input port changes faster than the master can read, this data may be lost. The DATA 2 and DATA 3 are lost because these data did not meet the set-up time and hold time (see Figure 14).



A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (Output mode). Input data is lost.

Fig 14. Read input port register

Simple code for Read cycle:

```
<S> <slave address + R> <ACK> <DATA in> <ACK> <DATA in> ... <NACK> <P>
```

### 8.4 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9672 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9672 registers and I<sup>2</sup>C-bus/SMBus state machine will initialize to their default states of all I/Os to inputs with weak current source to  $V_{DD}$ . Thereafter  $V_{DD}$  must be lowered below  $V_{POR}$  and back up to the operation voltage for power-on reset cycle.

## 8.5 Interrupt output ( $\overline{\text{INT}}$ )

The PCA9672 provides an open-drain output ( $\overline{\text{INT}}$ ) which can be fed to a corresponding input of the microcontroller (see [Figure 15](#)). As soon as a port input is changed, the  $\overline{\text{INT}}$  will be active (LOW) and notify the microcontroller.

An interrupt is generated at any rising or falling edge of the port inputs. After time  $t_{V(Q)}$ , the signal  $\overline{\text{INT}}$  is valid.

The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master.

In the Write mode, the interrupt may be reset (HIGH) on the rising edge of the acknowledge bit of the data byte and also on the rising edge of the write to port pulse. The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see [Figure 13](#)).

The interrupt is reset (HIGH) in the rising edge of the read from port pulse (see [Figure 14](#)).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an  $\overline{\text{INT}}$ .

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

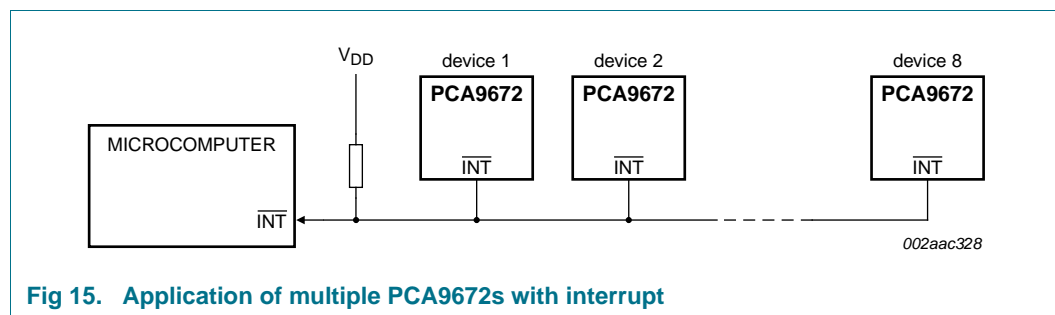


Fig 15. Application of multiple PCA9672s with interrupt

## 8.6 RESET input

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{W(\text{rst})}$ . The PCA9672 registers and I<sup>2</sup>C-bus state machine will be held in their default state until the  $\overline{\text{RESET}}$  input is once again HIGH. The  $\overline{\text{RESET}}$  input pin requires a pull-up resistor to  $V_{DD}$  if no active connection is used.

## 9. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 16](#)).

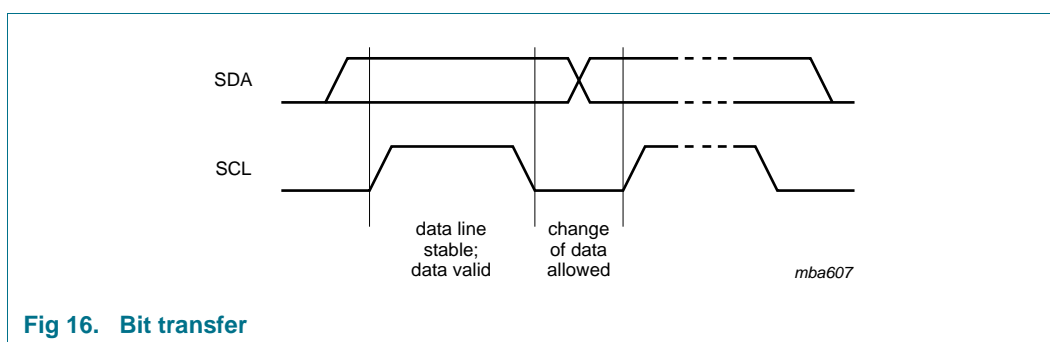


Fig 16. Bit transfer

#### 9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 17](#)).

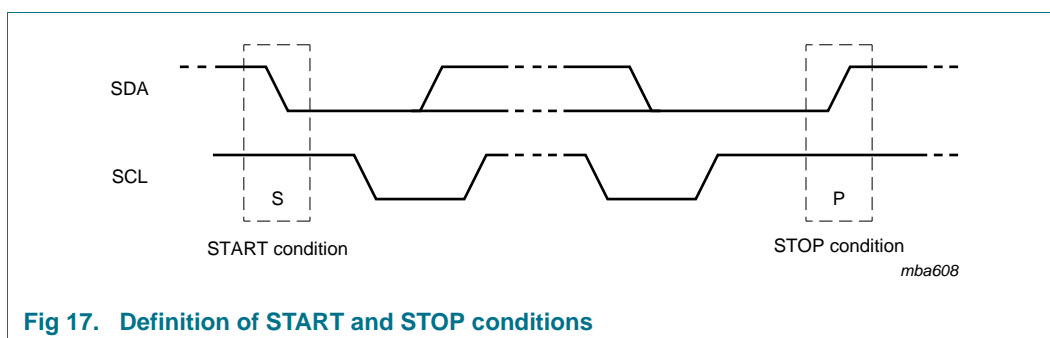


Fig 17. Definition of START and STOP conditions

### 9.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 18](#)).

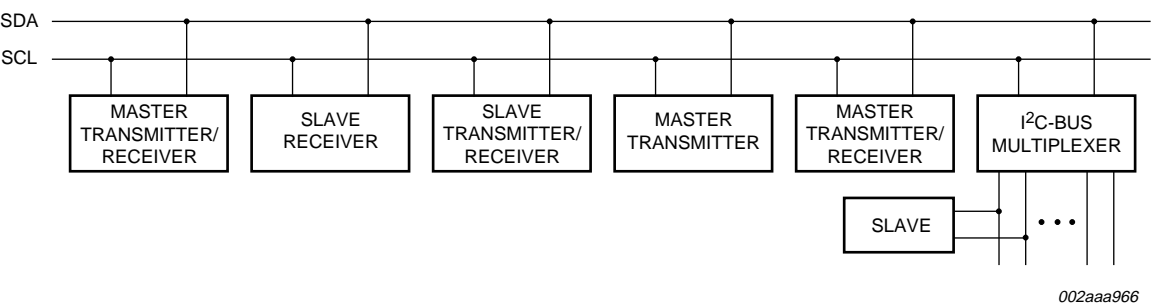


Fig 18. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is an active LOW level (generated by the receiving device) that indicates to the transmitter that the data transfer was successful.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that wants to issue an acknowledge bit has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge bit related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

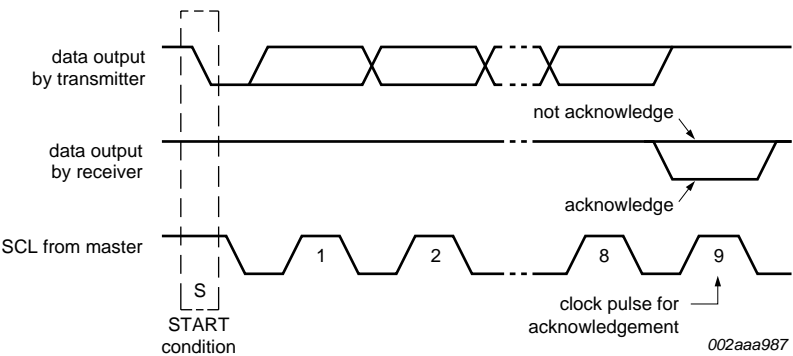


Fig 19. Acknowledgement on the I<sup>2</sup>C-bus

## 10. Application design-in information

### 10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in [Figure 20](#), P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, **the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports**. The desired HIGH or LOW logic levels may be written to the I/Os used as outputs (P2 to P7). If 10  $\mu$ A internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line ( $\overline{\text{INT}}$ ) that can be connected to the interrupt logic of the microprocessor. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there has been a change of data on its ports without having to communicate via the I<sup>2</sup>C-bus.

The GPIO also has a reset line ( $\overline{\text{RESET}}$ ) that can be connected to an output pin of the microcontroller.

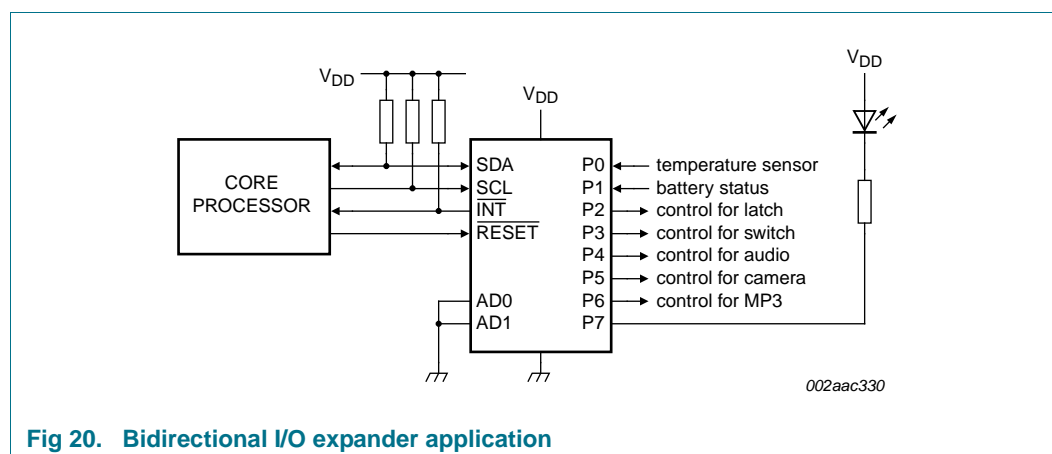


Fig 20. Bidirectional I/O expander application

### 10.2 How to read and write to I/O expander (example)

In the application example of PCA9672 shown in [Figure 20](#), the microcontroller wants to control the P3 switch ON and the P7 LED ON when the temperature sensor P0 changes.

1. When the system power on:

Core Processor needs to issue an initial command to set P0 and P1 as inputs and P[7:2] as outputs with value 1010 00 (LED off, MP3 off, camera on, audio off, switch off and latch off).

2. Operation:

When the temperature changes above the threshold, the temperature sensor signal will toggle from HIGH to LOW. The  $\overline{\text{INT}}$  will be activated and notifies the 'core processor', that there have been changes on the input pins. Read the input register. If P0 = 0 (temperature sensor has changed), then turn on LED and turn on switch.



## 3. Software code:

```
//System Power on
// write to PCA9672 with data 1010 0011b to set P[7:2] outputs and P[1:0] inputs
<S> <0100 0000> <ACK> <1010 0011> <ACK> <P> //Initial setting for PCA9672
while (INT == 1); //Monitor the interrupt pin. If INT = 1 do nothing
//When INT = 0 then read input ports
<S> <slave address read> <ACK> <1010 0010> <NACK> <P> //Read PCA9672 data
If (P0 == 0) //Temperature sensor activated
{
// write to PCA9672 with data 0010 1011b to turn on LED (P7), on Switch (P3)
and keep P[1:0] as input ports.
<S> <0100 0000> <ACK> <0010 1011> <ACK> <P> // Write to PCA9672
}
```

## 10.3 High current-drive load applications

The GPIO has a minimum guaranteed sinking current of 25 mA per bit at 5 V. In applications requiring additional drive, two port pins may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins can be connected together to drive 200 mA, which is the device recommended total limit. Each pin needs its own limiting resistor as shown in [Figure 21](#) to prevent damage to the device should all ports not be turned on at the same time.

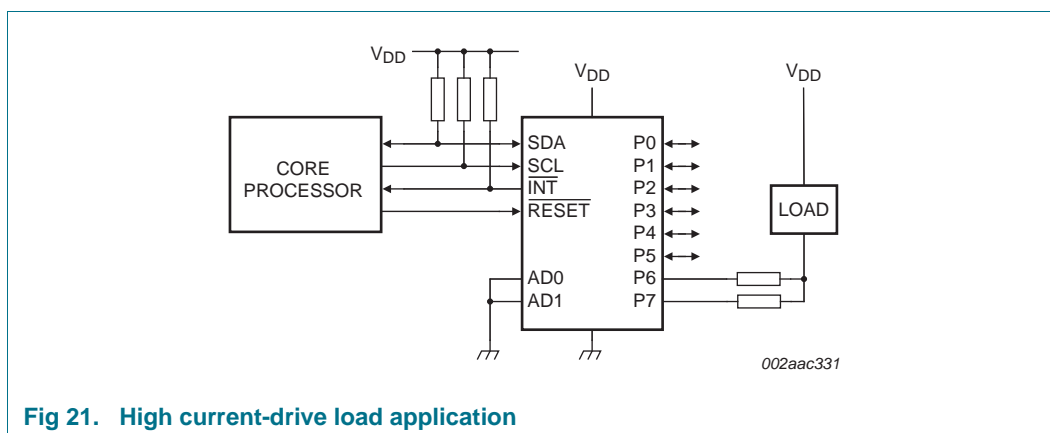


Fig 21. High current-drive load application

## 10.4 Migration path

NXP offers newer, more capable drop-in replacements for the PCF8574/74A in newer space-saving packages.

Table 5. Migration path

Type number	I <sup>2</sup> C-bus frequency	Voltage range	Number of addresses per device	Interrupt	Reset	Total package sink current
PCF8574/74A	100 kHz	2.5 V to 6 V	8	yes	no	80 mA
PCA8574/74A	400 kHz	2.3 V to 5.5 V	8	yes	no	200 mA
PCA9674/74A	1 MHz Fm+	2.3 V to 5.5 V	64	yes	no	200 mA
PCA9670	1 MHz Fm+	2.3 V to 5.5 V	64	no	yes	200 mA
PCA9672	1 MHz Fm+	2.3 V to 5.5 V	16	yes	yes	200 mA

PCA9670 replaces the interrupt output of the PCA9674 with hardware reset input to retain the maximum number of addresses. The PCA9672 replaces address A2 of the PCA9674 with hardware reset input to retain the interrupt, but limit the number of addresses.

## 11. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		−0.5	+6	V
I <sub>DD</sub>	supply current		-	±100	mA
I <sub>SS</sub>	ground supply current		-	±400	mA
V <sub>I</sub>	input voltage		V <sub>SS</sub> − 0.5	5.5	V
I <sub>I</sub>	input current		-	±20	mA
I <sub>O</sub>	output current	[1]	-	±50	mA
P <sub>tot</sub>	total power dissipation		-	400	mW
P <sub>out</sub>	power dissipation per output		-	100	mW
T <sub>j(max)</sub>	maximum junction temperature		-	125	°C
T <sub>stg</sub>	storage temperature		−65	+150	°C
T <sub>amb</sub>	ambient temperature	operating	−40	+85	°C

[1] Total package (maximum) output current is 400 mA.

## 12. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	SO16 package	115	°C/W
		TSSOP16 package	160	°C/W
		HVQFN16 package	40	°C/W

### 13. Static characteristics

**Table 8. Static characteristics**

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		2.3	-	5.5	V
$I_{DD}$	supply current	Operating mode; no load; $V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 1\text{ MHz}$ ; AD0, AD1 = static H or L	-	260	500	$\mu\text{A}$
$I_{stb}$	standby current	Standby mode; no load; $V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 0\text{ kHz}$	-	2.5	10	$\mu\text{A}$
$V_{POR}$	power-on reset voltage		[1] -	1.8	2.0	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 2.3\text{ V}$	20	-	-	mA
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 3.0\text{ V}$	25	-	-	mA
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 4.5\text{ V}$	30	-	-	mA
$I_L$	leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	4	10	pF
<b>I/Os; P0 to P7</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 2.3\text{ V}$	[2] 12	28	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 3.0\text{ V}$	[2] 17	35	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 4.5\text{ V}$	[2] 25	43	-	mA
$I_{OL(tot)}$	total LOW-level output current	$V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 4.5\text{ V}$	[2] -	-	200	mA
$I_{OH}$	HIGH-level output current	$V_{OH} = V_{SS}$	-30	-250	-300	$\mu\text{A}$
$I_{trt(pu)}$	transient boosted pull-up current	$V_{OH} = V_{SS}$ ; see <a href="#">Figure 13</a>	-0.5	-1.0	-	mA
$C_i$	input capacitance		[3] -	3	10	pF
$C_o$	output capacitance		[3] -	3	10	pF
<b>Input RESET</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2	-	5.5	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	3	5	pF
<b>Interrupt INT (see <a href="#">Figure 13</a> and <a href="#">Figure 14</a>)</b>						
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3.0	-	-	mA
$C_o$	output capacitance		-	2	5	pF

**Table 8.** Static characteristics ...continued $V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Inputs AD0, AD1</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	3	5	pF

[1] The power-on reset circuit resets the I<sup>2</sup>C-bus logic with  $V_{DD} < V_{POR}$  and set all I/Os to logic 1 (with current source to  $V_{DD}$ ).

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.

[3] The value is not tested, but verified on sampling basis.

## 14. Dynamic characteristics

**Table 9.** Dynamic characteristics $V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Fast mode Plus I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	0	1000	kHz
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	$\mu\text{s}$
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	$\mu\text{s}$
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	$\mu\text{s}$
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	$\mu\text{s}$
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	$\mu\text{s}$
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	50	450	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
$t_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals	[4][5]	-	300	$20 + 0.1C_b$ [3]	300	-	120	ns
$t_r$	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	-	120	ns
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns

**Table 9. Dynamic characteristics ...continued** $V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Fast mode Plus I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	Min	Max	

**Port timing;  $C_L \leq 100 \text{ pF}$  (see Figure 13 and Figure 14)**

$t_{V(Q)}$	data output valid time		-	4	-	4	-	4	$\mu\text{s}$
$t_{SU(D)}$	data input set-up time		0	-	0	-	0	-	$\mu\text{s}$
$t_{H(D)}$	data input hold time		4	-	4	-	4	-	$\mu\text{s}$

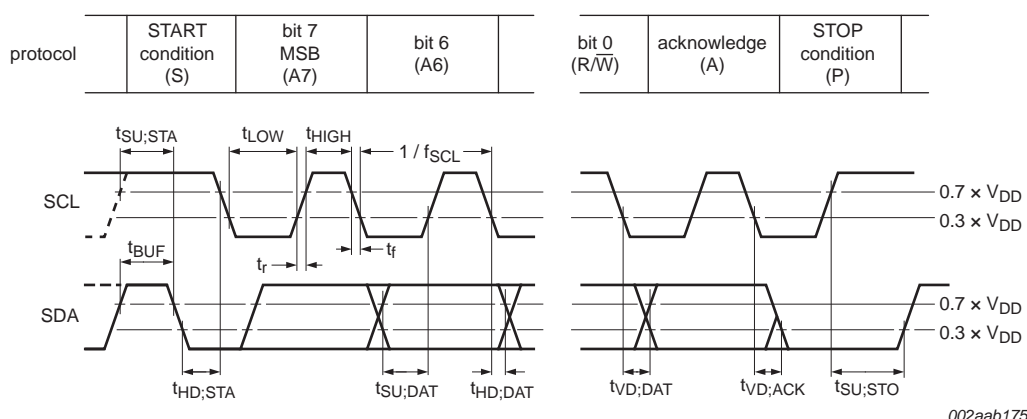
**Interrupt timing;  $C_L \leq 100 \text{ pF}$  (see Figure 13 and Figure 14)**

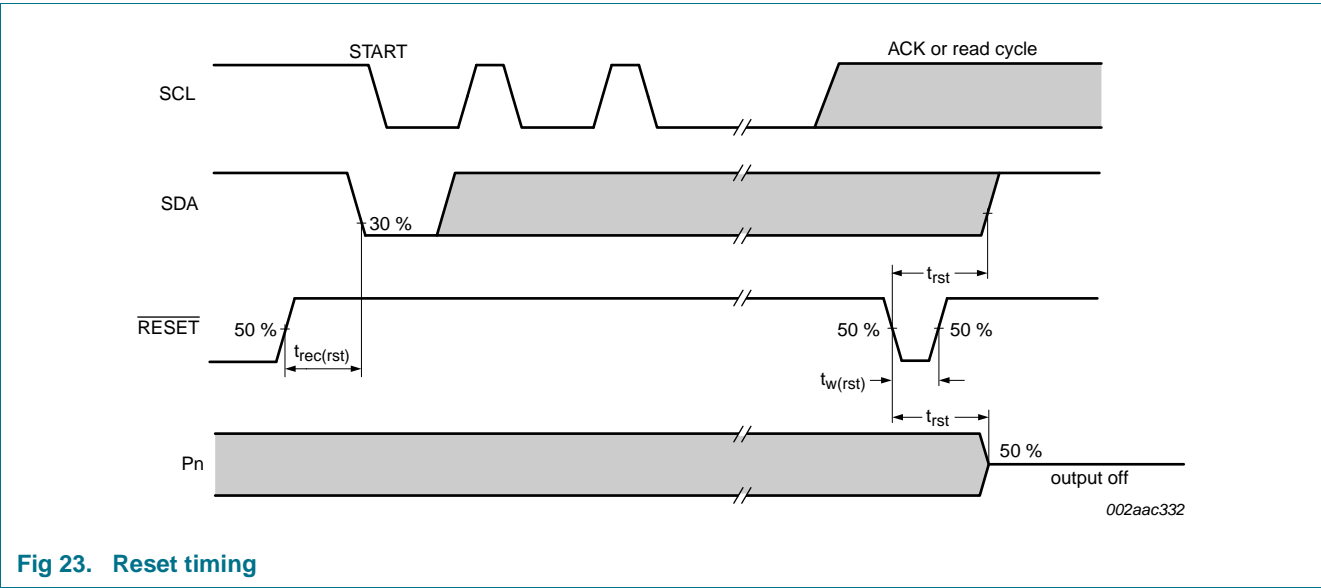
$t_{V(INT)}$	valid time on pin $\overline{INT}$	from port to $\overline{INT}$	-	4	-	4	-	4	$\mu\text{s}$
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	4	-	4	-	4	$\mu\text{s}$

**Reset timing (see Figure 23)**

$t_{W(rst)}$	reset pulse width		4	-	4	-	4	-	$\mu\text{s}$
$t_{rec(rst)}$	reset recovery time		0	-	0	-	0	-	$\mu\text{s}$
$t_{rst}$	reset time		100	-	100	-	100	-	$\mu\text{s}$

- [1]  $t_{VD,ACK}$  = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
- [2]  $t_{VD,DAT}$  = minimum time for SDA data out to be valid following SCL LOW.
- [3]  $C_b$  = total capacitance of one bus line in pF.
- [4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the  $V_{IL}$  of the SCL signal) in order to bridge the undefined region SCL's falling edge.
- [5] The maximum  $t_f$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage  $t_f$  is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- [6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .**Fig 22. I<sup>2</sup>C-bus timing diagram**



15. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads;  
 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

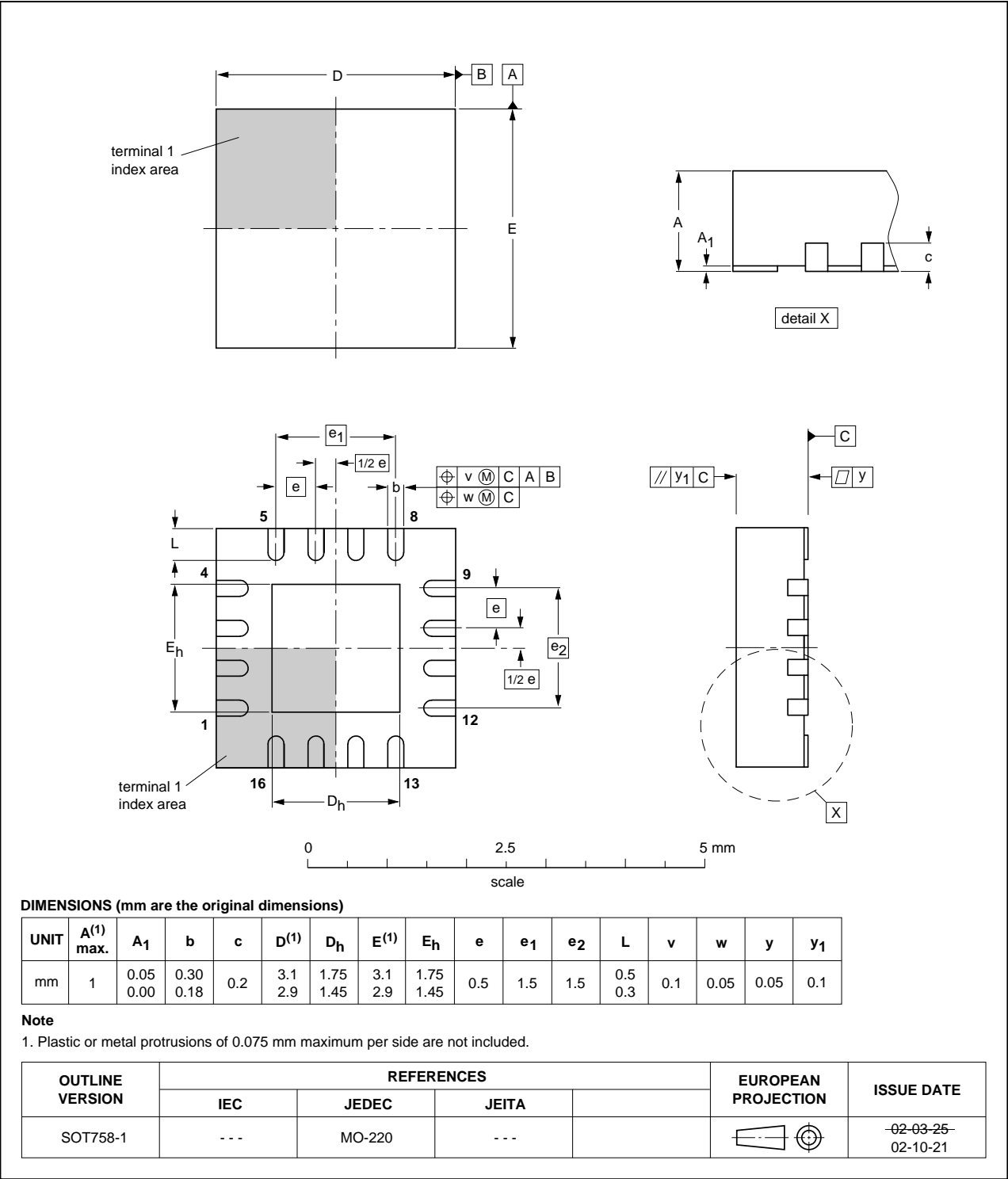


Fig 24. Package outline SOT758-1 (HVQFN16)

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

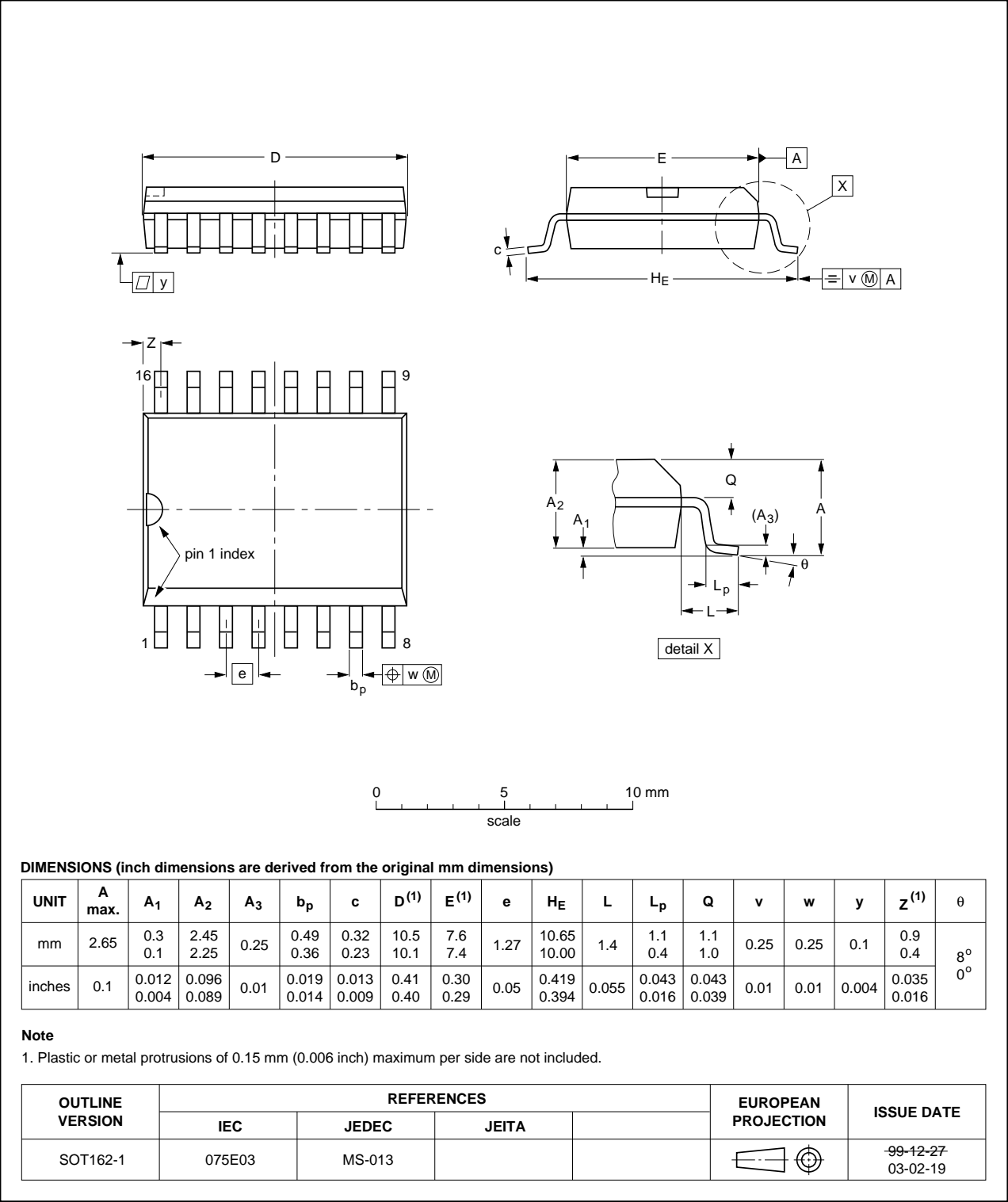


Fig 25. Package outline SOT162-1 (SO16)



TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

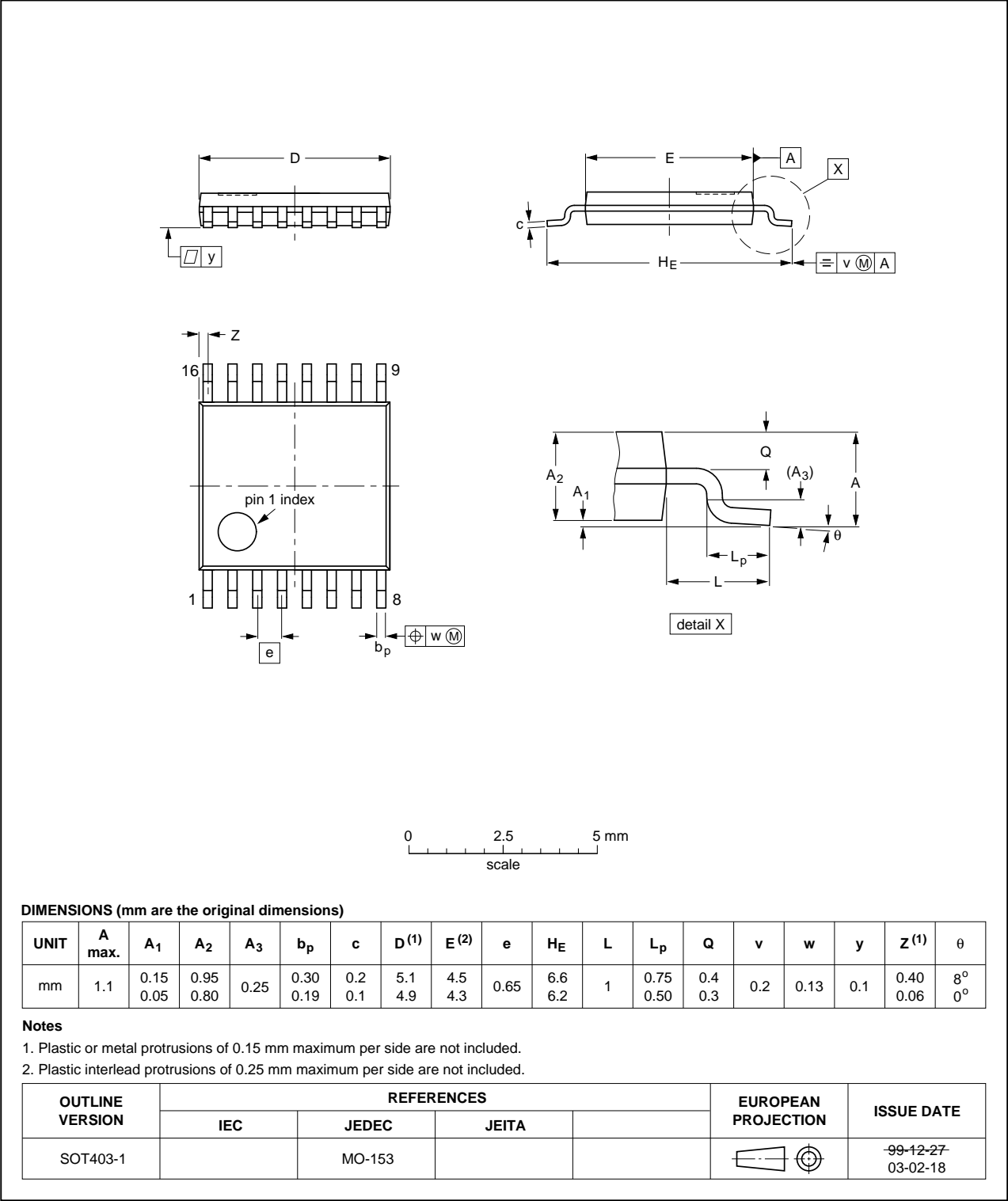


Fig 26. Package outline SOT403-1 (TSSOP16)

## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 27](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

**Table 10. SnPb eutectic process (from J-STD-020D)**

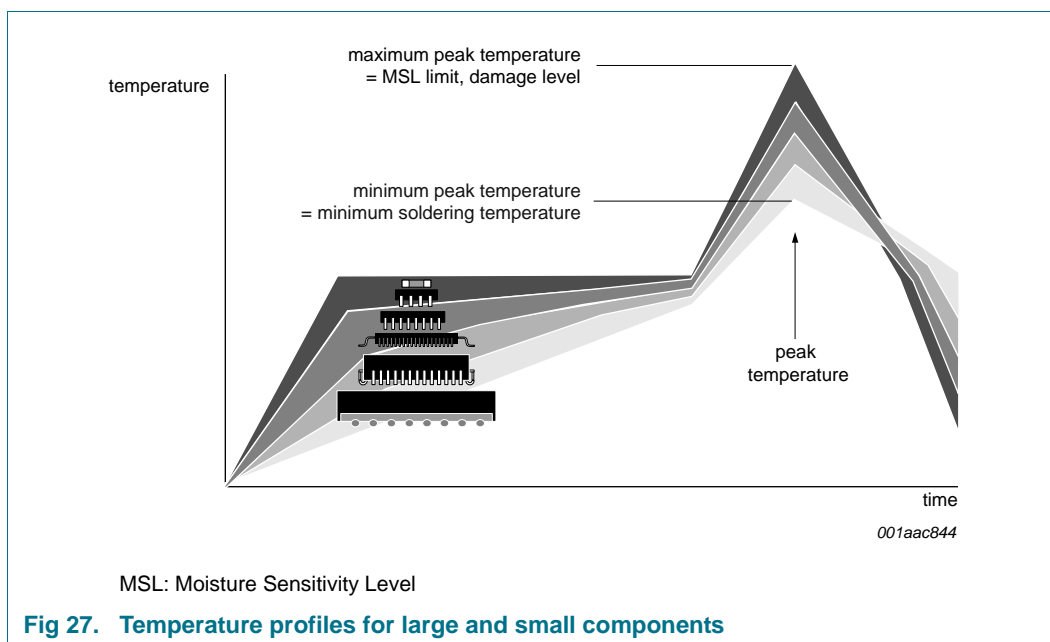
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 11. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 27](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

18. Soldering: PCB footprints

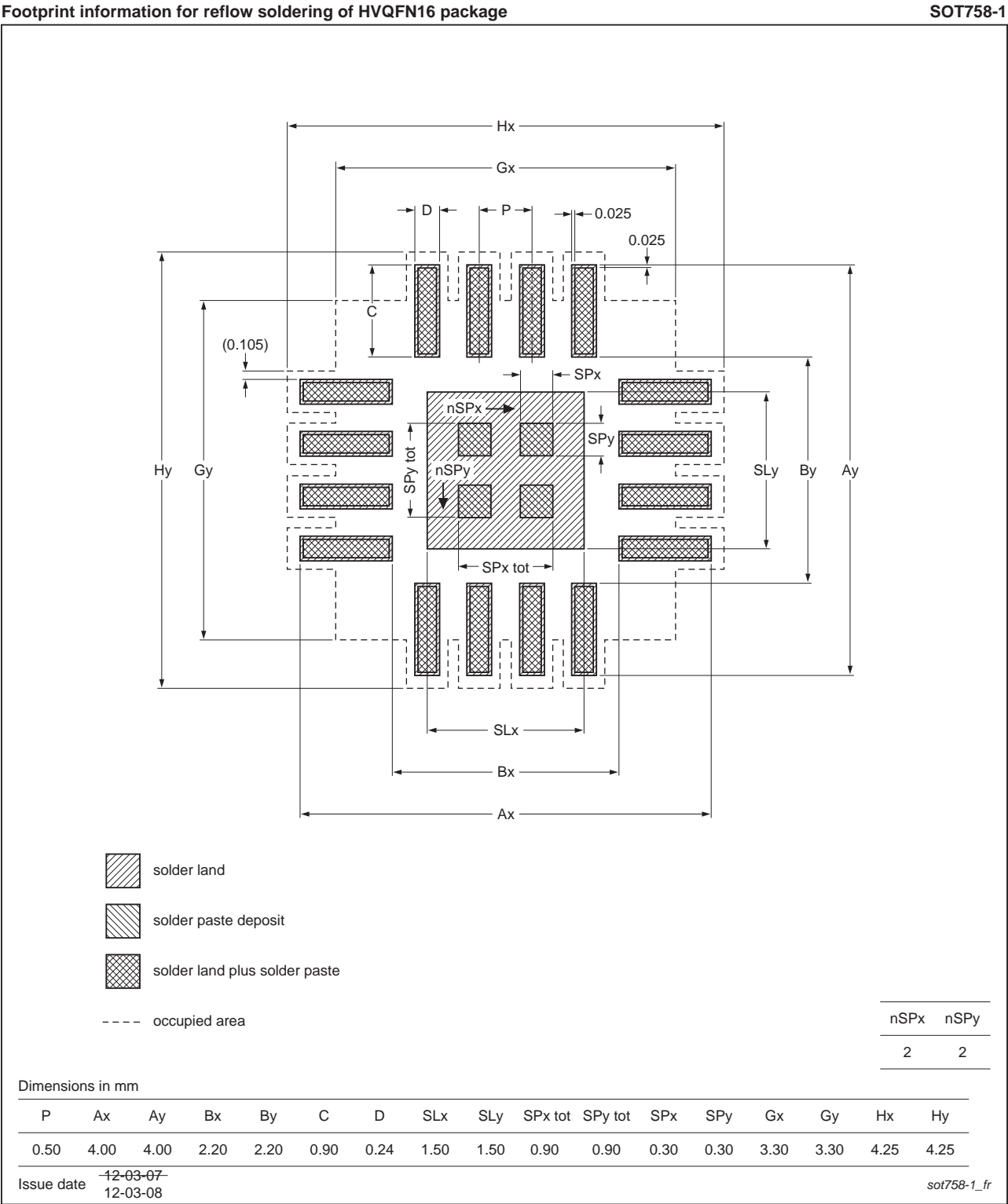


Fig 28. PCB footprint for SOT758-1 (HVQFN16); reflow soldering

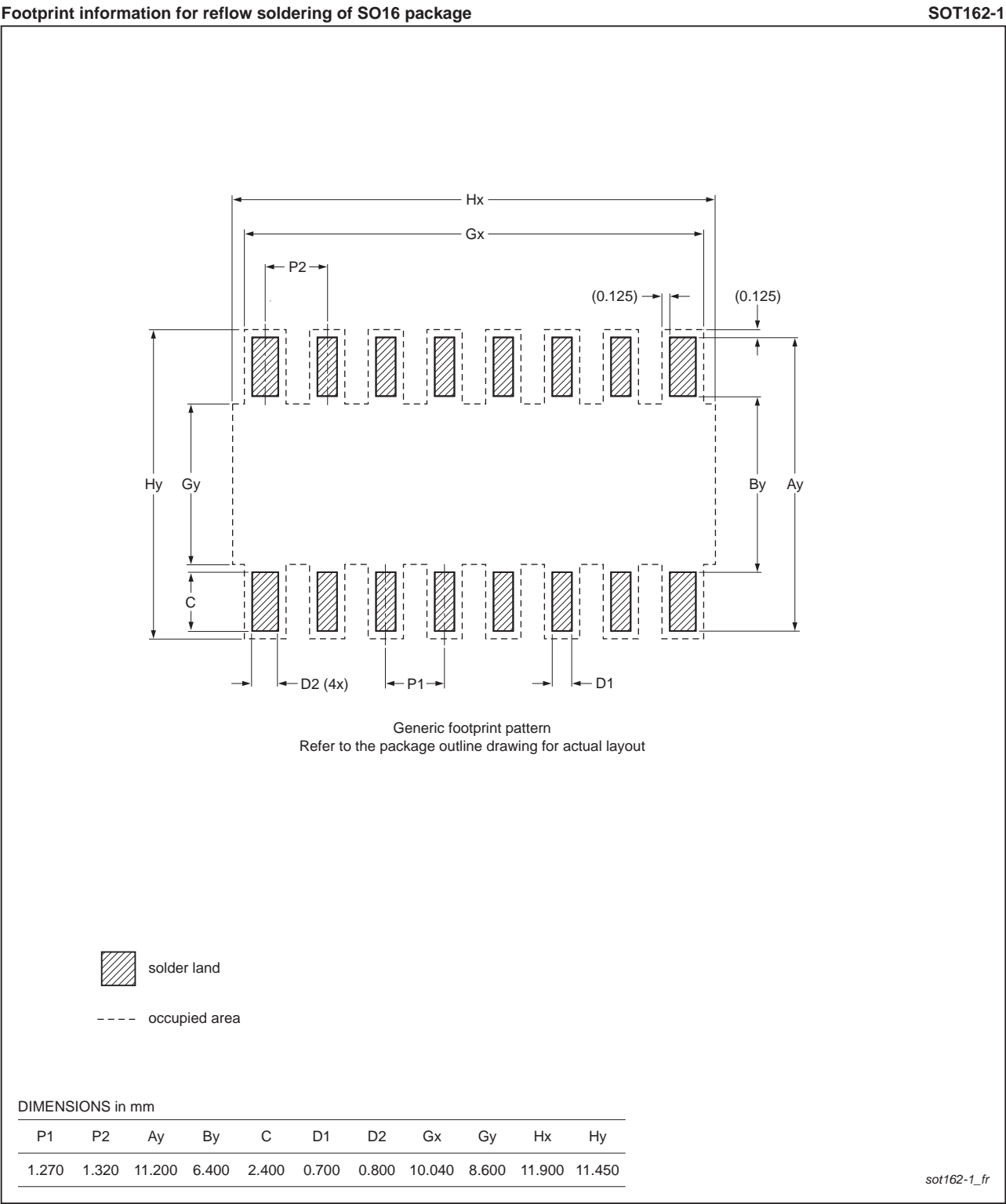


Fig 29. PCB footprint for SOT162-1 (SO16); reflow soldering

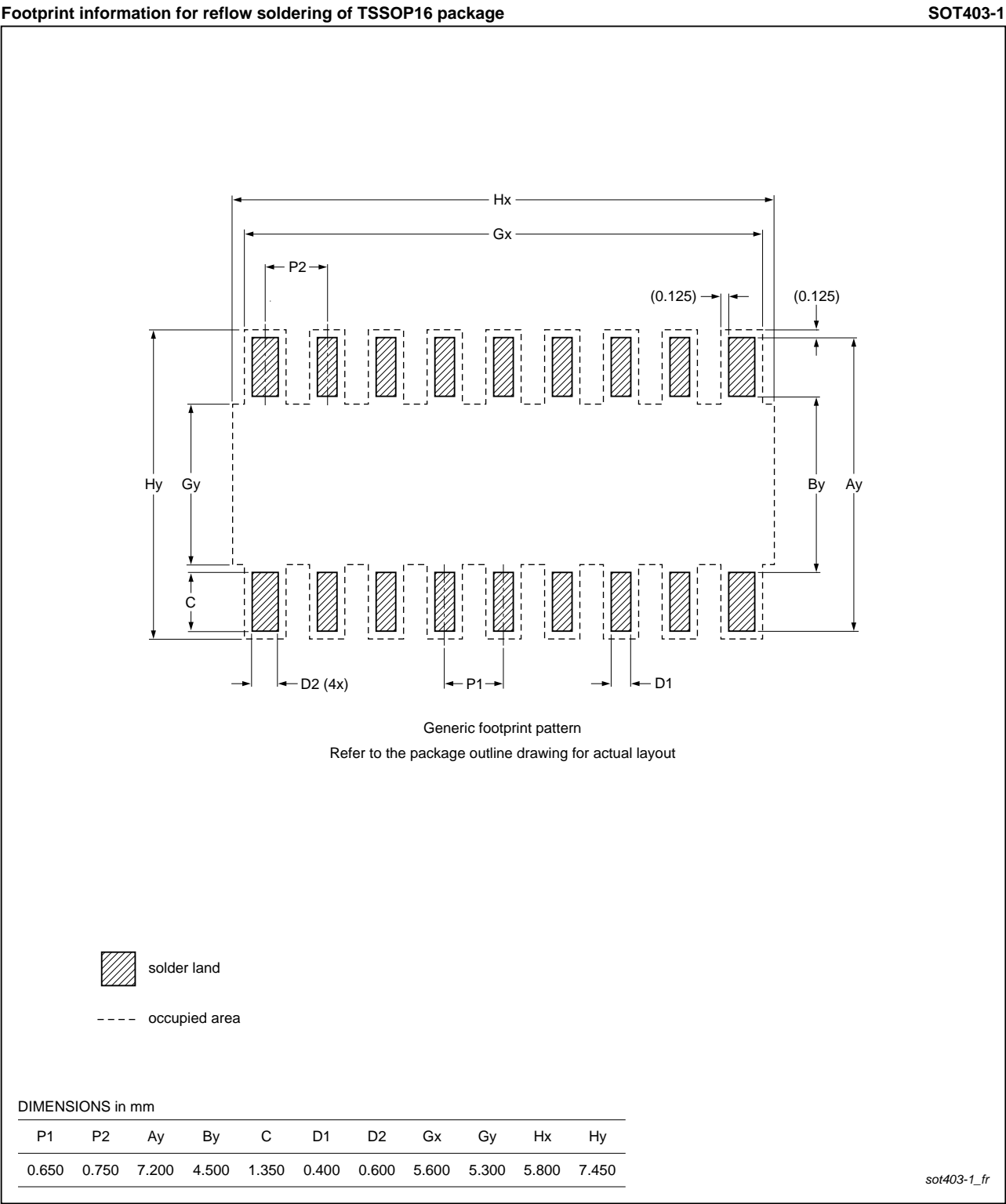


Fig 30. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

## 19. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
LED	Light Emitting Diode
IC	Integrated Circuit
I <sup>2</sup> C-bus	Inter IC bus
ID	Identification
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PLC	Programmable Logic Controller
PWM	Pulse Width Modulation
RAID	Redundant Array of Independent Disks

## 20. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9672 v.3	20130527	Product data sheet	-	PCA9672 v.2

Modifications:

- [Section 1 “General description”](#) re-written
- [Section 2 “Features and benefits”](#) re-written
- [Section 3 “Applications”](#):
  - added (new) third bullet item “Keypads”
  - added (new) eighth bullet item “Mobile devices”
- Added [Section 4.1 “Ordering options”](#)
- [Figure 1 “Block diagram of PCA9672”](#) modified: switched positions of blocks “INTERRUPT LOGIC” and “LP FILTER”
- [Figure 2 “Simplified schematic diagram of P0 to P7”](#) modified: removed diode between “V<sub>DD</sub>” and “P0 to P7” signals
- [Section 7.1 “Device address”](#):
  - first paragraph re-written
  - fourth paragraph: inserted phrase “or the newer PCA8574”
- [Section 7.2.1 “Software Reset”](#): added paragraph following [Figure 9](#)



Table 13. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications: (continued)	<ul style="list-style-type: none"> <li>• <a href="#">Section 7.2.2 “Device ID (PCA9672 ID field)”</a>: <ul style="list-style-type: none"> <li>– first bullet item following first paragraph changed from “8 bits with the manufacturer name” to “12 bits with the manufacturer name”</li> <li>– second bullet item following first paragraph re-written</li> <li>– <a href="#">List item 6. on page 8</a> changed from “starting with the 8 manufacturer bits ... , followed by the 13 part identification bits” to “starting with the 12 manufacturer bits ... , followed by the 9 part identification bits”</li> <li>– <a href="#">Figure 10 “PCA9672 Device ID field”</a> updated</li> <li>– <a href="#">Figure 11</a> modified: added “Sr” bit (ReSTART condition)</li> <li>– added paragraph following <a href="#">Figure 11</a></li> </ul> </li> <li>• <a href="#">Section 8.1 “Quasi-bidirectional I/Os”</a> re-written</li> <li>• <a href="#">Section 8.2 “Writing to the port (Output mode)”</a> re-written</li> <li>• <a href="#">Section 8.3 “Reading from a port (Input mode)”</a> re-written</li> <li>• <a href="#">Section 8.4 “Power-on reset”</a>: second and third sentences re-written</li> <li>• <a href="#">Section 8.5 “Interrupt output (INT)”</a>: fourth, fifth and sixth paragraphs re-written; added (new) seventh paragraph</li> <li>• <a href="#">Section 8.6 “RESET input”</a>: added (new) third sentence</li> <li>• <a href="#">Section 9.3 “Acknowledge”</a>: <ul style="list-style-type: none"> <li>– first paragraph, third sentence re-written</li> <li>– second paragraph, third sentence re-written</li> </ul> </li> <li>• <a href="#">Section 10.1 “Bidirectional I/O expander applications”</a>: <ul style="list-style-type: none"> <li>– second paragraph: second sentence changed from “there is incoming data or a change of data” to “there has been a change of data”</li> <li>– added (new) third paragraph</li> </ul> </li> <li>• Added <a href="#">Section 10.2 “How to read and write to I/O expander (example)”</a></li> <li>• <a href="#">Section 10.3 “High current-drive load applications”</a>: <ul style="list-style-type: none"> <li>– first sentence changed from “maximum sinking current of 25 mA per bit” to “minimum guaranteed sinking current of 25 mA per bit at 5 V”</li> <li>– deleted phrase “in the same octal” from second sentence</li> <li>– appended phrase “which is the device recommended total limit” to fourth sentence</li> <li>– added (new) fifth sentence</li> <li>– <a href="#">Figure 21 “High current-drive load application”</a> modified: added resistors on P6 and P7 signals</li> </ul> </li> <li>• Added <a href="#">Section 10.4 “Migration path”</a></li> <li>• <a href="#">Table 6 “Limiting values”</a>: added <math>T_{j(max)}</math> limits</li> <li>• Added <a href="#">Section 12 “Thermal characteristics”</a></li> <li>• <a href="#">Table 8 “Static characteristics”</a>: <ul style="list-style-type: none"> <li>– sub-section “I/Os; P0 to P7”: added <math>V_{IL}</math> characteristic</li> <li>– sub-section “I/Os; P0 to P7”: added <math>V_{IH}</math> characteristic</li> <li>– sub-section “Input RESET” is corrected by removing <math>I_{OH}</math> row</li> </ul> </li> <li>• <a href="#">Table 9 “Dynamic characteristics”</a>, sub-section “Interrupt timing”: <ul style="list-style-type: none"> <li>– symbol/parameter changed from “<math>t_{v(D)}</math>, data input valid time” to “<math>t_{v(INT)}</math>, valid time on pin <math>\overline{INT}</math>”</li> <li>– symbol/parameter changed from “<math>t_{d(rst)}</math>, reset delay time” to “<math>t_{rst(INT)}</math>, reset time on pin <math>\overline{INT}</math>”</li> </ul> </li> <li>• Added <a href="#">Section 18 “Soldering: PCB footprints”</a></li> </ul>			
PCA9672 v.2	20070706	Product data sheet	-	PCA9672 v.1
PCA9672 v.1	20060620	Objective data sheet	-	-

## 21. Legal information

### 21.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 27 May 2013

Document identifier: PCA9672