Freescale Semiconductor, Inc.
Data Sheet

Document Number: MC9S08SG32
Rev. 9, 04/2015

# MC9S08SG32 with Addenda Covers: MC9S08SG32 and MC9S08SG16

Rev. 9 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16) has three parts:

- The revision 2 addendum to revision 8.1 of the data sheet, immediately following this cover page.
- The revision 1 addendum to revision 8 of the data sheet.
- Revision 8 of the data sheet, following the addendums. The changes described in the addendums have not been implemented in the specified pages.

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Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08SG32AD
Rev. 2, 04/2015

# Addendum to Rev. 8.1 of the MC9S08SG32 Covers: MC9S08SG32 and MC9S08SG16

This addendum identifies changes to Rev. 8.1 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16). The changes described in this addendum have not been implemented in the specified pages.

## 1 Update to the "Nonvolatile Register Summary" table for NVFTRIM and NVOPT

| Location: | Table 4-4. Nonvolatile Register Summary, Page 47 |
|---|---|

For the NVFTRIM and NVOPT registers in Table 4-4, "Nonvolatile Register Summary," all reserved bits should be marked as "—" (not "0").

## 2 Update to the "Instruction Set Summary" table for BRA and BRN

| Location: | Table 7-2. Instruction Set Summary (Sheet 3 of 9), Page 106 |
|---|---|

In Table 7-2, "Instruction Set Summary," remove "(if I = 1)" from the BRA instruction and remove "(if I = 0)" from the BRN instruction. The BRA and BRN instructions do not depend on the I bit.

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# MC9S08SG32 DataSheet Addendum

by: Microcontroller Solutions Group

This is the MC9S08SG32 DataSheet set consisting of the following files:

- MC9S08SG32 DataSheet Addendum, Rev 1
- MC9S08SG32 DataSheet, Rev 8

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**Freescale Semiconductor**
Addendum

MC9S08SG32AD
Rev. 1, 02/2012

# MC9S08SG32 Data Sheet Addendum

by: Microcontroller Solutions Group

This errata document describes updates to the *MC9S08SG32 Data Sheet*, order number MC9S08SG32. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

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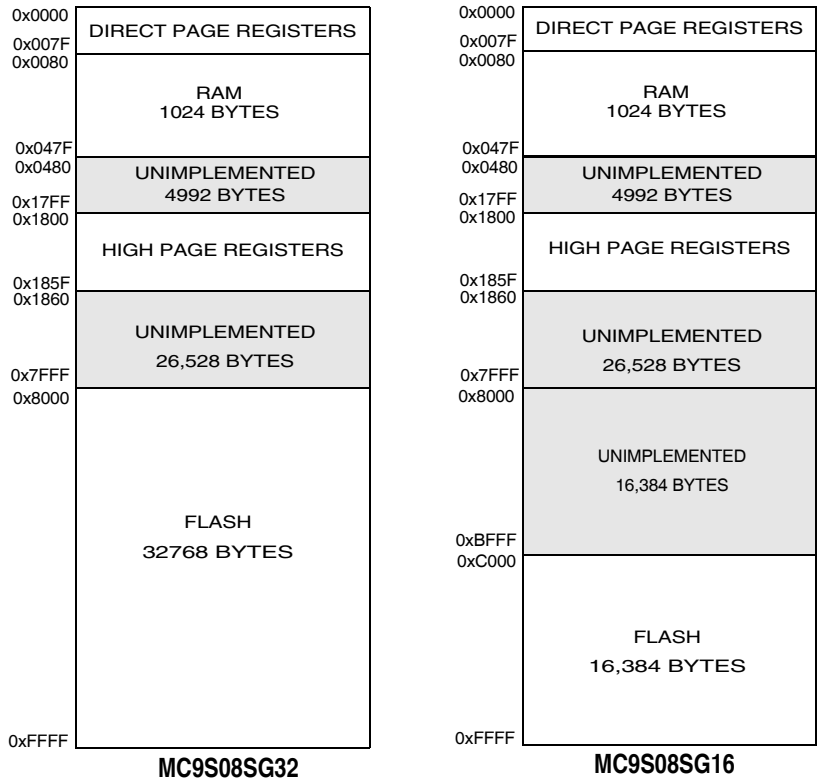
# 1 Addendum for Revision 8.0

**Table 1. MC9S08SG32 Rev. 1 Addendum**

| Location | Description |
|---|---|
| Chapter “Memory”/ Section “MC9S08SG32 Series Memory Map”/Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map/Page 39 | In Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map for device MC9S08SG16 change the value of “Unimplemented Bytes” from “26,538” to “26,528”.   |

## Table 1. MC9S08SG32 Rev. 1 Addendum

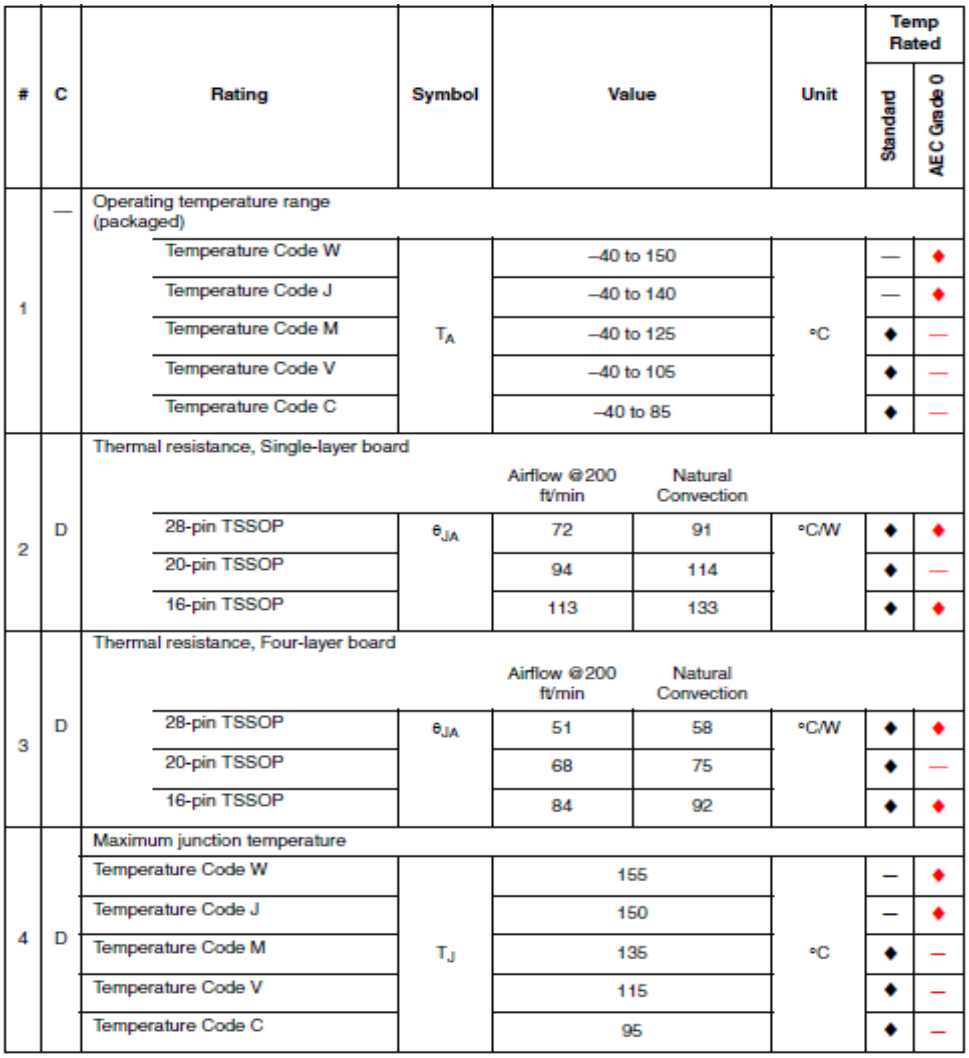
<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Chapter “Electrical Characteristics”/Section “Thermal Characteristics”/Table A-3. Thermal Characteristics/Page 293</td><td>Update Table A-3. Thermal Characteristics as follows:<br>• —Change the value for row “Thermal resistance,Single-layer board/28-pin TSSOP/Airflow @200ft/min.” from 71 to 72 C/W<br>—Change the value for 16-pin TSSOP/Thermalresistance<br>1.Single layer board / Airflow @ 200ft/min. from 108 to 113 C/W.<br>2.Four layer board / Airflow @ 200ft/min. from 78 to 84 C/W.<br>• Update parameter 4 of Table “A-3.Thermal Characteristics” .<br> 
<table>
<tr><th rowspan="2">#</th><th rowspan="2">C</th><th rowspan="2">Rating</th><th rowspan="2">Symbol</th><th rowspan="2">Value</th><th rowspan="2">Unit</th><th colspan="2">Temp Rated</th></tr>
<tr><th>Standard</th><th>AEC Grade 0</th></tr>
<tr><td rowspan="6">1</td><td rowspan="6">—</td><td colspan="6">Operating temperature range (packaged)</td></tr>
<tr><td>Temperature Code W</td><td rowspan="5">$T_A$</td><td>–40 to 150</td><td rowspan="5">°C</td><td>—</td><td>◆</td></tr>
<tr><td>Temperature Code J</td><td>–40 to 140</td><td>—</td><td>◆</td></tr>
<tr><td>Temperature Code M</td><td>–40 to 125</td><td>◆</td><td>—</td></tr>
<tr><td>Temperature Code V</td><td>–40 to 105</td><td>◆</td><td>—</td></tr>
<tr><td>Temperature Code C</td><td>–40 to 85</td><td>◆</td><td>—</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">D</td><td colspan="6">Thermal resistance, Single-layer board</td></tr>
<tr><td></td><td></td><td>Airflow @200 ft/min</td><td>Natural Convection</td><td></td><td></td></tr>
<tr><td>28-pin TSSOP</td><td rowspan="3">$\theta_{JA}$</td><td>72</td><td>91</td><td rowspan="3">°C/W</td><td>◆</td><td>◆</td></tr>
<tr><td>20-pin TSSOP</td><td>94</td><td>114</td><td>◆</td><td>—</td></tr>
<tr><td>16-pin TSSOP</td><td>113</td><td>133</td><td>◆</td><td>◆</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">D</td><td colspan="6">Thermal resistance, Four-layer board</td></tr>
<tr><td></td><td></td><td>Airflow @200 ft/min</td><td>Natural Convection</td><td></td><td></td></tr>
<tr><td>28-pin TSSOP</td><td rowspan="3">$\theta_{JA}$</td><td>51</td><td>58</td><td rowspan="3">°C/W</td><td>◆</td><td>◆</td></tr>
<tr><td>20-pin TSSOP</td><td>68</td><td>75</td><td>◆</td><td>—</td></tr>
<tr><td>16-pin TSSOP</td><td>84</td><td>92</td><td>◆</td><td>◆</td></tr>
<tr><td rowspan="6">4</td><td rowspan="6">D</td><td colspan="6">Maximum junction temperature</td></tr>
<tr><td>Temperature Code W</td><td rowspan="5">$T_J$</td><td>155</td><td rowspan="5">°C</td><td>—</td><td>◆</td></tr>
<tr><td>Temperature Code J</td><td>150</td><td>—</td><td>◆</td></tr>
<tr><td>Temperature Code M</td><td>135</td><td>◆</td><td>—</td></tr>
<tr><td>Temperature Code V</td><td>115</td><td>◆</td><td>—</td></tr>
<tr><td>Temperature Code C</td><td>95</td><td>◆</td><td>—</td></tr>
</table>
</td></tr>
<tr><td>Chapter “Electrical Characteristics”/Section “DC Characteristics”/Table A-6. DC Characteristics/Page 298</td><td>In the Table “DC Characteristics” add note 11 and 12 for parameter #18.<br>Note 11: Device functionality is guaranteed between the LVD threshold VLVD0 and VDD Min. When VDD is below the minimum operating voltage (VDD Min), the analog parameters for the IO pins, ACMP and ADC, are not guaranteed to meet data sheet performance parameters.<br>Note 12: In addition to LVD, it is recommended to also use the LVW feature. LVW can trigger an interrupt and be used as an indicator to warn that the VDD is dropping,so that the software can take actions accordingly before the VDD drops below VDD Min.</td></tr>
</table>

**Table 1. MC9S08SG32 Rev. 1 Addendum**

| Location | Description |
|---|---|
| Chapter “Electrical Characteristics”/Section “Flash Specifications”/Table “A-16. Flash Characteristics”/Page 323 | In Table A-16 Flash Characteristics/row 9/column "Characteristic", change the temperature parameter names as follows:<br><br>Standard: -40°C to +125°C<br>HT: -40°C to +150°C<br>T = 25°C |

# 2 Revision History

Table 2 provides a revision history for this document.

**Table 2. Revision History Table**

| Rev. Number | Substantive Changes | Date of Release |
|---|---|---|
| 1.0 | • Initial release.<br>Changes done in Chapter “Electrical Characteristics”. | 02/2012 |

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**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
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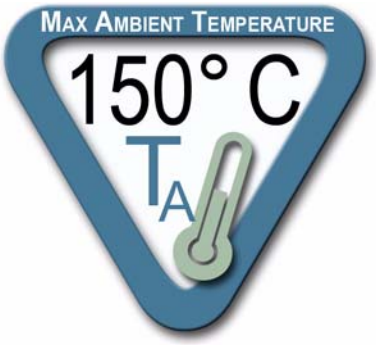
MC9S08SG32AD
Rev. 1
02/2012

# MC9S08SG32
# MC9S08SG16
# Data Sheet

***Now Includes High-Temperature (up to 150 °C) Devices!***




***HCS08***
***Microcontrollers***

MC9S08SG32
Rev. 8
5/2010

freescale.com

# MC9S08SG32 Series Features

### 8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 36-MHz HCS08 CPU for temperatures greater than 125 °C
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

### On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature from –40 up to 150 °C
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

### Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time counter for use in run, wait, and stop

### Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and:
  - 1.5% deviation over temperature –40 to 125 °C
  - 3% deviation for temperature > 125 °C
- ICS supports bus frequencies from 2 MHz to 20 MHz

### System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

### Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module containing two comparators and 9 trigger modes. Eight-deep FIFO for storing change-of-flow address and event-only data. Debug module supports both tag and force breakpoints

### Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMP** — Analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be optionally routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- **MTIM** — 8-bit modulo counter with 8-bit prescaler and overflow interrupt
- **TPMx** — Two 2-channel timer pwm modules (TPM1, TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components, runs in all MCU modes

### Input/Output

- 22 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Ganged output option for PTB[5:2] and PTC[3:0]; allows single write to change state of multiple pins
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins

### Package Options

- 28-TSSOP, 20-TSSOP, 16-TSSOP (20-pin package options not available on high-temperature rated devices).

# MC9S08SG32 Data Sheet

Covers MC9S08SG32
MC9S08SG16

MC9S08SG32
Rev. 8
5/2010

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# Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

| Revision Number | Revision Date | Description of Changes |
|---|---|---|
| 1 | 6/2007 | Updated the TPM module, incorporated minor revisions for the $T_j$, PTxSE slew rate, FPROT and Appendix B packaging information. -SAMPLES DRAFT- |
| 2 | 10/2007 | Qualify Draft includes updates to TPM module and the Electricals appendix. Also, revised the order numbering information. |
| 3 | 5/2008 | Updated some electricals and made some minor grammatical/formatting revisions. Corrected the SPI block module version. Removed incorrect ADC temperature sensor value from the Features section. Updated the package information with a special mask set identifier. |
| 4 | 5/2008 | Added the EMC Radiated Emissions data. Removed the Susceptibility Data. Updated the Corporate addresses on the back cover. |
| 5 | 03/2009 | Added the High Temperature Device Specifications and updated the charts. |
| 6 | 04/2009 | Updated ADC characteristics for Temp Sensor Slope to be a range of 25 C–150 Çadded Control Timing table row 2 to separate standard characteristics from the AEC Grade 0 characteristics, and included the text, “AEC Grade 0” to the text of footnote 3 for Table B-1 Device Numbering System. Added notes to the ADC chapter specifying that, for this device, there are only 16 analog input pins and consequently no APCTL3 register. Updated the Literature Request information on the back cover. |
| 7 | 10/2009 | Revised Table A-6 DC Characteristics, Row 24 Bandgap Voltage Reference for AEC Grade 0 from 1.21V to 1.22 V. Removed AEC Grade 0 (red diamond) from the Table A-9 ICS Frequency Specifications, Row 9 Total deviation of trimmed DCO output frequency over voltage and temperature so that it is not listed for AEC Grade 0. |

| Revision Number | Revision Date | Description of Changes |
|---|---|---|
| 8 | 5/2010 | • In the A.9 ICS Characteristic table, changed row 9 parameter classification from a D to a P to indicate that these parameters are guaranteed during production testing on each individual device.<br>• In the A.16 Flash Charateristic table, added the AEC temperature range to row 9.<br>• Revised Figure 2-1 so that the RESET pin shows the overbar. |

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|---|---|---|

# Chapter 1
# Device Overview

The MC9S08SG32 devices are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). The MC9S08SG32 Series high-temperature devices have been qualified to meet or exceed AEC Grade 0 requirements to allow them to operate up to 150 °C $T_A$. All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

## 1.1 Devices in the MC9S08SG32 Series

Table 1-1 summarizes the feature set available in the MC9S08SG32 series of MCUs.

**Table 1-1. MC9S08SG32 Series Features by MCU and Package**

| Feature | MC9S08SG32 | | | MC9S08SG16 | | |
|---|---|---|---|---|---|---|
| FLASH size (bytes) | 32768 | | | 16384 | | |
| RAM size (bytes) | 1024 | | | 1024 | | |
| Pin quantity | 28 | 20 | 16 | 28 | 20 | 16 |
| ACMP | yes | | | yes | | |
| ADC channels | 16 | 12 | 8 | 16 | 12 | 8 |
| DBG | yes | | | yes | | |
| ICS | yes | | | yes | | |
| IIC | yes | | | yes | | |
| MTIM | yes | | | yes | | |
| Pin Interrupts | 8 | | | 8 | | |
| Pin I/O | 22 | 16 | 12 | 22 | 16 | 12 |
| RTC | yes | | | yes | | |
| SCI | yes | | | yes | | |
| SPI | yes | | | yes | | |
| TPM1 channels | yes | | | yes | | |
| TPM2 channels | yes | | | yes | | |
| XOSC | yes | | | yes | | |

## 1.2 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08SG32 Series MCU.

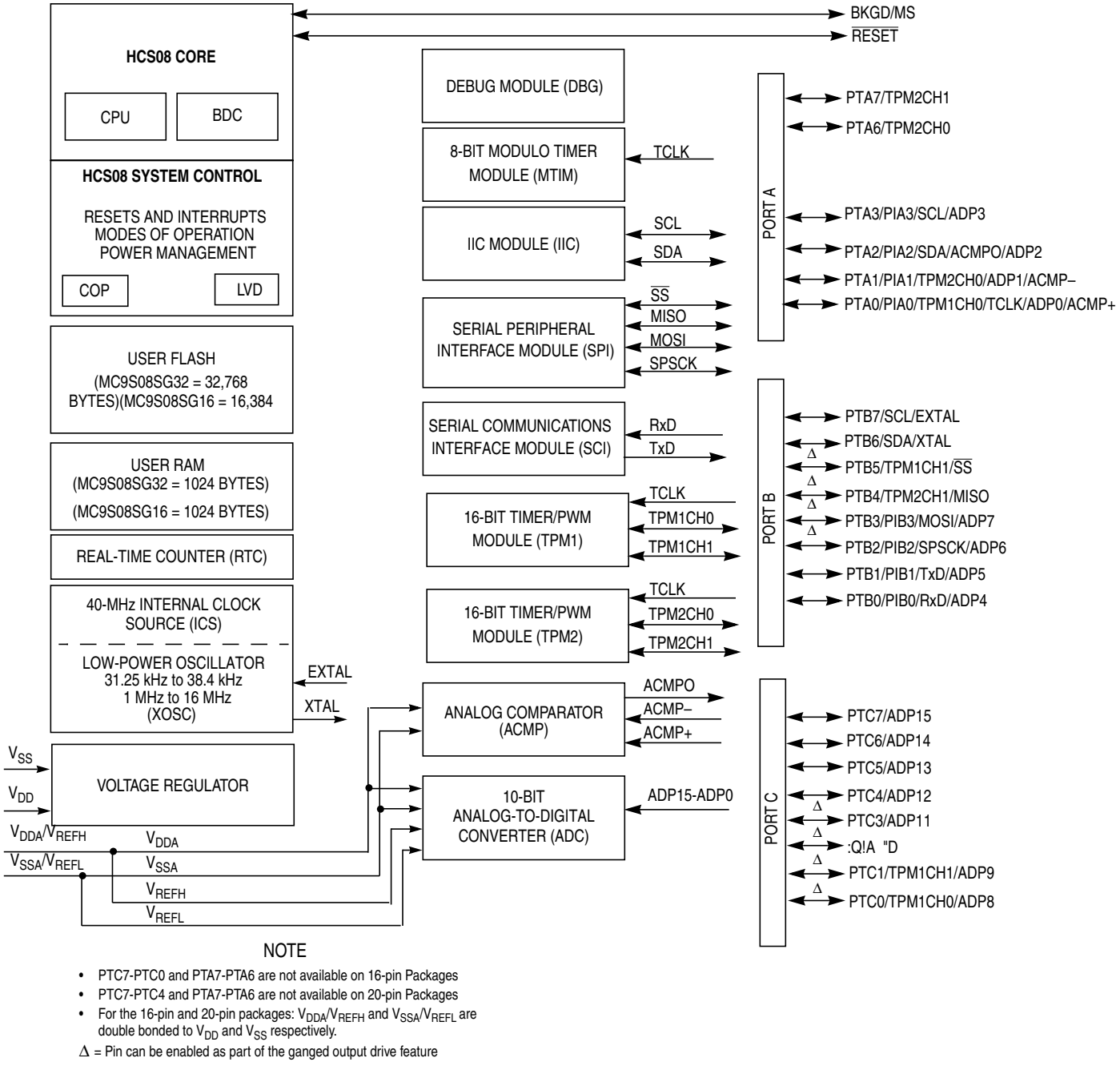



**Figure 1-1. MC9S08SG32 Series Block Diagram**

Table 1-2 provides the functional version of the on-chip modules.

**Table 1-2. Module Versions**

| Module | | Version |
|---|---|---|
| Analog Comparator (5V) | (ACMP) | 3 |
| Analog-to-Digital Converter | (ADC10) | 1 |
| Central Processor Unit | (CPU) | 3 |
| Inter-Integrated Circuit | (IIC) | 2 |
| Internal Clock Source | (ICS) | 2 |
| Low Power Oscillator | (XOSC) | 1 |
| Modulo Timer | (MTIM) | 1 |
| On-Chip In-Circuit Emulator | (DBG) | 2 |
| Real-Time Counter | (RTC) | 1 |
| Serial Peripheral Interface | (SPI) | 3 |
| Serial Communications Interface | (SCI) | 4 |
| Timer Pulse Width Modulator | (TPM) | 3 |

## 1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following defines the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of ICSOUT.
- ICSOUT — Primary output of the ICS and is twice the bus frequency.
- ICSLCLK — Development tools can select this clock source to speed up BDC communications in systems where the bus clock is configured to run at a very slow frequency.
- ICSERCLK — External reference clock can be selected as the RTC clock source and as the alternate clock for the ADC module.
- ICSIRCLK — Internal reference clock can be selected as the RTC clock source.
- ICSFFCLK — Fixed frequency clock can be selected as clock source for the TPM1, TPM2 and MTIM modules.
- LPOCLK — Independent 1-kHz clock source that can be selected as the clock source for the COP and RTC modules.
- TCLK — External input clock source for TPM1, TPM2 and MTIM and is referenced as TPMCLK in TPM chapters.

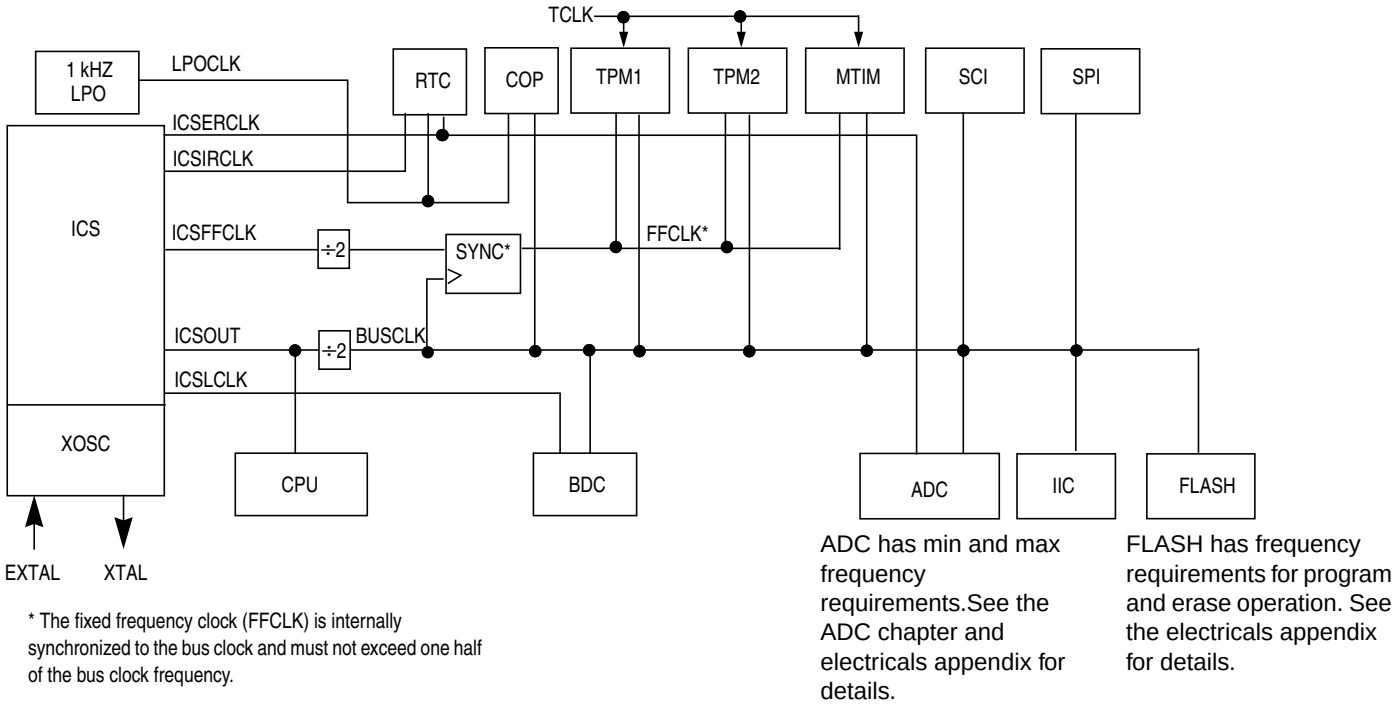



**Figure 1-2. System Clock Distribution Diagram**

# Chapter 2
# Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

## 2.1 Device Pin Assignment

The following figures show the pin assignments for the MC9S08SG32 Series devices.

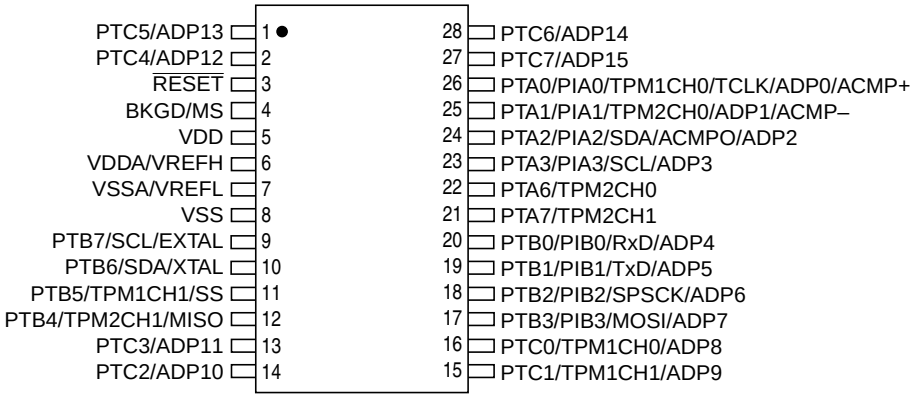



**Figure 2-1. 28-Pin TSSOP**

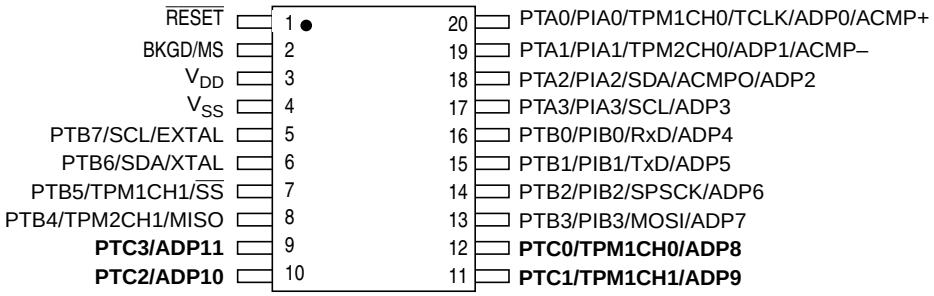



**Figure 2-2. 20-Pin TSSOP[1]**

1. 20-Pin TSSOP package not available for the high-temperature rated devices.

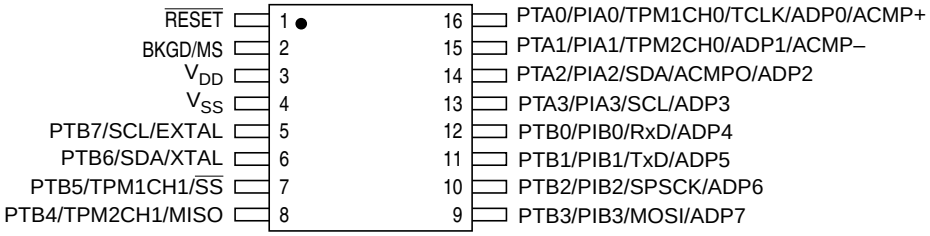
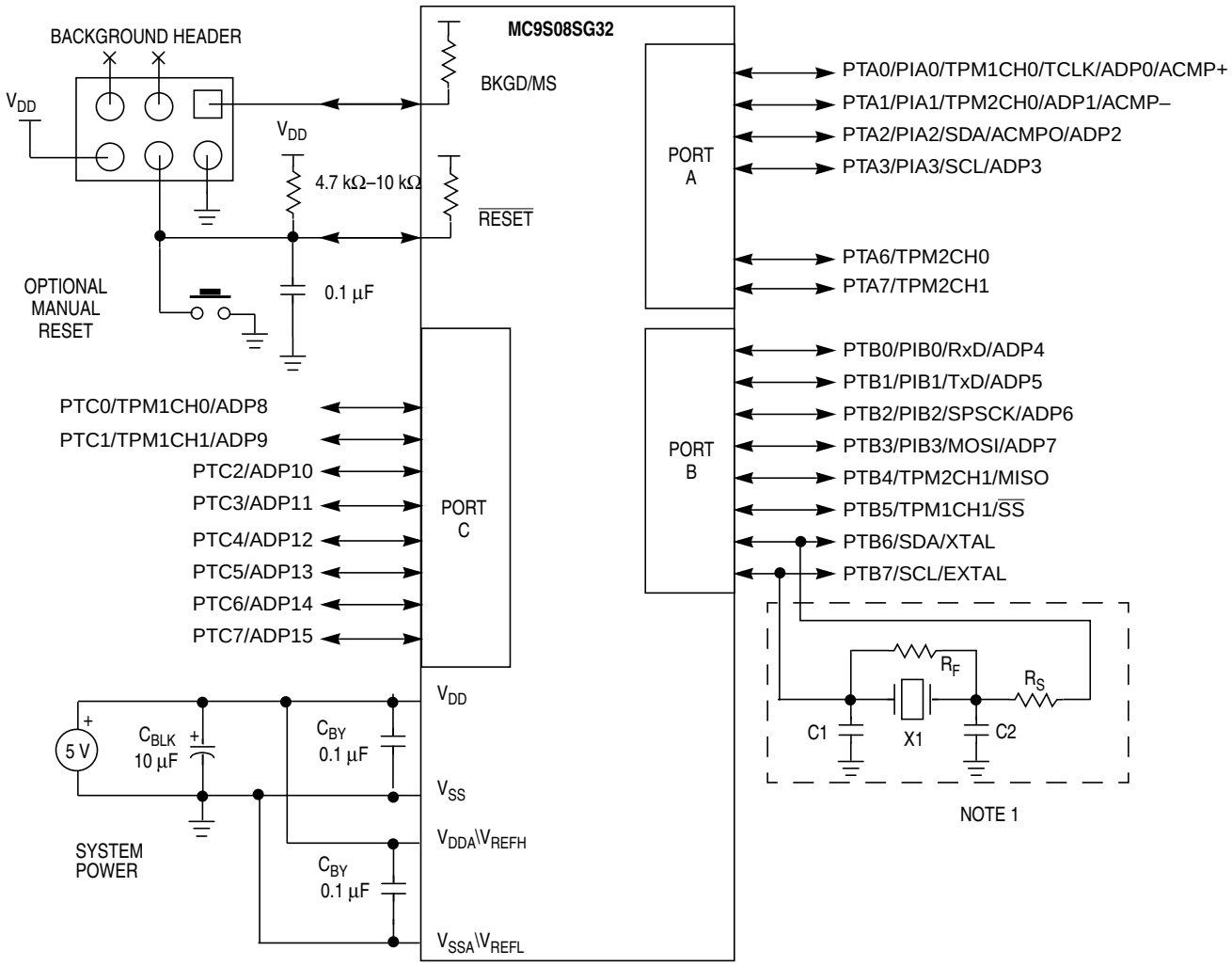



**Figure 2-3. 16-Pin TSSOP**

## 2.2 Recommended System Connections

Figure 2-4 shows pin connections that are common to MC9S08SG32 Series application systems.




NOTES:
1. External crystal circuit not required if using the internal clock option.
2. RESET pin can only be used to reset into user mode, you can not enter BDM using RESET pin. BDM can be entered by holding MS low during POR or writing a 1 to BDFR in SBDFR with MS low after issuing BDM command.
3. RC filter on RESET pin recommended for noisy environments.
4. For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

**Figure 2-4. Basic System Connections**

### 2.2.1 Power

$V_{DD}$ and $V_{SS}$ are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10-µF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1-µF ceramic bypass capacitor located as near to the MCU power pins as practical to suppress high-frequency noise. Each pin must have a bypass capacitor for best noise suppression.

$V_{DDA}$ and $V_{SSA}$ are the analog power supply pins for MCU. This voltage source supplies power to the ADC module. A 0.1 µF ceramic bypass capacitor should be located as near to the MCU power pins as practical to suppress high-frequency noise. The $V_{REFH}$ and $V_{REFL}$ pins are the voltage reference high and voltage reference low inputs, respectively for the ADC module. For this MCU, $V_{DDA}$ shares the $V_{REFH}$ pin and these pins are available only in the 28-pin packages. In the 16-pin and 20-pin packages, they are double bonded to the $V_{DD}$ pin. For this MCU, $V_{SSA}$ shares the $V_{REFL}$ pin and these pins are available only in the 28-pin packages. In the 16-pin and 20-pin packages, they are double bonded to the $V_{SS}$ pin.

### 2.2.2 Oscillator (XOSC)

Immediately after reset, the MCU uses an internally generated clock provided by the clock source generator (ICS) module. For more information on the ICS, see Chapter 11, “Internal Clock Source (S08ICSV2).”

The oscillator (XOSC) in this MCU is a Pierce oscillator that can accommodate a crystal or ceramic resonator. Rather than a crystal or ceramic resonator, an external oscillator can be connected to the EXTAL input pin.

Refer to Figure 2-4 for the following discussion. $R_S$ (when used) and $R_F$ should be low-inductance resistors such as carbon composition resistors. Wire-wound resistors, and some metal film resistors, have too much inductance. C1 and C2 normally should be high-quality ceramic capacitors that are specifically designed for high-frequency applications.

$R_F$ is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup; its value is not generally critical. Typical systems use 1 MΩ to 10 MΩ. Higher values are sensitive to humidity and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5-pF to 25-pF range and are chosen to match the requirements of a specific crystal or resonator. Be sure to take into account printed circuit board (PCB) capacitance and MCU pin capacitance when selecting C1 and C2. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2 (which are usually the same size). As a first-order approximation, use 10 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

### 2.2.3 $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is a dedicated pin with open-drain drive containing an internal pull-up device. Internal power-on reset and low-voltage reset circuitry typically make external reset circuitry unnecessary. This pin is normally connected to the standard 6-pin background debug connector so a development system can directly reset the MCU system. If desired, a manual external reset can be added by supplying a simple switch to ground (pull reset pin low to force a reset).

Whenever any reset is initiated (whether from an external signal or from an internal system), the $\overline{\text{RESET}}$ pin is driven low for about 66 bus cycles. The reset circuitry decodes the cause of reset and records it by setting a corresponding bit in the system reset status register (SRS).

**NOTE**

- This pin does not contain a clamp diode to $V_{DD}$ and should not be driven above $V_{DD}$.
- The voltage measured on the internally pulled up $\overline{\text{RESET}}$ pin will not be pulled to $V_{DD}$. The internal gates connected to this pin are pulled to $V_{DD}$. If the $\overline{\text{RESET}}$ pin is required to drive to a $V_{DD}$ level, an external pullup should be used.
- In EMC-sensitive applications, an external RC filter is recommended on the $\overline{\text{RESET}}$. See Figure 2-4 for an example.

### 2.2.4 Background / Mode Select (BKGD/MS)

During a power-on-reset (POR) or background debug force reset (see Section 5.7.2, “System Background Debug Force Reset Register (SBDFR),” for more information), the BKGD/MS pin functions as a mode select pin. Immediately after any reset, the pin functions as the background pin and can be used for background debug communication. The BKGD/MS pin contains an internal pullup device.

If nothing is connected to this pin, the MCU enters normal operating mode at the rising edge of the internal reset after a POR or force BDC reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during a POR or immediately after issuing a background debug force reset, which will force the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU’s BDC clock per bit time. The target MCU’s BDC clock could be as fast as the maximum bus clock rate, so there must never be any significant capacitance connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

### 2.2.5 General-Purpose I/O and Peripheral Ports

The MC9S08SG32 Series of MCUs support up to 22 general-purpose I/O pins which are shared with on-chip peripheral functions (timers, serial I/O, ADC, etc.).

When a port pin is configured as a general-purpose output or a peripheral uses the port pin as an output, software can select one of two drive strengths and enable or disable slew rate control. When a port pin is configured as a general-purpose input or a peripheral uses the port pin as an input, software can enable a pull-up device. Immediately after reset, all of these pins are configured as high-impedance general-purpose inputs with internal pull-up devices disabled.

When an on-chip peripheral system is controlling a pin, data direction control bits still determine what is read from port data registers even though the peripheral module controls the pin direction by controlling the enable for the pin's output buffer. For information about controlling these pins as general-purpose I/O pins, see Chapter 6, "Parallel Input/Output Control."

The MC9S08SG32 Series devices contain a ganged output drive feature that allows a safe and reliable method of allowing pins to be tied together externally to produce a higher output current drive. See Section 6.3, "Ganged Output" for more information for configuring the port pins for ganged output drive.

**NOTE**

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pull-up devices or change the direction of unused pins to outputs so they do not float.

When using the 20-pin devices, either enable on-chip pullup devices or change the direction of non-bonded PTC7-PTC4 and PTA7-PTA6 pins to outputs so the pins do not float.

When using the 16-pin devices, either enable on-chip pullup devices or change the direction of non-bonded out PTC7-PTC0 and PTA7-PTA6 pins to outputs so the pins do not float.

**Table 2-1. Pin Availability by Package Pin-Count**

| Pin Number | | | Priority (Lowest → Highest) | | | | | |
|---|---|---|---|---|---|---|---|---|
| 28-pin | 20-pin[1] | 16-pin | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 | Alt 5 |
| 1 | — | — | PTC5 | | | | | ADP13 |
| 2 | — | — | PTC4 | | | | | ADP12 |
| 3 | 1 | 1 | | | | | | $\overline{\text{RESET}}$[2] |
| 4 | 2 | 2 | | | | | BKGD | MS |
| 5 | 3 | 3 | | | | | | $V_{DD}$ |
| 6 | | | | | | | $V_{DDA}$ | $V_{REFH}$ |
| 7 | 4 | 4 | | | | | $V_{SSA}$ | $V_{REFL}$ |
| 8 | | | | | | | | $V_{SS}$ |
| 9 | 5 | 5 | PTB7 | SCL[3] | EXTAL | | | |
| 10 | 6 | 6 | PTB6 | SDA[3] | XTAL | | | |
| 11 | 7 | 7 | PTB5 | TPM1CH1[4] | $\overline{\text{SS}}$ | PTC0[5] | | |
| 12 | 8 | 8 | PTB4 | TPM2CH1[6] | MISO | PTC0[5] | | |
| 13 | 9 | — | PTC3 | | | PTC0[5] | ADP11 | |
| 14 | 10 | — | PTC2 | | | PTC0[5] | ADP10 | |
| 15 | 11 | — | PTC1 | | TPM1CH1[4] | PTC0[5] | ADP9 | |
| 16 | 12 | — | PTC0 | | TPM1CH0[4] | PTC0[5] | ADP8 | |
| 17 | 13 | 9 | PTB3 | PIB3 | MOSI | PTC0[5] | ADP7 | |
| 18 | 14 | 10 | PTB2 | PIB2 | SPSCK | PTC0[5] | ADP6 | |

**Table 2-1. Pin Availability by Package Pin-Count (continued)**

| Pin Number | | | Priority (Lowest → Highest) | | | | | |
|---|---|---|---|---|---|---|---|---|
| **28-pin** | **20-pin[1]** | **16-pin** | **Port Pin** | **Alt 1** | **Alt 2** | **Alt 3** | **Alt 4** | **Alt 5** |
| 19 | 15 | 11 | PTB1 | PIB1 | TxD | | ADP5 | |
| 20 | 16 | 12 | PTB0 | PIB0 | RxD | | ADP4 | |
| 21 | — | — | PTA7 | TPM2CH1[6] | | | | |
| 22 | — | — | PTA6 | TPM2CH0[6] | | | | |
| 23 | 17 | 13 | PTA3 | PIA3 | SCL[3] | | ADP3 | |
| 24 | 18 | 14 | PTA2 | PIA2 | SDA[3] | ACMPO | ADP2 | |
| 25 | 19 | 15 | PTA1 | PIA1 | TPM2CH0[6] | | ADP1[7] | ACMP-[7] |
| 26 | 20 | 16 | PTA0 | PIA0 | TPM1CH0[4] | TCLK | ADP0[7] | ACMP+[7] |
| 27 | — | — | PTC7 | | | | | ADP15 |
| 28 | — | — | PTC6 | | | | | ADP14 |

1 The 20-pin package is not available for the high-temperature rated devices.

2 Pin is open drain with an internal pullup that is always enabled. Pin does not contain a clamp diode to $V_{DD}$ and should not be driven above $V_{DD}$. The voltage measured on the internally pulled up $\overline{\text{RESET}}$ will not be pulled to $V_{DD}$. The internal gates connected to this pin are pulled to $V_{DD}$.

3 IIC pins can be repositioned using IICPS in SOPT2, default reset locations are PTA2, PTA3.

4 TPM1CHx pins can be repositioned using T1CHxPS bits in SOPT2, default reset locations are PTA0, PTB5.

5 This port pin is part of the ganged output feature. When pin is enabled for ganged output, it will have priority over all digital modules. The output data, drive strength and slew-rate control of this port pin will follow the configuration for the PTC0 pin, even in 16-pin packages where PTC0 doesn't bond out.

6 TPM2CHx pins can be repositioned using T2CHxPS bits in SOPT2, default reset locations are PTA1, PTB4.

7 If ACMP and ADC are both enabled, both will have access to the pin.

# Chapter 3
# Modes of Operation

## 3.1 Introduction

The operating modes of the MC9S08SG32 Series are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

## 3.2 Features

- Active background mode for code development
- Wait mode — CPU shuts down to conserve power; system clocks are running and full regulation is maintained
- Stop modes — System clocks are stopped and voltage regulator is in standby
  - Stop3 — All internal circuits are powered for fast recovery
  - Stop2 — Partial power down of internal circuits, RAM content is retained

## 3.3 Run Mode

This is the normal operating mode for the MC9S08SG32 Series. This mode is selected upon the MCU exiting reset if the BKGD/MS pin is high. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at 0xFFFE–0xFFFF after reset.

## 3.4 Active Background Mode

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 core. The BDC, together with the on-chip debug module (DBG), provide the means for analyzing MCU operation during software development.

Active background mode is entered in any of the following ways:

- When the BKGD/MS pin is low during POR or immediately after issuing a background debug force reset (see Section 5.7.2, “System Background Debug Force Reset Register (SBDFR)”)
- When a BACKGROUND command is received through the BKGD/MS pin
- When a BGND instruction is executed
- When encountering a BDC breakpoint
- When encountering a DBG breakpoint

After entering active background mode, the CPU is held in a suspended state waiting for serial background commands rather than executing instructions from the user application program.

Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running. Non-intrusive commands can be issued through the BKGD/MS pin while the MCU is in run mode; non-intrusive commands can also be executed when the MCU is in the active background mode. Non-intrusive commands include:
  - Memory access commands
  - Memory-access-with-status commands
  - BDC register access commands
  - The BACKGROUND command
- Active background commands, which can only be executed while the MCU is in active background mode. Active background commands include commands to:
  - Read or write CPU registers
  - Trace one user program instruction at a time
  - Leave active background mode to return to the user application program (GO)

The active background mode is used to program a bootloader or user application program into the FLASH program memory before the MCU is operated in run mode for the first time. When the MC9S08SG32 Series is shipped from the Freescale Semiconductor factory, the FLASH program memory is erased by default unless specifically noted so there is no program that could be executed in run mode until the FLASH memory is initially programmed. The active background mode can also be used to erase and reprogram the FLASH memory after it has been previously programmed.

For additional information about the active background mode, refer to the Development Support chapter.

## 3.5 Wait Mode

Wait mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The I bit in CCR is cleared when the CPU enters the wait mode, enabling interrupts. When an interrupt request occurs, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

While the MCU is in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from wait mode and enter active background mode.

## 3.6 Stop Modes

One of two stop modes is entered upon execution of a STOP instruction when STOPE in SOPT1. In any stop mode, the bus and CPU clocks are halted. The ICS module can be configured to leave the reference clocks running. See Chapter 11, “Internal Clock Source (S08ICSV2),” for more information.

Table 3-1 shows all of the control bits that affect stop mode selection and the mode selected under various conditions. The selected mode is entered following the execution of a STOP instruction.

**Table 3-1. Stop Mode Selection**

| STOPE | ENBDM [1] | LVDE | LVDSE | PPDC | Stop Mode |
|---|---|---|---|---|---|
| 0 | x | x | | x | Stop modes disabled; illegal opcode reset if STOP instruction executed |
| 1 | 1 | x | | x | Stop3 with BDM enabled [2] |
| 1 | 0 | Both bits must be 1 | | x | Stop3 with voltage regulator active |
| 1 | 0 | Either bit a 0 | | 0 | Stop3 |
| 1 | 0 | Either bit a 0 | | 1 | Stop2 |

1 ENBDM is located in the BDCSCR, which is only accessible through BDC commands, see Section 17.4.1.1, “BDC Status and Control Register (BDCSCR)”.

2 When in Stop3 mode with BDM enabled, The $S_{IDD}$ will be near $R_{IDD}$ levels because internal clocks are enabled.

## 3.6.1 Stop3 Mode

Stop3 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. The states of all of the internal registers and logic, RAM contents, and I/O pin states are maintained.

Stop3 can be exited by asserting $\overline{\text{RESET}}$, or by an interrupt from one of the following sources: the real-time counter (RTC), LVD system, ACMP, ADC, SCI or any pin interrupts.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, then the MCU is reset and operation will resume after taking the reset vector. Exit by means of one of the internal interrupt sources results in the MCU taking the appropriate interrupt vector.

### 3.6.1.1 LVD Enabled in Stop3 Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. For configuring the LVD system for interrupt or reset, refer to Section 5.6, “Low-Voltage Detect (LVD) System”. If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode.

For the ADC to operate in stop mode, the LVD must be enabled when entering stop3.

For the ACMP to operate in stop mode with compare to internal bandgap option, the LVD must be enabled when entering stop3.

### 3.6.1.2 Active BDM Enabled in Stop3 Mode

Entry into the active background mode from run mode is enabled if ENBDM in BDCSCR is set. This register is described in Chapter 17, “Development Support.” If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode. Because of this, background debug communication remains possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation.

Most background commands are not available in stop mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from stop and enter active background mode if the ENBDM bit is set. After entering background debug mode, all background commands are available.

### 3.6.2 Stop2 Mode

Stop2 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. Most of the internal circuitry of the MCU is powered off in stop2 with the exception of the RAM. Upon entering stop2, all I/O pin control signals are latched so that the pins retain their states during stop2.

Exit from stop2 is performed by asserting the wake-up pin ($\overline{\text{RESET}}$) on the MCU.

In addition, the real-time counter (RTC) can wake the MCU from stop2, if enabled.

Upon wake-up from stop2 mode, the MCU starts up as from a power-on reset (POR):

- All module control and status registers are reset
- The LVD reset function is enabled and the MCU remains in the reset state if $V_{DD}$ is below the LVD trip point (low trip point selected due to POR)
- The CPU takes the reset vector

In addition to the above, upon waking up from stop2, the PPDF bit in SPMSC2 is set. This flag is used to direct user code to go to a stop2 recovery routine. PPDF remains set and the I/O pin states remain latched until a 1 is written to PPDACK in SPMSC2.

To maintain I/O states for pins that were configured as general-purpose I/O before entering stop2, the user must restore the contents of the I/O port registers, which have been saved in RAM, to the port registers before writing to the PPDACK bit. If the port registers are not restored from RAM before writing to PPDACK, then the pins will switch to their reset states when PPDACK is written.

For pins that were configured as peripheral I/O, the user must reconfigure the peripheral module that interfaces to the pin before writing to the PPDACK bit. If the peripheral module is not enabled before writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

### 3.6.3 On-Chip Peripheral Modules in Stop Modes

When the MCU enters any stop mode, system clocks to the internal peripheral modules are stopped. Even in the exception case (ENBDM = 1), where clocks to the background debug logic continue to operate, clocks to the peripheral systems are halted to reduce power consumption. Refer to Section 3.6.2, “Stop2 Mode,” and Section 3.6.1, “Stop3 Mode,” for specific information on system behavior in stop modes.

**Table 3-2. Stop Mode Behavior**

| Peripheral | Mode | |
|---|---|---|
| | Stop2 | Stop3 |
| CPU | Off | Standby |
| RAM | Standby | Standby |
| FLASH | Off | Standby |
| Parallel Port Registers | Off | Standby |
| ADC | Off | Optionally On[1] |
| ACMP | Off | Optionally On[2] |
| BDM | Off[3] | Optionally On |
| ICS | Off | Optionally On[4] |
| IIC | Off | Standby |
| LVD/LVW | Off[5] | Optionally On |
| MTIM | Off | Standby |
| RTC | Optionally On | Optionally On |
| SCI | Off | Standby |
| SPI | Off | Standby |
| TPM | Off | Standby |
| Voltage Regulator | Standby | Optionally On[6] |
| XOSC | Off | Optionally On[7] |
| I/O Pins | States Held | States Held |

1 Requires the asynchronous ADC clock and LVD to be enabled, else in standby.

2 Requires the LVD to be enabled when compare to internal band-up reference option is enabled.

3 If ENBDM is set when entering stop2, the MCU will actually enter stop3.

4 IRCLKEN and IREFSTEN set in ICSC1, else in standby.

5 If LVDSE is set when entering stop2, the MCU will actually enter stop3.

6 Voltage regulator will be on if BDM is enabled or if LVD is enabled when entering stop3.

7 ERCLKEN and EREFSTEN set in ICSC2, else in standby. For high frequency range (RANGE in ICSC2 set) requires the LVD to also be enabled in stop3.

# Chapter 4
# Memory

## 4.1 MC9S08SG32 Series Memory Map

As shown in Figure 4-1, on-chip memory in the MC9S08SG32 Series series of MCUs consists of RAM, FLASH program memory for nonvolatile data storage, and I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers (0x0000 through 0x007F)
- High-page registers (0x1800 through 0x185F)
- Nonvolatile registers (0xFFB0 through 0xFFBF)

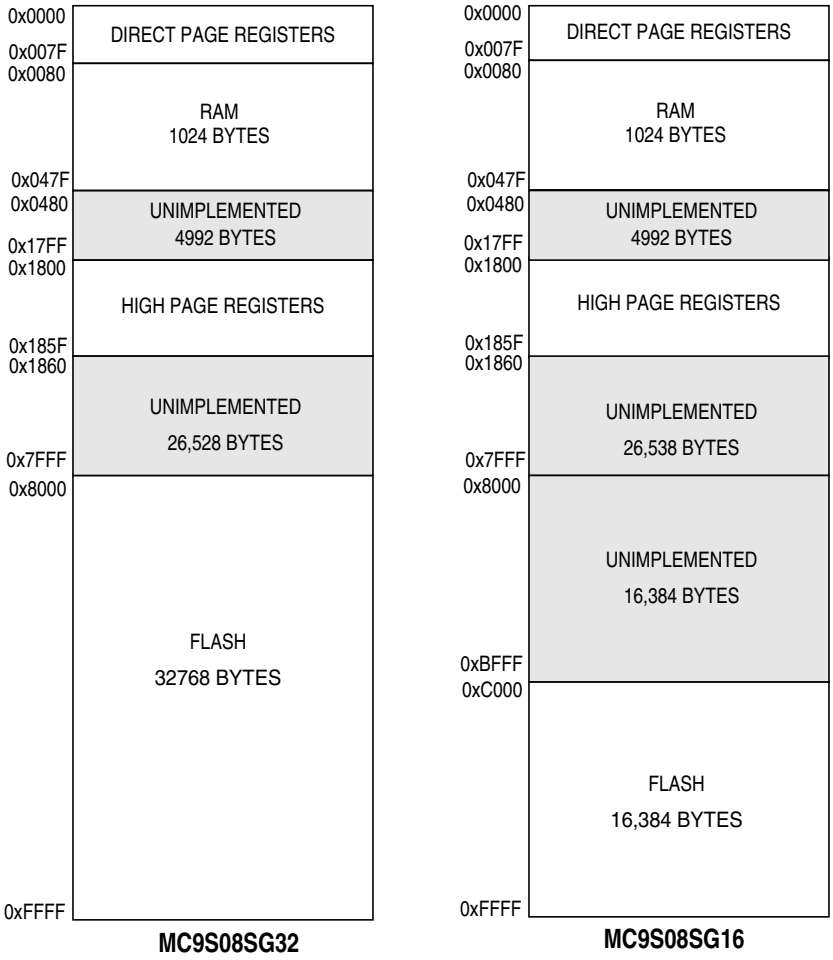



**Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map**

## 4.2 Reset and Interrupt Vector Assignments

Table 4-1 shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the Freescale Semiconductor provided equate file for the MC9S08SG32 Series.

**Table 4-1. Reset and Interrupt Vectors**

| Address (High/Low) | Vector | Vector Name |
|---|---|---|
| 0xFFC0:0xFFC1 | Reserved | — |
| 0xFFC2:0xFFC3 | ACMP | Vacmp |
| 0xFFC4:0xFFC5 | Reserved | — |
| 0xFFC6:0xFFC7 | Reserved | — |
| 0xFFC8:0xFFC9 | Reserved | — |
| 0xFFCA:0xFFCB | MTIM Overflow | Vmtim |
| 0xFFCC:0xFFCD | RTC | Vrtc |
| 0xFFCE:0xFFCF | IIC | Viic |
| 0xFFD0:0xFFD1 | ADC Conversion | Vadc |
| 0xFFD2:0xFFD3 | Reserved | — |
| 0xFFD4:0xFFD5 | Port B Pin Interrupt | Vportb |
| 0xFFD6:0xFFD7 | Port A Pin Interrupt | Vporta |
| 0xFFD8:0xFFD9 | Reserved | — |
| 0xFFDA:0xFFDB | SCI Transmit | Vscitx |
| 0xFFDC:0xFFDD | SCI Receive | Vscirx |
| 0xFFDE:0xFFDF | SCI Error | Vsc1err |
| 0xFFE0:0xFFE1 | SPI | Vspi |
| 0xFFE2:0xFFE3 | TPM2 Overflow | Vtpm2ovf |
| 0xFFE4:0xFFE5 | TPM2 Channel 1 | Vtpm2ch1 |
| 0xFFE6:0xFFE7 | TPM2 Channel 0 | Vtpm2ch0 |
| 0xFFE8:0xFFE9 | TPM1 Overflow | Vtpm1ovf |
| 0xFFEA:0xFFEB | Reserved | — |
| 0xFFEC:0xFFED | Reserved | — |
| 0xFFEE:0xFFEF | Reserved | — |
| 0xFFF0:0xFFF1 | Reserved | — |
| 0xFFF2:0xFFF3 | TPM1 Channel 1 | Vtpm1ch1 |
| 0xFFF4:0xFFF5 | TPM1 Channel 0 | Vtpm1ch0 |
| 0xFFF6:0xFFF7 | Reserved | — |
| 0xFFF8:0xFFF9 | Low Voltage Detect | Vlvd |
| 0xFFFA:0xFFFB | Reserved | — |
| 0xFFFC:0xFFFD | SWI | Vswi |
| 0xFFFE:0xFFFF | Reset | Vreset |

## 4.3 Register Addresses and Bit Assignments

The registers in the MC9S08SG32 Series are divided into these groups:

- Direct-page registers are located in the first 128 locations in the memory map; these are accessible with efficient direct addressing mode instructions.
- High-page registers are used much less often, so they are located above 0x1800 in the memory map. This leaves more room in the direct page for more frequently used registers and RAM.
- The nonvolatile register area consists of a block of 16 locations in FLASH memory at 0xFFB0–0xFFBF. Nonvolatile register locations include:
  - NVPROT and NVOPT are loaded into working registers at reset
  - An 8-byte backdoor comparison key that optionally allows a user to gain controlled access to secure memory

  Because the nonvolatile register locations are FLASH memory, they must be erased and programmed like other FLASH memory locations.

Direct-page registers can be accessed with efficient direct addressing mode instructions. Bit manipulation instructions can be used to access any bit in any direct-page register. Table 4-2 is a summary of all user-accessible direct-page registers and control bits.

The direct page registers in Table 4-2 can use the more efficient direct addressing mode, which requires only the lower byte of the address. Because of this, the lower byte of the address in column one is shown in bold text. In Table 4-3 and Table 4-4, the whole address in column one is shown in bold. In Table 4-2, Table 4-3, and Table 4-4, the register names in column two are shown in bold to set them apart from the bit names to the right. Cells that are not associated with named bits are shaded. A shaded cell with a 0 indicates this unused or reserved bit always reads as a 0 and should be written as 0. A shaded cell with a 1 indicates this unused or reserved bit always reads as a 1and should be written as 1. Shaded cells with dashes indicate unused or reserved bit locations that could read as 1s or 0s.

**Table 4-2. Direct-Page Register Summary (Sheet 1 of 3)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0000 | **PTAD** | PTAD7 | PTAD6 | — | — | PTAD3 | PTAD2 | PTAD1 | PTAD0 |
| 0x0001 | **PTADD** | PTADD7 | PTADD6 | — | — | PTADD3 | PTADD2 | PTADD1 | PTADD0 |
| 0x0002 | **PTBD** | PTBD7 | PTBD6 | PTBD5 | PTBD4 | PTBD3 | PTBD2 | PTBD1 | PTBD0 |
| 0x0003 | **PTBDD** | PTBDD7 | PTBDD6 | PTBDD5 | PTBDD4 | PTBDD3 | PTBDD2 | PTBDD1 | PTBDD0 |
| 0x0004 | **PTCD** | PTCD7 | PTCD6 | PTCD5 | PTCD4 | PTCD3 | PTCD2 | PTCD1 | PTCD0 |
| 0x0005 | **PTCDD** | PTCDD7 | PTCDD6 | PTCDD5 | PTCDD4 | PTCDD3 | PTCDD2 | PTCDD1 | PTCDD0 |
| 0x0006 | Reserved | — | — | — | — | — | — | — | — |
| 0x0007 | Reserved | — | — | — | — | — | 0 | 0 | 0 |
| 0x0008–0x000D | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x000E | **ACMPSC** | ACME | ACBGS | ACF | ACIE | ACO | ACOPE | ACMOD1 | ACMOD0 |
| 0x000F | Reserved | — | — | — | — | — | — | — | — |
| 0x0010 | **ADCSC1** | COCO | AIEN | ADCO | ADCH | | | | |
| 0x0011 | **ADCSC2** | ADACT | ADTRG | ACFE | ACFGT | — | — | — | — |
| 0x0012 | **ADCRH** | 0 | 0 | 0 | 0 | 0 | 0 | ADR9 | ADR8 |
| 0x0013 | **ADCRL** | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
| 0x0014 | **ADCVH** | 0 | 0 | 0 | 0 | 0 | 0 | ADCV9 | ADCV8 |
| 0x0015 | **ADCVL** | ADCV7 | ADCV6 | ADCV5 | ADCV4 | ADCV3 | ADCV2 | ADCV1 | ADCV0 |
| 0x0016 | **ADCCFG** | ADLPC | ADIV | | ADLSMP | MODE | | ADICLK | |
| 0x0017 | **APCTL1** | ADPC7 | ADPC6 | ADPC5 | ADPC4 | ADPC3 | ADPC2 | ADPC1 | ADPC0 |
| 0x0018 | **APCTL2** | ADPC15 | ADPC14 | ADPC13 | ADPC12 | ADPC11 | ADPC10 | ADPC9 | ADPC8 |
| 0x0019–0x001B | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x001C | **MTIMSC** | TOF | TOIE | TRST | TSTP | 0 | 0 | 0 | 0 |
| 0x001D | **MTIMCLK** | 0 | 0 | CLKS | | PS | | | |
| 0x001E | **MTIMCNT** | CNT | | | | | | | |
| 0x001F | **MTIMMOD** | MOD | | | | | | | |
| 0x0020 | **TPM1SC** | TOF | TOIE | CPWMS | CLKSB | CLKSA | PS2 | PS1 | PS0 |
| 0x0021 | **TPM1CNTH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0022 | **TPM1CNTL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0023 | **TPM1MODH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0024 | **TPM1MODL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0025 | **TPM1C0SC** | CH0F | CH0IE | MS0B | MS0A | ELS0B | ELS0A | 0 | 0 |
| 0x0026 | **TPM1C0VH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0027 | **TPM1C0VL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0028 | **TPM1C1SC** | CH1F | CH1IE | MS1B | MS1A | ELS1B | ELS1A | 0 | 0 |
| 0x0029 | **TPM1C1VH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x002A | **TPM1C1VL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

**Table 4-2. Direct-Page Register Summary (Sheet 2 of 3)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x002B–0x0037 | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| 0x0038 | **SCIBDH** | LBKDIE | RXEDGIE | 0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| 0x0039 | **SCIBDL** | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| 0x003A | **SCIC1** | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| 0x003B | **SCIC2** | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| 0x003C | **SCIS1** | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| 0x003D | **SCIS2** | LBKDIF | RXEDGIF | 0 | RXINV | RWUID | BRK13 | LBKDE | RAF |
| 0x003E | **SCIC3** | R8 | T8 | TXDIR | TXINV | ORIE | NEIE | FEIE | PEIE |
| 0x003F | **SCID** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0040–0x0047 | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| 0x0048 | **ICSC1** | CLKS | | RDIV | | | IREFS | IRCLKEN | IREFSTEN |
| 0x0049 | **ICSC2** | BDIV | | RANGE | HGO | LP | EREFS | ERCLKEN | EREFSTEN |
| 0x004A | **ICSTRM** | TRIM | | | | | | | |
| 0x004B | **ICSSC** | 0 | 0 | 0 | IREFST | CLKST | | OSCINIT | FTRIM |
| 0x004C–0x004F | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| 0x0050 | **SPIC1** | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| 0x0051 | **SPIC2** | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| 0x0052 | **SPIBR** | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| 0x0053 | **SPIS** | SPRF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| 0x0054 | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0055 | **SPID** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0056–0x0057 | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| 0x0058 | **IICA** | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | 0 |
| 0x0059 | **IICF** | MULT | | ICR | | | | | |
| 0x005A | **IICC1** | IICEN | IICIE | MST | TX | TXAK | RSTA | 0 | 0 |
| 0x005B | **IICS** | TCF | IAAS | BUSY | ARBL | 0 | SRW | IICIF | RXAK |
| 0x005C | **IICD** | DATA | | | | | | | |
| 0x005D | **IICC2** | GCAEN | ADEXT | 0 | 0 | 0 | AD10 | AD9 | AD8 |
| 0x005E–0x005F | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| 0x0060 | **TPM2SC** | TOF | TOIE | CPWMS | CLKSB | CLKSA | PS2 | PS1 | PS0 |
| 0x0061 | **TPM2CNTH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0062 | **TPM2CNTL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0063 | **TPM2MODH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0064 | **TPM2MODL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0065 | **TPM2C0SC** | CH0F | CH0IE | MS0B | MS0A | ELS0B | ELS0A | 0 | 0 |

**Table 4-2. Direct-Page Register Summary (Sheet 3 of 3)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0066 | **TPM2C0VH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x0067 | **TPM2C0VL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x0068 | **TPM2C1SC** | CH1F | CH1IE | MS1B | MS1A | ELS1B | ELS1A | 0 | 0 |
| 0x0069 | **TPM2C1VH** | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x006A | **TPM2C1VL** | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x006B | Reserved | — | — | — | — | — | — | — | — |
| 0x006C | **RTCSC** | RTIF | RTCLKS | | RTIE | RTCPS | | | |
| 0x006D | **RTCCNT** | RTCCNT | | | | | | | |
| 0x006E | **RTCMOD** | RTCMOD | | | | | | | |
| 0x006F - 0x007F | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |

High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at 0x1800.

**Table 4-3. High-Page Register Summary (Sheet 1 of 2)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x1800 | SRS | POR | PIN | COP | ILOP | ILAD | 0 | LVD | 0 |
| 0x1801 | SBDFR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BDFR |
| 0x1802 | SOPT1 | COPT | | STOPE | 0 | 0 | IICPS | 0 | 0 |
| 0x1803 | SOPT2 | COPCLKS | COPW | 0 | ACIC | T2CH1PS | T2CH0PS | T1CH1PS | T1CH0PS |
| 0x1804 – 0x1805 | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x1806 | SDIDH | 1 | — | — | — | ID11 | ID10 | ID9 | ID8 |
| 0x1807 | SDIDL | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 0x1808 | Reserved | — | — | — | — | — | — | — | — |
| 0x1809 | SPMSC1 | LVWF | LVWACK | LVWIE | LVDRE | LVDSE | LVDE | 0 | BGBE |
| 0x180A | SPMSC2 | 0 | 0 | LVDV | LVWV | PPDF | PPDACK | — | PPDC |
| 0x180B–0 x180F | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x1810 | DBGCAH | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x1811 | DBGCAL | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x1812 | DBGCBH | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x1813 | DBGCBL | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x1814 | DBGFH | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| 0x1815 | DBGFL | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0x1816 | DBGC | DBGEN | ARM | TAG | BRKEN | RWA | RWAEN | RWB | RWBEN |
| 0x1817 | DBGT | TRGSEL | BEGIN | 0 | 0 | TRG3 | TRG2 | TRG1 | TRG0 |
| 0x1818 | DBGS | AF | BF | ARMF | 0 | CNT3 | CNT2 | CNT1 | CNT0 |
| 0x1819–0x 181F | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x1820 | FCDIV | DIVLD | PRDIV8 | DIV | | | | | |
| 0x1821 | FOPT | KEYEN | FNORED | 0 | 0 | 0 | 0 | SEC | |
| 0x1822 | Reserved | — | — | — | — | — | — | — | — |
| 0x1823 | FCNFG | 0 | 0 | KEYACC | 0 | 0 | 0 | 0 | 0 |
| 0x1824 | FPROT | FPS | | | | | | | FPDIS |
| 0x1825 | FSTAT | FCBEF | FCCF | FPVIOL | FACCERR | 0 | FBLANK | 0 | 0 |
| 0x1826 | FCMD | FCMD | | | | | | | |
| 0x1827– 0x183F | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| 0x1840 | PTAPE | PTAPE7 | PTAPE6 | — | — | PTAPE3 | PTAPE2 | PTAPE1 | PTAPE0 |
| 0x1841 | PTASE | PTASE7 | PTASE6 | — | — | PTASE3 | PTASE2 | PTASE1 | PTASE0 |
| 0x1842 | PTADS | PTADS7 | PTADS6 | — | — | PTADS3 | PTADS2 | PTADS1 | PTADS0 |
| 0x1843 | Reserved | — | — | — | — | — | — | — | — |
| 0x1844 | PTASC | 0 | 0 | 0 | 0 | PTAIF | PTAACK | PTAIE | PTAMOD |

**Table 4-3. High-Page Register Summary (Sheet 2 of 2)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x1845 | **PTAPS** | 0 | 0 | 0 | 0 | PTAPS3 | PTAPS2 | PTAPS1 | PTAPS0 |
| 0x1846 | **PTAES** | 0 | 0 | 0 | 0 | PTAES3 | PTAES2 | PTAES1 | PTAES0 |
| 0x1847 | Reserved | — | — | — | — | — | — | — | — |
| 0x1848 | **PTBPE** | PTBPE7 | PTBPE6 | PTBPE5 | PTBPE4 | PTBPE3 | PTBPE2 | PTBPE1 | PTBPE0 |
| 0x1849 | **PTBSE** | PTBSE7 | PTBSE6 | PTBSE5 | PTBSE4 | PTBSE3 | PTBSE2 | PTBSE1 | PTBSE0 |
| 0x184A | **PTBDS** | PTBDS7 | PTBDS6 | PTBDS5 | PTBDS4 | PTBDS3 | PTBDS2 | PTBDS1 | PTBDS0 |
| 0x184B | Reserved | — | — | — | — | — | — | — | — |
| 0x184C | **PTBSC** | 0 | 0 | 0 | 0 | PTBIF | PTBACK | PTBIE | PTBMOD |
| 0x184D | **PTBPS** | 0 | 0 | 0 | 0 | PTBPS3 | PTBPS2 | PTBPS1 | PTBPS0 |
| 0x184E | **PTBES** | 0 | 0 | 0 | 0 | PTBES3 | PTBES2 | PTBES1 | PTBES0 |
| 0x184F | Reserved | — | — | — | — | — | — | — | — |
| 0x1850 | **PTCPE** | PTCPE7 | PTCPE6 | PTCPE5 | PTCPE4 | PTCPE3 | PTCPE2 | PTCPE1 | PTCPE0 |
| 0x1851 | **PTCSE** | PTCSE7 | PTCSE6 | PTCSE5 | PTCSE4 | PTCSE3 | PTCSE2 | PTCSE1 | PTCSE0 |
| 0x1852 | **PTCDS** | PTCDS7 | PTCDS6 | PTCDS5 | PTCDS4 | PTCDS3 | PTCDS2 | PTCDS1 | PTCDS0 |
| 0x1853 | **GNGC** | GNGPS7 | GNGPS6 | GNGPS5 | GNGPS4 | GNGPS3 | GNGPS2 | GNGPS1 | GNGEN |
| 0x1854 | Reserved | — | — | — | — | — | 1 | 1 | 1 |
| 0x1855 | Reserved | — | — | — | — | — | 1 | 1 | 1 |
| 0x1856 | Reserved | — | — | — | — | — | 0 | 0 | 0 |
| 0x1857–<br>0x185F | Reserved | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |

Nonvolatile FLASH registers, shown in Table 4-4, are located in the FLASH memory. These registers include an 8-byte backdoor key, NVBACKKEY, which can be used to gain access to secure memory resources. During reset events, the contents of NVPROT and NVOPT in the nonvolatile register area of the FLASH memory are transferred into corresponding FPROT and FOPT working registers in the high-page registers to control security and block protection options.

**Table 4-4. Nonvolatile Register Summary**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **0xFFAE** | **NVFTRIM** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FTRIM |
| **0xFFAF** | **NVTRIM** | TRIM | | | | | | | |
| **0xFFB0 – 0xFFB7** | **NVBACKKEY** | 8-Byte Comparison Key | | | | | | | |
| **0xFFB8 – 0xFFBC** | Reserved | — — | — — | — — | — — | — — | — — | — — | — — |
| **0xFFBD** | **NVPROT** | FPS | | | | | | | FPDIS |
| **0xFFBE** | Reserved | — | — | — | — | — | — | — | — |
| **0xFFBF** | **NVOPT** | KEYEN | FNORED | 0 | 0 | 0 | 0 | SEC | |

Provided the key enable (KEYEN) bit is 1, the 8-byte comparison key can be used to temporarily disengage memory security. This key mechanism can be accessed only through user code running in secure memory. (A security key cannot be entered directly through background debug commands.) This security key can be disabled completely by programming the KEYEN bit to 0. If the security key is disabled, the only way to disengage security is by mass erasing the FLASH if needed (normally through the background debug interface) and verifying that FLASH is blank. To avoid returning to secure mode after the next reset, program the security bits (SEC) to the unsecured state (1:0).

## 4.4 RAM

The MC9S08SG32 Series includes static RAM. The locations in RAM below 0x0100 can be accessed using the more efficient direct addressing mode, and any single bit in this area can be accessed with the bit manipulation instructions (BCLR, BSET, BRCLR, and BRSET). Locating the most frequently accessed program variables in this area of RAM is preferred.

The RAM retains data when the MCU is in low-power wait, stop2, or stop3 mode. At power-on the contents of RAM are uninitialized. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention ($V_{RAM}$).

For compatibility with M68HC05 MCUs, the HCS08 resets the stack pointer to 0x00FF. In the MC9S08SG32 Series, it is usually best to reinitialize the stack pointer to the top of the RAM so the direct page RAM can be used for frequently accessed RAM variables and bit-addressable program variables. Include the following 2-instruction sequence in your reset initialization routine (where RamLast is equated to the highest address of the RAM in the Freescale Semiconductor-provided equate file).

```
LDHX    #RamLast+1    ;point one past RAM
TXS                   ;SP<-(H:X-1)
```

When security is enabled, the RAM is considered a secure memory resource and is not accessible through BDM or through code executing from non-secure memory. See Section 4.6, “Security”, for a detailed description of the security feature.

## 4.5 FLASH

The FLASH memory is intended primarily for program storage. In-circuit programming allows the operating program to be loaded into the FLASH memory after final assembly of the application product. It is possible to program the entire array through the single-wire background debug interface. Because no special voltages are needed for FLASH erase and programming operations, in-application programming is also possible through other software-controlled communication paths. For a more detailed discussion of in-circuit and in-application programming, refer to the *HCS08 Family Reference Manual, Volume I,* Freescale Semiconductor document order number HCS08RMv1/D.

### 4.5.1 Features

Features of the FLASH memory include:

- FLASH size
  - MC9S08SG32: 32,768 bytes (64 pages of 512 bytes each)
  - MC9S08SG16: 16,384 bytes (32 pages of 512 bytes each)
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature
- Flexible block protection and vector redirection
- Security feature for FLASH and RAM
- Auto power-down for low-frequency read accesses

### 4.5.2 Program and Erase Times

Before any program or erase command can be accepted, the FLASH clock divider register (FCDIV) must be written to set the internal clock for the FLASH module to a frequency ($f_{FCLK}$) between 150 kHz and 200 kHz (see Section 4.7.1, “FLASH Clock Divider Register (FCDIV)”). This register can be written only once, so normally this write is done during reset initialization. FCDIV cannot be written if the access error flag, FACCERR in FSTAT, is set. The user must ensure that FACCERR is not set before writing to the FCDIV register. One period of the resulting clock ($1/f_{FCLK}$) is used by the command processor to time program and erase pulses. An integer number of these timing pulses are used by the command processor to complete a program or erase command.

Table 4-5 shows program and erase times. The bus clock frequency and FCDIV determine the frequency of FCLK ($f_{FCLK}$). The time for one cycle of FCLK is $t_{FCLK} = 1/f_{FCLK}$. The times are shown as a number of cycles of FCLK and as an absolute time for the case where $t_{FCLK} = 5$ µs. Program and erase times shown include overhead for the command state machine and enabling and disabling of program and erase voltages.

**Table 4-5. Program and Erase Times**

| Parameter | Cycles of FCLK | Time if FCLK = 200 kHz |
|---|---|---|
| Byte program | 9 | 45 µs |
| Byte program (burst) | 4 | 20 µs[1] |
| Page erase | 4000 | 20 ms |
| Mass erase | 20,000 | 100 ms |

1 Excluding start/end overhead

### 4.5.3 Program and Erase Command Execution

The steps for executing any of the commands are listed below. The FCDIV register must be initialized and any error flags cleared before beginning command execution. The command execution steps are:

1. Write a data value to an address in the FLASH array. The address and data information from this write is latched into the FLASH interface. This write is a required first step in any command sequence. For erase and blank check commands, the value of the data is not important. For page erase commands, the address may be any address in the 512-byte page of FLASH to be erased. For mass erase and blank check commands, the address can be any address in the FLASH memory. Whole pages of 512 bytes are the smallest block of FLASH that may be erased.

   **NOTE**

   Do not program any byte in the FLASH more than once after a successful erase operation. Reprogramming bits to a byte that is already programmed is not allowed without first erasing the page in which the byte resides or mass erasing the entire FLASH memory. Programming without first erasing may disturb data stored in the FLASH.

2. Write the command code for the desired command to FCMD. The five valid commands are blank check (0x05), byte program (0x20), burst program (0x25), page erase (0x40), and mass erase (0x41). The command code is latched into the command buffer.
3. Write a 1 to the FCBEF bit in FSTAT to clear FCBEF and launch the command (including its address and data information).

A partial command sequence can be aborted manually by writing a 0 to FCBEF any time after the write to the memory array and before writing the 1 that clears FCBEF and launches the complete command. Aborting a command in this way sets the FACCERR access error flag, which must be cleared before starting a new command.

A strictly monitored procedure must be obeyed or the command will not be accepted. This minimizes the possibility of any unintended changes to the FLASH memory contents. The command complete flag (FCCF) indicates when a command is complete. The command sequence must be completed by clearing FCBEF to launch the command. Figure 4-2 is a flowchart for executing all of the commands except for burst programming. The FCDIV register must be initialized before using any FLASH commands. This must be done only once following a reset.

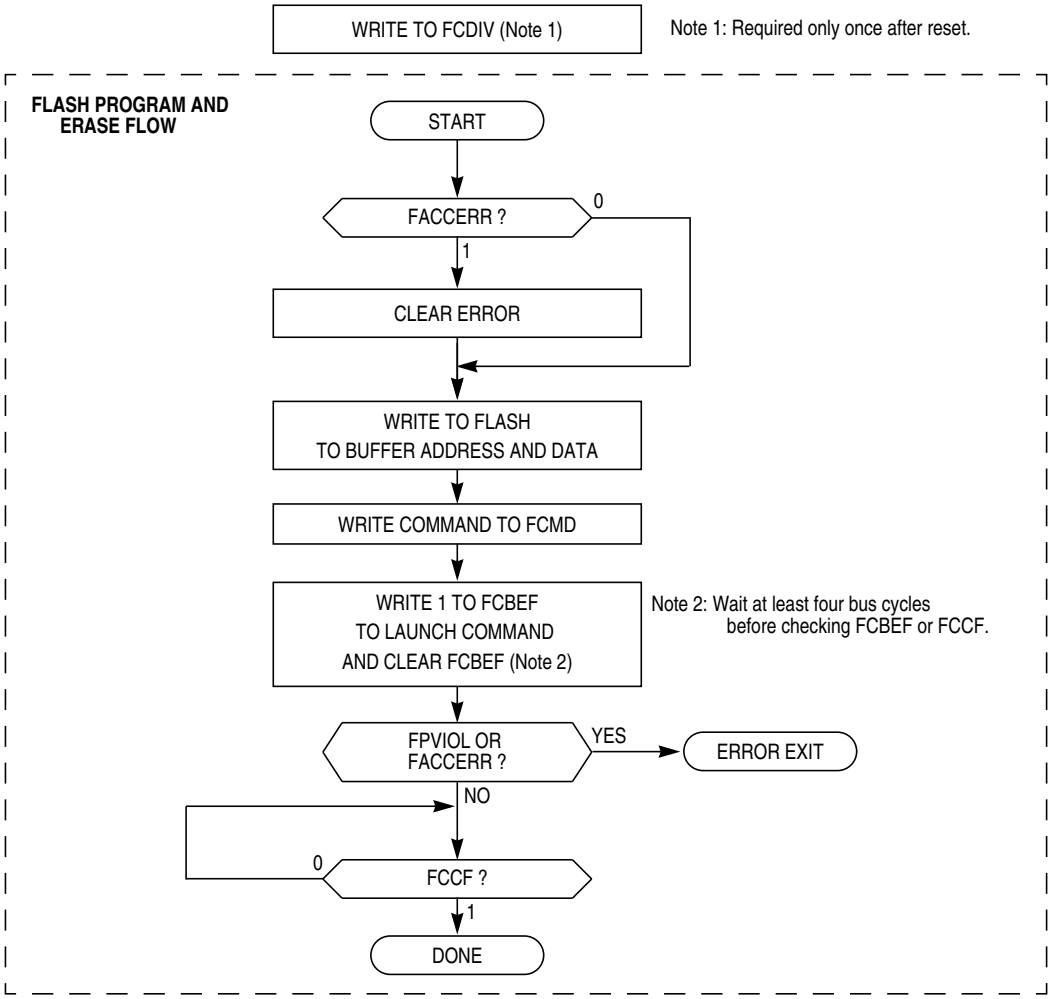



**Figure 4-2. FLASH Program and Erase Flowchart**

## 4.5.4 Burst Program Execution

The burst program command is used to program sequential bytes of data in less time than would be required using the standard program command. This is possible because the high voltage to the FLASH array does not need to be disabled between program operations. Ordinarily, when a program or erase command is issued, an internal charge pump associated with the FLASH memory must be enabled to supply high voltage to the array. Upon completion of the command, the charge pump is turned off. When a burst program command is issued, the charge pump is enabled and then remains enabled after completion of the burst program operation if these two conditions are met:

- The next burst program command has been queued before the current program operation has completed.
- The next sequential address selects a byte on the same physical row as the current byte being programmed. A row of FLASH memory consists of 64 bytes. A byte within a row is selected by addresses A5 through A0. A new row begins when addresses A5 through A0 are all zero.

The first byte of a series of sequential bytes being programmed in burst mode will take the same amount of time to program as a byte programmed in standard mode. Subsequent bytes will program in the burst program time provided that the conditions above are met. In the case the next sequential address is the beginning of a new row, the program time for that byte will be the standard time instead of the burst time. This is because the high voltage to the array must be disabled and then enabled again. If a new burst command has not been queued before the current command completes, then the charge pump will be disabled and high voltage removed from the array.

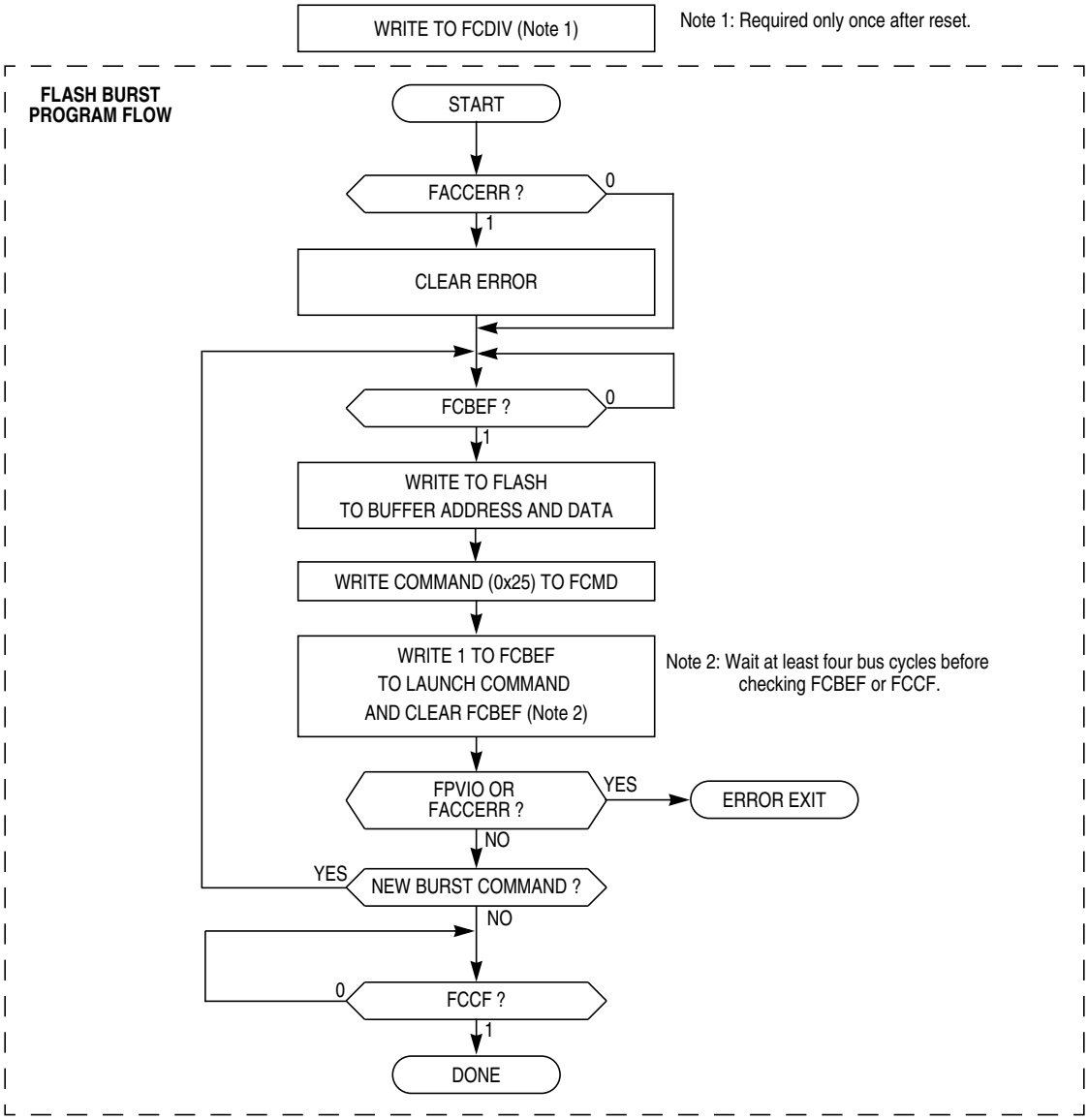



**Figure 4-3. FLASH Burst Program Flowchart**

### 4.5.5 Access Errors

An access error occurs whenever the command execution protocol is violated.

Any of the following specific actions will cause the access error flag (FACCERR) in FSTAT to be set. Before any command can be processed, write a 1 to FACCERR in FSTAT to clear the access error flag (FACCERR).

- Writing to a FLASH address before the internal FLASH clock frequency has been set by writing to the FCDIV register
- Writing to a FLASH address while FCBEF is not set (A new command cannot be started until the command buffer is empty.)
- Writing a second time to a FLASH address before launching the previous command (There is only one write to FLASH for every command.)
- Writing a second time to FCMD before launching the previous command (There is only one write to FCMD for every command.)
- Writing to any FLASH control register other than FCMD after writing to a FLASH address
- Writing any command code other than the five allowed codes (0x05, 0x20, 0x25, 0x40, or 0x41) to FCMD
- Writing any FLASH control register other than the write to FSTAT (to clear FCBEF and launch the command) after writing the command to FCMD
- The MCU enters stop mode while a program or erase command is in progress (The command is aborted.)
- Writing the byte program, burst program, or page erase command code (0x20, 0x25, or 0x40) with a background debug command while the MCU is secured (The background debug controller can only do blank check and mass erase commands when the MCU is secure.)
- Writing 0 to FCBEF to cancel a partial command

### 4.5.6 FLASH Block Protection

The block protection feature prevents the protected region of FLASH from program or erase changes. Block protection is controlled through the FLASH protection register (FPROT). When enabled, block protection begins at any 512 byte boundary below the last address of FLASH, 0xFFFF. (See Section 4.7.4, “FLASH Protection Register (FPROT and NVPROT)”).

After exit from reset, FPROT is loaded with the contents of the NVPROT location, which is in the nonvolatile register block of the FLASH memory. FPROT cannot be changed directly from application software so a runaway program cannot alter the block protection settings. Because NVPROT is within the last 512 bytes of FLASH, if any amount of memory is protected, NVPROT is itself protected and cannot be altered (intentionally or unintentionally) by the application software. FPROT can be written through background debug commands, which allows a way to erase and reprogram a protected FLASH memory.

The block protection mechanism is illustrated in Figure 4-4. The FPS bits are used as the upper bits of the last address of unprotected memory. This address is formed by concatenating FPS7:FPS1 with logic 1 bits as shown. For example, to protect the last 1536 bytes of memory (addresses 0xFA00 through 0xFFFF), the FPS bits must be set to 1111 100, which results in the value 0xF9FF as the last address of unprotected

memory. In addition to programming the FPS bits to the appropriate value, FPDIS (bit 0 of NVPROT) must be programmed to logic 0 to enable block protection. Therefore the value 0xF8 must be programmed into NVPROT to protect addresses 0xFA00 through 0xFFFF.

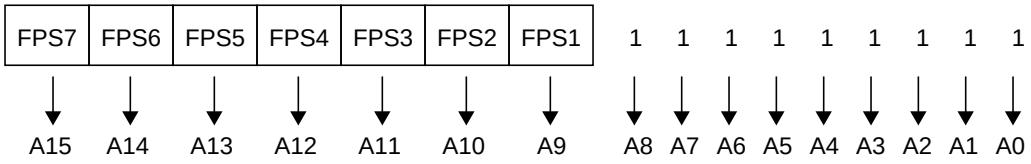



**Figure 4-4. Block Protection Mechanism**

One use for block protection is to block protect an area of FLASH memory for a bootloader program. This bootloader program then can be used to erase the rest of the FLASH memory and reprogram it. Because the bootloader is protected, it remains intact even if MCU power is lost in the middle of an erase and reprogram operation.

### 4.5.7 Vector Redirection

Whenever any block protection is enabled, the reset and interrupt vectors will be protected. Vector redirection allows users to modify interrupt vector information without unprotecting bootloader and reset vector space. Vector redirection is enabled by programming the FNORED bit in the NVOPT register located at address 0xFFBF to zero. For redirection to occur, at least some portion but not all of the FLASH memory must be block protected by programming the NVPROT register located at address 0xFFBD. All of the interrupt vectors (memory locations 0xFFC0–0xFFFD) are redirected, though the reset vector (0xFFFE:FFFF) is not.

For example, if 512 bytes of FLASH are protected, the protected address region is from 0xFE00 through 0xFFFF. The interrupt vectors (0xFFC0–0xFFFD) are redirected to the locations 0xFDC0–0xFDFD. Now, if an SPI interrupt is taken for instance, the values in the locations 0xFDE0:FDE1 are used for the vector instead of the values in the locations 0xFFE0:FFE1. This allows the user to reprogram the unprotected portion of the FLASH with new program code including new interrupt vector values while leaving the protected area, which includes the default vector locations, unchanged.

## 4.6 Security

The MC9S08SG32 Series includes circuitry to prevent unauthorized access to the contents of FLASH and RAM memory. When security is engaged, FLASH and RAM are considered secure resources. Direct-page registers, high-page registers, and the background debug controller are considered unsecured resources. Programs executing within secure memory have normal access to any MCU memory locations and resources. Attempts to access a secure memory location with a program executing from an unsecured memory space or through the background debug interface are blocked (writes are ignored and reads return all 0s).

Security is engaged or disengaged based on the state of two nonvolatile register bits (SEC01:SEC00) in the FOPT register. During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into the working FOPT register in high-page register space. A user engages security by programming the NVOPT location which can be done at the same time the FLASH memory is programmed. The 1:0 state

disengages security and the other three combinations engage security. Notice the erased state (1:1) makes the MCU secure. During development, whenever the FLASH is erased, it is good practice to immediately program the SEC00 bit to 0 in NVOPT so SEC01:SEC00 = 1:0. This would allow the MCU to remain unsecured after a subsequent reset.

The on-chip debug module cannot be enabled while the MCU is secure. The separate background debug controller can still be used for background memory access commands of unsecured resources.

A user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. If the nonvolatile KEYEN bit in NVOPT/FOPT is 0, the backdoor key is disabled and there is no way to disengage security without completely erasing all FLASH locations. If KEYEN is 1, a secure user program can temporarily disengage security by:

1. Writing 1 to KEYACC in the FCNFG register. This makes the FLASH module interpret writes to the backdoor comparison key locations (NVBACKKEY through NVBACKKEY+7) as values to be compared against the key rather than as the first step in a FLASH program or erase command.
2. Writing the user-entered key values to the NVBACKKEY through NVBACKKEY+7 locations. These writes must be done in order starting with the value for NVBACKKEY and ending with NVBACKKEY+7. STHX should not be used for these writes because these writes cannot be done on adjacent bus cycles. User software normally would get the key codes from outside the MCU system through a communication interface such as a serial I/O.
3. Writing 0 to KEYACC in the FCNFG register. If the 8-byte key that was just written matches the key stored in the FLASH locations, SEC01:SEC00 are automatically changed to 1:0 and security will be disengaged until the next reset.

The security key can be written only from secure memory (either RAM or FLASH), so it cannot be entered through background commands without the cooperation of a secure user program.

The backdoor comparison key (NVBACKKEY through NVBACKKEY+7) is located in FLASH memory locations in the nonvolatile register space so users can program these locations exactly as they would program any other FLASH memory location. The nonvolatile registers are in the same 512-byte block of FLASH as the reset and interrupt vectors, so block protecting that space also block protects the backdoor comparison key. Block protects cannot be changed from user application programs, so if the vector space is block protected, the backdoor security key mechanism cannot permanently change the block protect, security settings, or the backdoor key.

Security can always be disengaged through the background debug interface by taking these steps:

1. Disable any block protections by writing FPROT. FPROT can be written only with background debug commands, not from application software.
2. Mass erase FLASH if necessary.
3. Blank check FLASH. Provided FLASH is completely erased, security is disengaged until the next reset.

   To avoid returning to secure mode after the next reset, program NVOPT so SEC01:SEC00 = 1:0.

## 4.7 FLASH Registers and Control Bits

The FLASH module has nine 8-bit registers in the high-page register space, two locations (NVOPT, NVPROT) in the nonvolatile register space in FLASH memory are copied into corresponding high-page control registers (FOPT, FPROT) at reset. There is also an 8-byte comparison key in FLASH memory. Refer to Table 4-3 and Table 4-4 for the absolute address assignments for all FLASH registers. This section refers to registers and control bits only by their names. A Freescale Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

### 4.7.1 FLASH Clock Divider Register (FCDIV)

Bit 7 of this register is a read-only flag. Bits 6:0 may be read at any time but can be written only one time. Before any erase or programming operations are possible, write to this register to set the frequency of the clock for the nonvolatile memory system within acceptable limits.

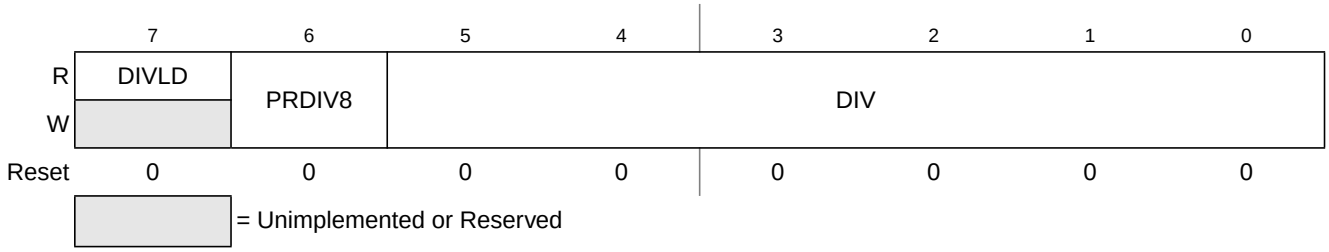



**Figure 4-5. FLASH Clock Divider Register (FCDIV)**

**Table 4-6. FCDIV Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>DIVLD | **Divisor Loaded Status Flag** — When set, this read-only status flag indicates that the FCDIV register has been written since reset. Reset clears this bit and the first write to this register causes this bit to become set regardless of the data written.<br>0 FCDIV has not been written since reset; erase and program operations disabled for FLASH.<br>1 FCDIV has been written since reset; erase and program operations enabled for FLASH. |
| 6<br>PRDIV8 | **Prescale (Divide) FLASH Clock by 8**<br>0 Clock input to the FLASH clock divider is the bus rate clock.<br>1 Clock input to the FLASH clock divider is the bus rate clock divided by 8. |
| 5:0<br>DIV | **Divisor for FLASH Clock Divider** — The FLASH clock divider divides the bus rate clock (or the bus rate clock divided by 8 if PRDIV8 = 1) by the value in the 6-bit DIV field plus one. The resulting frequency of the internal FLASH clock must fall within the range of 200 kHz to 150 kHz for proper FLASH operations. Program/Erase timing pulses are one cycle of this internal FLASH clock which corresponds to a range of 5 µs to 6.7 µs. The automated programming logic uses an integer number of these pulses to complete an erase or program operation. See Equation 4-1 and Equation 4-2. |

$$\text{if PRDIV8 = 0 — } f_{FCLK} = f_{Bus} \div (\text{DIV} + 1) \qquad \textit{Eqn. 4-1}$$

$$\text{if PRDIV8 = 1 — } f_{FCLK} = f_{Bus} \div (8 \times (\text{DIV} + 1)) \qquad \textit{Eqn. 4-2}$$

Table 4-7 shows the appropriate values for PRDIV8 and DIV for selected bus frequencies.

**Table 4-7. FLASH Clock Divider Settings**

| $f_{Bus}$ | PRDIV8 (Binary) | DIV (Decimal) | $f_{FCLK}$ | Program/Erase Timing Pulse (5 µs Min, 6.7 µs Max) |
|---|---|---|---|---|
| 20 MHz | 1 | 12 | 192.3 kHz | 5.2 µs |
| 10 MHz | 0 | 49 | 200 kHz | 5 µs |
| 8 MHz | 0 | 39 | 200 kHz | 5 µs |
| 4 MHz | 0 | 19 | 200 kHz | 5 µs |
| 2 MHz | 0 | 9 | 200 kHz | 5 µs |
| 1 MHz | 0 | 4 | 200 kHz | 5 µs |
| 200 kHz | 0 | 0 | 200 kHz | 5 µs |
| 150 kHz | 0 | 0 | 150 kHz | 6.7 µs |

## 4.7.2 FLASH Options Register (FOPT and NVOPT)

During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into FOPT. To change the value in this register, erase and reprogram the NVOPT location in FLASH memory as usual and then issue a new MCU reset.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | KEYEN | FNORED | 0 | 0 | 0 | 0 | SEC01 | SEC00 |
| W | | | | | | | | |
| Reset | This register is loaded from nonvolatile location NVOPT during reset. | | | | | | | |

= Unimplemented or Reserved

**Figure 4-6. FLASH Options Register (FOPT)**

**Table 4-8. FOPT Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>KEYEN | **Backdoor Key Mechanism Enable** — When this bit is 0, the backdoor key mechanism cannot be used to disengage security. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. For more detailed information about the backdoor key mechanism, refer to Section 4.6, “Security.”<br>0 No backdoor key access allowed.<br>1 If user firmware writes an 8-byte value that matches the nonvolatile backdoor key (NVBACKKEY through NVBACKKEY+7 in that order), security is temporarily disengaged until the next MCU reset. |
| 6<br>FNORED | **Vector Redirection Disable** — When this bit is 1, then vector redirection is disabled.<br>0 Vector redirection enabled.<br>1 Vector redirection disabled. |
| 1:0<br>SEC0[1:0] | **Security State Code** — This 2-bit field determines the security state of the MCU as shown in Table 4-9. When the MCU is secure, the contents of RAM and FLASH memory cannot be accessed by instructions from any unsecured source including the background debug interface. SEC01:SEC00 changes to 1:0 after successful backdoor key entry or a successful blank check of FLASH.<br>For more detailed information about security, refer to Section 4.6, “Security.” |

**Table 4-9. Security States[1]**

| SEC01:SEC00 | Description |
|---|---|
| 0:0 | secure |
| 0:1 | secure |
| 1:0 | unsecured |
| 1:1 | secure |

1 SEC01:SEC00 changes to 1:0 after successful backdoor key entry or a successful blank check of FLASH.

## 4.7.3 FLASH Configuration Register (FCNFG)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | KEYACC | 0 | 0 | 0 | 0 | 0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 4-7. FLASH Configuration Register (FCNFG)**

**Table 4-10. FCNFG Register Field Descriptions**

| Field | Description |
|---|---|
| 5<br>KEYACC | **Enable Writing of Access Key** — This bit enables writing of the backdoor comparison key. For more detailed information about the backdoor key mechanism, refer to Section 4.6, “Security.”<br>0 Writes to 0xFFB0–0xFFB7 are interpreted as the start of a FLASH programming or erase command.<br>1 Writes to NVBACKKEY (0xFFB0–0xFFB7) are interpreted as comparison key writes. |

## 4.7.4 FLASH Protection Register (FPROT and NVPROT)

During reset, the contents of the nonvolatile location NVPROT are copied from FLASH into FPROT. This register can be read at any time. If FPDIS = 0, protection can be increased (that is, a smaller value of FPS can be written). If FPDIS = 1, writes do not change protection.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | FPS(1) | | | | | | | FPDIS(1) |
| W | | | | | | | | |
| Reset | This register is loaded from nonvolatile location NVPROT during reset. | | | | | | | |

1 Background commands can be used to change the contents of these bits in FPROT.

**Figure 4-8. FLASH Protection Register (FPROT)**

**Table 4-11. FPROT Register Field Descriptions**

| Field | Description |
|---|---|
| 7:1<br>FPS | **FLASH Protect Select Bits** — When FPDIS = 0, this 7-bit field determines the ending address of unprotected FLASH locations at the high address end of the FLASH. Protected FLASH locations cannot be erased or programmed. |
| 0<br>FPDIS | **FLASH Protection Disable**<br>0 FLASH block specified by FPS[7:1] is block protected (program and erase not allowed).<br>1 No FLASH block is protected. |

## 4.7.5 FLASH Status Register (FSTAT)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | FCBEF | FCCF | FPVIOL | FACCERR | 0 | FBLANK | 0 | 0 |
| W | | | | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 4-9. FLASH Status Register (FSTAT)**

**Table 4-12. FSTAT Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>FCBEF | **FLASH Command Buffer Empty Flag** — The FCBEF bit is used to launch commands. It also indicates that the command buffer is empty so that a new command sequence can be executed when performing burst programming. The FCBEF bit is cleared by writing a 1 to it or when a burst program command is transferred to the array for programming. Only burst program commands can be buffered.<br>0 Command buffer is full (not ready for additional commands).<br>1 A new burst program command can be written to the command buffer. |
| 6<br>FCCF | **FLASH Command Complete Flag** — FCCF is set automatically when the command buffer is empty and no command is being processed. FCCF is cleared automatically when a new command is started (by writing 1 to FCBEF to register a command). Writing to FCCF has no meaning or effect.<br>0 Command in progress<br>1 All commands complete |
| 5<br>FPVIOL | **Protection Violation Flag** — FPVIOL is set automatically when a command is written that attempts to erase or program a location in a protected block (the erroneous command is ignored). FPVIOL is cleared by writing a 1 to FPVIOL.<br>0 No protection violation.<br>1 An attempt was made to erase or program a protected location. |

**Table 4-12. FSTAT Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 4<br>FACCERR | **Access Error Flag** — FACCERR is set automatically when the proper command sequence is not obeyed exactly (the erroneous command is ignored), if a program or erase operation is attempted before the FCDIV register has been initialized, or if the MCU enters stop while a command was in progress. For a more detailed discussion of the exact actions that are considered access errors, see Section 4.5.5, "Access Errors." FACCERR is cleared by writing a 1 to FACCERR. Writing a 0 to FACCERR has no meaning or effect.<br>0 No access error.<br>1 An access error has occurred. |
| 2<br>FBLANK | **FLASH Verified as All Blank (erased) Flag** — FBLANK is set automatically at the conclusion of a blank check command if the entire FLASH array was verified to be erased. FBLANK is cleared by clearing FCBEF to write a new valid command. Writing to FBLANK has no meaning or effect.<br>0 After a blank check command is completed and FCCF = 1, FBLANK = 0 indicates the FLASH array is not completely erased.<br>1 After a blank check command is completed and FCCF = 1, FBLANK = 1 indicates the FLASH array is completely erased (all 0xFF). |

## 4.7.6 FLASH Command Register (FCMD)

Only five command codes are recognized in normal user modes as shown in Table 4-13. Refer to Section 4.5.3, "Program and Erase Command Execution," for a detailed discussion of FLASH programming and erase operations.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | FCMD | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 4-10. FLASH Command Register (FCMD)**

**Table 4-13. FLASH Commands**

| Command | FCMD | Equate File Label |
|---|---|---|
| Blank check | 0x05 | mBlank |
| Byte program | 0x20 | mByteProg |
| Byte program — burst mode | 0x25 | mBurstProg |
| Page erase (512 bytes/page) | 0x40 | mPageErase |
| Mass erase (all FLASH) | 0x41 | mMassErase |

All other command codes are illegal and generate an access error.

It is not necessary to perform a blank check command after a mass erase operation. Only blank check is required as part of the security unlocking mechanism.

# Chapter 5
# Resets, Interrupts, and General System Control

## 5.1 Introduction

This section discusses basic reset and interrupt mechanisms and the various sources of reset and interrupt in the MC9S08SG32 Series. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data sheet. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog are not part of on-chip peripheral systems with their own chapters.

## 5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation
- System reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vector for each module (reduces polling overhead) (see Table 5-2)

## 5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with pull-up devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

The MC9S08SG32 Series has the following sources for reset:

- Power-on reset (POR)
- External pin reset (PIN)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect (ILOP)
- Illegal address detect (ILAD) - any address in memory map that is listed as unimplemented will produce an illegal address reset
- Background debug forced reset

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register (SRS).

## 5.4 Computer Operating Properly (COP) Watchdog

The COP watchdog is intended to force a system reset when the application software fails to execute as expected. To prevent a system reset from the COP timer (when it is enabled), application software must reset the COP counter periodically. If the application program gets lost and fails to reset the COP counter before it times out, a system reset is generated to force the system back to a known starting point.

After any reset, the COP watchdog is enabled (see Section 5.7.3, "System Options Register 1 (SOPT1)," for additional information). If the COP watchdog is not used in an application, it can be disabled by clearing COPT bits in SOPT1.

The COP counter is reset by writing 0x0055 and 0x00AA (in this order) to the address of SRS during the selected timeout period. Writes do not affect the data in the read-only SRS. As soon as the write sequence is done, the COP timeout period is restarted. If the program fails to do this during the time-out period, the MCU will reset. Also, if any value other than 0x0055 or 0x00AA is written to SRS, the MCU is immediately reset.

The COPCLKS bit in SOPT2 (see Section 5.7.4, "System Options Register 2 (SOPT2)," for additional information) selects the clock source used for the COP timer. The clock source options are either the bus clock or an internal 1-kHz clock source. With each clock source, there are three associated time-outs controlled by the COPT bits in SOPT1. Table 5-1 summaries the control functions of the COPCLKS and COPT bits. The COP watchdog defaults to operation from the 1-kHz clock source and the longest time-out ($2^{10}$ cycles).

**Table 5-1. COP Configuration Options**

| Control Bits | | Clock Source | COP Window[1] Opens (COPW = 1) | COP Overflow Count |
|---|---|---|---|---|
| COPCLKS | COPT[1:0] | | | |
| N/A | 0:0 | N/A | N/A | COP is disabled |
| 0 | 0:1 | 1 kHz | N/A | $2^5$ cycles (32 ms[2]) |
| 0 | 1:0 | 1 kHz | N/A | $2^8$ cycles (256 ms[1]) |
| 0 | 1:1 | 1 kHz | N/A | $2^{10}$ cycles (1.024 s[1]) |
| 1 | 0:1 | Bus | 6144 cycles | $2^{13}$ cycles |
| 1 | 1:0 | Bus | 49,152 cycles | $2^{16}$ cycles |
| 1 | 1:1 | Bus | 196,608 cycles | $2^{18}$ cycles |

1 Windowed COP operation requires the user to clear the COP timer in the last 25% of the selected timeout period. This column displays the minimum number of clock counts required before the COP timer can be reset when in windowed COP mode (COPW = 1).

2 Values shown in milliseconds based on $t_{LPO}$ = 1 ms. See $t_{LPO}$ in the appendix Section A.12.1, "Control Timing," for the tolerance of this value.

When the bus clock source is selected, windowed COP operation is available by setting COPW in the SOPT2 register. In this mode, writes to the SRS register to clear the COP timer must occur in the last 25% of the selected timeout period. A premature write immediately resets the MCU. When the 1-kHz clock source is selected, windowed COP operation is not available.

The COP counter is initialized by the first writes to the SOPT1 and SOPT2 registers after any system reset. Subsequent writes to SOPT1 and SOPT2 have no effect on COP operation. Even if the application will use the reset default settings of COPT, COPCLKS, and COPW bits, the user should write to the write-once SOPT1 and SOPT2 registers during reset initialization to lock in the settings. This will prevent accidental changes if the application program gets lost.

The write to SRS that services (clears) the COP counter should not be placed in an interrupt service routine (ISR) because the ISR could continue to be executed periodically even if the main application program fails.

If the bus clock source is selected, the COP counter does not increment while the MCU is in background debug mode or while the system is in stop mode. The COP counter resumes when the MCU exits background debug mode or stop mode.

If the 1-kHz clock source is selected, the COP counter is re-initialized to zero upon entry to either background debug mode or stop mode and begins from zero upon exit from background debug mode or stop mode.

## 5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on a pin interrupt or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will become set. The CPU will not respond unless the local interrupt enable is a 1 to enable the interrupt and the I bit in the CCR is 0 to allow interrupts. The global interrupt mask (I bit) in the CCR is initially set after reset which prevents all maskable interrupt sources. The user program initializes the stack pointer and performs other system setup before clearing the I bit to allow the CPU to respond to interrupts.

When the CPU receives a qualified interrupt request, it completes the current instruction before responding to the interrupt. The interrupt sequence obeys the same cycle-by-cycle sequence as the SWI instruction and consists of:

- Saving the CPU registers on the stack
- Setting the I bit in the CCR to mask further interrupts
- Fetching the interrupt vector for the highest-priority interrupt that is currently pending
- Filling the instruction queue with the first three bytes of program information starting from the address fetched from the interrupt vector locations

While the CPU is responding to the interrupt, the I bit is automatically set to avoid the possibility of another interrupt interrupting the ISR itself (this is called nesting of interrupts). Normally, the I bit is restored to 0 when the CCR is restored from the value stacked on entry to the ISR. In rare cases, the I bit can be cleared inside an ISR (after clearing the status flag that generated the interrupt) so that other interrupts can be serviced without waiting for the first service routine to finish. This practice is not recommended for anyone

other than the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction which restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information from the stack.

**NOTE**

For compatibility with M68HC08 devices, the H register is not automatically saved and restored. It is good programming practice to push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

If more than one interrupt is pending when the I bit is cleared, the highest priority source is serviced first (see Table 5-2).

### 5.5.1 Interrupt Stack Frame

Figure 5-1 shows the contents and organization of a stack frame. Before the interrupt, the stack pointer (SP) points at the next available byte location on the stack. The current values of CPU registers are stored on the stack starting with the low-order byte of the program counter (PCL) and ending with the CCR. After stacking, the SP points at the next available location on the stack which is the address that is one less than the address where the CCR was saved. The PC value that is stacked is the address of the instruction in the main program that would have executed next if the interrupt had not occurred.

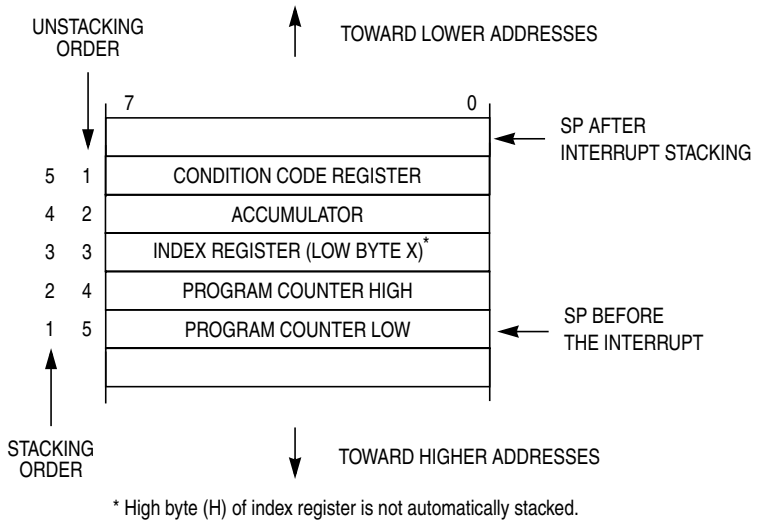



**Figure 5-1. Interrupt Stack Frame**

When an RTI instruction is executed, these values are recovered from the stack in reverse order. As part of the RTI sequence, the CPU fills the instruction pipeline by reading three bytes of program information, starting from the PC address recovered from the stack.

The status flag corresponding to the interrupt source must be acknowledged (cleared) before returning from the ISR. Typically, the flag is cleared at the beginning of the ISR so that if another interrupt is generated by this same source, it will be registered so it can be serviced after completion of the current ISR.

### 5.5.2 Interrupt Vectors, Sources, and Local Masks

Table 5-2 provides a summary of all interrupt sources. Higher-priority sources are located toward the bottom of the table. The high-order byte of the address for the interrupt service routine is located at the first address in the vector address column, and the low-order byte of the address for the interrupt service routine is located at the next higher address.

When an interrupt condition occurs, an associated flag bit becomes set. If the associated local interrupt enable is 1, an interrupt request is sent to the CPU. Within the CPU, if the global interrupt mask (I bit in the CCR) is 0, the CPU will finish the current instruction; stack the PCL, PCH, X, A, and CCR CPU registers; set the I bit; and then fetch the interrupt vector for the highest priority pending interrupt. Processing then continues in the interrupt service routine.

**Table 5-2. Vector Summary**

| Vector Priority | Vector Number | Address (High/Low) | Vector Name | Module | Source | Enable | Description |
|---|---|---|---|---|---|---|---|
| Lowest | 31 | 0xFFC0/0xFFC1 | — | — | — | — | — |
| | 30 | 0xFFC2/0xFFC3 | Vacmp | ACMP | ACF | ACIE | Analog comparator |
| | 29 | 0xFFC4/0xFFC5 | — | — | — | — | — |
| | 28 | 0xFFC6/0xFFC7 | — | — | — | — | — |
| | 27 | 0xFFC8/0xFFC9 | — | — | — | — | — |
| | 26 | 0xFFCA/0xFFCB | Vmtim | MTIM | TOF | TOIE | MTIM overflow |
| | 25 | 0xFFCC/0xFFCD | Vrtc | RTC | RTIF | RTIE | Real-time interrupt |
| | 24 | 0xFFCE/0xFFCF | Viic | IIC | IICIS | IICIE | IIC control |
| | 23 | 0xFFD0/0xFFD1 | Vadc | ADC | COCO | AIEN | ADC |
| | 22 | 0xFFD2/0xFFD3 | — | — | — | — | — |
| | 21 | 0xFFD4/0xFFD5 | Vportb | Port B | PTBIF | PTBIE | Port B Pins |
| | 20 | 0xFFD6/0xFFD7 | Vporta | Port A | PTAIF | PTAIE | Port A Pins |
| | 19 | 0xFFD8/0xFFD9 | — | — | — | — | — |
| | 18 | 0xFFDA/0xFFDB | Vscitx | SCI | TDRE, TC | TIE, TCIE | SCI transmit |
| | 17 | 0xFFDC/0xFFDD | Vscirx | SCI | IDLE, RDRF, LDBKDIF, RXEDGIF | ILIE, RIE, LBKDIE, RXEDGIE | SCI receive |
| | 16 | 0xFFDE/0xFFDF | Vscierr | SCI | OR, NF, FE, PF | ORIE, NFIE, FEIE, PFIE | SCI error |
| | 15 | 0xFFE0/0xFFE1 | Vspi | SPI | SPIF, MODF, SPTEF | SPIE, SPIE, SPTIE | SPI |
| | 14 | 0xFFE2/0xFFE3 | Vtpm2ovf | TPM2 | TOF | TOIE | TPM2 overflow |
| | 13 | 0xFFE4/0xFFE5 | Vtpm2ch1 | TPM2 | CH1F | CH1IE | TPM2 channel 1 |
| | 12 | 0xFFE6/0xFFE7 | Vtpm2ch0 | TPM2 | CH0F | CH0IE | TPM2 channel 0 |
| | 11 | 0xFFE8/0xFFE9 | Vtpm1ovf | TPM1 | TOF | TOIE | TPM1 overflow |
| | 10 | 0xFFEA/0xFFEB | — | — | — | — | — |
| | 9 | 0xFFEC/0xFFED | — | — | — | — | — |
| | 8 | 0xFFEE/0xFFEF | — | — | — | — | — |
| | 7 | 0xFFF0/0xFFF1 | — | — | — | — | — |
| | 6 | 0xFFF2/0xFFF3 | Vtpm1ch1 | TPM1 | CH1F | CH1IE | TPM1 channel 1 |
| | 5 | 0xFFF4/0xFFF5 | Vtpm1ch0 | TPM1 | CH0F | CH0IE | TPM1 channel 0 |
| | 4 | 0xFFF6/0xFFF7 | — | — | — | — | — |
| | 3 | 0xFFF8/0xFFF9 | Vlvd | Systemcontrol | LVWF | LVWIE | Low-voltage warning |
| | 2 | 0xFFFA/0xFFFB | — | — | — | — | — |
| | 1 | 0xFFFC/0xFFFD | Vswi | Core | SWI Instruction | — | Software interrupt |
| Highest | 0 | 0xFFFE/0xFFFF | Vreset | System control | COP,<br>LVD,<br>$\overline{\text{RESET}}$ pin,<br>Illegal opcode,<br>Illegal address | COPE<br>LVDRE<br>—<br>—<br>— | Watchdog timer<br>Low-voltage detect<br>External pin<br>Illegal opcode<br>Illegal address |

## 5.6 Low-Voltage Detect (LVD) System

The MC9S08SG32 Series includes a system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit and a LVD circuit with trip voltages for warning and detection. The LVD circuit is enabled when LVDE in SPMSC1 is set to 1. The LVD is disabled upon entering any of the stop modes unless LVDSE is set in SPMSC1. If LVDSE and LVDE are both set, then the MCU cannot enter stop2, and the current consumption in stop3 with the LVD enabled will be higher.

### 5.6.1 Power-On Reset Operation

When power is initially applied to the MCU, or when the supply voltage drops below the power-on reset rearm voltage level, $V_{POR}$, the POR circuit will cause a reset condition. As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above the low voltage detection low threshold, $V_{LVDL}$. Both the POR bit and the LVD bit in SRS are set following a POR.

### 5.6.2 Low-Voltage Detection (LVD) Reset Operation

The LVD can be configured to generate a reset upon detection of a low voltage condition by setting LVDRE to 1. The low voltage detection threshold is determined by the LVDV bit. After an LVD reset has occurred, the LVD system will hold the MCU in reset until the supply voltage has risen above the low voltage detection threshold. The LVD bit in the SRS register is set following either an LVD reset or POR.

### 5.6.3 Low-Voltage Warning (LVW) Interrupt Operation

The LVD system has a low voltage warning flag to indicate to the user that the supply voltage is approaching the low voltage condition. When a low voltage warning condition is detected and is configured for interrupt operation (LVWIE set to 1), LVWF in SPMSC1 will be set and an LVW interrupt request will occur.

## 5.7 Reset, Interrupt, and System Control Registers and Control Bits

One 8-bit register in the direct page register space and eight 8-bit registers in the high-page register space are related to reset and interrupt systems.

Refer to Table 4-2 and Table 4-3 in Chapter 4, “Memory,” of this data sheet for the absolute address assignments for all registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

Some control bits in the SOPT1 and SPMSC2 registers are related to modes of operation. Although brief descriptions of these bits are provided here, the related functions are discussed in greater detail in Chapter 3, “Modes of Operation.”

## 5.7.1 System Reset Status Register (SRS)

This high page register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to BDFR in the SBDFR register, none of the status bits in SRS will be set. Writing any value to this register address causes a COP reset when the COP is enabled except the values 0x55 and 0xAA. Writing a 0x55-0xAA sequence to this address clears the COP watchdog timer without affecting the contents of this register. The reset state of these bits depends on what caused the MCU to reset.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | POR | PIN | COP | ILOP | ILAD | 0 | LVD | 0 |
| W | Writing 0x55, 0xAA to SRS address clears COP watchdog timer. | | | | | | | |
| POR: | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| LVR: | u[1] | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Any other reset: | 0 | Note[2] | Note[2] | Note[2] | Note[2] | 0 | 0 | 0 |

1 u = unaffected

2 Any of these reset sources that are active at the time of reset entry will cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset entry will be cleared.

**Figure 5-2. System Reset Status (SRS)**

**Table 5-3. SRS Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>POR | **Power-On Reset** — Reset was caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVR) status bit is also set to indicate that the reset occurred while the internal supply was below the LVR threshold.<br>0 Reset not caused by POR.<br>1 POR caused reset. |
| 6<br>PIN | **External Reset Pin** — Reset was caused by an active-low level on the external reset pin.<br>0 Reset not caused by external reset pin.<br>1 Reset came from external reset pin. |
| 5<br>COP | **Computer Operating Properly (COP) Watchdog** — Reset was caused by the COP watchdog timer timing out. This reset source can be blocked by COPE = 0.<br>0 Reset not caused by COP timeout.<br>1 Reset caused by COP timeout. |
| 4<br>ILOP | **Illegal Opcode** — Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register.<br>0 Reset not caused by an illegal opcode.<br>1 Reset caused by an illegal opcode. |

**Table 5-3. SRS Register Field Descriptions**

| Field | Description |
|---|---|
| 3<br>ILAD | **Illegal Address** — Reset was caused by an attempt to access either data or an instruction at an unimplemented memory address.<br>0 Reset not caused by an illegal address<br>1 Reset caused by an illegal address |
| 1<br>LVD | **Low Voltage Detect** — If the LVDRE bit is set and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR.<br>0 Reset not caused by LVD trip or POR.<br>1 Reset caused by LVD trip or POR. |

## 5.7.2 System Background Debug Force Reset Register (SBDFR)

This high page register contains a single write-only control bit. A serial background command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | | | | | | | | BDFR[1] |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

1 BDFR is writable only through serial background debug commands, not from user programs.

**Figure 5-3. System Background Debug Force Reset Register (SBDFR)**

**Table 5-4. SBDFR Register Field Descriptions**

| Field | Description |
|---|---|
| 0<br>BDFR | **Background Debug Force Reset** — A serial background command such as WRITE_BYTE can be used to allow an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program. |

## 5.7.3 System Options Register 1 (SOPT1)

This high page register is a write-once register so only the first write after reset is honored. It can be read at any time. Any subsequent attempt to write to SOPT1 (intentionally or unintentionally) is ignored to avoid accidental changes to these sensitive settings. SOPT1 should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | COPT | | STOPE | 0 | 0 | IICPS | 0 | 0 |
| W | | | | | | | | |
| Reset: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 5-4. System Options Register 1 (SOPT1)**

**Table 5-5. SOPT1 Register Field Descriptions**

| Field | Description |
|---|---|
| 7:6<br>COPT[1:0] | **COP Watchdog Timeout** — These write-once bits select the timeout period of the COP. COPT along with COPCLKS in SOPT2 defines the COP timeout period. See Table 5-1. |
| 5<br>STOPE | **Stop Mode Enable** — This write-once bit is used to enable stop mode. If stop mode is disabled and a user program attempts to execute a STOP instruction, an illegal opcode reset is forced.<br>0 Stop mode disabled.<br>1 Stop mode enabled. |
| 2<br>IICPS | **IIC Pin Select** — This bit selects the location of the SDA and SCL pins of the IIC module.<br>0 SDA on PTA2, SCL on PTA3.<br>1 SDA on PTB6, SCL on PTB7. |

## 5.7.4 System Options Register 2 (SOPT2)

This high page register contains bits to configure MCU specific features on the MC9S08SG32 Series devices.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | COPCLKS[1] | COPW[1] | 0 | ACIC | T2CH1PS | T2CH0PS | T1CH1PS | T1CH0PS |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 5-5. System Options Register 2 (SOPT2)**

1 This bit can be written only one time after reset. Additional writes are ignored.

**Table 5-6. SOPT2 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>COPCLKS | **COP Watchdog Clock Select** — This write-once bit selects the clock source of the COP watchdog.<br>0 Internal 1-kHz clock is source to COP.<br>1 Bus clock is source to COP. |
| 6<br>COPW | **COP Window** — This write-once bit selects the COP operation mode. When set, the 0x55-0xAA write sequence to the SRS register must occur in the last 25% of the selected period. Any write to the SRS register during the first 75% of the selected period will reset the MCU.<br>0 Normal COP operation<br>1 Window COP operation (only if COPCLKS = 1) |
| 4<br>ACIC | **Analog Comparator to Input Capture Enable**— This bit connects the output of ACMP to TPM1 input channel 0.<br>0 ACMP output not connected to TPM1 input channel 0.<br>1 ACMP output connected to TPM1 input channel 0. |
| 3<br>T2CH1PS | **TPM2CH1 Pin Select**— This selects the location of the TPM2CH1 pin of the TPM2 module.<br>0 TPM2CH1 on PTB4.<br>1 TPM2CH1 on PTA7. |
| 2<br>T2CH0PS | **TPM2CH0 Pin Select**— This bit selects the location of the TPM2CH0 pin of the TPM2 module.<br>0 TPM2CH0 on PTA1.<br>1 TPM2CH0 on PTA6. |
| 1<br>T1CH1PS | **TPM1CH1 Pin Select**— This bit selects the location of the TPM1CH1 pin of the TPM1 module.<br>0 TPM1CH1 on PTB5.<br>1 TPM1CH1 on PTC1. |
| 0<br>T1CH0PS | **TPM1CH0 Pin Select**— This bit selects the location of the TPM1CH0 pin of the TPM1 module.<br>0 TPM1CH0 on PTA0.<br>1 TPM1CH0 on PTC0. |

## 5.7.5 System Device Identification Register (SDIDH, SDIDL)

These high page read-only registers are included so host development systems can identify the HCS08 derivative and revision number. This allows the development software to recognize where specific memory blocks, registers, and control bits are located in a target MCU.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 1 | | | | ID11 | ID10 | ID9 | ID8 |
| W | | | | | | | | |
| Reset: | 1[1] | — | — | — | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

1 - Bit 7 is a mask option tie off that is used internally to determine that the device is a MC9S08SG32 Series.

**Figure 5-6. System Device Identification Register — High (SDIDH)**

**Table 5-7. SDIDH Register Field Descriptions**

| Field | Description |
|---|---|
| 7 | Bit 7 will read as a 1 for the MC9S08SG32 Series devices; writes have no effect. |
| 6:4<br>Reserved | Bits 6:4 are reserved. Reading these bits will result in an indeterminate value; writes have no effect. |
| 3:0<br>ID[11:8] | **Part Identification Number** — Each derivative in the HCS08 Family has a unique identification number. The MC9S08SG32 is hard coded to the value 0x01A. See also ID bits in Table 5-8. |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

= Unimplemented or Reserved

**Figure 5-7. System Device Identification Register — Low (SDIDL)**

**Table 5-8. SDIDL Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>ID[7:0] | **Part Identification Number** — Each derivative in the HCS08 Family has a unique identification number. The MC9S08SG32 is hard coded to the value 0x01A. See also ID bits in Table 5-7. |

## 5.7.6 System Power Management Status and Control 1 Register (SPMSC1)

This high page register contains status and control bits to support the low-voltage detect function, and to enable the bandgap voltage reference for use by the ADC and ACMP modules. This register should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | LVWF[1] | 0 | LVWIE | LVDRE[2] | LVDSE[2] | LVDE[2] | 0 | BGBE |
| W | | LVWACK | | | | | | |
| Reset: | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

= Unimplemented or Reserved

1 LVWF will be set in the case when $V_{Supply}$ transitions below the trip point or after reset and $V_{Supply}$ is already below $V_{LVW}$

2 This bit can be written only one time after reset. Additional writes are ignored.

**Figure 5-8. System Power Management Status and Control 1 Register (SPMSC1)**

**Table 5-9. SPMSC1 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>LVWF | **Low-Voltage Warning Flag** — The LVWF bit indicates the low voltage warning status.<br>0 Low voltage warning is not present.<br>1 Low voltage warning is present or was present. |
| 6<br>LVWACK | **Low-Voltage Warning Acknowledge** — The LVWF bit indicates the low voltage warning status.Writing a 1 to LVWACK clears LVWF to a 0 if a low voltage warning is not present. |
| 5<br>LVWIE | **Low-Voltage Warning Interrupt Enable** — This bit enables hardware interrupt requests for LVWF.<br>0 Hardware interrupt disabled (use polling).<br>1 Request a hardware interrupt when LVWF = 1. |
| 4<br>LVDRE | **Low-Voltage Detect Reset Enable** — This write-once bit enables LVD events to generate a hardware reset (provided LVDE = 1).<br>0 LVD events do not generate hardware resets.<br>1 Force an MCU reset when an enabled low-voltage detect event occurs. |
| 3<br>LVDSE | **Low-Voltage Detect Stop Enable** — Provided LVDE = 1, this write-once bit determines whether the low-voltage detect function operates when the MCU is in stop mode.<br>0 Low-voltage detect disabled during stop mode.<br>1 Low-voltage detect enabled during stop mode. |
| 2<br>LVDE | **Low-Voltage Detect Enable** — This write-once bit enables low-voltage detect logic and qualifies the operation of other bits in this register.<br>0 LVD logic disabled.<br>1 LVD logic enabled. |
| 0<br>BGBE | **Bandgap Buffer Enable** — This bit enables an internal buffer for the bandgap voltage reference for use by the ADC and ACMP modules.<br>0 Bandgap buffer disabled.<br>1 Bandgap buffer enabled. |

## 5.7.7 System Power Management Status and Control 2 Register (SPMSC2)

This register is used to report the status of the low voltage warning function, and to configure the stop mode behavior of the MCU. This register should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | LVDV[1] | LVWV | PPDF | 0 | 0 | PPDC[2] |
| W | | | | | | PPDACK | | |
| Power-on Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LVD Reset: | 0 | 0 | u | u | 0 | 0 | 0 | 0 |
| Any other Reset: | 0 | 0 | u | u | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved  u = Unaffected by reset

1 This bit can be written only one time after power-on reset. Additional writes are ignored.

2 This bit can be written only one time after reset. Additional writes are ignored.

**Figure 5-9. System Power Management Status and Control 2 Register (SPMSC2)**

**Table 5-10. SPMSC2 Register Field Descriptions**

| Field | Description |
|---|---|
| 5<br>LVDV | **Low-Voltage Detect Voltage Select** — This write-once bit selects the low voltage detect (LVD) trip point setting. It also selects the warning voltage range. See Table 5-11. |
| 4<br>LVWV | **Low-Voltage Warning Voltage Select** — This bit selects the low voltage warning (LVW) trip point voltage. See Table 5-11. |
| 3<br>PPDF | **Partial Power Down Flag** — This read-only status bit indicates that the MCU has recovered from stop2 mode.<br>0 MCU has not recovered from stop2 mode.<br>1 MCU recovered from stop2 mode. |
| 2<br>PPDACK | **Partial Power Down Acknowledge** — Writing a 1 to PPDACK clears the PPDF bit |
| 0<br>PPDC | **Partial Power Down Control** — This write-once bit controls whether stop2 or stop3 mode is selected.<br>0 Stop3 mode enabled.<br>1 Stop2, partial power down, mode enabled. |

**Table 5-11. LVD and LVW trip point typical values[1]**

| LVDV:LVWV | LVW Trip Point | LVD Trip Point |
|---|---|---|
| 0:0 | $V_{LVW0}$ = 2.74 V | $V_{LVD0}$ = 2.56 V |
| 0:1 | $V_{LVW1}$ = 2.92 V | |
| 1:0 | $V_{LVW2}$ = 4.3 V | $V_{LVD1}$ = 4.0 V |
| 1:1 | $V_{LVW3}$ = 4.6 V | |

1 See Electrical Characteristics appendix for minimum and maximum values.

# Chapter 6
# Parallel Input/Output Control

This section explains software controls related to parallel input/output (I/O) and pin control. The MC9S08SG32 has three parallel I/O ports which include a total of 22 I/O pins. See Chapter 2, “Pins and Connections,” for more information about pin assignments and external hardware considerations of these pins.

Many of these pins are shared with on-chip peripherals such as timer systems, communication systems, or pin interrupts as shown in Table 2-1. The peripheral modules have priority over the general-purpose I/O functions so that when a peripheral is enabled, the I/O functions associated with the shared pins are disabled.

After reset, the shared peripheral functions are disabled and the pins are configured as inputs (PTxDDn = 0). The pin control functions for each pin are configured as follows: slew rate disabled (PTxSEn = 0), low drive strength selected (PTxDSn = 0), and internal pull-ups disabled (PTxPEn = 0).

**NOTE**

Not all general-purpose I/O pins are available on all packages. To avoid extra current drain from floating input pins, the user’s reset initialization routine in the application program must either enable on-chip pull-up devices or change the direction of unconnected pins to outputs so the pins do not float.

## 6.1 Port Data and Data Direction

Reading and writing of parallel I/Os are performed through the port data registers. The direction, either input or output, is controlled through the port data direction registers. The parallel I/O port function for an individual pin is illustrated in the block diagram shown in Figure 6-1.

The data direction control bit (PTxDDn) determines whether the output buffer for the associated pin is enabled, and also controls the source for port data register reads. The input buffer for the associated pin is always enabled unless the pin is enabled as an analog function or is an output-only pin.

When a shared digital function is enabled for a pin, the output buffer is controlled by the shared function. However, the data direction register bit will continue to control the source for reads of the port data register.

When a shared analog function is enabled for a pin, both the input and output buffers are disabled. A value of 0 is read for any port data bit where the bit is an input (PTxDDn = 0) and the input buffer is disabled. In general, whenever a pin is shared with both an alternate digital function and an analog function, the analog function has priority such that if both the digital and analog functions are enabled, the analog function controls the pin.

It is a good programming practice to write to the port data register before changing the direction of a port pin to become an output. This ensures that the pin will not be driven momentarily with an old data value that happened to be in the port data register.

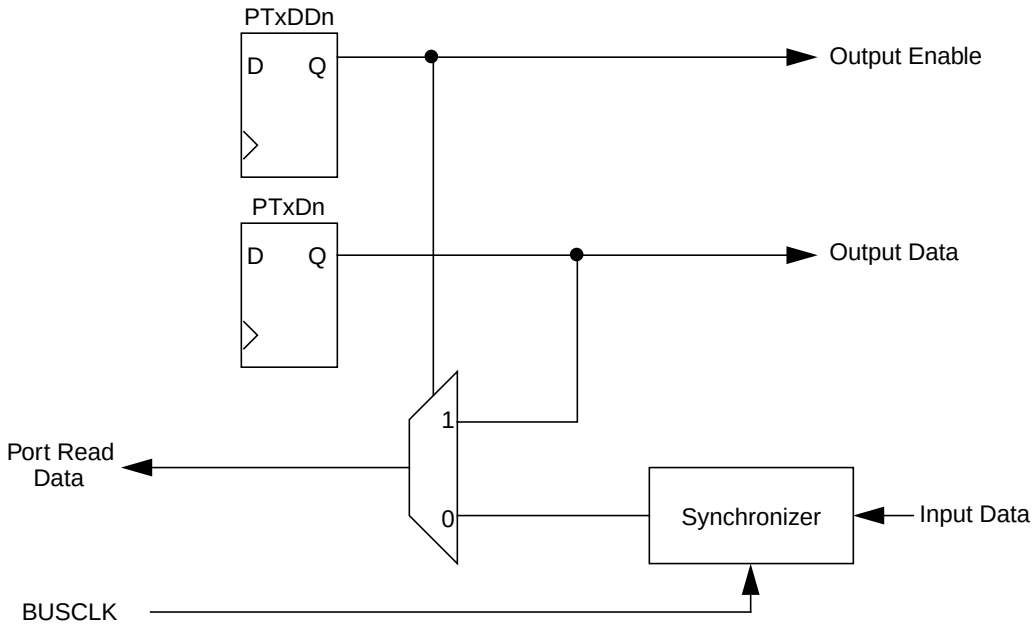



**Figure 6-1. Parallel I/O Block Diagram**

## 6.2 Pull-up, Slew Rate, and Drive Strength

Associated with the parallel I/O ports is a set of registers located in the high page register space that operate independently of the parallel I/O registers. These registers are used to control pull-ups, slew rate, and drive strength for the pins.

An internal pull-up device can be enabled for each port pin by setting the corresponding bit in the pull-up enable register (PTxPEn). The pull-up device is disabled if the pin is configured as an output by the parallel I/O control logic or any shared peripheral function regardless of the state of the corresponding pull-up enable register bit. The pull-up device is also disabled if the pin is controlled by an analog function.

Slew rate control can be enabled for each port pin by setting the corresponding bit in the slew rate control register (PTxSEn). When enabled, slew control limits the rate at which an output can transition in order to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.

An output pin can be selected to have high output drive strength by setting the corresponding bit in the drive strength select register (PTxDSn). When high drive is selected, a pin is capable of sourcing and sinking greater current. Even though every I/O pin can be selected as high drive, the user must ensure that the total current source and sink limits for the MCU are not exceeded. Drive strength selection is intended to affect the DC behavior of I/O pins. However, the AC behavior is also affected. High drive allows a pin to drive a greater load with the same switching speed as a low drive enabled pin into a smaller load. Because of this, the EMC emissions may be affected by enabling pins as high drive.

## 6.3 Ganged Output

The MC9S08SG32 Series devices contain a feature that allows for up to eight port pins to be tied together externally to allow higher output current drive. The ganged output drive control register (GNGC) is a write-once register that is used to enabled the ganged output feature and select which port pins will be used as ganged outputs. The GNGEN bit in GNGC enables ganged output. The GNGPS[7:1] bits are used to select which pin will be part of the ganged output.

When GNGEN is set, any pin that is enabled as a ganged output will be automatically configured as an output and follow the data, drive strength and slew rate control of PTC0. The ganged output drive pin mapping is shown in Table 6-1.

**NOTE**

See the DC characteristics in the electrical section for maximum Port I/O currents allowed for this MCU.

When a pin is enabled as ganged output, this feature will have priority over any digital module. An enabled analog function will have priority over the ganged output pin. See Table 2-1 for information on pin priority.

**Table 6-1. Ganged Output Pin Enable**

| | GNGC Register Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **GNGPS7** | **GNGPS6** | **GNGPS5** | **GNGPS4** | **GNGPS3** | **GNGPS2** | **GNGPS1** | **GNGEN[1]** |
| **Port Pin [2]** | PTB5 | PTB4 | PTB3 | PTB2 | PTC3 | PTC2 | PTC1 | PTC0 |
| **Data Direction Control** | Pin is automatically configured as output when pin is enabled as ganged output. | | | | | | | |
| **Data Control** | PTCD0 in PTCD controls data value of output | | | | | | | |
| **Drive Strength Control** | PTCDS0 in PTCDS controls drive strength of output | | | | | | | |
| **Slew Rate Control** | PTCSE0 in PTCSE controls slew rate of output | | | | | | | |

1 Ganged output on PTC3-PTC0 not available on 16-pin packages, however PTC0 control registers are still used to control ganged output.

2 When GNGEN = 1, PTC0 is forced to an output, regardless of the value in PTCDD0 in PTCDD.

## 6.4 Pin Interrupts

Port A[3:0] and port B[3:0] pins can be configured as external interrupt inputs and as an external means of waking the MCU from stop3 or wait low-power modes.

The block diagram for the pin interrupts is shown.

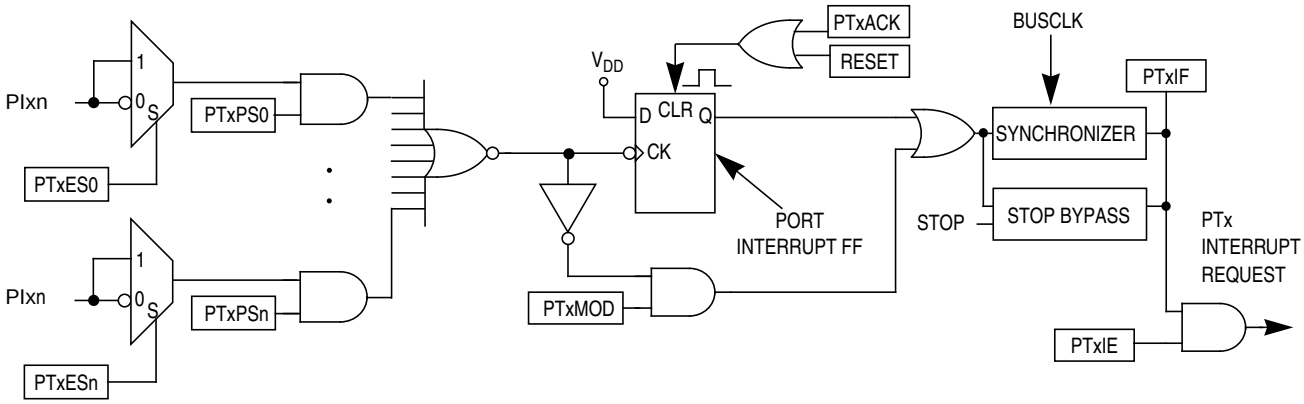



**Figure 6-2. Pin Interrupt Block Diagram**

Writing to the PTxPSn bits in the port interrupt pin enable register (PTxPS) independently enables or disables each port pin interrupt. Each port can be configured as edge sensitive or edge and level sensitive based on the PTxMOD bit in the port interrupt status and control register (PTxSC). Edge sensitivity can be software programmed to be either falling or rising; the level can be either low or high. The polarity of the edge or edge and level sensitivity is selected using the PTxESn bits in the port interrupt edge select register (PTxES).

Synchronous logic is used to detect edges. Prior to detecting an edge, enabled pin interrupt inputs must be at the deasserted logic level. A falling edge is detected when an enabled port input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle. A rising edge is detected when the input signal is seen as a logic 0 during one bus cycle and then a logic 1 during the next cycle.

### 6.4.1 Edge-Only Sensitivity

A valid edge on an enabled pin interrupt sets PTxIF in PTxSC. If PTxIE in PTxSC is set, an interrupt request is presented to the CPU. To clear PTxIF, write a 1 to PTxACK in PTxSC.

**NOTE**

If a pin is enabled for interrupt on edge-sensitive only, a falling (or rising) edge on the pin does not latch an interrupt request if another pin interrupt is already asserted.

To prevent losing an interrupt request on one pin because another pin is asserted, software can disable the asserted pin interrupt while having the unasserted pin interrupt enabled. The asserted status of a pin is reflected by its associated I/O general purpose data register.

### 6.4.2 Edge and Level Sensitivity

A valid edge or level on an enabled pin interrupt sets PTxIF in PTxSC. If PTxIE in PTxSC is set, an interrupt request is presented to the CPU. To clear PTxIF, write a 1 to PTxACK in PTxSC provided all enabled pin interrupt inputs are at their de-asserted levels. PTxIF remains set if any enabled pin interrupt is asserted while attempting to clear by writing a 1 to PTxACK.

### 6.4.3 Pull-up/Pull-down Resistors

The pin interrupts can be configured to use an internal pull-up/pull-down resistor using the associated I/O port pull-up enable register. If an internal resistor is enabled, the PTxES register is used to select whether the resistor is a pull-up (PTxESn = 0) or a pull-down (PTxESn = 1).

### 6.4.4 Pin Interrupt Initialization

When a pin interrupt is first enabled, it is possible to get a false interrupt flag. To prevent a false interrupt request during pin interrupt initialization, the user should do the following:

1. Mask interrupts by clearing PTxIE in PTxSC.
2. Select the pin polarity by setting the appropriate PTxESn bits in PTxES.
3. If using internal pull-up/pull-down device, configure the associated pull enable bits in PTxPE.
4. Enable the interrupt pins by setting the appropriate PTxPSn bits in PTxPS.
5. Write to PTxACK in PTxSC to clear any false interrupts.
6. Set PTxIE in PTxSC to enable interrupts.

## 6.5 Pin Behavior in Stop Modes

Pin behavior following execution of a STOP instruction depends on the stop mode that is entered. An explanation of pin behavior for the various stop modes follows:

- Stop2 mode is a partial power-down mode, whereby I/O latches are maintained in their state as before the STOP instruction was executed. CPU register status and the state of I/O registers should be saved in RAM before the STOP instruction is executed to place the MCU in stop2 mode. Upon recovery from stop2 mode, before accessing any I/O, the user should examine the state of the PPDF bit in the SPMSC2 register. If the PPDF bit is 0, I/O must be initialized as if a power on reset had occurred. If the PPDF bit is 1, I/O data previously stored in RAM, before the STOP instruction was executed, peripherals may require being initialized and restored to their pre-stop condition. The user must then write a 1 to the PPDACK bit in the SPMSC2 register. Access to I/O is now permitted again in the user application program.
- In stop3 mode, all I/O is maintained because internal logic circuity stays powered up. Upon recovery, normal I/O function is available to the user.

## 6.6 Parallel I/O and Pin Control Registers

This section provides information about the registers associated with the parallel I/O ports. The data and data direction registers are located in page zero of the memory map. The pull up, slew rate, drive strength, and interrupt control registers are located in the high page section of the memory map.

Refer to tables in Chapter 4, “Memory,” for the absolute address assignments for all parallel I/O and their pin control registers. This section refers to registers and control bits only by their names. A Freescale Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

## 6.6.1 Port A Registers

Port A is controlled by the registers listed below.

### 6.6.1.1 Port A Data Register (PTAD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTAD7 | PTAD6 | R | R | PTAD3 | PTAD2 | PTAD1 | PTAD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-3. Port A Data Register (PTAD)**

**Table 6-2. PTAD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:6, 3:0<br>PTAD[7:6, 3:0] | **Port A Data Register Bits** — For port A pins that are inputs, reads return the logic level on the pin. For port A pins that are configured as outputs, reads return the last value written to this register.<br>Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out the corresponding MCU pin.<br>Reset forces PTAD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled. |
| 5:4<br>Reserved | **Reserved Bits** — These bits are unused on this MCU, writes have no affect and could read as 1s or 0s. |

### 6.6.1.2 Port A Data Direction Register (PTADD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTADD7 | PTADD6 | R | R | PTADD3 | PTADD2 | PTADD1 | PTADD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-4. Port A Data Direction Register (PTADD)**

**Table 6-3. PTADD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:6, 3:0<br>PTADD[7:6, 3:0] | **Data Direction for Port A Bits** — These read/write bits control the direction of port A pins and what is read for PTAD reads.<br>0 Input (output driver disabled) and reads return the pin value.<br>1 Output driver enabled for port A bit n and PTAD reads return the contents of PTADn. |
| 5:4<br>Reserved | **Reserved Bits** — These bits are unused on this MCU, writes have no affect and could read as 1s or 0s. |

### 6.6.1.3 Port A Pull Enable Register (PTAPE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTAPE7 | PTAPE6 | R | R | PTAPE3 | PTAPE2 | PTAPE1 | PTAPE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-5. Internal Pull Enable for Port A Register (PTAPE)**

**Table 6-4. PTAPE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:5,3:0<br>PTAPE[7:5, 3:0] | **Internal Pull Enable for Port A Bits** — Each of these control bits determines if the internal pull-up or pull-down device is enabled for the associated PTA pin. For port A pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled.<br>0 Internal pull-up/pull-down device disabled for port A bit n.<br>1 Internal pull-up/pull-down device enabled for port A bit n. |
| 5:4<br>Reserved | **Reserved Bits** — These bits are unused on this MCU, writes have no affect and could read as 1s or 0s. |

**NOTE**

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured to detect rising edges.

### 6.6.1.4 Port A Slew Rate Enable Register (PTASE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTASE7 | PTASE6 | R | R | PTASE3 | PTASE2 | PTASE1 | PTASE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-6. Slew Rate Enable for Port A Register (PTASE)**

**Table 6-5. PTASE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:5,3:0<br>PTASE[7:5, 3:0] | **Output Slew Rate Enable for Port A Bits** — Each of these control bits determines if the output slew rate control is enabled for the associated PTA pin. For port A pins that are configured as inputs, these bits have no effect.<br>0 Output slew rate control disabled for port A bit n.<br>1 Output slew rate control enabled for port A bit n. |
| 5:4<br>Reserved | **Reserved Bits** — These bits are unused on this MCU, writes have no affect and could read as 1s or 0s. |

### 6.6.1.5 Port A Drive Strength Selection Register (PTADS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTADS7 | PTADS6 | R | R | PTADS3 | PTADS2 | PTADS1 | PTADS0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-7. Drive Strength Selection for Port A Register (PTADS)**

**Table 6-6. PTADS Register Field Descriptions**

| Field | Description |
|---|---|
| 7:5,3:0<br>PTADS[7:5, 3:0] | **Output Drive Strength Selection for Port A Bits** — Each of these control bits selects between low and high output drive for the associated PTA pin. For port A pins that are configured as inputs, these bits have no effect.<br>0 Low output drive strength selected for port A bit n.<br>1 High output drive strength selected for port A bit n. |
| 5:4<br>Reserved | **Reserved Bits** — These bits are unused on this MCU, writes have no affect and could read as 1s or 0s. |

### 6.6.1.6 Port A Interrupt Status and Control Register (PTASC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTAIF | 0 | PTAIE | PTAMOD |
| W | | | | | | PTAACK | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-8. Port A Interrupt Status and Control Register (PTASC)**

**Table 6-7. PTASC Register Field Descriptions**

| Field | Description |
|---|---|
| 3<br>PTAIF | **Port A Interrupt Flag** — PTAIF indicates when a port A interrupt is detected. Writes have no effect on PTAIF.<br>0 No port A interrupt detected.<br>1 Port A interrupt detected. |
| 2<br>PTAACK | **Port A Interrupt Acknowledge** — Writing a 1 to PTAACK is part of the flag clearing mechanism. PTAACK always reads as 0. |
| 1<br>PTAIE | **Port A Interrupt Enable** — PTAIE determines whether a port A interrupt is enabled.<br>0 Port A interrupt request not enabled.<br>1 Port A interrupt request enabled. |
| 0<br>PTAMOD | **Port A Detection Mode** — PTAMOD (along with the PTAES bits) controls the detection mode of the port A interrupt pins.<br>0 Port A pins detect edges only.<br>1 Port A pins detect both edges and levels. |

### 6.6.1.7 Port A Interrupt Pin Select Register (PTAPS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTAPS3 | PTAPS2 | PTAPS1 | PTAPS0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-9. Port A Interrupt Pin Select Register (PTAPS)**

**Table 6-8. PTAPS Register Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PTAPS[3:0] | **Port A Interrupt Pin Selects** — Each of the PTAPSn bits enable the corresponding port A interrupt pin.<br>0 Pin not enabled as interrupt.<br>1 Pin enabled as interrupt. |

### 6.6.1.8 Port A Interrupt Edge Select Register (PTAES)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTAES3 | PTAES2 | PTAES1 | PTAES0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-10. Port A Edge Select Register (PTAES)**

**Table 6-9. PTAES Register Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PTAES[3:0] | **Port A Edge Selects** — Each of the PTAESn bits serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.<br>0 A pull-up device is connected to the associated pin and detects falling edge/low level for interrupt generation.<br>1 A pull-down device is connected to the associated pin and detects rising edge/high level for interrupt generation. |

## 6.6.2 Port B Registers

Port B is controlled by the registers listed below.

### 6.6.2.1 Port B Data Register (PTBD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTBD7 | PTBD6 | PTBD5 | PTBD4 | PTBD3 | PTBD2 | PTBD1 | PTBD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-11. Port B Data Register (PTBD)**

**Table 6-10. PTBD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTBD[7:0] | **Port B Data Register Bits** — For port B pins that are inputs, reads return the logic level on the pin. For port B pins that are configured as outputs, reads return the last value written to this register.<br>Writes are latched into all bits of this register. For port B pins that are configured as outputs, the logic level is driven out the corresponding MCU pin.<br>Reset forces PTBD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled. |

### 6.6.2.2 Port B Data Direction Register (PTBDD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTBDD7 | PTBDD6 | PTBDD5 | PTBDD4 | PTBDD3 | PTBDD2 | PTBDD1 | PTBDD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-12. Port B Data Direction Register (PTBDD)**

**Table 6-11. PTBDD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTBDD[7:0] | **Data Direction for Port B Bits** — These read/write bits control the direction of port B pins and what is read for PTBD reads.<br>0 Input (output driver disabled) and reads return the pin value.<br>1 Output driver enabled for port B bit n and PTBD reads return the contents of PTBDn. |

### 6.6.2.3 Port B Pull Enable Register (PTBPE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTBPE7 | PTBPE6 | PTBPE5 | PTBPE4 | PTBPE3 | PTBPE2 | PTBPE1 | PTBPE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-13. Internal Pull Enable for Port B Register (PTBPE)**

**Table 6-12. PTBPE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTBPE[7:0] | **Internal Pull Enable for Port B Bits** — Each of these control bits determines if the internal pull-up or pull-down device is enabled for the associated PTB pin. For port B pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled.<br>0 Internal pull-up/pull-down device disabled for port B bit n.<br>1 Internal pull-up/pull-down device enabled for port B bit n. |

**NOTE**

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured to detect rising edges.

### 6.6.2.4 Port B Slew Rate Enable Register (PTBSE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTBSE7 | PTBSE6 | PTBSE5 | PTBSE4 | PTBSE3 | PTBSE2 | PTBSE1 | PTBSE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-14. Slew Rate Enable for Port B Register (PTBSE)**

**Table 6-13. PTBSE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTBSE[7:0] | **Output Slew Rate Enable for Port B Bits** — Each of these control bits determines if the output slew rate control is enabled for the associated PTB pin. For port B pins that are configured as inputs, these bits have no effect.<br>0 Output slew rate control disabled for port B bit n.<br>1 Output slew rate control enabled for port B bit n. |

### 6.6.2.5 Port B Drive Strength Selection Register (PTBDS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTBDS7 | PTBDS6 | PTBDS5 | PTBDS4 | PTBDS3 | PTBDS2 | PTBDS1 | PTBDS0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-15. Drive Strength Selection for Port B Register (PTBDS)**

**Table 6-14. PTBDS Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTBDS[7:0] | **Output Drive Strength Selection for Port B Bits** — Each of these control bits selects between low and high output drive for the associated PTB pin. For port B pins that are configured as inputs, these bits have no effect.<br>0 Low output drive strength selected for port B bit n.<br>1 High output drive strength selected for port B bit n. |

### 6.6.2.6 Port B Interrupt Status and Control Register (PTBSC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTBIF | 0 | PTBIE | PTBMOD |
| W | | | | | | PTBACK | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-16. Port B Interrupt Status and Control Register (PTBSC)**

**Table 6-15. PTBSC Register Field Descriptions**

| Field | Description |
|---|---|
| 3<br>PTBIF | **Port B Interrupt Flag** — PTBIF indicates when a Port B interrupt is detected. Writes have no effect on PTBIF.<br>0 No Port B interrupt detected.<br>1 Port B interrupt detected. |
| 2<br>PTBACK | **Port B Interrupt Acknowledge** — Writing a 1 to PTBACK is part of the flag clearing mechanism. PTBACK always reads as 0. |
| 1<br>PTBIE | **Port B Interrupt Enable** — PTBIE determines whether a port B interrupt is enabled.<br>0 Port B interrupt request not enabled.<br>1 Port B interrupt request enabled. |
| 0<br>PTBMOD | **Port B Detection Mode** — PTBMOD (along with the PTBES bits) controls the detection mode of the port B interrupt pins.<br>0 Port B pins detect edges only.<br>1 Port B pins detect both edges and levels. |

### 6.6.2.7 Port B Interrupt Pin Select Register (PTBPS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTBPS3 | PTBPS2 | PTBPS1 | PTBPS0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-17. Port B Interrupt Pin Select Register (PTBPS)**

**Table 6-16. PTBPS Register Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PTBPS[3:0] | **Port B Interrupt Pin Selects** — Each of the PTBPSn bits enable the corresponding port B interrupt pin.<br>0 Pin not enabled as interrupt.<br>1 Pin enabled as interrupt. |

### 6.6.2.8 Port B Interrupt Edge Select Register (PTBES)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PTBES3 | PTBES2 | PTBES1 | PTBES0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-18. Port B Edge Select Register (PTBES)**

**Table 6-17. PTBES Register Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PTBES[3:0] | **Port B Edge Selects** — Each of the PTBESn bits serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.<br>0 A pull-up device is connected to the associated pin and detects falling edge/low level for interrupt generation.<br>1 A pull-down device is connected to the associated pin and detects rising edge/high level for interrupt generation. |

## 6.6.3 Port C Registers

Port C is controlled by the registers listed below.

### 6.6.3.1 Port C Data Register (PTCD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTCD7 | PTCD6 | PTCD5 | PTCD4 | PTCD3 | PTCD2 | PTCD1 | PTCD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-19. Port C Data Register (PTCD)**

**Table 6-18. PTCD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTCD[7:0] | **Port C Data Register Bits** — For port C pins that are inputs, reads return the logic level on the pin. For port C pins that are configured as outputs, reads return the last value written to this register.<br>Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out the corresponding MCU pin.<br>Reset forces PTCD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups disabled. |

### 6.6.3.2 Port C Data Direction Register (PTCDD)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTCDD7 | PTCDD6 | PTCDD5 | PTCDD4 | PTCDD3 | PTCDD2 | PTCDD1 | PTCDD0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-20. Port C Data Direction Register (PTCDD)**

**Table 6-19. PTCDD Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTCDD[7:0] | **Data Direction for Port C Bits** — These read/write bits control the direction of port C pins and what is read for PTCD reads.<br>0 Input (output driver disabled) and reads return the pin value.<br>1 Output driver enabled for port C bit n and PTCD reads return the contents of PTCDn. |

### 6.6.3.3 Port C Pull Enable Register (PTCPE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTCPE7 | PTCPE6 | PTCPE5 | PTCPE4 | PTCPE3 | PTCPE2 | PTCPE1 | PTCPE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-21. Internal Pull Enable for Port C Register (PTCPE)**

**Table 6-20. PTCPE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTCPE[7:0] | **Internal Pull Enable for Port C Bits** — Each of these control bits determines if the internal pull-up device is enabled for the associated PTC pin. For port C pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled.<br>0 Internal pull-up device disabled for port C bit n.<br>1 Internal pull-up device enabled for port C bit n. |

### 6.6.3.4 Port C Slew Rate Enable Register (PTCSE)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTCSE7 | PTCSE6 | PTCSE5 | PTCSE4 | PTCSE3 | PTCSE2 | PTCSE1 | PTCSE0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-22. Slew Rate Enable for Port C Register (PTCSE)**

**Table 6-21. PTCSE Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTCSE[7:0] | **Output Slew Rate Enable for Port C Bits** — Each of these control bits determines if the output slew rate control is enabled for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect.<br>0 Output slew rate control disabled for port C bit n.<br>1 Output slew rate control enabled for port C bit n. |

### 6.6.3.5 Port C Drive Strength Selection Register (PTCDS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTCDS7 | PTCDS6 | PTCDS5 | PTCDS4 | PTCDS3 | PTCDS2 | PTCDS1 | PTCDS0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-23. Drive Strength Selection for Port C Register (PTCDS)**

**Table 6-22. PTCDS Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PTCDS[7:0] | **Output Drive Strength Selection for Port C Bits** — Each of these control bits selects between low and high output drive for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect.<br>0 Low output drive strength selected for port C bit n.<br>1 High output drive strength selected for port C bit n. |

### 6.6.3.6 Ganged Output Drive Control Register (GNGC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | GNGPS7 | GNGPS6 | GNGPS5 | GNGPS4 | GNGPS3 | GNGPS2 | GNGPS1 | GNGEN |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-24. Ganged Output Drive Control Register (GNGC)**

**Table 6-23. GNGC Register Field Descriptions**

| Field | Description |
|---|---|
| 7:1<br>GNGP[7:1] | **Ganged Output Pin Select Bits**— These write-once control bits selects whether the associated pin (see Table 6-1for pins available) is enabled for ganged output. When GNGEN = 1, all enabled ganged output pins will be controlled by the data, drive strength and slew rate settings for PTCO.<br>0 Associated pin is not part of the ganged output drive.<br>1 Associated pin is part of the ganged output drive. Requires GNGEN = 1. |
| 0<br>GNGEN | **Ganged Output Drive Enable Bit**— This write-once control bit selects whether the ganged output drive feature is enabled.<br>0 Ganged output drive disabled.<br>1 Ganged output drive enabled. PTC0 forced to output regardless of the value of PTCDD0 in PTCDD. |

# Chapter 7
# Central Processor Unit (S08CPUV3)

## 7.1 Introduction

This section provides summary information about the registers, addressing modes, and instruction set of the CPU of the HCS08 Family. For a more detailed discussion, refer to the *HCS08 Family Reference Manual, volume 1*, Freescale Semiconductor document order number HCS08RMV1/D.

The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers (MCU).

### 7.1.1 Features

Features of the HCS08 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 Families
- All registers and memory are mapped to a single 64-Kbyte address space
- 16-bit stack pointer (any size stack anywhere in 64-Kbyte address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
  - Inherent — Operands in internal registers
  - Relative — 8-bit signed offset to branch destination
  - Immediate — Operand in next object code byte(s)
  - Direct — Operand in memory at 0x0000–0x00FF
  - Extended — Operand anywhere in 64-Kbyte address space
  - Indexed relative to H:X — Five submodes including auto increment
  - Indexed relative to SP — Improves C efficiency dramatically
- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

## 7.2 Programmer's Model and CPU Registers

Figure 7-1 shows the five CPU registers. CPU registers are not part of the memory map.

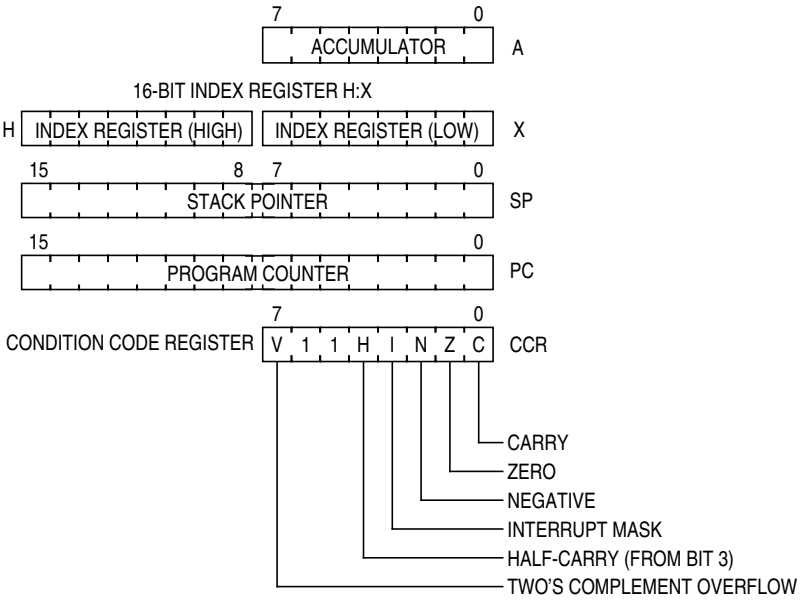



**Figure 7-1. CPU Registers**

### 7.2.1 Accumulator (A)

The A accumulator is a general-purpose 8-bit register. One operand input to the arithmetic logic unit (ALU) is connected to the accumulator and the ALU results are often stored into the A accumulator after arithmetic and logical operations. The accumulator can be loaded from memory using various addressing modes to specify the address where the loaded data comes from, or the contents of A can be stored to memory using various addressing modes to specify the address where data from A will be stored.

Reset has no effect on the contents of the A accumulator.

### 7.2.2 Index Register (H:X)

This 16-bit register is actually two separate 8-bit registers (H and X), which often work together as a 16-bit address pointer where H holds the upper byte of an address and X holds the lower byte of the address. All indexed addressing mode instructions use the full 16-bit value in H:X as an index reference pointer; however, for compatibility with the earlier M68HC05 Family, some instructions operate only on the low-order 8-bit half (X).

Many instructions treat X as a second general-purpose 8-bit register that can be used to hold 8-bit data values. X can be cleared, incremented, decremented, complemented, negated, shifted, or rotated. Transfer instructions allow data to be transferred from A or transferred to A where arithmetic and logical operations can then be performed.

For compatibility with the earlier M68HC05 Family, H is forced to 0x00 during reset. Reset has no effect on the contents of X.

### 7.2.3 Stack Pointer (SP)

This 16-bit address pointer register points at the next available location on the automatic last-in-first-out (LIFO) stack. The stack may be located anywhere in the 64-Kbyte address space that has RAM and can be any size up to the amount of available RAM. The stack is used to automatically save the return address for subroutine calls, the return address and CPU registers during interrupts, and for local variables. The AIS (add immediate to stack pointer) instruction adds an 8-bit signed immediate value to SP. This is most often used to allocate or deallocate space for local variables on the stack.

SP is forced to 0x00FF at reset for compatibility with the earlier M68HC05 Family. HCS08 programs normally change the value in SP to the address of the last location (highest address) in on-chip RAM during reset initialization to free up direct page RAM (from the end of the on-chip registers to 0x00FF).

The RSP (reset stack pointer) instruction was included for compatibility with the M68HC05 Family and is seldom used in new HCS08 programs because it only affects the low-order half of the stack pointer.

### 7.2.4 Program Counter (PC)

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

During normal program execution, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, interrupt, and return operations load the program counter with an address other than that of the next sequential location. This is called a change-of-flow.

During reset, the program counter is loaded with the reset vector that is located at 0xFFFE and 0xFFFF. The vector stored there is the address of the first instruction that will be executed after exiting the reset state.

### 7.2.5 Condition Code Register (CCR)

The 8-bit condition code register contains the interrupt mask (I) and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code bits in general terms. For a more detailed explanation of how each instruction sets the CCR bits, refer to the *HCS08 Family Reference Manual, volume 1,* Freescale Semiconductor document order number HCS08RMv1.

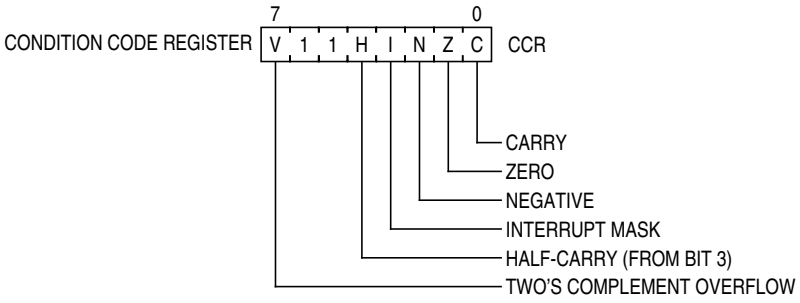



**Figure 7-2. Condition Code Register**

**Table 7-1. CCR Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>V | **Two's Complement Overflow Flag** — The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.<br>0 No overflow<br>1 Overflow |
| 4<br>H | **Half-Carry Flag** — The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C condition code bits to automatically add a correction value to the result from a previous ADD or ADC on BCD operands to correct the result to a valid BCD value.<br>0 No carry between bits 3 and 4<br>1 Carry between bits 3 and 4 |
| 3<br>I | **Interrupt Mask Bit** — When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the first instruction of the interrupt service routine is executed.<br>Interrupts are not recognized at the instruction boundary after any instruction that clears I (CLI or TAP). This ensures that the next instruction after a CLI or TAP will always be executed without the possibility of an intervening interrupt, provided I was set.<br>0 Interrupts enabled<br>1 Interrupts disabled |
| 2<br>N | **Negative Flag** — The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result. Simply loading or storing an 8-bit or 16-bit value causes N to be set if the most significant bit of the loaded or stored value was 1.<br>0 Non-negative result<br>1 Negative result |
| 1<br>Z | **Zero Flag** — The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of 0x00 or 0x0000. Simply loading or storing an 8-bit or 16-bit value causes Z to be set if the loaded or stored value was all 0s.<br>0 Non-zero result<br>1 Zero result |
| 0<br>C | **Carry/Borrow Flag** — The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.<br>0 No carry out of bit 7<br>1 Carry out of bit 7 |

## 7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

### 7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

### 7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

### 7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

### 7.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000–0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.

### 7.3.5 Extended Addressing Mode (EXT)

In extended addressing mode, the full 16-bit address of the operand is located in the next two bytes of program memory after the opcode (high byte first).

### 7.3.6 Indexed Addressing Mode

Indexed addressing mode has seven variations including five that use the 16-bit H:X index register pair and two that use the stack pointer as the base reference.

#### 7.3.6.1 Indexed, No Offset (IX)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair as the address of the operand needed to complete the instruction.

#### 7.3.6.2 Indexed, No Offset with Post Increment (IX+)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair as the address of the operand needed to complete the instruction. The index register pair is then incremented (H:X = H:X + 0x0001) after the operand has been fetched. This addressing mode is only used for MOV and CBEQ instructions.

#### 7.3.6.3 Indexed, 8-Bit Offset (IX1)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction.

#### 7.3.6.4 Indexed, 8-Bit Offset with Post Increment (IX1+)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction. The index register pair is then incremented (H:X = H:X + 0x0001) after the operand has been fetched. This addressing mode is used only for the CBEQ instruction.

#### 7.3.6.5 Indexed, 16-Bit Offset (IX2)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus a 16-bit offset included in the instruction as the address of the operand needed to complete the instruction.

#### 7.3.6.6 SP-Relative, 8-Bit Offset (SP1)

This variation of indexed addressing uses the 16-bit value in the stack pointer (SP) plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction.

#### 7.3.6.7 SP-Relative, 16-Bit Offset (SP2)

This variation of indexed addressing uses the 16-bit value in the stack pointer (SP) plus a 16-bit offset included in the instruction as the address of the operand needed to complete the instruction.

## 7.4 Special Operations

The CPU performs a few special operations that are similar to instructions but do not have opcodes like other CPU instructions. In addition, a few instructions such as STOP and WAIT directly affect other MCU circuitry. This section provides additional information about these operations.

### 7.4.1 Reset Sequence

Reset can be caused by a power-on-reset (POR) event, internal conditions such as the COP (computer operating properly) watchdog, or by assertion of an external active-low reset pin. When a reset event occurs, the CPU immediately stops whatever it is doing (the MCU does not wait for an instruction boundary before responding to a reset event). For a more detailed discussion about how the MCU recognizes resets and determines the source, refer to the Resets, Interrupts, and System Configuration chapter.

The reset event is considered concluded when the sequence to determine whether the reset came from an internal source is done and when the reset pin is no longer asserted. At the conclusion of a reset event, the CPU performs a 6-cycle sequence to fetch the reset vector from 0xFFFE and 0xFFFF and to fill the instruction queue in preparation for execution of the first program instruction.

### 7.4.2 Interrupt Sequence

When an interrupt is requested, the CPU completes the current instruction before responding to the interrupt. At this point, the program counter is pointing at the start of the next instruction, which is where the CPU should return after servicing the interrupt. The CPU responds to an interrupt by performing the same sequence of operations as for a software interrupt (SWI) instruction, except the address used for the vector fetch is determined by the highest priority interrupt that is pending when the interrupt sequence started.

The CPU sequence for an interrupt is:

1. Store the contents of PCL, PCH, X, A, and CCR on the stack, in that order.
2. Set the I bit in the CCR.
3. Fetch the high-order half of the interrupt vector.
4. Fetch the low-order half of the interrupt vector.
5. Delay for one free bus cycle.
6. Fetch three bytes of program information starting at the address indicated by the interrupt vector to fill the instruction queue in preparation for execution of the first instruction in the interrupt service routine.

After the CCR contents are pushed onto the stack, the I bit in the CCR is set to prevent other interrupts while in the interrupt service routine. Although it is possible to clear the I bit with an instruction in the

interrupt service routine, this would allow nesting of interrupts (which is not recommended because it leads to programs that are difficult to debug and maintain).

For compatibility with the earlier M68HC05 MCUs, the high-order half of the H:X index register pair (H) is not saved on the stack as part of the interrupt sequence. The user must use a PSHH instruction at the beginning of the service routine to save H and then use a PULH instruction just before the RTI that ends the interrupt service routine. It is not necessary to save H if you are certain that the interrupt service routine does not use any instructions or auto-increment addressing modes that might change the value of H.

The software interrupt (SWI) instruction is like a hardware interrupt except that it is not masked by the global I bit in the CCR and it is associated with an instruction opcode within the program so it is not asynchronous to program execution.

### 7.4.3 Wait Mode Operation

The WAIT instruction enables interrupts by clearing the I bit in the CCR. It then halts the clocks to the CPU to reduce overall power consumption while the CPU is waiting for the interrupt or reset event that will wake the CPU from wait mode. When an interrupt or reset event occurs, the CPU clocks will resume and the interrupt or reset event will be processed normally.

If a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in wait mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in wait mode.

### 7.4.4 Stop Mode Operation

Usually, all system clocks, including the crystal oscillator (when used), are halted during stop mode to minimize power consumption. In such systems, external circuitry is needed to control the time spent in stop mode and to issue a signal to wake up the target MCU when it is time to resume processing. Unlike the earlier M68HC05 and M68HC08 MCUs, the HCS08 can be configured to keep a minimum set of clocks running in stop mode. This optionally allows an internal periodic signal to wake the target MCU from stop mode.

When a host debug system is connected to the background debug pin (BKGD) and the ENBDM control bit has been set by a serial command through the background interface (or because the MCU was reset into active background mode), the oscillator is forced to remain active when the MCU enters stop mode. In this case, if a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in stop mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in stop mode.

Recovery from stop mode depends on the particular HCS08 and whether the oscillator was stopped in stop mode. Refer to the Modes of Operation chapter for more details.

### 7.4.5 BGND Instruction

The BGND instruction is new to the HCS08 compared to the M68HC08. BGND would not be used in normal user programs because it forces the CPU to stop processing user instructions and enter the active background mode. The only way to resume execution of the user program is through reset or by a host debug system issuing a GO, TRACE1, or TAGGO serial command through the background debug interface.

Software-based breakpoints can be set by replacing an opcode at the desired breakpoint address with the BGND opcode. When the program reaches this breakpoint address, the CPU is forced to active background mode rather than continuing the user program.

## 7.5 HCS08 Instruction Set Summary

Table 7-2 provides a summary of the HCS08 instruction set in all possible addressing modes. The table shows operand construction, execution time in internal bus clock cycles, and cycle-by-cycle details for each addressing mode variation of each instruction.

**Table 7-2. Instruction Set Summary (Sheet 1 of 9)**

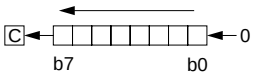
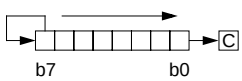
| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| ADC *#opr8i*<br>ADC *opr8a*<br>ADC *opr16a*<br>ADC *oprx16*,X<br>ADC *oprx8*,X<br>ADC ,X<br>ADC *oprx16*,SP<br>ADC *oprx8*,SP | Add with Carry<br>A ← (A) + (M) + (C) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A9 ii<br>B9 dd<br>C9 hh ll<br>D9 ee ff<br>E9 ff<br>F9<br>9E D9 ee ff<br>9E E9 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 ↕ | – ↕ ↕ ↕ |
| ADD *#opr8i*<br>ADD *opr8a*<br>ADD *opr16a*<br>ADD *oprx16*,X<br>ADD *oprx8*,X<br>ADD ,X<br>ADD *oprx16*,SP<br>ADD *oprx8*,SP | Add without Carry<br>A ← (A) + (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | AB ii<br>BB dd<br>CB hh ll<br>DB ee ff<br>EB ff<br>FB<br>9E DB ee ff<br>9E EB ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 ↕ | – ↕ ↕ ↕ |
| AIS *#opr8i* | Add Immediate Value (Signed) to Stack Pointer<br>SP ← (SP) + (M) | IMM | A7 ii | 2 | pp | – 1 1 – | – – – – |
| AIX *#opr8i* | Add Immediate Value (Signed) to Index Register (H:X)<br>H:X ← (H:X) + (M) | IMM | AF ii | 2 | pp | – 1 1 – | – – – – |
| AND *#opr8i*<br>AND *opr8a*<br>AND *opr16a*<br>AND *oprx16*,X<br>AND *oprx8*,X<br>AND ,X<br>AND *oprx16*,SP<br>AND *oprx8*,SP | Logical AND<br>A ← (A) & (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A4 ii<br>B4 dd<br>C4 hh ll<br>D4 ee ff<br>E4 ff<br>F4<br>9E D4 ee ff<br>9E E4 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |
| ASL *opr8a*<br>ASLA<br>ASLX<br>ASL *oprx8*,X<br>ASL ,X<br>ASL *oprx8*,SP | Arithmetic Shift Left<br>  <br>(Same as LSL) | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 38 dd<br>48<br>58<br>68 ff<br>78<br>9E 68 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| ASR *opr8a*<br>ASRA<br>ASRX<br>ASR *oprx8*,X<br>ASR ,X<br>ASR *oprx8*,SP | Arithmetic Shift Right<br>  | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 37 dd<br>47<br>57<br>67 ff<br>77<br>9E 67 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |

**Table 7-2. Instruction Set Summary (Sheet 2 of 9)**

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| BCC *rel* | Branch if Carry Bit Clear (if C = 0) | REL | 24 rr | 3 | ppp | – 1 1 – | – – – – |
| BCLR *n*,*opr8a* | Clear Bit n in Memory (Mn ← 0) | DIR (b0)<br>DIR (b1)<br>DIR (b2)<br>DIR (b3)<br>DIR (b4)<br>DIR (b5)<br>DIR (b6)<br>DIR (b7) | 11 dd<br>13 dd<br>15 dd<br>17 dd<br>19 dd<br>1B dd<br>1D dd<br>1F dd | 5<br>5<br>5<br>5<br>5<br>5<br>5<br>5 | rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp | – 1 1 – | – – – – |
| BCS *rel* | Branch if Carry Bit Set (if C = 1)(Same as BLO) | REL | 25 rr | 3 | ppp | – 1 1 – | – – – – |
| BEQ *rel* | Branch if Equal (if Z = 1) | REL | 27 rr | 3 | ppp | – 1 1 – | – – – – |
| BGE *rel* | Branch if Greater Than or Equal To (if N ⊕ V = 0) (Signed) | REL | 90 rr | 3 | ppp | – 1 1 – | – – – – |
| BGND | Enter active background if ENBDM=1<br>Waits for and processes BDM commands until GO, TRACE1, or TAGGO | INH | 82 | 5+ | fp...ppp | – 1 1 – | – – – – |
| BGT *rel* | Branch if Greater Than (if Z \| (N ⊕ V) = 0) (Signed) | REL | 92 rr | 3 | ppp | – 1 1 – | – – – – |
| BHCC *rel* | Branch if Half Carry Bit Clear (if H = 0) | REL | 28 rr | 3 | ppp | – 1 1 – | – – – – |
| BHCS *rel* | Branch if Half Carry Bit Set (if H = 1) | REL | 29 rr | 3 | ppp | – 1 1 – | – – – – |
| BHI *rel* | Branch if Higher (if C \| Z = 0) | REL | 22 rr | 3 | ppp | – 1 1 – | – – – – |
| BHS *rel* | Branch if Higher or Same (if C = 0) (Same as BCC) | REL | 24 rr | 3 | ppp | – 1 1 – | – – – – |
| BIH *rel* | Branch if IRQ Pin High (if IRQ pin = 1) | REL | 2F rr | 3 | ppp | – 1 1 – | – – – – |
| BIL *rel* | Branch if IRQ Pin Low (if IRQ pin = 0) | REL | 2E rr | 3 | ppp | – 1 1 – | – – – – |
| BIT #*opr8i*<br>BIT *opr8a*<br>BIT *opr16a*<br>BIT *oprx16*,X<br>BIT *oprx8*,X<br>BIT ,X<br>BIT *oprx16*,SP<br>BIT *oprx8*,SP | Bit Test (A) & (M)(CCR Updated but Operands Not Changed) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A5 ii<br>B5 dd<br>C5 hh ll<br>D5 ee ff<br>E5 ff<br>F5<br>9E D5 ee ff<br>9E E5 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |
| BLE *rel* | Branch if Less Than or Equal To (if Z \| (N ⊕ V) = 1) (Signed) | REL | 93 rr | 3 | ppp | – 1 1 – | – – – – |
| BLO *rel* | Branch if Lower (if C = 1) (Same as BCS) | REL | 25 rr | 3 | ppp | – 1 1 – | – – – – |
| BLS *rel* | Branch if Lower or Same (if C \| Z = 1) | REL | 23 rr | 3 | ppp | – 1 1 – | – – – – |
| BLT *rel* | Branch if Less Than (if N ⊕ V = 1) (Signed) | REL | 91 rr | 3 | ppp | – 1 1 – | – – – – |
| BMC *rel* | Branch if Interrupt Mask Clear (if I = 0) | REL | 2C rr | 3 | ppp | – 1 1 – | – – – – |
| BMI *rel* | Branch if Minus (if N = 1) | REL | 2B rr | 3 | ppp | – 1 1 – | – – – – |
| BMS *rel* | Branch if Interrupt Mask Set (if I = 1) | REL | 2D rr | 3 | ppp | – 1 1 – | – – – – |
| BNE *rel* | Branch if Not Equal (if Z = 0) | REL | 26 rr | 3 | ppp | – 1 1 – | – – – – |

## Table 7-2. Instruction Set Summary (Sheet 3 of 9)

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| BPL *rel* | Branch if Plus (if N = 0) | REL | 2A rr | 3 | ppp | – 1 1 – | – – – – |
| BRA *rel* | Branch Always (if I = 1) | REL | 20 rr | 3 | ppp | – 1 1 – | – – – – |
| BRCLR *n*,*opr8a*,*rel* | Branch if Bit *n* in Memory Clear (if (Mn) = 0) | DIR (b0)<br>DIR (b1)<br>DIR (b2)<br>DIR (b3)<br>DIR (b4)<br>DIR (b5)<br>DIR (b6)<br>DIR (b7) | 01 dd rr<br>03 dd rr<br>05 dd rr<br>07 dd rr<br>09 dd rr<br>0B dd rr<br>0D dd rr<br>0F dd rr | 5<br>5<br>5<br>5<br>5<br>5<br>5<br>5 | rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp | – 1 1 – | – – – ↕ |
| BRN *rel* | Branch Never (if I = 0) | REL | 21 rr | 3 | ppp | – 1 1 – | – – – – |
| BRSET *n*,*opr8a*,*rel* | Branch if Bit *n* in Memory Set (if (Mn) = 1) | DIR (b0)<br>DIR (b1)<br>DIR (b2)<br>DIR (b3)<br>DIR (b4)<br>DIR (b5)<br>DIR (b6)<br>DIR (b7) | 00 dd rr<br>02 dd rr<br>04 dd rr<br>06 dd rr<br>08 dd rr<br>0A dd rr<br>0C dd rr<br>0E dd rr | 5<br>5<br>5<br>5<br>5<br>5<br>5<br>5 | rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp<br>rpppp | – 1 1 – | – – – ↕ |
| BSET *n*,*opr8a* | Set Bit *n* in Memory (Mn ← 1) | DIR (b0)<br>DIR (b1)<br>DIR (b2)<br>DIR (b3)<br>DIR (b4)<br>DIR (b5)<br>DIR (b6)<br>DIR (b7) | 10 dd<br>12 dd<br>14 dd<br>16 dd<br>18 dd<br>1A dd<br>1C dd<br>1E dd | 5<br>5<br>5<br>5<br>5<br>5<br>5<br>5 | rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp<br>rfwpp | – 1 1 – | – – – – |
| BSR *rel* | Branch to Subroutine PC ← (PC) + $0002<br>push (PCL); SP ← (SP) – $0001<br>push (PCH); SP ← (SP) – $0001<br>PC ← (PC) + *rel* | REL | AD rr | 5 | ssppp | – 1 1 – | – – – – |
| CBEQ *opr8a*,*rel*<br>CBEQA #*opr8i*,*rel*<br>CBEQX #*opr8i*,*rel*<br>CBEQ *oprx8*,X+,*rel*<br>CBEQ ,X+,*rel*<br>CBEQ *oprx8*,SP,*rel* | Compare and... Branch if (A) = (M)<br>Branch if (A) = (M)<br>Branch if (X) = (M)<br>Branch if (A) = (M)<br>Branch if (A) = (M)<br>Branch if (A) = (M) | DIR<br>IMM<br>IMM<br>IX1+<br>IX+<br>SP1 | 31 dd<br>41 rrii<br>51 rrii<br>61 rrff<br>71 rrrrf<br>9E 61 f rr | 5<br>4<br>4<br>5<br>5<br>6 | rpppp<br>pppp<br>pppp<br>rpppp<br>rfppp<br>prpppp | – 1 1 – | – – – – |
| CLC | Clear Carry Bit (C ← 0) | INH | 98 | 1 | p | – 1 1 – | – – – 0 |
| CLI | Clear Interrupt Mask Bit (I ← 0) | INH | 9A | 1 | p | – 1 1 – | 0 – – – |
| CLR *opr8a*<br>CLRA<br>CLRX<br>CLRH<br>CLR *oprx8*,X<br>CLR ,X<br>CLR *oprx8*,SP | Clear M ← $00<br>A ← $00<br>X ← $00<br>H ← $00<br>M ← $00<br>M ← $00<br>M ← $00 | DIR<br>INH<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 3F dd<br>4F<br>5F<br>8C<br>6F ff<br>7F<br>9E 6F ff | 5<br>1<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | 0 1 1 – | – 0 1 – |

**Table 7-2. Instruction Set Summary (Sheet 4 of 9)**

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| CMP #*opr8i*<br>CMP *opr8a*<br>CMP *opr16a*<br>CMP *oprx16*,X<br>CMP *oprx8*,X<br>CMP ,X<br>CMP *oprx16*,SP<br>CMP *oprx8*,SP | Compare Accumulator with Memory A – M<br>(CCR Updated But Operands Not Changed) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A1 ii<br>B1 dd<br>C1 hh ll<br>D1 ee ff<br>E1 ff<br>F1<br>9E D1 ee ff<br>9E E1 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| COM *opr8a*<br>COMA<br>COMX<br>COM *oprx8*,X<br>COM ,X<br>COM *oprx8*,SP | Complement (One's Complement)<br>M ← ($\overline{M}$)= $FF – (M)<br>A ← ($\overline{A}$) = $FF – (A)<br>X ← ($\overline{X}$) = $FF – (X)<br>M ← ($\overline{M}$) = $FF – (M)<br>M ← ($\overline{M}$) = $FF – (M)<br>M ← ($\overline{M}$) = $FF – (M) | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 33 dd<br>43<br>53<br>63 ff<br>73<br>9E 63 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | 0 1 1 – | – ↕ ↕ 1 |
| CPHX *opr16a*<br>CPHX #*opr16i*<br>CPHX *opr8a*<br>CPHX *oprx8*,SP | Compare Index Register (H:X) with Memory<br>(H:X) – (M:M + $0001)<br>(CCR Updated But Operands Not Changed) | EXT<br>IMM<br>DIR<br>SP1 | 3E hh ll<br>65 jj kk<br>75 dd<br>9E F3 ff | 6<br>3<br>5<br>6 | prrfpp<br>ppp<br>rrfpp<br>prrfpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| CPX #*opr8i*<br>CPX *opr8a*<br>CPX *opr16a*<br>CPX *oprx16*,X<br>CPX *oprx8*,X<br>CPX ,X<br>CPX *oprx16*,SP<br>CPX *oprx8*,SP | Compare X (Index Register Low) with Memory<br>X – M<br>(CCR Updated But Operands Not Changed) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A3 ii<br>B3 dd<br>C3 hh ll<br>D3 ee ff<br>E3 ff<br>F3<br>9E D3 ee ff<br>9E E3 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| DAA | Decimal Adjust Accumulator After ADD or ADC of BCD Values | INH | 72 | 1 | p | U 1 1 – | – ↕ ↕ ↕ |
| DBNZ *opr8a*,*rel*<br>DBNZA *rel*<br>DBNZX *rel*<br>DBNZ *oprx8*,X,*rel*<br>DBNZ ,X,*rel*<br>DBNZ *oprx8*,SP,*rel* | Decrement A, X, or M and Branch if Not Zero (if (result) ≠ 0)<br>DBNZX Affects X Not H | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 3B dd rr<br>4B rr<br>5B rr<br>6B ff rr<br>7B rr<br>9E 6B ff rr | 7<br>4<br>4<br>7<br>6<br>8 | rfwpppp<br>fppp<br>fppp<br>rfwpppp<br>rfwppp<br>prfwpppp | – 1 1 – | – – – – |
| DEC *opr8a*<br>DECA<br>DECX<br>DEC *oprx8*,X<br>DEC ,X<br>DEC *oprx8*,SP | Decrement<br>M ← (M) – $01<br>A ← (A) – $01<br>X ← (X) – $01<br>M ← (M) – $01<br>M ← (M) – $01<br>M ← (M) – $01 | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 3A dd<br>4A<br>5A<br>6A ff<br>7A<br>9E 6A ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ – |
| DIV | Divide<br>A ← (H:A)÷(X); H ← Remainder | INH | 52 | 6 | fffffp | – 1 1 – | – – ↕ ↕ |
| EOR #*opr8i*<br>EOR *opr8a*<br>EOR *opr16a*<br>EOR *oprx16*,X<br>EOR *oprx8*,X<br>EOR ,X<br>EOR *oprx16*,SP<br>EOR *oprx8*,SP | Exclusive OR Memory with Accumulator<br>A ← (A ⊕ M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A8 ii<br>B8 dd<br>C8 hh ll<br>D8 ee ff<br>E8 ff<br>F8<br>9E D8 ee ff<br>9E E8 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |

## Table 7-2. Instruction Set Summary (Sheet 5 of 9)

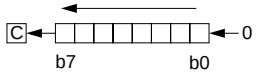
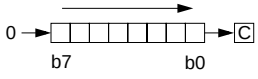
| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| INC *oprx8*,X<br>INC ,X<br>INC *oprx8*,SP | Increment M ← (M) + $01<br>A ← (A) + $01<br>X ← (X) + $01<br>M ← (M) + $01<br>M ← (M) + $01<br>M ← (M) + $01 | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 3C dd<br>4C<br>5C<br>6C ff<br>7C<br>9E 6C ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ – |
| JMP *opr8a*<br>JMP *opr16a*<br>JMP *oprx16*,X<br>JMP *oprx8*,X<br>JMP ,X | Jump<br>PC ← Jump Address | DIR<br>EXT<br>IX2<br>IX1<br>IX | BC dd<br>CC hh ll<br>DC ee ff<br>EC ff<br>FC | 3<br>4<br>4<br>3<br>3 | ppp<br>pppp<br>pppp<br>ppp<br>ppp | – 1 1 – | – – – – |
| JSR *opr8a*<br>JSR *opr16a*<br>JSR *oprx16*,X<br>JSR *oprx8*,X<br>JSR ,X | Jump to Subroutine<br>PC ← (PC) + *n* (*n* = 1, 2, or 3)<br>Push (PCL); SP ← (SP) – $0001<br>Push (PCH); SP ← (SP) – $0001<br>PC ← Unconditional Address | DIR<br>EXT<br>IX2<br>IX1<br>IX | BD dd<br>CD hh ll<br>DD ee ff<br>ED ff<br>FD | 5<br>6<br>6<br>5<br>5 | ssppp<br>pssppp<br>pssppp<br>ssppp<br>ssppp | – 1 1 – | – – – – |
| LDA *#opr8i*<br>LDA *opr8a*<br>LDA *opr16a*<br>LDA *oprx16*,X<br>LDA *oprx8*,X<br>LDA ,X<br>LDA *oprx16*,SP<br>LDA *oprx8*,SP | Load Accumulator from Memory<br>A ← (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A6 ii<br>B6 dd<br>C6 hh ll<br>D6 ee ff<br>E6 ff<br>F6<br>9E D6 ee ff<br>9E E6 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |
| LDHX *#opr16i*<br>LDHX *opr8a*<br>LDHX *opr16a*<br>LDHX ,X<br>LDHX *oprx16*,X<br>LDHX *oprx8*,X<br>LDHX *oprx8*,SP | Load Index Register (H:X)<br>H:X ← (M:M + $0001) | IMM<br>DIR<br>EXT<br>IX<br>IX2<br>IX1<br>SP1 | 45 jj kk<br>55 dd<br>32 hh ll<br>9E AE<br>9E BE ee ff<br>9E CE ff<br>9E FE ff | 3<br>4<br>5<br>5<br>6<br>5<br>5 | ppp<br>rrpp<br>prrpp<br>prrfp<br>pprrpp<br>prrpp<br>prrpp | 0 1 1 – | – ↕ ↕ – |
| LDX *#opr8i*<br>LDX *opr8a*<br>LDX *opr16a*<br>LDX *oprx16*,X<br>LDX *oprx8*,X<br>LDX ,X<br>LDX *oprx16*,SP<br>LDX *oprx8*,SP | Load X (Index Register Low) from Memory<br>X ← (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | AE ii<br>BE dd<br>CE hh ll<br>DE ee ff<br>EE ff<br>FE<br>9E DE ee ff<br>9E EE ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |
| LSL *oprx8*,X<br>LSL ,X<br>LSL *oprx8*,SP | Logical Shift Left<br>  <br><br>(Same as ASL) | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 38 dd<br>48<br>58<br>68 ff<br>78<br>9E 68 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| LSR *oprx8*,X<br>LSR ,X<br>LSR *oprx8*,SP | Logical Shift Right<br>  <br> | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 34 dd<br>44<br>54<br>64 ff<br>74<br>9E 64 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – 0 ↕ ↕ |

**Table 7-2. Instruction Set Summary (Sheet 6 of 9)**

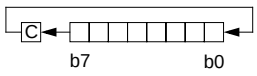
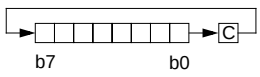
| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR V 1 1 H | Affecton CCR I N Z C |
|---|---|---|---|---|---|---|---|
| MOV *opr8a*,*opr8a*<br>MOV *opr8a*,X+<br>MOV *#opr8i*,*opr8a*<br>MOV ,X+,*opr8a* | Move<br>$(M)_{destination} \leftarrow (M)_{source}$<br>In IX+/DIR and DIR/IX+ Modes, H:X ← (H:X) + $0001 | DIR/DIR<br>DIR/IX+<br>IMM/DIR<br>IX+/DIR | 4E dd dd<br>5E dd<br>6E ii dd<br>7E dd | 5<br>5<br>4<br>5 | rpwpp<br>rfwpp<br>pwpp<br>rfwpp | 0 1 1 – | – ↕ ↕ – |
| MUL | Unsigned multiply<br>X:A ← (X) × (A) | INH | 42 | 5 | fffffp | – 1 1 0 | – – – 0 |
| NEG *opr8a*<br>NEGA<br>NEGX<br>NEG *oprx8*,X<br>NEG ,X<br>NEG *oprx8*,SP | Negate (Two's Complement)<br>M ← – (M) = $00 – (M)<br>A ← – (A) = $00 – (A)<br>X ← – (X) = $00 – (X)<br>M ← – (M) = $00 – (M)<br>M ← – (M) = $00 – (M)<br>M ← – (M) = $00 – (M) | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 30 dd<br>40<br>50<br>60 ff<br>70<br>9E 60 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| NOP | No Operation — Uses 1 Bus Cycle | INH | 9D | 1 | p | – 1 1 – | – – – – |
| NSA | Nibble Swap Accumulator<br>A ← (A[3:0]:A[7:4]) | INH | 62 | 1 | p | – 1 1 – | – – – – |
| ORA *#opr8i*<br>ORA *opr8a*<br>ORA *opr16a*<br>ORA *oprx16*,X<br>ORA *oprx8*,X<br>ORA ,X<br>ORA *oprx16*,SP<br>ORA *oprx8*,SP | Inclusive OR Accumulator and Memory<br>A ← (A) \| (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | AA ii<br>BA dd<br>CA hh ll<br>DA ee ff<br>EA ff<br>FA<br>9E DA ee ff<br>9E EA ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | 0 1 1 – | – ↕ ↕ – |
| PSHA | Push Accumulator onto Stack<br>Push (A); SP ← (SP) – $0001 | INH | 87 | 2 | sp | – 1 1 – | – – – – |
| PSHH | Push H (Index Register High) onto Stack<br>Push (H); SP ← (SP) – $0001 | INH | 8B | 2 | sp | – 1 1 – | – – – – |
| PSHX | Push X (Index Register Low) onto Stack<br>Push (X); SP ← (SP) – $0001 | INH | 89 | 2 | sp | – 1 1 – | – – – – |
| PULA | Pull Accumulator from Stack<br>SP ← (SP + $0001); Pull (A) | INH | 86 | 3 | ufp | – 1 1 – | – – – – |
| PULH | Pull H (Index Register High) from Stack<br>SP ← (SP + $0001); Pull (H) | INH | 8A | 3 | ufp | – 1 1 – | – – – – |
| PULX | Pull X (Index Register Low) from Stack<br>SP ← (SP + $0001); Pull (X) | INH | 88 | 3 | ufp | – 1 1 – | – – – – |
| ROL *opr8a*<br>ROLA<br>ROLX<br>ROL *oprx8*,X<br>ROL ,X<br>ROL *oprx8*,SP | Rotate Left through Carry<br>  | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 39 dd<br>49<br>59<br>69 ff<br>79<br>9E 69 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| ROR *opr8a*<br>RORA<br>RORX<br>ROR *oprx8*,X<br>ROR ,X<br>ROR *oprx8*,SP | Rotate Right through Carry<br>  | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 36 dd<br>46<br>56<br>66 ff<br>76<br>9E 66 ff | 5<br>1<br>1<br>5<br>4<br>6 | rfwpp<br>p<br>p<br>rfwpp<br>rfwp<br>prfwpp | ↕ 1 1 – | – ↕ ↕ ↕ |

**Table 7-2. Instruction Set Summary (Sheet 7 of 9)**

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| RSP | Reset Stack Pointer (Low Byte)<br>SPL ← $FF<br>(High Byte Not Affected) | INH | 9C | 1 | p | – 1 1 – | – – – – |
| RTI | Return from Interrupt<br>SP ← (SP) + $0001; Pull (CCR)<br>SP ← (SP) + $0001; Pull (A)<br>SP ← (SP) + $0001; Pull (X)<br>SP ← (SP) + $0001; Pull (PCH)<br>SP ← (SP) + $0001; Pull (PCL) | INH | 80 | 9 | uuuuufppp | ↕ 1 1 ↕ | ↕ ↕ ↕ ↕ |
| RTS | Return from Subroutine<br>SP ← SP + $0001; Pull (PCH)<br>SP ← SP + $0001; Pull (PCL) | INH | 81 | 5 | ufppp | – 1 1 – | – – – – |
| SBC *#opr8i*<br>SBC *opr8a*<br>SBC *opr16a*<br>SBC *oprx16*,X<br>SBC *oprx8*,X<br>SBC ,X<br>SBC *oprx16*,SP<br>SBC *oprx8*,SP | Subtract with Carry<br>A ← (A) – (M) – (C) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A2 ii<br>B2 dd<br>C2 hh ll<br>D2 ee ff<br>E2 ff<br>F2<br>9E D2 ee ff<br>9E E2 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| SEC | Set Carry Bit<br>(C ← 1) | INH | 99 | 1 | p | – 1 1 – | – – – 1 |
| SEI | Set Interrupt Mask Bit<br>(I ← 1) | INH | 9B | 1 | p | – 1 1 – | 1 – – – |
| STA *opr8a*<br>STA *opr16a*<br>STA *oprx16*,X<br>STA *oprx8*,X<br>STA ,X<br>STA *oprx16*,SP<br>STA *oprx8*,SP | Store Accumulator in Memory<br>M ← (A) | DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | B7 dd<br>C7 hh ll<br>D7 ee ff<br>E7 ff<br>F7<br>9E D7 ee ff<br>9E E7 ff | 3<br>4<br>4<br>3<br>2<br>5<br>4 | wpp<br>pwpp<br>pwpp<br>wpp<br>wp<br>ppwpp<br>pwpp | 0 1 1 – | – ↕ ↕ – |
| STHX *opr8a*<br>STHX *opr16a*<br>STHX *oprx8*,SP | Store H:X (Index Reg.)<br>(M:M + $0001) ← (H:X) | DIR<br>EXT<br>SP1 | 35 dd<br>96 hh ll<br>9E FF ff | 4<br>5<br>5 | wwpp<br>pwwpp<br>pwwpp | 0 1 1 – | – ↕ ↕ – |
| STOP | Enable Interrupts: Stop Processing<br>Refer to MCU Documentation<br>I bit ← 0; Stop Processing | INH | 8E | 2 | fp... | – 1 1 – | 0 – – – |
| STX *opr8a*<br>STX *opr16a*<br>STX *oprx16*,X<br>STX *oprx8*,X<br>STX ,X<br>STX *oprx16*,SP<br>STX *oprx8*,SP | Store X (Low 8 Bits of Index Register)in Memory<br>M ← (X) | DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | BF dd<br>CF hh ll<br>DF ee ff<br>EF ff<br>FF<br>9E DF ee ff<br>9E EF ff | 3<br>4<br>4<br>3<br>2<br>5<br>4 | wpp<br>pwpp<br>pwpp<br>wpp<br>wp<br>ppwpp<br>pwpp | 0 1 1 – | – ↕ ↕ – |

**Table 7-2. Instruction Set Summary (Sheet 8 of 9)**

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| SUB *#opr8i*<br>SUB *opr8a*<br>SUB *opr16a*<br>SUB *oprx16*,X<br>SUB *oprx8*,X<br>SUB ,X<br>SUB *oprx16*,SP<br>SUB *oprx8*,SP | Subtract<br>A ← (A) – (M) | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX<br>SP2<br>SP1 | A0 ii<br>B0 dd<br>C0 hh ll<br>D0 ee ff<br>E0 ff<br>F0<br>9E D0 ee ff<br>9E E0 ff | 2<br>3<br>4<br>4<br>3<br>3<br>5<br>4 | pp<br>rpp<br>prpp<br>prpp<br>rpp<br>rfp<br>pprpp<br>prpp | ↕ 1 1 – | – ↕ ↕ ↕ |
| SWI | Software Interrupt<br>PC ← (PC) + $0001<br>Push (PCL); SP ← (SP) – $0001<br>Push (PCH); SP ← (SP) – $0001<br>Push (X); SP ← (SP) – $0001<br>Push (A); SP ← (SP) – $0001<br>Push (CCR); SP ← (SP) – $0001<br>I ← 1;<br>PCH ← Interrupt Vector High Byte<br>PCL ← Interrupt Vector Low Byte | INH | 83 | 11 | ssssvvfppp | – 1 1 – | 1 – – – |
| TAP | Transfer Accumulator to CCR<br>CCR ← (A) | INH | 84 | 1 | p | ↕ 1 1 ↕ | ↕ ↕ ↕ ↕ |
| TAX | Transfer Accumulator to X (Index Register Low)<br>X ← (A) | INH | 97 | 1 | p | – 1 1 – | – – – – |
| TPA | Transfer CCR to Accumulator<br>A ← (CCR) | INH | 85 | 1 | p | – 1 1 – | – – – – |
| TST *opr8a*<br>TSTA<br>TSTX<br>TST *oprx8*,X<br>TST ,X<br>TST *oprx8*,SP | Test for Negative or Zero (M) – $00<br>(A) – $00<br>(X) – $00<br>(M) – $00<br>(M) – $00<br>(M) – $00 | DIR<br>INH<br>INH<br>IX1<br>IX<br>SP1 | 3D dd<br>4D<br>5D<br>6D ff<br>7D<br>9E 6D ff | 4<br>1<br>1<br>4<br>3<br>5 | rfpp<br>p<br>p<br>rfpp<br>rfp<br>prfpp | 0 1 1 – | – ↕ ↕ – |
| TSX | Transfer SP to Index Reg.<br>H:X ← (SP) + $0001 | INH | 95 | 2 | fp | – 1 1 – | – – – – |
| TXA | Transfer X (Index Reg. Low) to Accumulator<br>A ← (X) | INH | 9F | 1 | p | – 1 1 – | – – – – |

## Table 7-2. Instruction Set Summary (Sheet 9 of 9)

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affecton CCR | |
|---|---|---|---|---|---|---|---|
| | | | | | | V 1 1 H | I N Z C |
| TXS | Transfer Index Reg. to SP<br>SP ← (H:X) – $0001 | INH | 94 | 2 | fp | – 1 1 – | – – – – |
| WAIT | Enable Interrupts; Wait for Interrupt<br>I bit ← 0; Halt CPU | INH | 8F | 2+ | fp... | – 1 1 – | 0 – – – |

**Source Form:** Everything in the source forms columns, *except expressions in italic characters*, is literal information which must appear in the assembly source file exactly as shown. The initial 3- to 5-letter mnemonic and the characters (#, ( ) and +) are always a literal characters.

| | |
|---|---|
| *n* | Any label or expression that evaluates to a single integer in the range 0-7. |
| *opr8i* | Any label or expression that evaluates to an 8-bit immediate value. |
| *opr16i* | Any label or expression that evaluates to a 16-bit immediate value. |
| *opr8a* | Any label or expression that evaluates to an 8-bit direct-page address ($00xx). |
| *opr16a* | Any label or expression that evaluates to a 16-bit address. |
| *oprx8* | Any label or expression that evaluates to an unsigned 8-bit value, used for indexed addressing. |
| *oprx16* | Any label or expression that evaluates to a 16-bit value, used for indexed addressing. |
| *rel* | Any label or expression that refers to an address that is within –128 to +127 locations from the start of the next instruction. |

**Operation Symbols:**

| | |
|---|---|
| A | Accumulator |
| CCR | Condition code register |
| H | Index register high byte |
| M | Memory location |
| *n* | Any bit |
| *opr* | Operand (one or two bytes) |
| PC | Program counter |
| PCH | Program counter high byte |
| PCL | Program counter low byte |
| *rel* | Relative program counter offset byte |
| SP | Stack pointer |
| SPL | Stack pointer low byte |
| X | Index register low byte |
| & | Logical AND |
| \| | Logical OR |
| ⊕ | Logical EXCLUSIVE OR |
| ( ) | Contents of |
| + | Add |
| – | Subtract, Negation (two's complement) |
| × | Multiply |
| ÷ | Divide |
| # | Immediate value |
| ← | Loaded with |
| : | Concatenated with |

**Addressing Modes:**

| | |
|---|---|
| DIR | Direct addressing mode |
| EXT | Extended addressing mode |
| IMM | Immediate addressing mode |
| INH | Inherent addressing mode |
| IX | Indexed, no offset addressing mode |
| IX1 | Indexed, 8-bit offset addressing mode |
| IX2 | Indexed, 16-bit offset addressing mode |
| IX+ | Indexed, no offset, post increment addressing mode |
| IX1+ | Indexed, 8-bit offset, post increment addressing mode |
| REL | Relative addressing mode |
| SP1 | Stack pointer, 8-bit offset addressing mode |
| SP2 | Stack pointer 16-bit offset addressing mode |

**Cycle-by-Cycle Codes:**

| | |
|---|---|
| f | Free cycle. This indicates a cycle where the CPU does not require use of the system buses. An f cycle is always one cycle of the system bus clock and is always a read cycle. |
| p | Program fetch; read from next consecutive location in program memory |
| r | Read 8-bit operand |
| s | Push (write) one byte onto stack |
| u | Pop (read) one byte from stack |
| v | Read vector from $FFxx (high byte first) |
| w | Write 8-bit operand |

**CCR Bits:**

| | |
|---|---|
| V | Overflow bit |
| H | Half-carry bit |
| I | Interrupt mask |
| N | Negative bit |
| Z | Zero bit |
| C | Carry/borrow bit |

**CCR Effects:**

| | |
|---|---|
| ↕ | Set or cleared |
| – | Not affected |
| U | Undefined |

## Table 7-3. Opcode Map (Sheet 1 of 2)

| Bit-Manipulation | | Branch | Read-Modify-Write | | | | | Control | | Register/Memory | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 5 BRSET0 3 DIR | 10 5 BSET0 2 DIR | 20 3 BRA 2 REL | 30 5 NEG 2 DIR | 40 1 NEGA 1 INH | 50 1 NEGX 1 INH | 60 5 NEG 2 IX1 | 70 4 NEG 1 IX | 80 9 RTI 1 INH | 90 3 BGE 2 REL | A0 2 SUB 2 IMM | B0 3 SUB 2 DIR | C0 4 SUB 3 EXT | D0 4 SUB 3 IX2 | E0 3 SUB 2 IX1 | F0 3 SUB 1 IX |
| 01 5 BRCLR0 3 DIR | 11 5 BCLR0 2 DIR | 21 3 BRN 2 REL | 31 5 CBEQ 3 DIR | 41 4 CBEQA 3 IMM | 51 4 CBEQX 3 IMM | 61 5 CBEQ 3 IX1+ | 71 5 CBEQ 2 IX+ | 81 6 RTS 1 INH | 91 3 BLT 2 REL | A1 2 CMP 2 IMM | B1 3 CMP 2 DIR | C1 4 CMP 3 EXT | D1 4 CMP 3 IX2 | E1 3 CMP 2 IX1 | F1 3 CMP 1 IX |
| 02 5 BRSET1 3 DIR | 12 5 BSET1 2 DIR | 22 3 BHI 2 REL | 32 5 LDHX 3 EXT | 42 5 MUL 1 INH | 52 6 DIV 1 INH | 62 1 NSA 1 INH | 72 1 DAA 1 INH | 82 5+ BGND 1 INH | 92 3 BGT 2 REL | A2 2 SBC 2 IMM | B2 3 SBC 2 DIR | C2 4 SBC 3 EXT | D2 4 SBC 3 IX2 | E2 3 SBC 2 IX1 | F2 3 SBC 1 IX |
| 03 5 BRCLR1 3 DIR | 13 5 BCLR1 2 DIR | 23 3 BLS 2 REL | 33 5 COM 2 DIR | 43 1 COMA 1 INH | 53 1 COMX 1 INH | 63 5 COM 2 IX1 | 73 4 COM 1 IX | 83 11 SWI 1 INH | 93 3 BLE 2 REL | A3 2 CPX 2 IMM | B3 3 CPX 2 DIR | C3 4 CPX 3 EXT | D3 4 CPX 3 IX2 | E3 3 CPX 2 IX1 | F3 3 CPX 1 IX |
| 04 5 BRSET2 3 DIR | 14 5 BSET2 2 DIR | 24 3 BCC 2 REL | 34 5 LSR 2 DIR | 44 1 LSRA 1 INH | 54 1 LSRX 1 INH | 64 5 LSR 2 IX1 | 74 4 LSR 1 IX | 84 1 TAP 1 INH | 94 2 TXS 1 INH | A4 2 AND 2 IMM | B4 3 AND 2 DIR | C4 4 AND 3 EXT | D4 4 AND 3 IX2 | E4 3 AND 2 IX1 | F4 3 AND 1 IX |
| 05 5 BRCLR2 3 DIR | 15 5 BCLR2 2 DIR | 25 3 BCS 2 REL | 35 4 STHX 2 DIR | 45 3 LDHX 3 IMM | 55 4 LDHX 2 DIR | 65 3 CPHX 3 IMM | 75 5 CPHX 2 DIR | 85 1 TPA 1 INH | 95 2 TSX 1 INH | A5 2 BIT 2 IMM | B5 3 BIT 2 DIR | C5 4 BIT 3 EXT | D5 4 BIT 3 IX2 | E5 3 BIT 2 IX1 | F5 3 BIT 1 IX |
| 06 5 BRSET3 3 DIR | 16 5 BSET3 2 DIR | 26 3 BNE 2 REL | 36 5 ROR 2 DIR | 46 1 RORA 1 INH | 56 1 RORX 1 INH | 66 5 ROR 2 IX1 | 76 4 ROR 1 IX | 86 3 PULA 1 INH | 96 5 STHX 3 EXT | A6 2 LDA 2 IMM | B6 3 LDA 2 DIR | C6 4 LDA 3 EXT | D6 4 LDA 3 IX2 | E6 3 LDA 2 IX1 | F6 3 LDA 1 IX |
| 07 5 BRCLR3 3 DIR | 17 5 BCLR3 2 DIR | 27 3 BEQ 2 REL | 37 5 ASR 2 DIR | 47 1 ASRA 1 INH | 57 1 ASRX 1 INH | 67 5 ASR 2 IX1 | 77 4 ASR 1 IX | 87 2 PSHA 1 INH | 97 1 TAX 1 INH | A7 2 AIS 2 IMM | B7 3 STA 2 DIR | C7 4 STA 3 EXT | D7 4 STA 3 IX2 | E7 3 STA 2 IX1 | F7 2 STA 1 IX |
| 08 5 BRSET4 3 DIR | 18 5 BSET4 2 DIR | 28 3 BHCC 2 REL | 38 5 LSL 2 DIR | 48 1 LSLA 1 INH | 58 1 LSLX 1 INH | 68 5 LSL 2 IX1 | 78 4 LSL 1 IX | 88 3 PULX 1 INH | 98 1 CLC 1 INH | A8 2 EOR 2 IMM | B8 3 EOR 2 DIR | C8 4 EOR 3 EXT | D8 4 EOR 3 IX2 | E8 3 EOR 2 IX1 | F8 3 EOR 1 IX |
| 09 5 BRCLR4 3 DIR | 19 5 BCLR4 2 DIR | 29 3 BHCS 2 REL | 39 5 ROL 2 DIR | 49 1 ROLA 1 INH | 59 1 ROLX 1 INH | 69 5 ROL 2 IX1 | 79 4 ROL 1 IX | 89 2 PSHX 1 INH | 99 1 SEC 1 INH | A9 2 ADC 2 IMM | B9 3 ADC 2 DIR | C9 4 ADC 3 EXT | D9 4 ADC 3 IX2 | E9 3 ADC 2 IX1 | F9 3 ADC 1 IX |
| 0A 5 BRSET5 3 DIR | 1A 5 BSET5 2 DIR | 2A 3 BPL 2 REL | 3A 5 DEC 2 DIR | 4A 1 DECA 1 INH | 5A 1 DECX 1 INH | 6A 5 DEC 2 IX1 | 7A 4 DEC 1 IX | 8A 3 PULH 1 INH | 9A 1 CLI 1 INH | AA 2 ORA 2 IMM | BA 3 ORA 2 DIR | CA 4 ORA 3 EXT | DA 4 ORA 3 IX2 | EA 3 ORA 2 IX1 | FA 3 ORA 1 IX |
| 0B 5 BRCLR5 3 DIR | 1B 5 BCLR5 2 DIR | 2B 3 BMI 2 REL | 3B 7 DBNZ 3 DIR | 4B 4 DBNZA 2 INH | 5B 4 DBNZX 2 INH | 6B 7 DBNZ 3 IX1 | 7B 6 DBNZ 2 IX | 8B 2 PSHH 1 INH | 9B 1 SEI 1 INH | AB 2 ADD 2 IMM | BB 3 ADD 2 DIR | CB 4 ADD 3 EXT | DB 4 ADD 3 IX2 | EB 3 ADD 2 IX1 | FB 3 ADD 1 IX |
| 0C 5 BRSET6 3 DIR | 1C 5 BSET6 2 DIR | 2C 3 BMC 2 REL | 3C 5 INC 2 DIR | 4C 1 INCA 1 INH | 5C 1 INCX 1 INH | 6C 5 INC 2 IX1 | 7C 4 INC 1 IX | 8C 1 CLRH 1 INH | 9C 1 RSP 1 INH | | BC 3 JMP 2 DIR | CC 4 JMP 3 EXT | DC 4 JMP 3 IX2 | EC 3 JMP 2 IX1 | FC 3 JMP 1 IX |
| 0D 5 BRCLR6 3 DIR | 1D 5 BCLR6 2 DIR | 2D 3 BMS 2 REL | 3D 4 TST 2 DIR | 4D 1 TSTA 1 INH | 5D 1 TSTX 1 INH | 6D 4 TST 2 IX1 | 7D 3 TST 1 IX | | 9D 1 NOP 1 INH | AD 5 BSR 2 REL | BD 5 JSR 2 DIR | CD 6 JSR 3 EXT | DD 6 JSR 3 IX2 | ED 5 JSR 2 IX1 | FD 5 JSR 1 IX |
| 0E 5 BRSET7 3 DIR | 1E 5 BSET7 2 DIR | 2E 3 BIL 2 REL | 3E 6 CPHX 3 EXT | 4E 5 MOV 3 DD | 5E 5 MOV 2 DIX+ | 6E 4 MOV 3 IMD | 7E 5 MOV 2 IX+D | 8E 2+ STOP 1 INH | 9E Page 2 | AE 2 LDX 2 IMM | BE 3 LDX 2 DIR | CE 4 LDX 3 EXT | DE 4 LDX 3 IX2 | EE 3 LDX 2 IX1 | FE 3 LDX 1 IX |
| 0F 5 BRCLR7 3 DIR | 1F 5 BCLR7 2 DIR | 2F 3 BIH 2 REL | 3F 5 CLR 2 DIR | 4F 1 CLRA 1 INH | 5F 1 CLRX 1 INH | 6F 5 CLR 2 IX1 | 7F 4 CLR 1 IX | 8F 2+ WAIT 1 INH | 9F 1 TXA 1 INH | AF 2 AIX 2 IMM | BF 3 STX 2 DIR | CF 4 STX 3 EXT | DF 4 STX 3 IX2 | EF 3 STX 2 IX1 | FF 2 STX 1 IX |

| | | | | | |
|---|---|---|---|---|---|
| **INH** | **Inherent** | **REL** | **Relative** | **SP1** | **Stack Pointer, 8-Bit Offset** |
| **IMM** | **Immediate** | **IX** | **Indexed, No Offset** | **SP2** | **Stack Pointer, 16-Bit Offset** |
| **DIR** | **Direct** | **IX1** | **Indexed, 8-Bit Offset** | **IX+** | **Indexed, No Offset with Post Increment** |
| **EXT** | **Extended** | **IX2** | **Indexed, 16-Bit Offset** | **IX1+** | **Indexed, 1-Byte Offset with Post Increment** |
| **DD** | **DIR to DIR** | **IMD** | **IMM to DIR** | | |
| **IX+D** | **IX+ to DIR** | **DIX+** | **DIR to IX+** | | |

**Opcode in Hexadecimal** F0 3 SUB **HCS08 Cycles**
**Instruction Mnemonic**
**Number of Bytes** 1 IX **Addressing Mode**

## Table 7-3. Opcode Map (Sheet 2 of 2)

| Bit-Manipulation | | Branch | Read-Modify-Write | | | | | Control | | Register/Memory | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 9E60 6 NEG 3 SP1 | | | | | | | 9ED0 5 SUB 4 SP2 | 9EE0 4 SUB 3 SP1 | |
| | | | | | | 9E61 6 CBEQ 4 SP1 | | | | | | | 9ED1 5 CMP 4 SP2 | 9EE1 4 CMP 3 SP1 | |
| | | | | | | | | | | | | | 9ED2 5 SBC 4 SP2 | 9EE2 4 SBC 3 SP1 | |
| | | | | | | 9E63 6 COM 3 SP1 | | | | | | | 9ED3 5 CPX 4 SP2 | 9EE3 4 CPX 3 SP1 | 9EF3 6 CPHX 3 SP1 |
| | | | | | | 9E64 6 LSR 3 SP1 | | | | | | | 9ED4 5 AND 4 SP2 | 9EE4 4 AND 3 SP1 | |
| | | | | | | | | | | | | | 9ED5 5 BIT 4 SP2 | 9EE5 4 BIT 3 SP1 | |
| | | | | | | 9E66 6 ROR 3 SP1 | | | | | | | 9ED6 5 LDA 4 SP2 | 9EE6 4 LDA 3 SP1 | |
| | | | | | | 9E67 6 ASR 3 SP1 | | | | | | | 9ED7 5 STA 4 SP2 | 9EE7 4 STA 3 SP1 | |
| | | | | | | 9E68 6 LSL 3 SP1 | | | | | | | 9ED8 5 EOR 4 SP2 | 9EE8 4 EOR 3 SP1 | |
| | | | | | | 9E69 6 ROL 3 SP1 | | | | | | | 9ED9 5 ADC 4 SP2 | 9EE9 4 ADC 3 SP1 | |
| | | | | | | 9E6A 6 DEC 3 SP1 | | | | | | | 9EDA 5 ORA 4 SP2 | 9EEA 4 ORA 3 SP1 | |
| | | | | | | 9E6B 8 DBNZ 4 SP1 | | | | | | | 9EDB 5 ADD 4 SP2 | 9EEB 4 ADD 3 SP1 | |
| | | | | | | 9E6C 6 INC 3 SP1 | | | | | | | | | |
| | | | | | | 9E6D 5 TST 3 SP1 | | | | | | | | | |
| | | | | | | | | | | 9EAE 5 LDHX 2 IX | 9EBE 6 LDHX 4 IX2 | 9ECE 5 LDHX 3 IX1 | 9EDE 5 LDX 4 SP2 | 9EEE 4 LDX 3 SP1 | 9EFE 5 LDHX 3 SP1 |
| | | | | | | 9E6F 6 CLR 3 SP1 | | | | | | | 9EDF 5 STX 4 SP2 | 9EEF 4 STX 3 SP1 | 9EFF 5 STHX 3 SP1 |

| | | | | | |
|---|---|---|---|---|---|
| **INH** | **Inherent** | **REL** | **Relative** | **SP1** | **Stack Pointer, 8-Bit Offset** |
| **IMM** | **Immediate** | **IX** | **Indexed, No Offset** | **SP2** | **Stack Pointer, 16-Bit Offset** |
| **DIR** | **Direct** | **IX1** | **Indexed, 8-Bit Offset** | **IX+** | **Indexed, No Offset with Post Increment** |
| **EXT** | **Extended** | **IX2** | **Indexed, 16-Bit Offset** | | |
| **DD** | **DIR to DIR** | **IMD** | **IMM to DIR** | **IX1+** | **Indexed, 1-Byte Offset with Post Increment** |
| **IX+D** | **IX+ to DIR** | **DIX+** | **DIR to IX+** | | |

**Note: All Sheet 2 Opcodes are Preceded by the Page 2 Prebyte (9E)**

**Prebyte (9E) and Opcode in Hexadecimal**
**Number of Bytes**

9E60 6
NEG
3 SP1

**HCS08 Cycles**
**Instruction Mnemonic**
**Addressing Mode**

# Chapter 8
# Analog Comparator 5-V (S08ACMPV3)

## 8.1 Introduction

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages or for comparing one analog input voltage to an internal reference voltage. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).

Figure 8-1 shows the MC9S08SG32 Series block diagram with the ACMP highlighted.

### 8.1.1 ACMP Configuration Information

When using the bandgap reference voltage for input to ACMP+, the user must enable the bandgap buffer by setting BGBE =1 in SPMSC1 see Section 5.7.6, “System Power Management Status and Control 1 Register (SPMSC1)”. For value of bandgap voltage reference see Section A.6, “DC Characteristics”.

### 8.1.2 ACMP/TPM Configuration Information

The ACMP module can be configured to connect the output of the analog comparator to TPM1 input capture channel 0 by setting ACIC in SOPT2. With ACIC set, the TPM1CH0 pin is not available externally regardless of the configuration of the TPM1 module for channel 0.

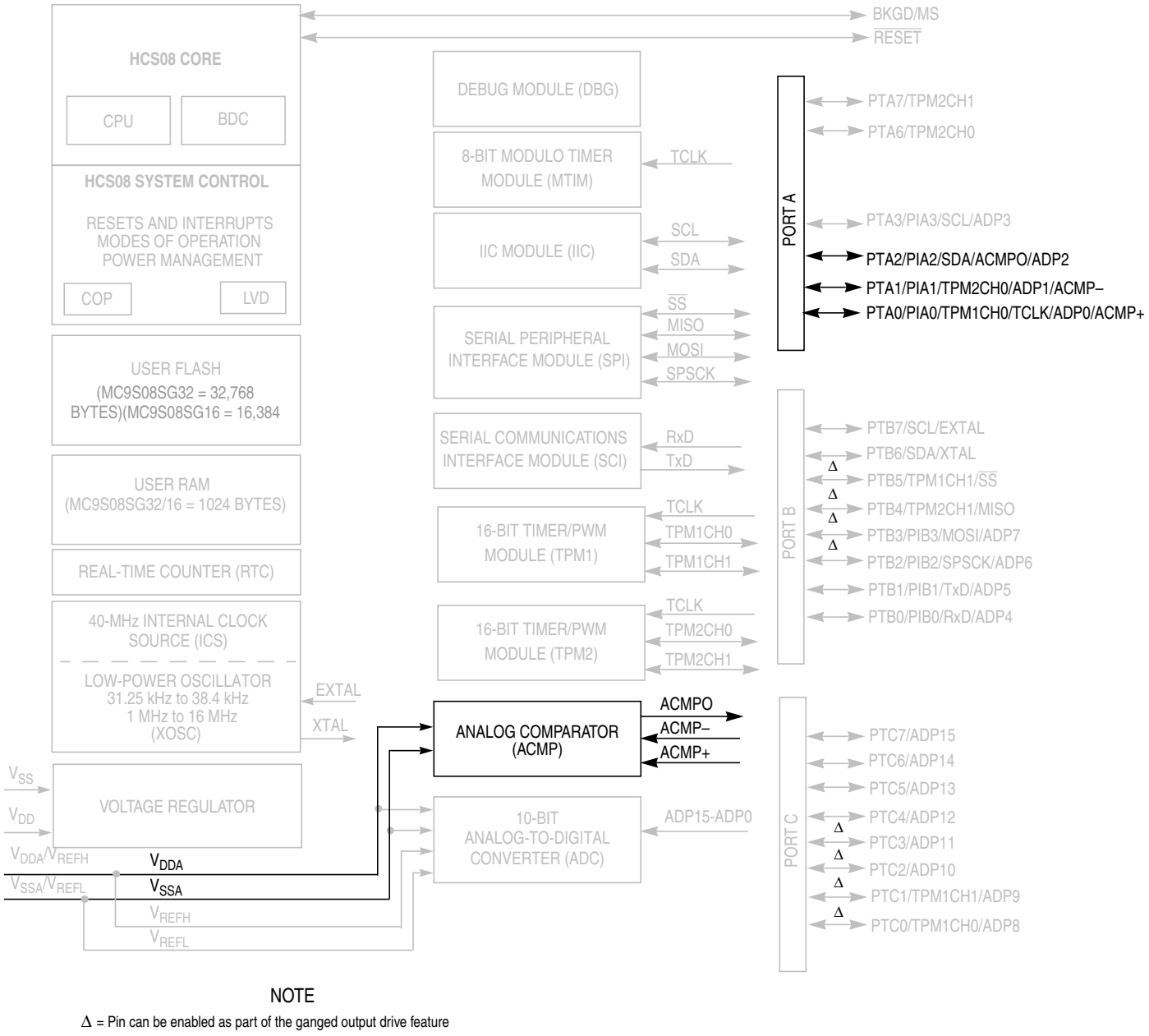



**Figure 8-1. MC9S08SG32 Series Block Diagram Highlighting ACMP Block and Pins**

## 8.2 Features

The ACMP has the following features:

- Full rail to rail supply operation.
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output.
- Option to compare to fixed internal bandgap reference voltage.
- Option to allow comparator output to be visible on a pin, ACMPO.
- Can operate in stop3 mode

## 8.3 Modes of Operation

This section defines the ACMP operation in wait, stop and background debug modes.

#### 8.3.0.1 ACMP in Wait Mode

The ACMP continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the ACMP can be used to bring the MCU out of wait mode if the ACMP interrupt, ACIE is enabled. For lowest possible current consumption, the ACMP should be disabled by software if not required as an interrupt source during wait mode.

#### 8.3.0.2 ACMP in Stop Modes

##### 8.3.0.2.1 Stop3 Mode Operation

The ACMP continues to operate in Stop3 mode if enabled and compare operation remains active. If ACOPE is enabled, comparator output operates as in the normal operating mode and comparator output is placed onto the external pin. The MCU is brought out of stop when a compare event occurs and ACIE is enabled; ACF flag sets accordingly.

If stop is exited with a reset, the ACMP will be put into its reset state.

##### 8.3.0.2.2 Stop2 Mode Operation

During Stop2 mode, the ACMP module will be fully powered down. Upon wake-up from Stop2 mode, the ACMP module will be in the reset state.

#### 8.3.0.3 ACMP in Active Background Mode

When the microcontroller is in active background mode, the ACMP will continue to operate normally.

## 8.4 Block Diagram

The block diagram for the Analog Comparator module is shown Figure 8-2.

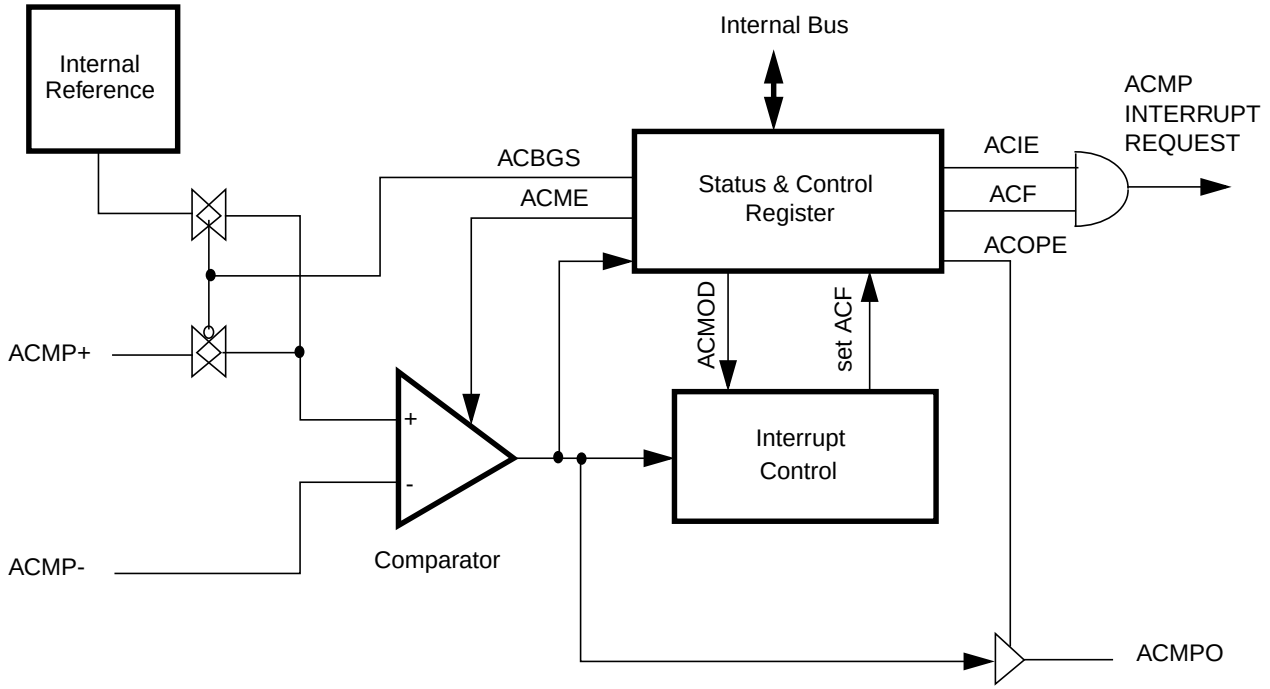



**Figure 8-2. Analog Comparator 5V (ACMP5) Block Diagram**

## 8.5 External Signal Description

The ACMP has two analog input pins, ACMP+ and ACMP- and one digital output pin ACMPO. Each of these pins can accept an input voltage that varies across the full operating voltage range of the MCU. As shown in Figure 8-2, the ACMP- pin is connected to the inverting input of the comparator, and the ACMP+ pin is connected to the comparator non-inverting input if ACBGS is a 0. As shown in Figure 8-2, the ACMPO pin can be enabled to drive an external pin.

The signal properties of ACMP are shown in Table 8-1.

**Table 8-1. Signal Properties**

| Signal | Function | I/O |
|---|---|---|
| ACMP- | Inverting analog input to the ACMP. (Minus input) | I |
| ACMP+ | Non-inverting analog input to the ACMP. (Positive input) | I |
| ACMPO | Digital output of the ACMP. | O |

## 8.6 Memory Map

### 8.6.1 Register Descriptions

The ACMP includes one register:

- An 8-bit status and control register

Refer to the direct-page register summary in the memory section of this data sheet for the absolute address assignments for all ACMP registers.This section refers to registers and control bits only by their names.

Some MCUs may have more than one ACMP, so register names include placeholder characters to identify which ACMP is being referenced.

### 8.6.1.1 ACMP Status and Control Register (ACMPSC)

ACMPSC contains the status flag and control bits which are used to enable and configure the ACMP.

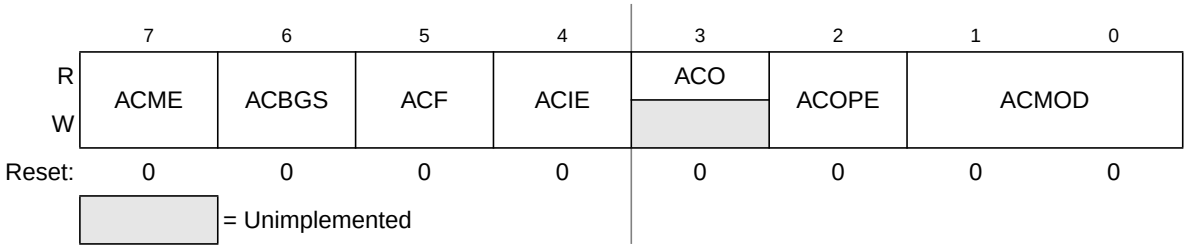



**Figure 8-3. ACMP Status and Control Register**

**Table 8-2. ACMP Status and Control Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ACME | **Analog Comparator Module Enable** — ACME enables the ACMP module.<br>0 ACMP not enabled<br>1 ACMP is enabled |
| 6<br>ACBGS | **Analog Comparator Bandgap Select** — ACBGS is used to select between the bandgap reference voltage or the ACMP+ pin as the input to the non-inverting input of the analog comparatorr.<br>0 External pin ACMP+ selected as non-inverting input to comparator<br>1 Internal reference select as non-inverting input to comparator<br>Note: refer to this chapter introduction to verify if any other config bits are necessary to enable the bandgap reference in the chip level. |
| 5<br>ACF | **Analog Comparator Flag** — ACF is set when a compare event occurs. Compare events are defined by ACMOD. ACF is cleared by writing a one to ACF.<br>0 Compare event has not occurred<br>1 Compare event has occurred |
| 4<br>ACIE | **Analog Comparator Interrupt Enable** — ACIE enables the interrupt from the ACMP. When ACIE is set, an interrupt will be asserted when ACF is set.<br>0 Interrupt disabled<br>1 Interrupt enabled |
| 3<br>ACO | **Analog Comparator Output** — Reading ACO will return the current value of the analog comparator output. ACO is reset to a 0 and will read as a 0 when the ACMP is disabled (ACME = 0). |
| 2<br>ACOPE | **Analog Comparator Output Pin Enable** — ACOPE is used to enable the comparator output to be placed onto the external pin, ACMPO.<br>0 Analog comparator output not available on ACMPO<br>1 Analog comparator output is driven out on ACMPO |
| 1:0<br>ACMOD | **Analog Comparator Mode** — ACMOD selects the type of compare event which sets ACF.<br>00 Encoding 0 — Comparator output falling edge<br>01 Encoding 1 — Comparator output rising edge<br>10 Encoding 2 — Comparator output falling edge<br>11 Encoding 3 — Comparator output rising or falling edge |

## 8.7 Functional Description

The analog comparator can be used to compare two analog input voltages applied to ACMP+ and ACMP-; or it can be used to compare an analog input voltage applied to ACMP- with an internal bandgap reference voltage. ACBGS is used to select between the bandgap reference voltage or the ACMP+ pin as the input to the non-inverting input of the analog comparator. The comparator output is high when the non-inverting input is greater than the inverting input, and is low when the non-inverting input is less than the inverting input. ACMOD is used to select the condition which will cause ACF to be set. ACF can be set on a rising edge of the comparator output, a falling edge of the comparator output, or either a rising or a falling edge (toggle). The comparator output can be read directly through ACO. The comparator output can be driven onto the ACMPO pin using ACOPE.

# Chapter 9
# Analog-to-Digital Converter (S08ADC10V1)

## 9.1 Introduction

The 10-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

**NOTE**

- MC9S08SG32 Series devices operate at a higher voltage range (2.7 V to 5.5 V) and do not include stop1 mode. Please ignore references to stop1.
- MC9S08SG32 Series devices have up to 16 analog inputs. Consequently, the APCTL3 register is not available on these devices.

The ADC channel assignments, alternate clock function, and hardware trigger function are configured as described below for the MC9S08SG32 Series family of devices.

### 9.1.1 Channel Assignments

The ADC channel assignments for the MC9S08SG32 Series devices are shown in Table 9-1. Reserved channels convert to an unknown value.This chapter shows bits for all S08ADCV1 channels. MC9S08SG32 Series MCUs do not use all of these channels. All bits corresponding to channels that are not available on a device are reserved.

**Table 9-1. ADC Channel Assignment**

| ADCH | Channel | Input |
|---|---|---|
| 00000 | AD0 | PTA0/AD0 |
| 00001 | AD1 | PTA1/ADP1 |
| 00010 | AD2 | PTA2/ADP2 |
| 00011 | AD3 | PTA3/ADP3 |
| 00100 | AD4 | PTB0/ADP4 |
| 00101 | AD5 | PTB1/ADP5 |
| 00110 | AD6 | PTB2/ADP6 |
| 00111 | AD7 | PTB3/ADP7 |
| 01000 | AD8 | PTC0/ADP8 |
| 01001 | AD9 | PTC1/ADP9 |
| 01010 | AD10 | PTC2/ADP10 |
| 01011 | AD11 | PTC3/ADP11 |
| 01100 | AD12 | PTC4/ADP12 |
| 01101 | AD13 | PTC5/ADP13 |
| 01110 | AD14 | PTC6/ADP14 |

| ADCH | Channel | Input |
|---|---|---|
| 10000 | AD16 | $V_{SS}$ |
| 10001 | AD17 | $V_{SS}$ |
| 10010 | AD18 | $V_{SS}$ |
| 10011 | AD19 | $V_{SS}$ |
| 10100 | AD20 | $V_{SS}$ |
| 10101 | AD21 | $V_{SS}$ |
| 10110 | AD22 | Reserved |
| 10111 | AD23 | Reserved |
| 11000 | AD24 | Reserved |
| 11001 | AD25 | Reserved |
| 11010 | AD26 | Temperature Sensor[1] |
| 11011 | AD27 | Internal Bandgap[2] |
| 11100 | - | Reserved |
| 11101 | $V_{REFH}$ | $V_{DD}$ |
| 11110 | $V_{REFL}$ | $V_{SS}$ |

**Table 9-1. ADC Channel Assignment (continued)**

| ADCH | Channel | Input |
|---|---|---|
| 01111 | AD15 | PTC7/ADP15 |

| ADCH | Channel | Input |
|---|---|---|
| 11111 | Module Disabled | None |

1 For information, see Section 9.1.5, “Temperature Sensor”.

2 Requires BGBE =1 in SPMSC1 see Section 5.7.6, “System Power Management Status and Control 1 Register (SPMSC1)”. For value of bandgap voltage reference see A.6, “DC Characteristics”.

## 9.1.2 Analog Power and Ground Signal Names

References to $V_{DDAD}$ and $V_{SSAD}$ in this chapter correspond to signals $V_{DDA}$ and $V_{SSA}$, respectively.

## 9.1.3 Alternate Clock

The ADC module is capable of performing conversions using the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock, ALTCLK. The alternate clock for the MC9S08SG32 Series MCU devices is the external reference clock (ICSERCLK).

The selected clock source must run at a frequency such that the ADC conversion clock (ADCK) runs at a frequency within its specified range ($f_{ADCK}$) after being divided down from the ALTCLK input as determined by the ADIV bits.

ALTCLK is active while the MCU is in wait mode provided the conditions described above are met. This allows ALTCLK to be used as the conversion clock source for the ADC while the MCU is in wait mode.

ALTCLK cannot be used as the ADC conversion clock source while the MCU is in either stop2 or stop3.

## 9.1.4 Hardware Trigger

The ADC hardware trigger, ADHWT, is the output from the real time counter (RTC). The RTC counter can be clocked by either ICSERCLK, ICSIRCLK or a nominal 1 kHz clock source.

The period of the RTC is determined by the input clock frequency, the RTCPS bits, and the RTCMOD register. When the ADC hardware trigger is enabled, a conversion is initiated upon an RTC counter overflow. The RTIE does not have to be set for RTC to cause a hardware trigger.

The RTC can be configured to cause a hardware trigger in MCU run, wait, and stop3.

## 9.1.5 Temperature Sensor

To use the on-chip temperature sensor, the user must perform the following:

- Configure ADC for long sample with a maximum of 1 MHz clock
- Convert the bandgap voltage reference channel (AD27)
  - — By converting the digital value of the bandgap voltage reference channel using the value of $V_{BG}$ the user can determine $V_{DD}$. For value of bandgap voltage, see Section A.6, “DC Characteristics”.
- Convert the temperature sensor channel (AD26)

— By using the calculated value of $V_{DD}$, convert the digital value of AD26 into a voltage, $V_{TEMP}$

Equation 9-1 provides an approximate transfer function of the temperature sensor.

$$Temp = 25 - ((V_{TEMP} - V_{TEMP25}) \div m) \qquad \textit{Eqn. 9-1}$$

where:

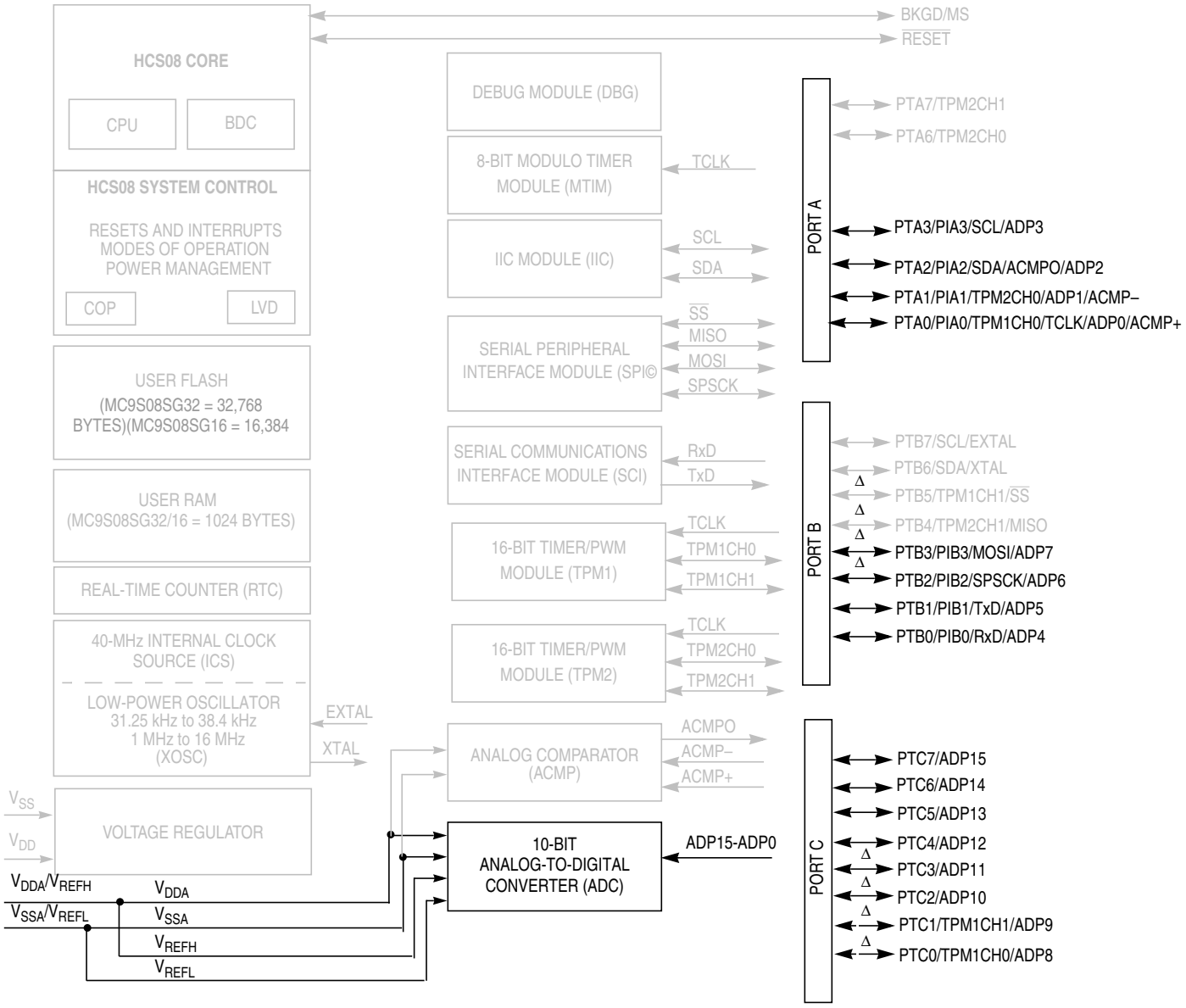
— $V_{TEMP}$ is the voltage of the temperature sensor channel at the ambient temperature.
— $V_{TEMP25}$ is the voltage of the temperature sensor channel at 25°C.
— m is the hot or cold voltage versus temperature slope in V/°C.

For temperature calculations, use the $V_{TEMP25}$ and m values from the ADC Electricals table.

In application code, the user reads the temperature sensor channel, calculates $V_{TEMP}$, and compares to $V_{TEMP25}$. If $V_{TEMP}$ is greater than $V_{TEMP25}$ the cold slope value is applied in Equation 9-1. If $V_{TEMP}$ is less than $V_{TEMP25}$ the hot slope value is applied in Equation 9-1. To improve accuracy the user should calibrate the bandgap voltage reference and temperature sensor.

Calibrating at 25°C will improve accuracy to ± 4.5°C.

Calibration at three points, -40°C, 25°C, and 125°C will improve accuracy to ± 2.5°C. Once calibration has been completed, the user will need to calculate the slope for both hot and cold. In application code, the user would then calculate the temperature using Equation 9-1 as detailed above and then determine if the temperature is above or below 25°C. Once determined if the temperature is above or below 25°C, the user can recalculate the temperature using the hot or cold slope value obtained during calibration.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin packages.
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin packages.
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature.

**Figure 9-1. MC9S08SG32 Series Block Diagram Highlighting ADC Block and Pins**

### 9.1.6 Features

Features of the ADC module include:

- Linear successive approximation algorithm with 10-bit resolution
- Up to 28 analog inputs[1]
- Output formatted in 10- or 8-bit right-justified unsigned format
- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in wait or stop3 modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value

### 9.1.7 ADC Module Block Diagram

Figure 9-2 provides a block diagram of the ADC module

1. Number of analog inputs varies according to the device and may be from external or internal sources. Refer to the introduction section to this chapter for AD0–AD27 channel input assignments.

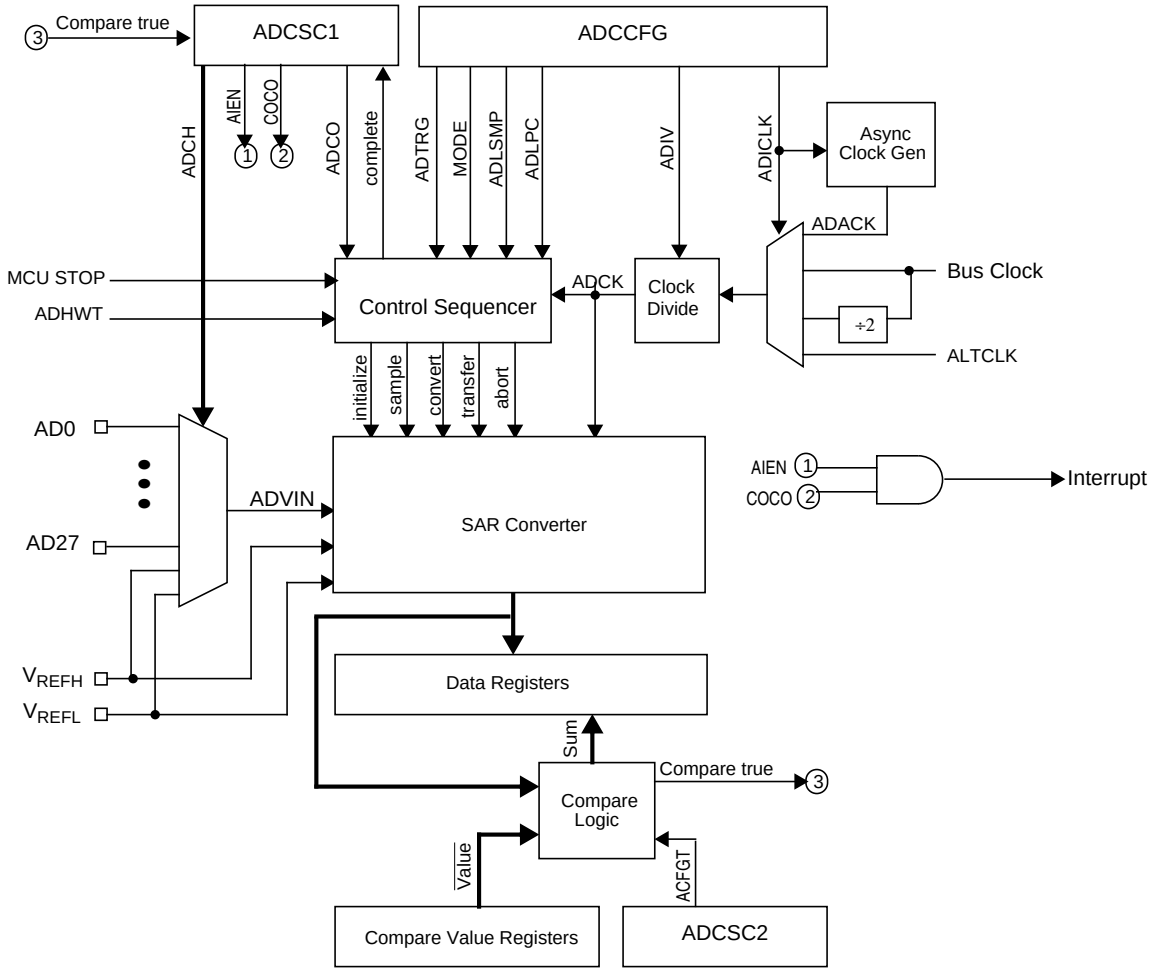



**Figure 9-2. ADC Block Diagram**

## 9.2 External Signal Description

The ADC module supports up to 28 separate analog inputs. It also requires four supply/reference/ground connections.

**Table 9-2. Signal Properties**

| Name | Function |
|---|---|
| AD27–AD0 | Analog Channel inputs |
| $V_{REFH}$ | High reference voltage |
| $V_{REFL}$ | Low reference voltage |
| $V_{DDA}$ | Analog power supply |
| $V_{SSA}$ | Analog ground |

### 9.2.1 Analog Power ($V_{DDA}$)

The ADC analog portion uses $V_{DDA}$ as its power connection. In some packages, $V_{DDA}$ is connected internally to $V_{DD}$. If externally available, connect the $V_{DDA}$ pin to the same voltage potential as $V_{DD}$. External filtering may be necessary to ensure clean $V_{DDA}$ for good results.

### 9.2.2 Analog Ground ($V_{SSA}$)

The ADC analog portion uses $V_{SSA}$ as its ground connection. In some packages, $V_{SSA}$ is connected internally to $V_{SS}$. If externally available, connect the $V_{SSA}$ pin to the same voltage potential as $V_{SS}$.

### 9.2.3 Voltage Reference High ($V_{REFH}$)

$V_{REFH}$ is the high reference voltage for the converter. In some packages, $V_{REFH}$ is connected internally to $V_{DDA}$. If externally available, $V_{REFH}$ may be connected to the same potential as $V_{DDA}$ or may be driven by an external source between the minimum $V_{DDA}$ spec and the $V_{DDA}$ potential ($V_{REFH}$ must never exceed $V_{DDA}$).

### 9.2.4 Voltage Reference Low ($V_{REFL}$)

$V_{REFL}$ is the low-reference voltage for the converter. In some packages, $V_{REFL}$ is connected internally to $V_{SSA}$. If externally available, connect the $V_{REFL}$ pin to the same voltage potential as $V_{SSA}$.

### 9.2.5 Analog Channel Inputs (ADx)

The ADC module supports up to 28 separate analog inputs. An input is selected for conversion through the ADCH channel select bits.

## 9.3 Register Definition

These memory-mapped registers control and monitor operation of the ADC:

- Status and control register, ADCSC1
- Status and control register, ADCSC2
- Data result registers, ADCRH and ADCRL
- Compare value registers, ADCCVH and ADCCVL
- Configuration register, ADCCFG
- Pin control registers, APCTLx[1]

1. Number of APCTLx registers depends on the number of external analog inputs available on the device. Please refer to the introduction of this module for external analog input assignments.

## 9.3.1 Status and Control Register 1 (ADCSC1)

This section describes the function of the ADC status and control register (ADCSC1). Writing ADCSC1 aborts the current conversion and initiates a new conversion (if the ADCH bits are equal to a value other than all 1s).

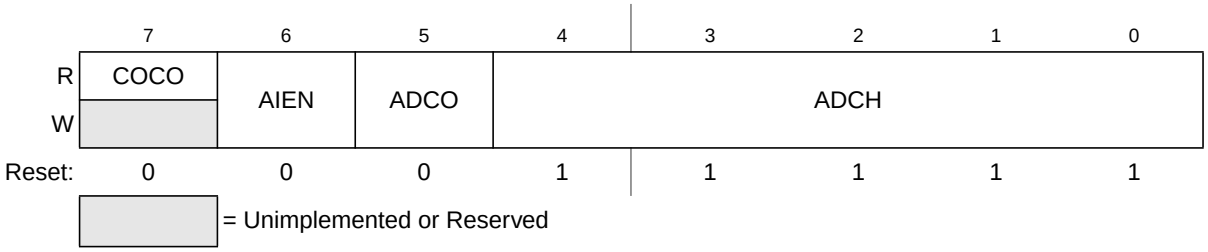



**Figure 9-3. Status and Control Register (ADCSC1)**

**Table 9-3. ADCSC1 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>COCO | **Conversion Complete Flag** — The COCO flag is a read-only bit set each time a conversion is completed when the compare function is disabled (ACFE = 0). When the compare function is enabled (ACFE = 1), the COCO flag is set upon completion of a conversion only if the compare result is true. This bit is cleared when ADCSC1 is written or whenever ADCRL is read.<br>0 Conversion not completed<br>1 Conversion completed |
| 6<br>AIEN | **Interrupt Enable** — AIEN enables conversion complete interrupts. When COCO becomes set while AIEN is high, an interrupt is asserted.<br>0 Conversion complete interrupt disabled<br>1 Conversion complete interrupt enabled |
| 5<br>ADCO | **Continuous Conversion Enable** — ADCO enables continuous conversions.<br>0 One conversion following a write to the ADCSC1 when software triggered operation is selected, or one conversion following assertion of ADHWT when hardware triggered operation is selected.<br>1 Continuous conversions initiated following a write to ADCSC1 when software triggered operation is selected. Continuous conversions are initiated by an ADHWT event when hardware triggered operation is selected. |
| 4:0<br>ADCH | **Input Channel Select** — The ADCH bits form a 5-bit field which that selects one of the input channels. The input channels are detailed in Table 9-4.<br>The successive approximation converter subsystem is turned off when the channel select bits are all set. This feature allows for explicit disabling of the ADC and isolation of the input channel from all sources. Terminating continuous conversions this way prevents an additional, single conversion from being performed. It is not necessary to set the channel select bits to all ones to place the ADC in a low-power state when continuous conversions are not enabled because the module automatically enters a low-power state when a conversion completes. |

**Table 9-4. Input Channel Select**

| ADCH | Input Select |
|---|---|
| 00000 | AD0 |
| 00001 | AD1 |
| 00010 | AD2 |
| 00011 | AD3 |

| ADCH | Input Select |
|---|---|
| 10000 | AD16 |
| 10001 | AD17 |
| 10010 | AD18 |
| 10011 | AD19 |

**Table 9-4. Input Channel Select (continued)**

| ADCH | Input Select |
|---|---|
| 00100 | AD4 |
| 00101 | AD5 |
| 00110 | AD6 |
| 00111 | AD7 |
| 01000 | AD8 |
| 01001 | AD9 |
| 01010 | AD10 |
| 01011 | AD11 |
| 01100 | AD12 |
| 01101 | AD13 |
| 01110 | AD14 |
| 01111 | AD15 |

| ADCH | Input Select |
|---|---|
| 10100 | AD20 |
| 10101 | AD21 |
| 10110 | AD22 |
| 10111 | AD23 |
| 11000 | AD24 |
| 11001 | AD25 |
| 11010 | AD26 |
| 11011 | AD27 |
| 11100 | Reserved |
| 11101 | $V_{REFH}$ |
| 11110 | $V_{REFL}$ |
| 11111 | Module disabled |

## 9.3.2 Status and Control Register 2 (ADCSC2)

The ADCSC2 register controls the compare function, conversion trigger, and conversion active of the ADC module.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | ADACT | ADTRG | ACFE | ACFGT | 0 | 0 | R[1] | R[1] |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

[1] Bits 1 and 0 are reserved bits that must always be written to 0.

**Figure 9-4. Status and Control Register 2 (ADCSC2)**

**Table 9-5. ADCSC2 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ADACT | **Conversion Active** — Indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted.<br>0 Conversion not in progress<br>1 Conversion in progress |
| 6<br>ADTRG | **Conversion Trigger Select** — Selects the type of trigger used for initiating a conversion. Two types of triggers are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADCSC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input.<br>0 Software trigger selected<br>1 Hardware trigger selected |

**Table 9-5. ADCSC2 Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 5<br>ACFE | **Compare Function Enable** — Enables the compare function.<br>0 Compare function disabled<br>1 Compare function enabled |
| 4<br>ACFGT | **Compare Function Greater Than Enable** — Configures the compare function to trigger when the result of the conversion of the input being monitored is greater than or equal to the compare level. The compare function defaults to triggering when the result of the compare of the input being monitored is less than the compare level.<br>0 Compare triggers when input is less than compare level<br>1 Compare triggers when input is greater than or equal to compare level |

## 9.3.3 Data Result High Register (ADCRH)

In 10-bit operation, ADCRH contains the upper two bits of 10-bit conversion data. In 10-bit mode, ADCRH is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. When configured for 8-bit mode, ADR[9:8] are cleared.

When automatic compare is not enabled, the value stored in ADCRH are the upper bits of the conversion result. When automatic compare is enabled, the conversion result is manipulated as described in Section 9.4.5, “Automatic Compare Function” prior to storage in ADCRH:ADCRL registers.

In 10-bit mode, reading ADCRH prevents the ADC from transferring subsequent conversion data into the result registers until ADCRL is read. If ADCRL is not read until after the next conversion is completed, the intermediate conversion data is lost. In 8-bit mode, there is no interlocking with ADCRL. If the MODE bits are changed, any data in ADCRH becomes invalid.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | ADR9 | ADR8 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 9-5. Data Result High Register (ADCRH)**

## 9.3.4 Data Result Low Register (ADCRL)

ADCRL contains the lower eight bits of a 10-bit conversion data, and all eight bits of 8-bit conversion data. ADCRL is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met.

When automatic compare is not enabled, the value stored in ADCRL is the lower eight bits of the conversion result. When automatic compare is enabled, the conversion result is manipulated as described in Section 9.4.5, “Automatic Compare Function” prior to storage in ADCRH:ADCRL registers.

In 10-bit mode, reading ADCRH prevents the ADC from transferring subsequent conversion data into the result registers until ADCRL is read. If ADCRL is not read until the after next conversion is completed,

the intermediate conversion data is lost. In 8-bit mode, there is no interlocking with ADCRH. If the MODE bits are changed, any data in ADCRL becomes invalid.

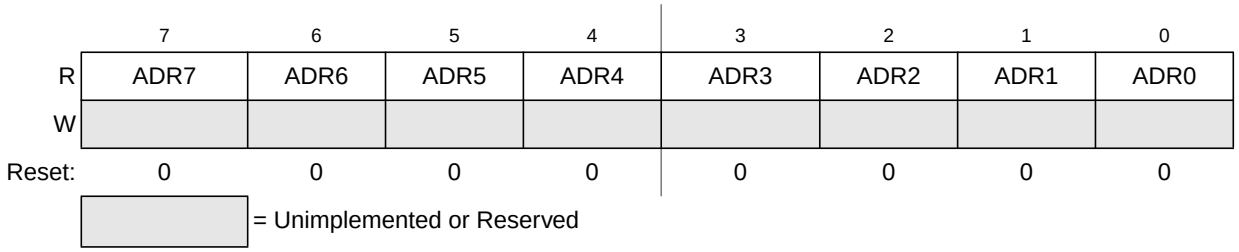



**Figure 9-6. Data Result Low Register (ADCRL)**

## 9.3.5 Compare Value High Register (ADCCVH)

In 10-bit mode, the ADCCVH register holds the upper two bits of the 10-bit compare value (ADCV[9:8]). When the compare function is enabled, these bits are compared to the upper two bits of the result following a conversion in 10-bit mode.

In 8-bit operation, ADCCVH is not used during compare.

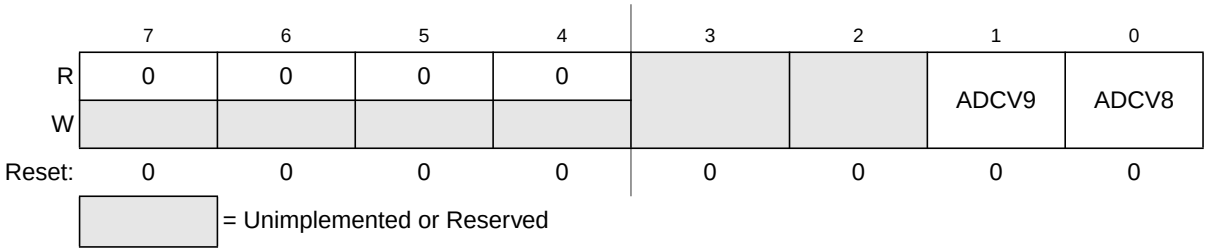



**Figure 9-7. Compare Value High Register (ADCCVH)**

## 9.3.6 Compare Value Low Register (ADCCVL)

The ADCCVL register holds the lower eight bits of the 10-bit compare value or all eight bits of the 8-bit compare value. When the compare function is enabled, bits ADCV[7:0] are compared to the lower eight bits of the result following a conversion in 10-bit or 8-bit mode.

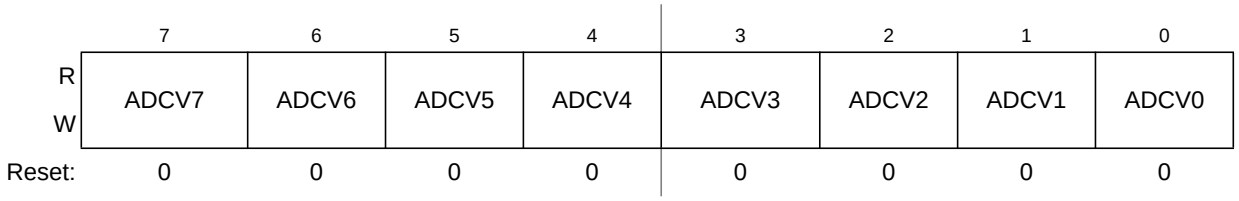



**Figure 9-8. Compare Value Low Register (ADCCVL)**

## 9.3.7 Configuration Register (ADCCFG)

ADCCFG selects the mode of operation, clock source, clock divide, and configures for low power and long sample time.

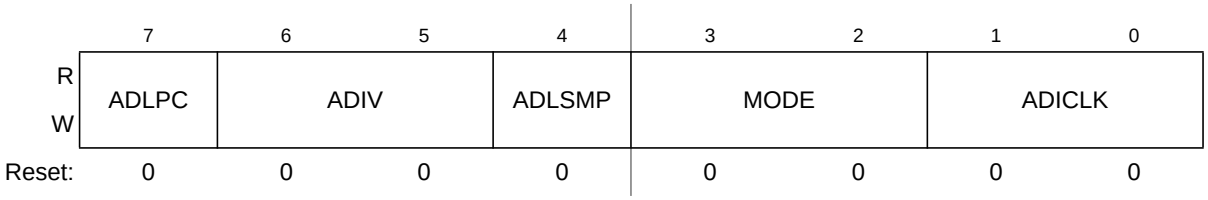



**Figure 9-9. Configuration Register (ADCCFG)**

**Table 9-6. ADCCFG Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ADLPC | **Low-Power Configuration** — ADLPC controls the speed and power configuration of the successive approximation converter. This optimizes power consumption when higher sample rates are not required.<br>0 High speed configuration<br>1 Low power configuration: {FC31}The power is reduced at the expense of maximum clock speed. |
| 6:5<br>ADIV | **Clock Divide Select** — ADIV selects the divide ratio used by the ADC to generate the internal clock ADCK. Table 9-7 shows the available clock configurations. |
| 4<br>ADLSMP | **Long Sample Time Configuration** — ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required.<br>0 Short sample time<br>1 Long sample time |
| 3:2<br>MODE | **Conversion Mode Selection** — MODE bits select between 10- or 8-bit operation. See Table 9-8. |
| 1:0<br>ADICLK | **Input Clock Select** — ADICLK bits select the input clock source to generate the internal clock ADCK. See Table 9-9. |

**Table 9-7. Clock Divide Select**

| ADIV | Divide Ratio | Clock Rate |
|---|---|---|
| 00 | 1 | Input clock |
| 01 | 2 | Input clock ÷ 2 |
| 10 | 4 | Input clock ÷ 4 |
| 11 | 8 | Input clock ÷ 8 |

**Table 9-8. Conversion Modes**

| MODE | Mode Description |
|---|---|
| 00 | 8-bit conversion (N=8) |
| 01 | Reserved |
| 10 | 10-bit conversion (N=10) |
| 11 | Reserved |

**Table 9-9. Input Clock Select**

| ADICLK | Selected Clock Source |
|---|---|
| 00 | Bus clock |
| 01 | Bus clock divided by 2 |
| 10 | Alternate clock (ALTCLK) |
| 11 | Asynchronous clock (ADACK) |

## 9.3.8 Pin Control 1 Register (APCTL1)

The pin control registers disable the digital interface to the associated MCU pins used as analog inputs to reduce digital noise and improve conversion accuracy. APCTL1 controls the pins associated with channels 0–7 of the ADC module.

Some MCUs may not use all bits implemented in this register. Bits in this register that do not have associated external analog inputs have no control function. Consult the ADC channel assignment in the module introduction.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | ADPC7 | ADPC6 | ADPC5 | ADPC4 | ADPC3 | ADPC2 | ADPC1 | ADPC0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-10. Pin Control 1 Register (APCTL1)**

**Table 9-10. APCTL1 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ADPC7 | **ADC Pin Control 7** — ADPC7 controls the pin associated with channel AD7.<br>0 AD7 pin I/O control enabled<br>1 AD7 pin I/O control disabled |
| 6<br>ADPC6 | **ADC Pin Control 6** — ADPC6 controls the pin associated with channel AD6.<br>0 AD6 pin I/O control enabled<br>1 AD6 pin I/O control disabled |
| 5<br>ADPC5 | **ADC Pin Control 5** — ADPC5 controls the pin associated with channel AD5.<br>0 AD5 pin I/O control enabled<br>1 AD5 pin I/O control disabled |
| 4<br>ADPC4 | **ADC Pin Control 4** — ADPC4 controls the pin associated with channel AD4.<br>0 AD4 pin I/O control enabled<br>1 AD4 pin I/O control disabled |
| 3<br>ADPC3 | **ADC Pin Control 3** — ADPC3 controls the pin associated with channel AD3.<br>0 AD3 pin I/O control enabled<br>1 AD3 pin I/O control disabled |
| 2<br>ADPC2 | **ADC Pin Control 2** — ADPC2 controls the pin associated with channel AD2.<br>0 AD2 pin I/O control enabled<br>1 AD2 pin I/O control disabled |

**Table 9-10. APCTL1 Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>ADPC1 | **ADC Pin Control 1** — ADPC1 controls the pin associated with channel AD1.<br>0 AD1 pin I/O control enabled<br>1 AD1 pin I/O control disabled |
| 0<br>ADPC0 | **ADC Pin Control 0** — ADPC0 controls the pin associated with channel AD0.<br>0 AD0 pin I/O control enabled<br>1 AD0 pin I/O control disabled |

## 9.3.9 Pin Control 2 Register (APCTL2)

The pin control registers disable the digital interface to the associated MCU pins used as analog inputs to reduce digital noise and improve conversion accuracy. APCTL2 controls channels 8–15 of the ADC module. This register is not implemented on MCUs that do not have associated external analog inputs. Consult the ADC channel assignment in the module introduction for information on availability of this register.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | ADPC15 | ADPC14 | ADPC13 | ADPC12 | ADPC11 | ADPC10 | ADPC9 | ADPC8 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-11. Pin Control 2 Register (APCTL2)**

**Table 9-11. APCTL2 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ADPC15 | **ADC Pin Control 15** — ADPC15 controls the pin associated with channel AD15.<br>0 AD15 pin I/O control enabled<br>1 AD15 pin I/O control disabled |
| 6<br>ADPC14 | **ADC Pin Control 14** — ADPC14 controls the pin associated with channel AD14.<br>0 AD14 pin I/O control enabled<br>1 AD14 pin I/O control disabled |
| 5<br>ADPC13 | **ADC Pin Control 13** — ADPC13 controls the pin associated with channel AD13.<br>0 AD13 pin I/O control enabled<br>1 AD13 pin I/O control disabled |
| 4<br>ADPC12 | **ADC Pin Control 12** — ADPC12 controls the pin associated with channel AD12.<br>0 AD12 pin I/O control enabled<br>1 AD12 pin I/O control disabled |
| 3<br>ADPC11 | **ADC Pin Control 11** — ADPC11 controls the pin associated with channel AD11.<br>0 AD11 pin I/O control enabled<br>1 AD11 pin I/O control disabled |
| 2<br>ADPC10 | **ADC Pin Control 10** — ADPC10 controls the pin associated with channel AD10.<br>0 AD10 pin I/O control enabled<br>1 AD10 pin I/O control disabled |

**Table 9-11. APCTL2 Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>ADPC9 | **ADC Pin Control 9** — ADPC9 controls the pin associated with channel AD9.<br>0 AD9 pin I/O control enabled<br>1 AD9 pin I/O control disabled |
| 0<br>ADPC8 | **ADC Pin Control 8** — ADPC8 controls the pin associated with channel AD8.<br>0 AD8 pin I/O control enabled<br>1 AD8 pin I/O control disabled |

## 9.3.10 Pin Control 3 Register (APCTL3)

The pin control registers disable the digital interface to the associated MCU pins used as analog inputs to reduce digital noise and improve conversion accuracy. APCTL3 controls channels 16–23 of the ADC module. This register is not implemented on MCUs that do not have associated external analog inputs. Consult the ADC channel assignment in the module introduction for information on availability of this register.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | ADPC23 | ADPC22 | ADPC21 | ADPC20 | ADPC19 | ADPC18 | ADPC17 | ADPC16 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-12. Pin Control 3 Register (APCTL3)**

**Table 9-12. APCTL3 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ADPC23 | **ADC Pin Control 23** — ADPC23 controls the pin associated with channel AD23.<br>0 AD23 pin I/O control enabled<br>1 AD23 pin I/O control disabled |
| 6<br>ADPC22 | **ADC Pin Control 22** — ADPC22 controls the pin associated with channel AD22.<br>0 AD22 pin I/O control enabled<br>1 AD22 pin I/O control disabled |
| 5<br>ADPC21 | **ADC Pin Control 21** — ADPC21 controls the pin associated with channel AD21.<br>0 AD21 pin I/O control enabled<br>1 AD21 pin I/O control disabled |
| 4<br>ADPC20 | **ADC Pin Control 20** — ADPC20 controls the pin associated with channel AD20.<br>0 AD20 pin I/O control enabled<br>1 AD20 pin I/O control disabled |
| 3<br>ADPC19 | **ADC Pin Control 19** — ADPC19 controls the pin associated with channel AD19.<br>0 AD19 pin I/O control enabled<br>1 AD19 pin I/O control disabled |
| 2<br>ADPC18 | **ADC Pin Control 18** — ADPC18 controls the pin associated with channel AD18.<br>0 AD18 pin I/O control enabled<br>1 AD18 pin I/O control disabled |

**Table 9-12. APCTL3 Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>ADPC17 | **ADC Pin Control 17** — ADPC17 controls the pin associated with channel AD17.<br>0 AD17 pin I/O control enabled<br>1 AD17 pin I/O control disabled |
| 0<br>ADPC16 | **ADC Pin Control 16** — ADPC16 controls the pin associated with channel AD16.<br>0 AD16 pin I/O control enabled<br>1 AD16 pin I/O control disabled |

## 9.4 Functional Description

The ADC module is disabled during reset or when the ADCH bits are all high. The module is idle when a conversion has completed and another conversion has not been initiated. When idle, the module is in its lowest power state.

The ADC can perform an analog-to-digital conversion on any of the software selectable channels. The selected channel voltage is converted by a successive approximation algorithm into an 11-bit digital result. In 8-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 9-bit digital result.

When the conversion is completed, the result is placed in the data registers (ADCRH and ADCRL).In 10-bit mode, the result is rounded to 10 bits and placed in ADCRH and ADCRL. In 8-bit mode, the result is rounded to 8 bits and placed in ADCRL. The conversion complete flag (COCO) is then set and an interrupt is generated if the conversion complete interrupt has been enabled (AIEN = 1).

The ADC module has the capability of automatically comparing the result of a conversion with the contents of its compare registers. The compare function is enabled by setting the ACFE bit and operates with any of the conversion modes and configurations.

### 9.4.1 Clock Select and Divide Control

One of four clock sources can be selected as the clock source for the ADC module. This clock source is then divided by a configurable value to generate the input clock to the converter (ADCK). The clock is selected from one of the following sources by means of the ADICLK bits.

- The bus clock, which is equal to the frequency at which software is executed. This is the default selection following reset.
- The bus clock divided by two. For higher bus clock rates, this allows a maximum divide by 16 of the bus clock.
- ALTCLK, as defined for this MCU (See module section introduction).
- The asynchronous clock (ADACK). This clock is generated from a clock source within the ADC module. When selected as the clock source, this clock remains active while the MCU is in wait or stop3 mode and allows conversions in these modes for lower noise operation.

Whichever clock is selected, its frequency must fall within the specified frequency range for ADCK. If the available clocks are too slow, the ADC does not perform according to specifications. If the available clocks

are too fast, the clock must be divided to the appropriate frequency. This divider is specified by the ADIV bits and can be divide-by 1, 2, 4, or 8.

### 9.4.2 Input Select and Pin Control

The pin control registers (APCTLx) disable the digital interface to the I/O of the pins used as analog inputs. When a pin control register bit is set, the following conditions are forced for the associated MCU pin:

- The output buffer is forced to its high impedance state.
- The input buffer is disabled. A read of the I/O port returns a zero for any pin with its input buffer disabled.
- The pullup is disabled.

### 9.4.3 Hardware Trigger

The ADC module has a selectable asynchronous hardware conversion trigger, ADHWT, that is enabled when the ADTRG bit is set. This source is not available on all MCUs. Consult the module introduction for information on the ADHWT source specific to this MCU.

When ADHWT source is available and hardware trigger is enabled (ADTRG=1), a conversion is initiated on the rising edge of ADHWT. If a conversion is in progress when a rising edge occurs, the rising edge is ignored. In continuous convert configuration, only the initial rising edge to launch continuous conversions is observed. The hardware trigger function operates in conjunction with any of the conversion modes and configurations.

### 9.4.4 Conversion Control

Conversions can be performed in either 10-bit mode or 8-bit mode as determined by the MODE bits. Conversions can be initiated by either a software or hardware trigger. In addition, the ADC module can be configured for low power operation, long sample time, continuous conversion, and automatic compare of the conversion result to a software determined compare value.

#### 9.4.4.1 Initiating Conversions

A conversion is initiated:

- Following a write to ADCSC1 (with ADCH bits not all 1s) if software triggered operation is selected.
- Following a hardware trigger (ADHWT) event if hardware triggered operation is selected.
- Following the transfer of the result to the data registers when continuous conversion is enabled.

If continuous conversions are enabled, a new conversion is automatically initiated after the completion of the current conversion. In software triggered operation, continuous conversions begin after ADCSC1 is written and continue until aborted. In hardware triggered operation, continuous conversions begin after a hardware trigger event and continue until aborted.

#### 9.4.4.2 Completing Conversions

A conversion is completed when the result of the conversion is transferred into the data result registers, ADCRH and ADCRL. This is indicated by the setting of COCO. An interrupt is generated if AIEN is high at the time that COCO is set.

A blocking mechanism prevents a new result from overwriting previous data in ADCRH and ADCRL if the previous data is in the process of being read while in 10-bit MODE (the ADCRH register has been read but the ADCRL register has not). When blocking is active, the data transfer is blocked, COCO is not set, and the new result is lost. In the case of single conversions with the compare function enabled and the compare condition false, blocking has no effect and ADC operation is terminated. In all other cases of operation, when a data transfer is blocked, another conversion is initiated regardless of the state of ADCO (single or continuous conversions enabled).

If single conversions are enabled, the blocking mechanism could result in several discarded conversions and excess power consumption. To avoid this issue, the data registers must not be read after initiating a single conversion until the conversion completes.

#### 9.4.4.3 Aborting Conversions

Any conversion in progress is aborted when:

- A write to ADCSC1 occurs (the current conversion will be aborted and a new conversion will be initiated, if ADCH are not all 1s).
- A write to ADCSC2, ADCCFG, ADCCVH, or ADCCVL occurs. This indicates a mode of operation change has occurred and the current conversion is therefore invalid.
- The MCU is reset.
- The MCU enters stop mode with ADACK not enabled.

When a conversion is aborted, the contents of the data registers, ADCRH and ADCRL, are not altered. However, they continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset, ADCRH and ADCRL return to their reset states.

#### 9.4.4.4 Power Control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, the ADACK clock generator is also enabled.

Power consumption when active can be reduced by setting ADLPC. This results in a lower maximum value for $f_{ADCK}$ (see the electrical specifications).

#### 9.4.4.5 Sample Time and Total Conversion Time

The total conversion time depends on the sample time (as determined by ADLSMP), the MCU bus frequency, the conversion mode (8-bit or 10-bit), and the frequency of the conversion clock ($f_{ADCK}$). After the module becomes active, sampling of the input begins. ADLSMP selects between short and long sample times.When sampling is complete, the converter is isolated from the input channel and a successive

approximation algorithm is performed to determine the digital value of the analog signal. The result of the conversion is transferred to ADCRH and ADCRL upon completion of the conversion algorithm.

If the bus frequency is less than the $f_{ADCK}$ frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADLSMP=0). If the bus frequency is less than 1/11th of the $f_{ADCK}$ frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADLSMP=1).

The maximum total conversion time for different conditions is summarized in Table 9-13.

**Table 9-13. Total Conversion Time vs. Control Conditions**

| Conversion Type | ADICLK | ADLSMP | Max Total Conversion Time |
|---|---|---|---|
| Single or first continuous 8-bit | 0x, 10 | 0 | 20 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 10-bit | 0x, 10 | 0 | 23 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 8-bit | 0x, 10 | 1 | 40 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 10-bit | 0x, 10 | 1 | 43 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 8-bit | 11 | 0 | 5 µs + 20 ADCK + 5 bus clock cycles |
| Single or first continuous 10-bit | 11 | 0 | 5 µs + 23 ADCK + 5 bus clock cycles |
| Single or first continuous 8-bit | 11 | 1 | 5 µs + 40 ADCK + 5 bus clock cycles |
| Single or first continuous 10-bit | 11 | 1 | 5 µs + 43 ADCK + 5 bus clock cycles |
| Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}$ | xx | 0 | 17 ADCK cycles |
| Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}$ | xx | 0 | 20 ADCK cycles |
| Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}/11$ | xx | 1 | 37 ADCK cycles |
| Subsequent continuous 10-bit; $f_{BUS} \geq f_{ADCK}/11$ | xx | 1 | 40 ADCK cycles |

The maximum total conversion time is determined by the clock source chosen and the divide ratio selected. The clock source is selectable by the ADICLK bits, and the divide ratio is specified by the ADIV bits. For example, in 10-bit mode, with the bus clock selected as the input clock source, the input clock divide-by-1 ratio selected, and a bus frequency of 8 MHz, then the conversion time for a single conversion is:

$$\text{Conversion time} = \frac{23 \text{ ADCK cyc}}{8 \text{ MHz}/1} + \frac{5 \text{ bus cyc}}{8 \text{ MHz}} = 3.5 \text{ µs}$$

$$\text{Number of bus cycles} = 3.5 \text{ µs} \times 8 \text{ MHz} = 28 \text{ cycles}$$

**NOTE**

The ADCK frequency must be between $f_{ADCK}$ minimum and $f_{ADCK}$ maximum to meet ADC specifications.

### 9.4.5 Automatic Compare Function

The compare function is enabled by the ACFE bit. The compare function can be configured to check for an upper or lower limit. After the input is sampled and converted, the compare value (ADCCVH and ADCCVL) is subtracted from the conversion result. When comparing to an upper limit (ACFGT = 1), if the conversion result is greater-than or equal-to the compare value, COCO is set. When comparing to a lower limit (ACFGT = 0), if the result is less than the compare value, COCO is set. An ADC interrupt is generated upon the setting of COCO if the ADC interrupt is enabled (AIEN = 1).

The subtract operation of two positive values (the conversion result less the compare value) results in a signed value that is 1-bit wider than the bit-width of the two terms. The final value transferred to the ADCRH and ADCRL registers is the result of the subtraction operation, excluding the sign bit. The value of the sign bit can be derived based on ACFGT control setting. When ACFGT=1, the sign bit of any value stored in ADCRH and ADCRL is always 0, indicating a positive result for the subtract operation. When ACFGT = 1, the sign bit of any result is always 1, indicating a negative result for the subtract operation.

Upon completion of a conversion while the compare function is enabled, if the compare condition is not true, COCO is not set and no data is transferred to the result registers.

**NOTE**

The compare function can monitor the voltage on a channel while the MCU is in wait or stop3 mode. The ADC interrupt wakes the MCU when the compare condition is met.

An example of compare operation eases understanding of the compare feature. If the ADC is configured for 10-bit operation, ACFGT=0, and ADCCVH:ADCCVL= 0x200, then a conversion result of 0x080 causes the compare condition to be met and the COCO bit is set. A value of 0x280 is stored in ADCRH:ADCRL. This is signed data without the sign bit and must be combined with a derived sign bit to have meaning. The value stored in ADCRH:ADCRL is calculated as follows.

The value to interpret from the data is (Result – Compare Value) = (0x080 – 0x200) = –0x180. A standard method for handling subtraction is to convert the second term to its 2’s complement, and then add the two terms. First calculate the 2’s complement of 0x200 by complementing each bit and adding 1. Note that prior to complementing, a sign bit of 0 is added so that the 10-bit compare value becomes a 11-bit signed value that is always positive.

```
  %101 1111 1111        <= 1’s complement of 0x200 compare value
+           %1
  ---------------
  %110 0000 0000        <= 2’s complement of 0x200 compare value
```

Then the conversion result of 0x080 is added to 2’s complement of 0x200:

```
   %000 1000 0000
+  %110 0000 0000
   ---------------
    %110 1000 0000      <= Subtraction result is –0x180 in signed 11-bit data
```

The subtraction result is an 11-bit signed value. The lower 10 bits (0x280) are stored in ADCRH:ADCRL. The sign bit is known to be 1 (negative) because the ACFGT=0, the COCO bit was set, and conversion data was updated in ADCRH:ADCRL.

A simpler way to use the data stored in ADCRH:ADCRL is to apply the following rules. When comparing for upper limit (ACFGT=1), the value in ADCRH:ADCRL is a positive value and does not need to be manipulated. This value is the difference between the conversion result and the compare value. When comparing for lower limit (ACFGT=0), ADCRH:ADCRL is a negative value without the sign bit. If the value from these registers is complemented and then a value of 1 is added, then the calculated value is the unsigned (i.e., absolute) difference between the conversion result and the compare value. In the previous example, 0x280 is stored in ADCRH:ADCRL. The following example shows how the absolute value of the difference is calculated.

```
%01 0111 1111 <= Complement of 10-bit value stored in ADCRH:ADCRL
+         %1
---------------
 %01 1000 0000<= Unsigned value 0x180 is the absolute value of (Result - Compare Value)
```

### 9.4.6 MCU Wait Mode Operation

Wait mode is a lower power-consumption standby mode from which recovery is fast because the clock sources remain active. If a conversion is in progress when the MCU enters wait mode, it continues until completion. Conversions can be initiated while the MCU is in wait mode by means of the hardware trigger or if continuous conversions are enabled.

The bus clock, bus clock divided by two, and ADACK are available as conversion clock sources while in wait mode. The use of ALTCLK as the conversion clock source in wait is dependent on the definition of ALTCLK for this MCU. Consult the module introduction for information on ALTCLK specific to this MCU.

A conversion complete event sets the COCO and generates an ADC interrupt to wake the MCU from wait mode if the ADC interrupt is enabled (AIEN = 1).

### 9.4.7 MCU Stop3 Mode Operation

Stop mode is a low power-consumption standby mode during which most or all clock sources on the MCU are disabled.

#### 9.4.7.1 Stop3 Mode With ADACK Disabled

If the asynchronous clock, ADACK, is not selected as the conversion clock, executing a stop instruction aborts the current conversion and places the ADC in its idle state. The contents of ADCRH and ADCRL are unaffected by stop3 mode.After exiting from stop3 mode, a software or hardware trigger is required to resume conversions.

#### 9.4.7.2 Stop3 Mode With ADACK Enabled

If ADACK is selected as the conversion clock, the ADC continues operation during stop3 mode. For guaranteed ADC operation, the MCU's voltage regulator must remain active during stop3 mode. Consult the module introduction for configuration information for this MCU.

If a conversion is in progress when the MCU enters stop3 mode, it continues until completion. Conversions can be initiated while the MCU is in stop3 mode by means of the hardware trigger or if continuous conversions are enabled.

A conversion complete event sets the COCO and generates an ADC interrupt to wake the MCU from stop3 mode if the ADC interrupt is enabled (AIEN = 1).

**NOTE**

The ADC module can wake the system from low-power stop and cause the MCU to begin consuming run-level currents without generating a system level interrupt. To prevent this scenario, software should ensure the data transfer blocking mechanism (discussed in Section 9.4.4.2, "Completing Conversions) is cleared when entering stop3 and continuing ADC conversions.

### 9.4.8 MCU Stop2 Mode Operation

The ADC module is automatically disabled when the MCU enters either stop2 mode. All module registers contain their reset values following exit from stop2. Therefore, the module must be re-enabled and re-configured following exit from stop2.

## 9.5 Initialization Information

This section gives an example that provides some basic direction on how to initialize and configure the ADC module. You can configure the module for 8-bit or 10-bit resolution, single or continuous conversion, and a polled or interrupt approach, among many other options. Refer to Table 9-7, Table 9-8, and Table 9-9 for information used in this example.

**NOTE**

Hexadecimal values designated by a preceding 0x, binary values designated by a preceding %, and decimal values have no preceding character.

### 9.5.1 ADC Module Initialization Example

#### 9.5.1.1 Initialization Sequence

Before the ADC module can be used to complete conversions, an initialization procedure must be performed. A typical sequence is as follows:

1. Update the configuration register (ADCCFG) to select the input clock source and the divide ratio used to generate the internal clock, ADCK. This register is also used for selecting sample time and low-power configuration.

2. Update status and control register 2 (ADCSC2) to select the conversion trigger (hardware or software) and compare function options, if enabled.
3. Update status and control register 1 (ADCSC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

#### 9.5.1.2 Pseudo-Code Example

In this example, the ADC module is set up with interrupts enabled to perform a single 10-bit conversion at low power with a long sample time on input channel 1, where the internal ADCK clock is derived from the bus clock divided by 1.

**ADCCFG = 0x98 (%10011000)**

```
Bit 7    ADLPC    1        Configures for low power (lowers maximum clock speed)
Bit 6:5  ADIV     00       Sets the ADCK to the input clock ÷ 1
Bit 4    ADLSMP   1        Configures for long sample time
Bit 3:2  MODE     10       Sets mode at 10-bit conversions
Bit 1:0  ADICLK   00       Selects bus clock as input clock source
```

**ADCSC2 = 0x00 (%00000000)**

```
Bit 7    ADACT    0        Flag indicates if a conversion is in progress
Bit 6    ADTRG    0        Software trigger selected
Bit 5    ACFE     0        Compare function disabled
Bit 4    ACFGT    0        Not used in this example
Bit 3:2           00       Reserved, always reads zero
Bit 1:0           00       Reserved for Freescale's internal use; always write zero
```

**ADCSC1 = 0x41 (%01000001)**

```
Bit 7    COCO     0        Read-only flag which is set when a conversion completes
Bit 6    AIEN     1        Conversion complete interrupt enabled
Bit 5    ADCO     0        One conversion only (continuous conversions disabled)
Bit 4:0  ADCH     00001    Input channel 1 selected as ADC input channel
```

**ADCRH/L = 0xxx**

```
Holds results of conversion. Read high byte (ADCRH) before low byte (ADCRL) so that
conversion data cannot be overwritten with data from the next conversion.
```

**ADCCVH/L = 0xxx**

```
Holds compare value when compare function enabled
```

**APCTL1=0x02**

```
AD1 pin I/O control disabled. All other AD pins remain general purpose I/O pins
```

**APCTL2=0x00**

```
All other AD pins remain general purpose I/O pins
```

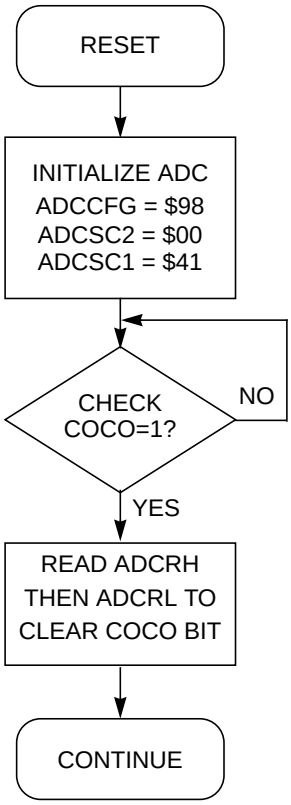



**Figure 9-13. Initialization Flowchart for Example**

## 9.6 Application Information

This section contains information for using the ADC module in applications. The ADC has been designed for integration into a microcontroller used in embedded control applications requiring an A/D converter.

### 9.6.1 External Pins and Routing

The following sections discuss the external pins associated with the ADC module and how they should be used for best results.

#### 9.6.1.1 Analog Supply Pins

The ADC module has analog power and ground supplies ($V_{DDA}$ and $V_{SSA}$) available as separate pins on some devices. $V_{SSA}$ is shared on the same pin as the MCU digital $V_{SS}$ on some devices. On other devices, $V_{SSA}$ and $V_{DDA}$ are shared with the MCU digital supply pins. In these cases, there are separate pads for the analog supplies which are bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

When available on a separate pin, both $V_{DDA}$ and $V_{SSA}$ must be connected to the same voltage potential as their corresponding MCU digital supply ($V_{DD}$ and $V_{SS}$) and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

If separate power supplies are used for analog and digital power, the ground connection between these supplies must be at the $V_{SSA}$ pin. This should be the only ground connection between these supplies if possible. The $V_{SSA}$ pin makes a good single point ground location.

### 9.6.1.2 Analog Reference Pins

In addition to the analog supplies, the ADC module has connections for two reference voltage inputs. The high reference is $V_{REFH}$, which may be shared on the same pin as $V_{DDA}$ on some devices. The low reference is $V_{REFL}$, which may be shared on the same pin as $V_{SSA}$ on some devices.

When available on a separate pin, $V_{REFH}$ may be connected to the same potential as $V_{DDA}$, or may be driven by an external source between the minimum $V_{DDA}$ spec and the $V_{DDA}$ potential ($V_{REFH}$ must never exceed $V_{DDA}$). When available on a separate pin, $V_{REFL}$ must be connected to the same voltage potential as $V_{SSA}$. $V_{REFH}$ and $V_{REFL}$ must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

AC current in the form of current spikes required to supply charge to the capacitor array at each successive approximation step is drawn through the $V_{REFH}$ and $V_{REFL}$ loop. The best external component to meet this current demand is a 0.1 µF capacitor with good high frequency characteristics. This capacitor is connected between $V_{REFH}$ and $V_{REFL}$ and must be placed as near as possible to the package pins. Resistance in the path is not recommended because the current causes a voltage drop that could result in conversion errors. Inductance in this path must be minimum (parasitic only).

### 9.6.1.3 Analog Input Pins

The external analog inputs are typically shared with digital I/O pins on MCU devices. The pin I/O control is disabled by setting the appropriate control bit in one of the pin control registers. Conversions can be performed on inputs without the associated pin control register bit set. It is recommended that the pin control register bit always be set when using a pin as an analog input. This avoids problems with contention because the output buffer is in its high impedance state and the pullup is disabled. Also, the input buffer draws dc current when its input is not at $V_{DD}$ or $V_{SS}$. Setting the pin control register bits for all pins used as analog inputs should be done to achieve lowest operating current.

Empirical data shows that capacitors on the analog inputs improve performance in the presence of noise or when the source impedance is high. Use of 0.01 µF capacitors with good high-frequency characteristics is sufficient. These capacitors are not necessary in all cases, but when used they must be placed as near as possible to the package pins and be referenced to $V_{SSA}$.

For proper conversion, the input voltage must fall between $V_{REFH}$ and $V_{REFL}$. If the input is equal to or exceeds $V_{REFH}$, the converter circuit converts the signal to 0x3FF (full scale 10-bit representation) or 0xFF (full scale 8-bit representation). If the input is equal to or less than $V_{REFL}$, the converter circuit converts it to 0x000. Input voltages between $V_{REFH}$ and $V_{REFL}$ are straight-line linear conversions. There is a brief current associated with $V_{REFL}$ when the sampling capacitor is charging. The input is sampled for 3.5 cycles of the ADCK source when ADLSMP is low, or 23.5 cycles when ADLSMP is high.

For minimal loss of accuracy due to current injection, pins adjacent to the analog input pins should not be transitioning during conversions.

## 9.6.2 Sources of Error

Several sources of error exist for A/D conversions. These are discussed in the following sections.

### 9.6.2.1 Sampling Error

For proper conversions, the input must be sampled long enough to achieve the proper accuracy. Given the maximum input resistance of approximately 7kΩ and input capacitance of approximately 5.5 pF, sampling to within 1/4LSB (at 10-bit resolution) can be achieved within the minimum sample window (3.5 cycles @ 8 MHz maximum ADCK frequency) provided the resistance of the external analog source ($R_{AS}$) is kept below 5 kΩ.

Higher source resistances or higher-accuracy sampling is possible by setting ADLSMP (to increase the sample window to 23.5 cycles) or decreasing ADCK frequency to increase sample time.

### 9.6.2.2 Pin Leakage Error

Leakage on the I/O pins can cause conversion error if the external analog source resistance ($R_{AS}$) is high. If this error cannot be tolerated by the application, keep $R_{AS}$ lower than $V_{DDA} / (2^N * I_{LEAK})$ for less than 1/4LSB leakage error (N = 8 in 8-bit mode or 10 in 10-bit mode).

### 9.6.2.3 Noise-Induced Errors

System noise that occurs during the sample or conversion process can affect the accuracy of the conversion. The ADC accuracy numbers are guaranteed as specified only if the following conditions are met:

- There is a 0.1 µF low-ESR capacitor from $V_{REFH}$ to $V_{REFL}$.
- There is a 0.1 µF low-ESR capacitor from $V_{DDA}$ to $V_{SSA}$.
- If inductive isolation is used from the primary supply, an additional 1 µF capacitor is placed from $V_{DDA}$ to $V_{SSA}$.
- $V_{SSA}$ (and $V_{REFL}$, if connected) is connected to $V_{SS}$ at a quiet point in the ground plane.
- Operate the MCU in wait or stop3 mode before initiating (hardware triggered conversions) or immediately after initiating (hardware or software triggered conversions) the ADC conversion.
  - For software triggered conversions, immediately follow the write to ADCSC1 with a wait instruction or stop instruction.
  - For stop3 mode operation, select ADACK as the clock source. Operation in stop3 reduces $V_{DD}$ noise but increases effective conversion time due to stop recovery.
- There is no I/O switching, input or output, on the MCU during the conversion.

There are some situations where external system activity causes radiated or conducted noise emissions or excessive $V_{DD}$ noise is coupled into the ADC. In these situations, or when the MCU cannot be placed in wait or stop3 or I/O activity cannot be halted, these recommended actions may reduce the effect of noise on the accuracy:

- Place a 0.01 µF capacitor ($C_{AS}$) on the selected input channel to $V_{REFL}$ or $V_{SSA}$ (this improves noise issues, but affects the sample rate based on the external analog source resistance).

- Average the result by converting the analog input many times in succession and dividing the sum of the results. Four samples are required to eliminate the effect of a 1LSB, one-time error.
- Reduce the effect of synchronous noise by operating off the asynchronous clock (ADACK) and averaging. Noise that is synchronous to ADCK cannot be averaged out.

### 9.6.2.4 Code Width and Quantization Error

The ADC quantizes the ideal straight-line transfer function into 1024 steps (in 10-bit mode). Each step ideally has the same height (1 code) and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N bit converter (in this case N can be 8 or 10), defined as 1LSB, is:

$$1_{LSB} = (V_{REFH} - V_{REFL}) / 2^N \qquad \textit{Eqn. 9-2}$$

There is an inherent quantization error due to the digitization of the result. For 8-bit or 10-bit conversions the code transitions when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2LSB in 8- or 10-bit mode. As a consequence, however, the code width of the first (0x000) conversion is only 1/2LSB and the code width of the last (0xFF or 0x3FF) is 1.5LSB.

### 9.6.2.5 Linearity Errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system should be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error ($E_{ZS}$) (sometimes called offset) — This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2LSB). If the first conversion is 0x001, then the difference between the actual 0x001 code width and its ideal (1LSB) is used.
- Full-scale error ($E_{FS}$) — This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5LSB). If the last conversion is 0x3FE, then the difference between the actual 0x3FE code width and its ideal (1LSB) is used.
- Differential non-linearity (DNL) — This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.
- Integral non-linearity (INL) — This error is defined as the highest-value the (absolute value of the) running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE) — This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function and includes all forms of error.

### 9.6.2.6 Code Jitter, Non-Monotonicity, and Missing Codes

Analog-to-digital converters are susceptible to three special forms of error. These are code jitter, non-monotonicity, and missing codes.

Code jitter is when, at certain points, a given input voltage converts to one of two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the

converter yields the lower code (and vice-versa). However, even small amounts of system noise can cause the converter to be indeterminate (between two codes) for a range of input voltages around the transition voltage. This range is normally around 1/2LSB and increases with noise. This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Section 9.6.2.3 reduces this error.

Non-monotonicity is defined as when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and have no missing codes.

# Chapter 10
# Inter-Integrated Circuit (S08IICV2)

## 10.1 Introduction

The inter-integrated circuit (IIC) provides a method of communication between a number of devices. The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

**NOTE**

The SDA and SCL should not be driven above $V_{DD}$. These pins are pseudo open-drain containing a protection diode to $V_{DD}$.

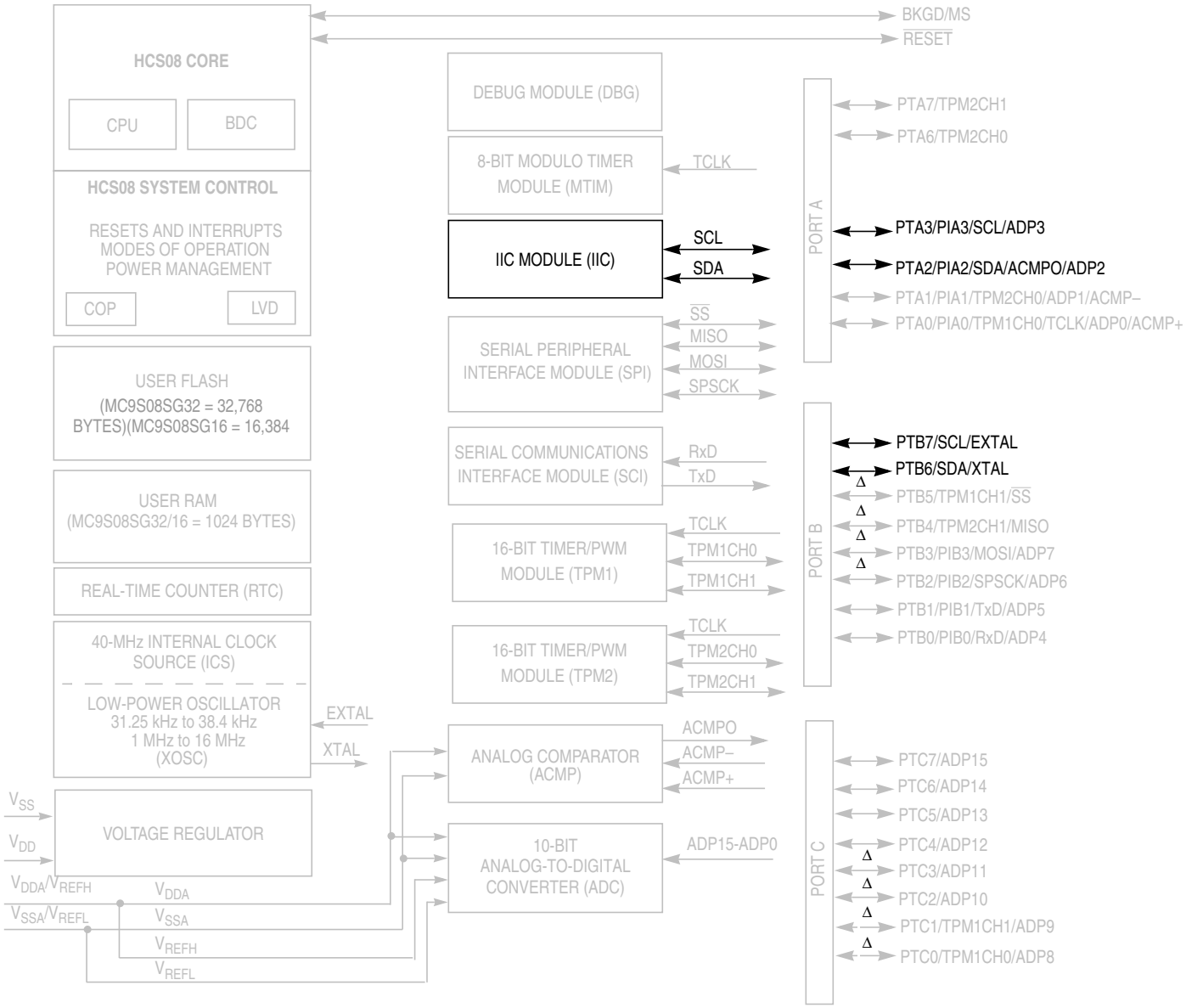
### 10.1.1 Module Configuration

The IIC module pins, SDA and SCL can be repositioned under software control using IICPS in SOPT1 as as shown in Table 10-1. IICPS in SOPT1 selects which general-purpose I/O ports are associated with IIC operation.

**Table 10-1. IIC Position Options**

| IICPS in SOPT1 | Port Pin for SDA | Port Pin for SCL |
|---|---|---|
| 0 (default) | PTA2 | PTA3 |
| 1 | PTB6 | PTB7 |

Figure 10-1 shows the MC9S08SG32 Series block diagram with the IIC module highlighted.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 10-1. MC9S08SG32 Series Block Diagram Highlighting IIC Block and Pins**

### 10.1.2 Features

The IIC includes these distinctive features:

- Compatible with IIC bus standard
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus busy detection
- General call recognition
- 10-bit address extension

### 10.1.3 Modes of Operation

A brief description of the IIC in the various MCU modes is given here.

- **Run mode** — This is the basic mode of operation. To conserve power in this mode, disable the module.
- **Wait mode** — The module continues to operate while the MCU is in wait mode and can provide a wake-up interrupt.
- **Stop mode** — The IIC is inactive in stop3 mode for reduced power consumption. The stop instruction does not affect IIC register states. Stop2 resets the register contents.

### 10.1.4 Block Diagram

Figure 10-2 is a block diagram of the IIC.

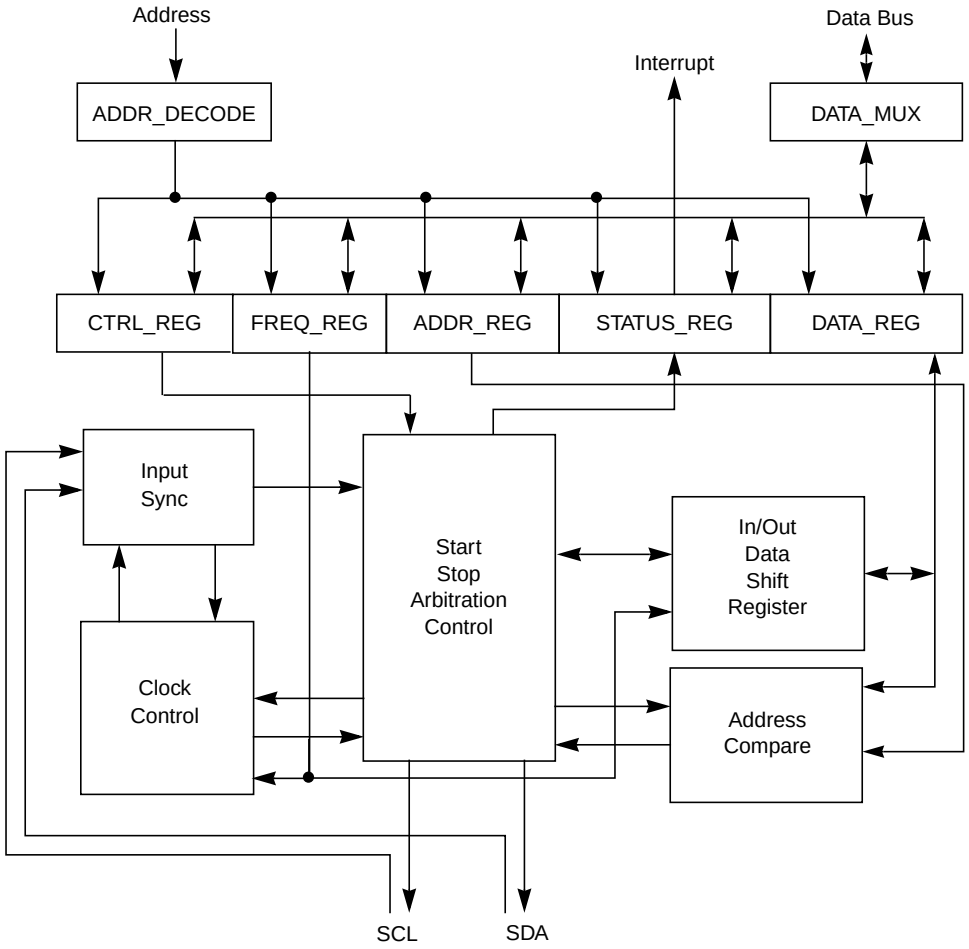



**Figure 10-2. IIC Functional Block Diagram**

## 10.2 External Signal Description

This section describes each user-accessible pin signal.

### 10.2.1 SCL — Serial Clock Line

The bidirectional SCL is the serial clock line of the IIC system.

### 10.2.2 SDA — Serial Data Line

The bidirectional SDA is the serial data line of the IIC system.

## 10.3 Register Definition

This section consists of the IIC register descriptions in address order.

Refer to the direct-page register summary in the memory chapter of this document for the absolute address assignments for all IIC registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

## 10.3.1 IIC Address Register (IICA)

**Figure 10-3. IIC Address Register (IICA)**

**Table 10-2. IICA Field Descriptions**

| Field | Description |
|---|---|
| 7–1<br>AD[7:1] | **Slave Address.** The AD[7:1] field contains the slave address to be used by the IIC module. This field is used on the 7-bit address scheme and the lower seven bits of the 10-bit address scheme. |

## 10.3.2 IIC Frequency Divider Register (IICF)

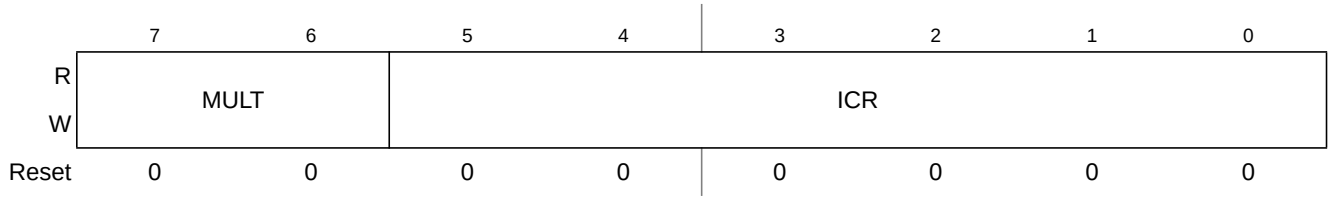



**Figure 10-4. IIC Frequency Divider Register (IICF)**

**Table 10-3. IICF Field Descriptions**

| Field | Description |
|---|---|
| 7–6<br>MULT | **IIC Multiplier Factor**. The MULT bits define the multiplier factor, mul. This factor, along with the SCL divider, generates the IIC baud rate. The multiplier factor mul as defined by the MULT bits is provided below.<br>00 mul = 01<br>01 mul = 02<br>10 mul = 04<br>11 Reserved |
| 5–0<br>ICR | **IIC Clock Rate**. The ICR bits are used to prescale the bus clock for bit rate selection. These bits and the MULT bits determine the IIC baud rate, the SDA hold time, the SCL Start hold time, and the SCL Stop hold time. Table 10-5 provides the SCL divider and hold values for corresponding values of the ICR.<br><br>The SCL divider multiplied by multiplier factor mul generates IIC baud rate.<br>$$\text{IIC baud rate} = \frac{\text{bus speed (Hz)}}{\text{mul} \times \text{SCLdivider}}$$ ***Eqn. 10-1***<br>SDA hold time is the delay from the falling edge of SCL (IIC clock) to the changing of SDA (IIC data).<br>$$\text{SDA hold time} = \text{bus period (s)} \times \text{mul} \times \text{SDA hold value}$$ Eqn. 10-2<br>SCL start hold time is the delay from the falling edge of SDA (IIC data) while SCL is high (Start condition) to the falling edge of SCL (IIC clock).<br>$$\text{SCL Start hold time} = \text{bus period (s)} \times \text{mul} \times \text{SCL Start hold value}$$ Eqn. 10-3<br>SCL stop hold time is the delay from the rising edge of SCL (IIC clock) to the rising edge of SDA SDA (IIC data) while SCL is high (Stop condition).<br>$$\text{SCL Stop hold time} = \text{bus period (s)} \times \text{mul} \times \text{SCL Stop hold value}$$ Eqn. 10-4 |

For example, if the bus speed is 8 MHz, the table below shows the possible hold time values with different ICR and MULT selections to achieve an IIC baud rate of 100kbps.

**Table 10-4. Hold Time Values for 8 MHz Bus Speed**

| MULT | ICR | Hold Times (μs) | | |
|---|---|---|---|---|
| | | SDA | SCL Start | SCL Stop |
| 0x2 | 0x00 | 3.500 | 3.000 | 5.500 |
| 0x1 | 0x07 | 2.500 | 4.000 | 5.250 |
| 0x1 | 0x0B | 2.250 | 4.000 | 5.250 |
| 0x0 | 0x14 | 2.125 | 4.250 | 5.125 |
| 0x0 | 0x18 | 1.125 | 4.750 | 5.125 |

**Table 10-5. IIC Divider and Hold Values**

| ICR (hex) | SCL Divider | SDA Hold Value | SCL Hold (Start) Value | SCL Hold (Stop) Value |
|---|---|---|---|---|
| **00** | 20 | 7 | 6 | 11 |
| **01** | 22 | 7 | 7 | 12 |
| **02** | 24 | 8 | 8 | 13 |
| **03** | 26 | 8 | 9 | 14 |
| **04** | 28 | 9 | 10 | 15 |
| **05** | 30 | 9 | 11 | 16 |
| **06** | 34 | 10 | 13 | 18 |
| **07** | 40 | 10 | 16 | 21 |
| **08** | 28 | 7 | 10 | 15 |
| **09** | 32 | 7 | 12 | 17 |
| **0A** | 36 | 9 | 14 | 19 |
| **0B** | 40 | 9 | 16 | 21 |
| **0C** | 44 | 11 | 18 | 23 |
| **0D** | 48 | 11 | 20 | 25 |
| **0E** | 56 | 13 | 24 | 29 |
| **0F** | 68 | 13 | 30 | 35 |
| **10** | 48 | 9 | 18 | 25 |
| **11** | 56 | 9 | 22 | 29 |
| **12** | 64 | 13 | 26 | 33 |
| **13** | 72 | 13 | 30 | 37 |
| **14** | 80 | 17 | 34 | 41 |
| **15** | 88 | 17 | 38 | 45 |
| **16** | 104 | 21 | 46 | 53 |
| **17** | 128 | 21 | 58 | 65 |
| **18** | 80 | 9 | 38 | 41 |
| **19** | 96 | 9 | 46 | 49 |
| **1A** | 112 | 17 | 54 | 57 |
| **1B** | 128 | 17 | 62 | 65 |
| **1C** | 144 | 25 | 70 | 73 |
| **1D** | 160 | 25 | 78 | 81 |
| **1E** | 192 | 33 | 94 | 97 |
| **1F** | 240 | 33 | 118 | 121 |

| ICR (hex) | SCL Divider | SDA Hold Value | SCL Hold (Start) Value | SCL Hold (Stop) Value |
|---|---|---|---|---|
| **20** | 160 | 17 | 78 | 81 |
| **21** | 192 | 17 | 94 | 97 |
| **22** | 224 | 33 | 110 | 113 |
| **23** | 256 | 33 | 126 | 129 |
| **24** | 288 | 49 | 142 | 145 |
| **25** | 320 | 49 | 158 | 161 |
| **26** | 384 | 65 | 190 | 193 |
| **27** | 480 | 65 | 238 | 241 |
| **28** | 320 | 33 | 158 | 161 |
| **29** | 384 | 33 | 190 | 193 |
| **2A** | 448 | 65 | 222 | 225 |
| **2B** | 512 | 65 | 254 | 257 |
| **2C** | 576 | 97 | 286 | 289 |
| **2D** | 640 | 97 | 318 | 321 |
| **2E** | 768 | 129 | 382 | 385 |
| **2F** | 960 | 129 | 478 | 481 |
| **30** | 640 | 65 | 318 | 321 |
| **31** | 768 | 65 | 382 | 385 |
| **32** | 896 | 129 | 446 | 449 |
| **33** | 1024 | 129 | 510 | 513 |
| **34** | 1152 | 193 | 574 | 577 |
| **35** | 1280 | 193 | 638 | 641 |
| **36** | 1536 | 257 | 766 | 769 |
| **37** | 1920 | 257 | 958 | 961 |
| **38** | 1280 | 129 | 638 | 641 |
| **39** | 1536 | 129 | 766 | 769 |
| **3A** | 1792 | 257 | 894 | 897 |
| **3B** | 2048 | 257 | 1022 | 1025 |
| **3C** | 2304 | 385 | 1150 | 1153 |
| **3D** | 2560 | 385 | 1278 | 1281 |
| **3E** | 3072 | 513 | 1534 | 1537 |
| **3F** | 3840 | 513 | 1918 | 1921 |

## 10.3.3 IIC Control Register (IICC1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | IICEN | IICIE | MST | TX | TXAK | 0 | 0 | 0 |
| W | | | | | | RSTA | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 10-5. IIC Control Register (IICC1)**

**Table 10-6. IICC1 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>IICEN | **IIC Enable.** The IICEN bit determines whether the IIC module is enabled.<br>0 IIC is not enabled<br>1 IIC is enabled |
| 6<br>IICIE | **IIC Interrupt Enable.** The IICIE bit determines whether an IIC interrupt is requested.<br>0 IIC interrupt request not enabled<br>1 IIC interrupt request enabled |
| 5<br>MST | **Master Mode Select.** The MST bit changes from a 0 to a 1 when a start signal is generated on the bus and master mode is selected. When this bit changes from a 1 to a 0 a stop signal is generated and the mode of operation changes from master to slave.<br>0 Slave mode<br>1 Master mode |
| 4<br>TX | **Transmit Mode Select.** The TX bit selects the direction of master and slave transfers. In master mode, this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit is always high. When addressed as a slave, this bit should be set by software according to the SRW bit in the status register.<br>0 Receive<br>1 Transmit |
| 3<br>TXAK | **Transmit Acknowledge Enable.** This bit specifies the value driven onto the SDA during data acknowledge cycles for master and slave receivers.<br>0 An acknowledge signal is sent out to the bus after receiving one data byte<br>1 No acknowledge signal response is sent |
| 2<br>RSTA | **Repeat start.** Writing a 1 to this bit generates a repeated start condition provided it is the current master. This bit is always read as cleared. Attempting a repeat at the wrong time results in loss of arbitration. |

## 10.3.4 IIC Status Register (IICS)

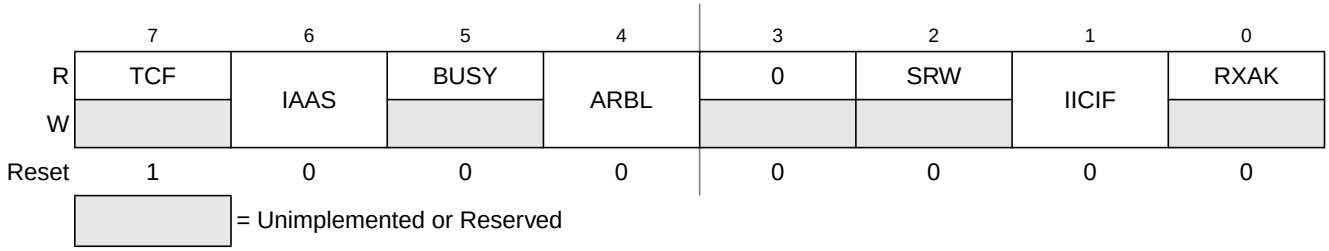



**Figure 10-6. IIC Status Register (IICS)**

**Table 10-7. IICS Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TCF | **Transfer Complete Flag.** This bit is set on the completion of a byte transfer. This bit is only valid during or immediately following a transfer to the IIC module or from the IIC module.The TCF bit is cleared by reading the IICD register in receive mode or writing to the IICD in transmit mode.<br>0 Transfer in progress<br>1 Transfer complete |
| 6<br>IAAS | **Addressed as a Slave.** The IAAS bit is set when the calling address matches the programmed slave address or when the GCAEN bit is set and a general call is received. Writing the IICC register clears this bit.<br>0 Not addressed<br>1 Addressed as a slave |
| 5<br>BUSY | **Bus Busy.** The BUSY bit indicates the status of the bus regardless of slave or master mode. The BUSY bit is set when a start signal is detected and cleared when a stop signal is detected.<br>0 Bus is idle<br>1 Bus is busy |
| 4<br>ARBL | **Arbitration Lost.** This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software by writing a 1 to it.<br>0 Standard bus operation<br>1 Loss of arbitration |
| 2<br>SRW | **Slave Read/Write.** When addressed as a slave, the SRW bit indicates the value of the R/W command bit of the calling address sent to the master.<br>0 Slave receive, master writing to slave<br>1 Slave transmit, master reading from slave |
| 1<br>IICIF | **IIC Interrupt Flag.** The IICIF bit is set when an interrupt is pending. This bit must be cleared by software, by writing a 1 to it in the interrupt routine. One of the following events can set the IICIF bit:<br>• One byte transfer completes<br>• Match of slave address to calling address<br>• Arbitration lost<br>0 No interrupt pending<br>1 Interrupt pending |
| 0<br>RXAK | **Receive Acknowledge**. When the RXAK bit is low, it indicates an acknowledge signal has been received after the completion of one byte of data transmission on the bus. If the RXAK bit is high it means that no acknowledge signal is detected.<br>0 Acknowledge received<br>1 No acknowledge received |

## 10.3.5 IIC Data I/O Register (IICD)

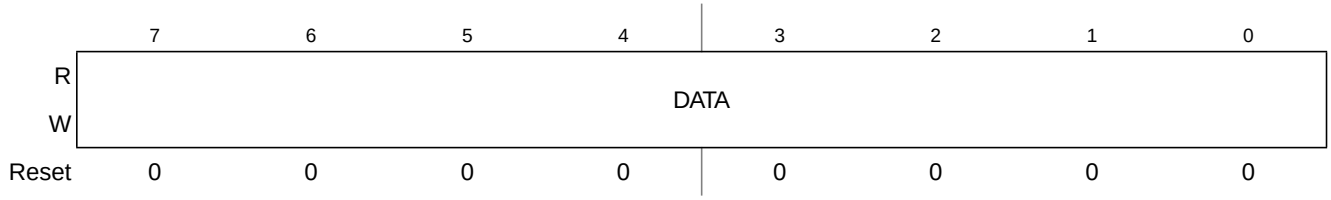



**Figure 10-7. IIC Data I/O Register (IICD)**

**Table 10-8. IICD Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>DATA | **Data** — In master transmit mode, when data is written to the IICD, a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates receiving of the next byte of data. |

**NOTE**

When transitioning out of master receive mode, the IIC mode should be switched before reading the IICD register to prevent an inadvertent initiation of a master receive data transfer.

In slave mode, the same functions are available after an address match has occurred.

The TX bit in IICC must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, reading the IICD does not initiate the receive.

Reading the IICD returns the last byte received while the IIC is configured in master receive or slave receive modes. The IICD does not reflect every byte transmitted on the IIC bus, nor can software verify that a byte has been written to the IICD correctly by reading it back.

In master transmit mode, the first byte of data written to IICD following assertion of MST is used for the address transfer and should comprise of the calling address (in bit 7 to bit 1) concatenated with the required R/$\overline{W}$ bit (in position bit 0).

## 10.3.6 IIC Control Register 2 (IICC2)

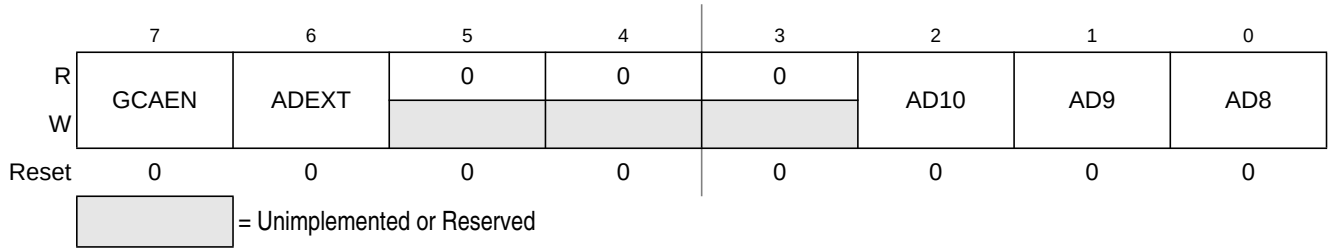



**Figure 10-8. IIC Control Register (IICC2)**

**Table 10-9. IICC2 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>GCAEN | **General Call Address Enable.** The GCAEN bit enables or disables general call address.<br>0 General call address is disabled<br>1 General call address is enabled |
| 6<br>ADEXT | **Address Extension.** The ADEXT bit controls the number of bits used for the slave address.<br>0 7-bit address scheme<br>1 10-bit address scheme |
| 2–0<br>AD[10:8] | Slave Address. The AD[10:8] field contains the upper three bits of the slave address in the 10-bit address scheme. This field is only valid when the ADEXT bit is set. |

## 10.4 Functional Description

This section provides a complete functional description of the IIC module.

### 10.4.1 IIC Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. A logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts:

- Start signal
- Slave address transmission
- Data transfer
- Stop signal

The stop signal should not be confused with the CPU stop instruction. The IIC bus system communication is described briefly in the following sections and illustrated in Figure 10-9.

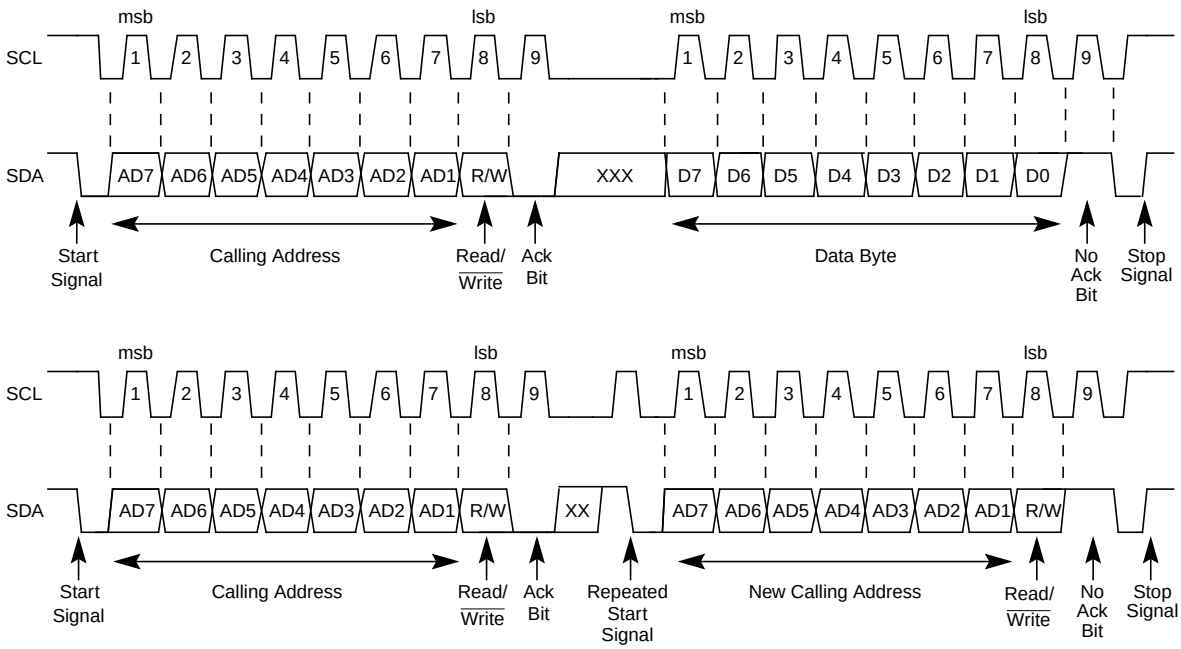



**Figure 10-9. IIC Bus Transmission Signals**

### 10.4.1.1 Start Signal

When the bus is free, no master device is engaging the bus (SCL and SDA lines are at logical high), a master may initiate communication by sending a start signal. As shown in Figure 10-9, a start signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

### 10.4.1.2 Slave Address Transmission

The first byte of data transferred immediately after the start signal is the slave address transmitted by the master. This is a seven-bit calling address followed by a R/$\overline{W}$ bit. The R/$\overline{W}$ bit tells the slave the desired direction of data transfer.

1 = Read transfer, the slave transmits data to the master.
0 = Write transfer, the master transmits data to the slave.

Only the slave with a calling address that matches the one transmitted by the master responds by sending back an acknowledge bit. This is done by pulling the SDA low at the ninth clock (see Figure 10-9).

No two slaves in the system may have the same address. If the IIC module is the master, it must not transmit an address equal to its own slave address. The IIC cannot be master and slave at the same time. However, if arbitration is lost during an address cycle, the IIC reverts to slave mode and operates correctly even if it is being addressed by another master.

#### 10.4.1.3 Data Transfer

Before successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the R/$\overline{W}$ bit sent by the calling master.

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in Figure 10-9. There is one clock pulse on SCL for each data bit, the msb being transferred first. Each data byte is followed by a 9th (acknowledge) bit, which is signalled from the receiving device. An acknowledge is signalled by pulling the SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit time, the SDA line must be left high by the slave. The master interprets the failed acknowledge as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets this as an end of data transfer and releases the SDA line.

In either case, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a stop signal.
- Commences a new calling by generating a repeated start signal.

#### 10.4.1.4 Stop Signal

The master can terminate the communication by generating a stop signal to free the bus. However, the master may generate a start signal followed by a calling command without generating a stop signal first. This is called repeated start. A stop signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see Figure 10-9).

The master can generate a stop even if the slave has generated an acknowledge at which point the slave must release the bus.

#### 10.4.1.5 Repeated Start Signal

As shown in Figure 10-9, a repeated start signal is a start signal generated without first generating a stop signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

#### 10.4.1.6 Arbitration Procedure

The IIC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case,

the transition from master to slave mode does not generate a stop condition. Meanwhile, a status bit is set by hardware to indicate loss of arbitration.

### 10.4.1.7 Clock Synchronization

Because wire-AND logic is performed on the SCL line, a high-to-low transition on the SCL line affects all the devices connected on the bus. The devices start counting their low period and after a device's clock has gone low, it holds the SCL line low until the clock high state is reached. However, the change of low to high in this device clock may not change the state of the SCL line if another device clock is still within its low period. Therefore, synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time (see Figure 10-10). When all devices concerned have counted off their low period, the synchronized clock SCL line is released and pulled high. There is then no difference between the device clocks and the state of the SCL line and all the devices start counting their high periods. The first device to complete its high period pulls the SCL line low again.

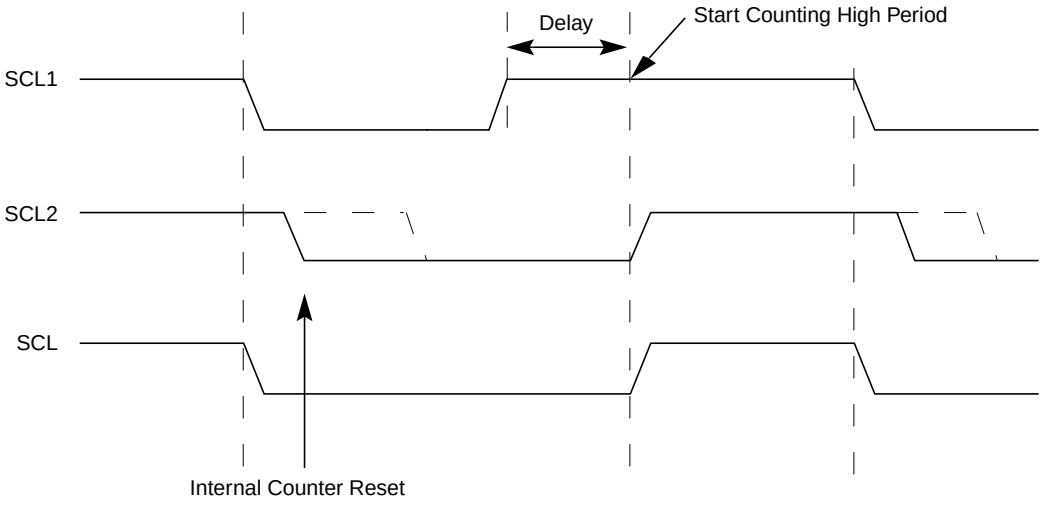



**Figure 10-10. IIC Clock Synchronization**

### 10.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such a case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

### 10.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

## 10.4.2 10-bit Address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

### 10.4.2.1 Master-Transmitter Addresses a Slave-Receiver

The transfer direction is not changed (see Table 10-10). When a 10-bit address follows a start condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/$\overline{W}$ direction bit) is 0. More than one device can find a match and generate an acknowledge (A1). Then, each slave that finds a match compares the eight bits of the second byte of the slave address with its own address. Only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

| S | Slave Address 1st 7 bits<br>11110 + AD10 + AD9 | R/W<br>0 | A1 | Slave Address 2nd byte<br>AD[8:1] | A2 | Data | A | ... | Data | A/A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 10-10. Master-Transmitter Addresses Slave-Receiver with a 10-bit Address**

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

### 10.4.2.2 Master-Receiver Addresses a Slave-Transmitter

The transfer direction is changed after the second R/$\overline{W}$ bit (see Table 10-11). Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated start condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the start condition (S) and tests whether the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

After a repeated start condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them are addressed because R/$\overline{W}$ = 1 (for 10-bit devices) or the 11110XX slave address (for 7-bit devices) does not match.

| S | Slave Address<br>1st 7 bits<br>11110 + AD10 + AD9 | R/W<br>0 | A1 | Slave Address<br>2nd byte<br>AD[8:1] | A2 | Sr | Slave Address<br>1st 7 bits<br>11110 + AD10 + AD9 | R/W<br>1 | A3 | Data | A | ... | Data | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 10-11. Master-Receiver Addresses a Slave-Transmitter with a 10-bit Address**

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

### 10.4.3 General Call Address

General calls can be requested in 7-bit address or 10-bit address. If the GCAEN bit is set, the IIC matches the general call address as well as its own slave address. When the IIC responds to a general call, it acts as a slave-receiver and the IAAS bit is set after the address cycle. Software must read the IICD register after the first byte transfer to determine whether the address matches is its own slave address or a general call. If the value is 00, the match is a general call. If the GCAEN bit is clear, the IIC ignores any data supplied from a general call address by not issuing an acknowledgement.

## 10.5 Resets

The IIC is disabled after reset. The IIC cannot cause an MCU reset.

## 10.6 Interrupts

The IIC generates a single interrupt.

An interrupt from the IIC is generated when any of the events in Table 10-12 occur, provided the IICIE bit is set. The interrupt is driven by bit IICIF (of the IIC status register) and masked with bit IICIE (of the IIC control register). The IICIF bit must be cleared by software by writing a 1 to it in the interrupt routine. You can determine the interrupt type by reading the status register.

**Table 10-12. Interrupt Summary**

| Interrupt Source | Status | Flag | Local Enable |
|---|---|---|---|
| Complete 1-byte transfer | TCF | IICIF | IICIE |
| Match of received calling address | IAAS | IICIF | IICIE |
| Arbitration Lost | ARBL | IICIF | IICIE |

### 10.6.1 Byte Transfer Interrupt

The TCF (transfer complete flag) bit is set at the falling edge of the ninth clock to indicate the completion of byte transfer.

### 10.6.2 Address Detect Interrupt

When the calling address matches the programmed slave address (IIC address register) or when the GCAEN bit is set and a general call is received, the IAAS bit in the status register is set. The CPU is interrupted, provided the IICIE is set. The CPU must check the SRW bit and set its Tx mode accordingly.

### 10.6.3 Arbitration Lost Interrupt

The IIC is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, the relative priority of the contending masters is determined by a data arbitration procedure. The IIC module asserts this interrupt when it loses the data arbitration process and the ARBL bit in the status register is set.

Arbitration is lost in the following circumstances:

- SDA sampled as a low when the master drives a high during an address or data transmit cycle.
- SDA sampled as a low when the master drives a high during the acknowledge bit of a data receive cycle.
- A start cycle is attempted when the bus is busy.
- A repeated start cycle is requested in slave mode.
- A stop condition is detected when the master did not request it.

This bit must be cleared by software writing a 1 to it.

# 10.7 Initialization/Application Information

**Module Initialization (Slave)**

1. Write: IICC2
   — to enable or disable general call
   — to select 10-bit or 7-bit addressing mode
2. Write: IICA
   — to set the slave address
3. Write: IICC1
   — to enable IIC and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in Figure 10-12

**Module Initialization (Master)**

1. Write: IICF
   — to set the IIC baud rate (example provided in this chapter)
2. Write: IICC1
   — to enable IIC and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in Figure 10-12
5. Write: IICC1
   — to enable TX
6. Write: IICC1
   — to enable MST (master mode)
7. Write: IICD
   — with the address of the target slave. (The lsb of this byte determines whether the communication is master receive or transmit.)

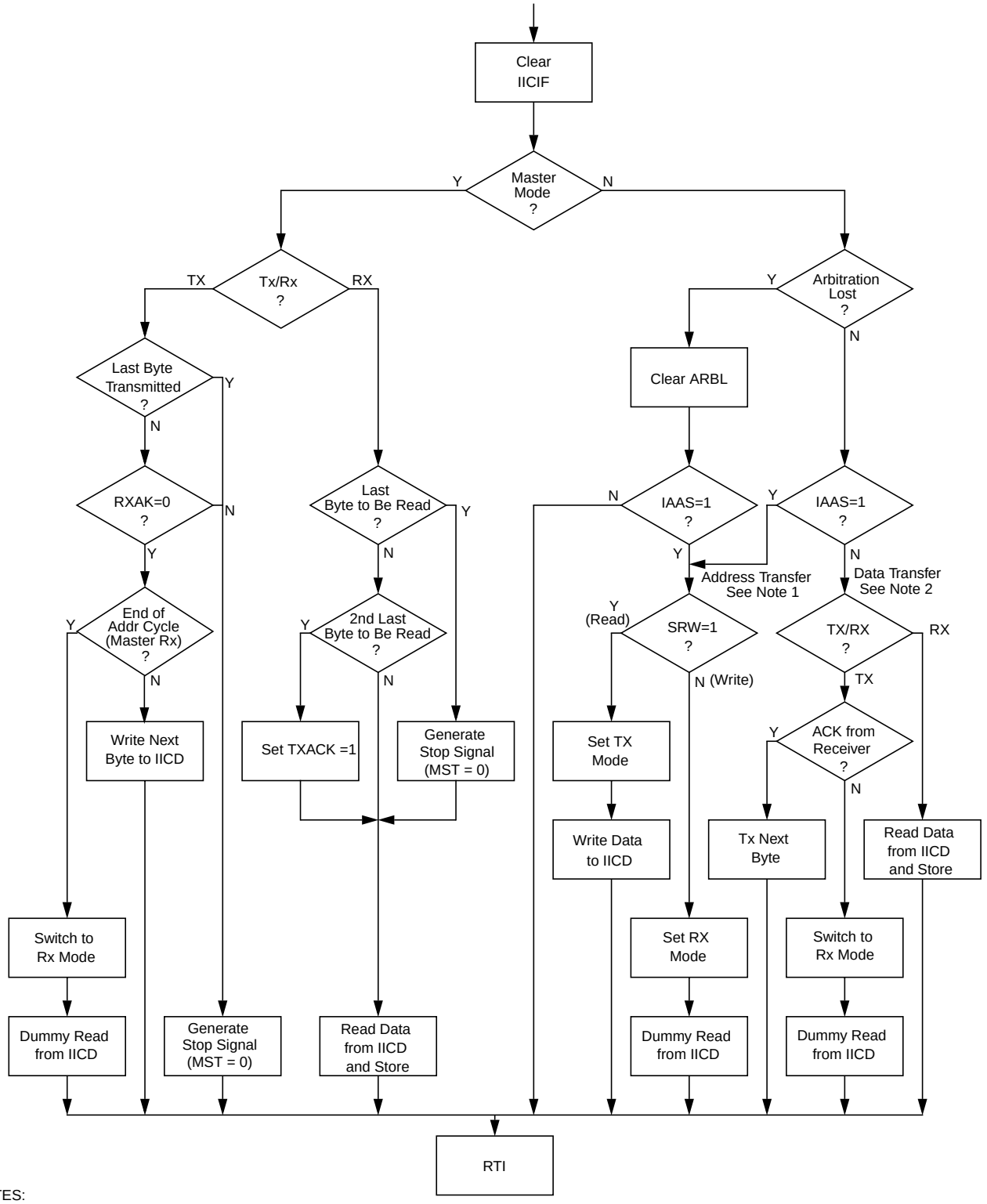
**Module Use**

The routine shown in Figure 10-12 can handle both master and slave IIC operations. For slave operation, an incoming IIC message that contains the proper address begins IIC communication. For master operation, communication must be initiated by writing to the IICD register.

**Register Model**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IICA | AD[7:1] | | | | | | | 0 |
| | When addressed as a slave (in slave mode), the module responds to this address | | | | | | | |
| IICF | MULT | | ICR | | | | | |
| | Baud rate = BUSCLK / (2 x MULT x (SCL DIVIDER)) | | | | | | | |
| IICC1 | IICEN | IICIE | MST | TX | TXAK | RSTA | 0 | 0 |
| | Module configuration | | | | | | | |
| IICS | TCF | IAAS | BUSY | ARBL | 0 | SRW | IICIF | RXAK |
| | Module status flags | | | | | | | |
| IICD | DATA | | | | | | | |
| | Data register; Write to transmit IIC data read to read IIC data | | | | | | | |
| IICC2 | GCAEN | ADEXT | 0 | 0 | 0 | AD10 | AD9 | AD8 |
| | Address configuration | | | | | | | |

**Figure 10-11. IIC Module Quick Start**




NOTES:
1. If general call is enabled, a check must be done to determine whether the received address was a general call address (0x00). If the received address was a general call address, then the general call must be handled by user software.
2. When 10-bit addressing is used to address a slave, the slave sees an interrupt following the first byte of the extended address. User software must ensure that for this interrupt, the contents of IICD are ignored and not treated as a valid data transfer

**Figure 10-12. Typical IIC Interrupt Routine**

# Chapter 11
# Internal Clock Source (S08ICSV2)

## 11.1 Introduction

The internal clock source (ICS) module provides clock source choices for the MCU. The module contains a frequency-locked loop (FLL) as a clock source that is controllable by either an internal or an external reference clock. The module can provide this FLL clock or either of the internal or external reference clocks as a source for the MCU system clock. There are also signals provided to control a low power oscillator (XOSC) module to allow the use of an external crystal/resonator as the external reference clock.

Whichever clock source is chosen, it is passed through a reduced bus divider (BDIV) which allows a lower final output clock frequency to be derived.

The bus frequency will be one-half of the ICSOUT frequency. After reset, the ICS is configured for FEI mode and BDIV is reset to 0:1 to introduce an extra divide-by-two before ICSOUT so the bus frequency is $f_{dco}/4$. At POR, the TRIM and FTRIM settings are reset to 0x80 and 0 respectively so the dco frequency is $f_{dco_ut}$. For other resets, the trim settings keep the value that was present before the reset.

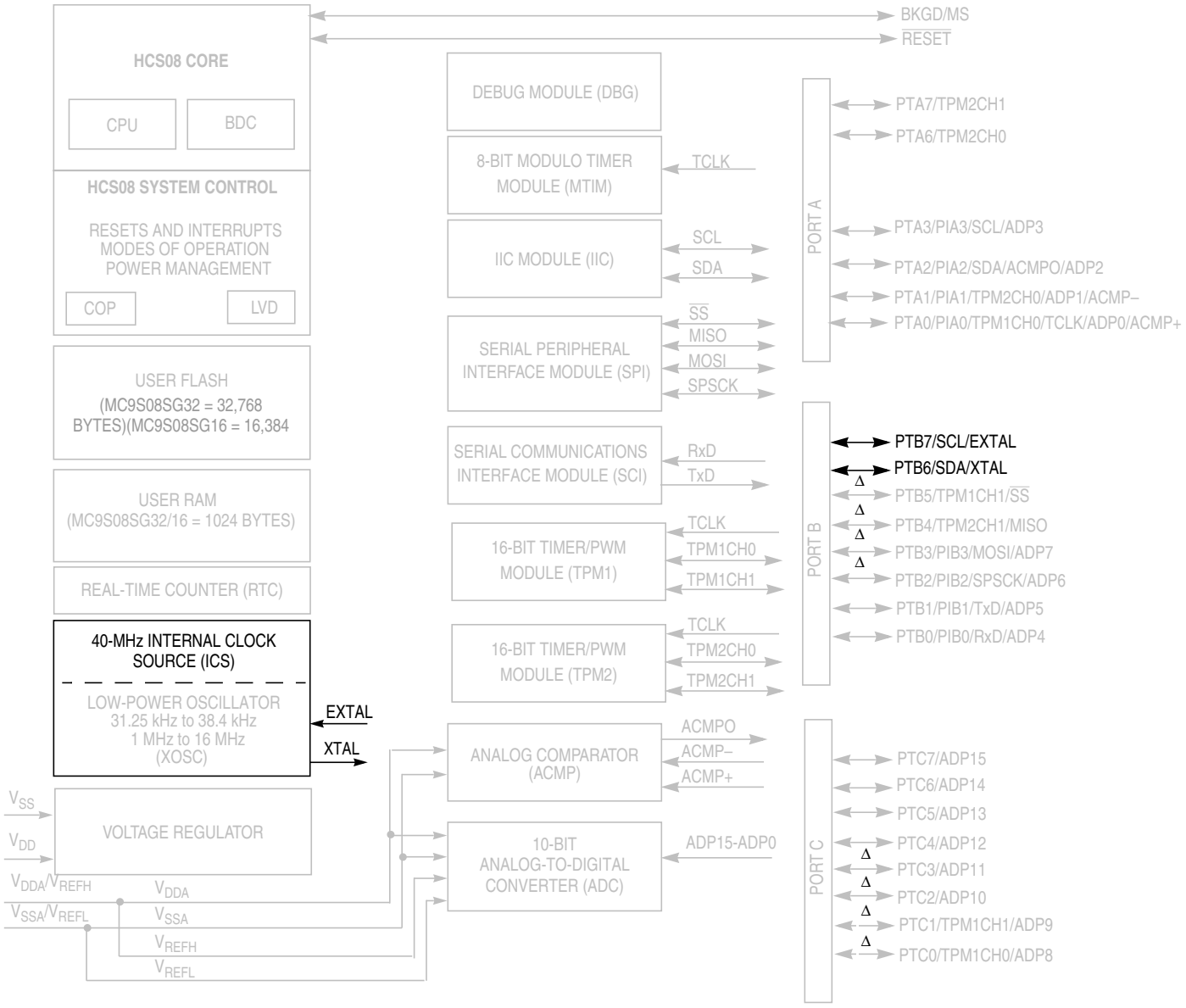
**NOTE**

Refer to Section 1.3, “System Clock Distribution for a detailed view of the distribution of clock sources throughout the MCU.

### 11.1.1 Module Configuration

When the internal reference is enabled in stop mode (IREFSTEN = 1), the voltage regulator must also be enabled in stop mode by setting the LVDE and LVDSE bits in the SPMSC1 register.

Figure 11-1 shows the MC9S08SG32 block diagram with the ICS highlighted.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 11-1. MC9S08SG32 Series Block Diagram Highlighting ICS Block and Pins**

### 11.1.2 Features

Key features of the ICS module follow. For device specific information, refer to the ICS Characteristics in the Electricals section of the documentation.

- Frequency-locked loop (FLL) is trimmable for accuracy using the internal 32 kHz reference over the specified temperature and voltage ranges
  - 0.1% resolution using 9-bit TRIM:FTRIM
  - 1.5% deviation for –40 °C to 125 °C standard-temperature rated devices
  - 3% deviation for AEC Grade 0 high-temperature rated devices (-40 to 150 °C)
- Internal or external reference clocks up to 5 MHz can be used to control the FLL
  - 3-bit select for reference divider is provided
- Internal reference clock has 9 trim bits available
- Internal or external reference clocks can be selected as the clock source for the MCU
- Whichever clock is selected as the source can be divided down
  - 2-bit select for clock divider is provided
    - Allowable dividers are: 1, 2, 4, 8
    - BDC clock is provided as a constant divide by 2 of the DCO output
- Control signals for a low power oscillator as the external reference clock are provided
  - HGO, RANGE, EREFS, ERCLKEN, EREFSTEN
- FLL Engaged Internal mode is automatically selected out of reset

### 11.1.3 Block Diagram

Figure 11-2 is the ICS block diagram.

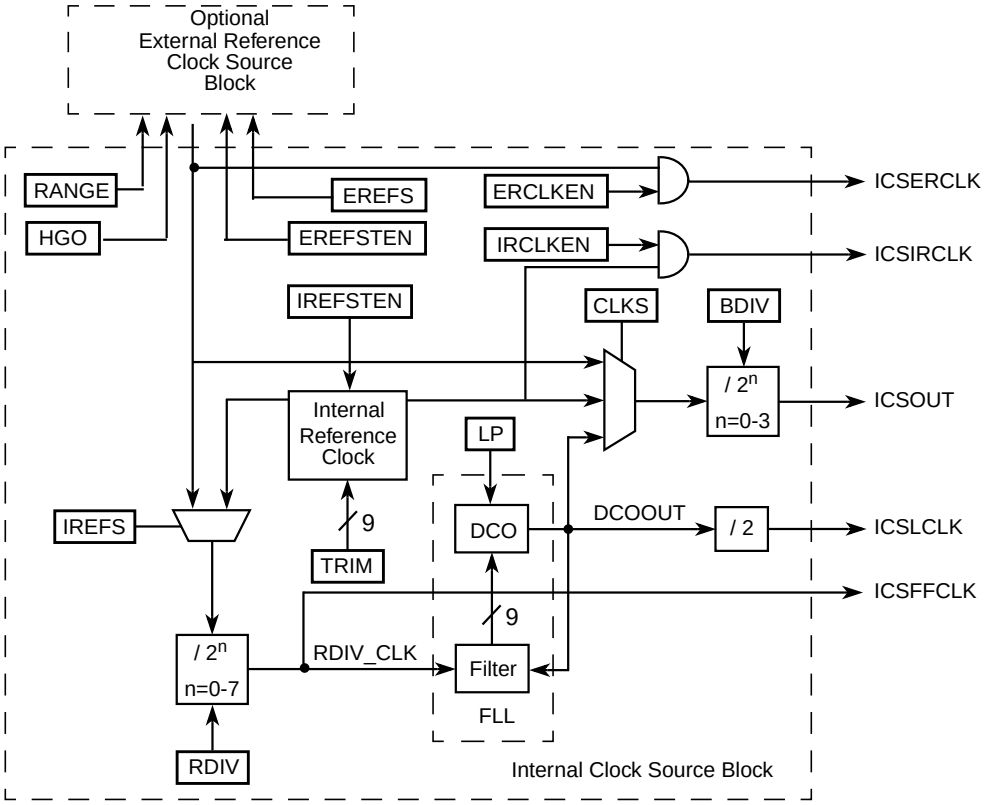



**Figure 11-2. Internal Clock Source (ICS) Block Diagram**

## 11.1.4 Modes of Operation

There are seven modes of operation for the ICS: FEI, FEE, FBI, FBILP, FBE, FBELP, and stop.

### 11.1.4.1 FLL Engaged Internal (FEI)

In FLL engaged internal mode, which is the default mode, the ICS supplies a clock derived from the FLL which is controlled by the internal reference clock. The BDC clock is supplied from the FLL.

### 11.1.4.2 FLL Engaged External (FEE)

In FLL engaged external mode, the ICS supplies a clock derived from the FLL which is controlled by an external reference clock. The BDC clock is supplied from the FLL.

### 11.1.4.3 FLL Bypassed Internal (FBI)

In FLL bypassed internal mode, the FLL is enabled and controlled by the internal reference clock, but is bypassed. The ICS supplies a clock derived from the internal reference clock. The BDC clock is supplied from the FLL.

#### 11.1.4.4 FLL Bypassed Internal Low Power (FBILP)

In FLL bypassed internal low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the internal reference clock. The BDC clock is not available.

#### 11.1.4.5 FLL Bypassed External (FBE)

In FLL bypassed external mode, the FLL is enabled and controlled by an external reference clock, but is bypassed. The ICS supplies a clock derived from the external reference clock. The external reference clock can be an external crystal/resonator supplied by an OSC controlled by the ICS, or it can be another external clock source. The BDC clock is supplied from the FLL.

#### 11.1.4.6 FLL Bypassed External Low Power (FBELP)

In FLL bypassed external low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the external reference clock. The external reference clock can be an external crystal/resonator supplied by an OSC controlled by the ICS, or it can be another external clock source. The BDC clock is not available.

#### 11.1.4.7 Stop (STOP)

In stop mode the FLL is disabled and the internal or external reference clocks can be selected to be enabled or disabled. The BDC clock is not available and the ICS does not provide an MCU clock source.

## 11.2 External Signal Description

There are no ICS signals that connect off chip.

## 11.3 Register Definition

Figure 11-1 is a summary of ICS registers.

**Table 11-1. ICS Register Summary**

| Name | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| ICSC1 | R | CLKS | | RDIV | | | IREFS | IRCLKEN | IREFSTEN |
| | W | | | | | | | | |
| ICSC2 | R | BDIV | | RANGE | HGO | LP | EREFS | ERCLKEN | EREFSTEN |
| | W | | | | | | | | |
| ICSTRM | R | TRIM | | | | | | | |
| | W | | | | | | | | |
| ICSSC | R | 0 | 0 | 0 | IREFST | CLKST | | OSCINIT | FTRIM |
| | W | | | | | | | | |

## 11.3.1 ICS Control Register 1 (ICSC1)

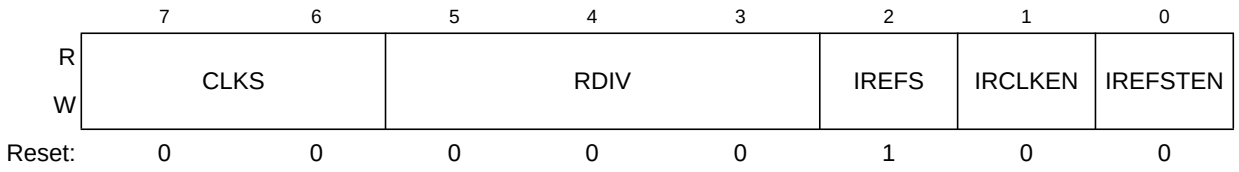



**Figure 11-3. ICS Control Register 1 (ICSC1)**

**Table 11-2. ICS Control Register 1 Field Descriptions**

| Field | Description |
|---|---|
| 7:6<br>CLKS | **Clock Source Select** — Selects the clock source that controls the bus frequency. The actual bus frequency depends on the value of the BDIV bits.<br>00 Output of FLL is selected.<br>01 Internal reference clock is selected.<br>10 External reference clock is selected.<br>11 Reserved, defaults to 00. |
| 5:3<br>RDIV | **Reference Divider** — Selects the amount to divide down the FLL reference clock selected by the IREFS bits. Resulting frequency must be in the range 31.25 kHz to 39.0625 kHz.<br>000 Encoding 0 — Divides reference clock by 1 (reset default)<br>001 Encoding 1 — Divides reference clock by 2<br>010 Encoding 2 — Divides reference clock by 4<br>011 Encoding 3 — Divides reference clock by 8<br>100 Encoding 4 — Divides reference clock by 16<br>101 Encoding 5 — Divides reference clock by 32<br>110 Encoding 6 — Divides reference clock by 64<br>111 Encoding 7 — Divides reference clock by 128 |
| 2<br>IREFS | **Internal Reference Select** — The IREFS bit selects the reference clock source for the FLL.<br>1 Internal reference clock selected<br>0 External reference clock selected |
| 1<br>IRCLKEN | **Internal Reference Clock Enable** — The IRCLKEN bit enables the internal reference clock for use as ICSIRCLK.<br>1 ICSIRCLK active<br>0 ICSIRCLK inactive |
| 0<br>IREFSTEN | **Internal Reference Stop Enable** — The IREFSTEN bit controls whether or not the internal reference clock remains enabled when the ICS enters stop mode.<br>1 Internal reference clock stays enabled in stop if IRCLKEN is set or if ICS is in FEI, FBI, or FBILP mode before entering stop<br>0 Internal reference clock is disabled in stop |

## 11.3.2 ICS Control Register 2 (ICSC2)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | BDIV | | RANGE | HGO | LP | EREFS | ERCLKEN | EREFSTEN |
| Reset: | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 11-4. ICS Control Register 2 (ICSC2)**

**Table 11-3. ICS Control Register 2 Field Descriptions**

| Field | Description |
|---|---|
| 7:6<br>BDIV | **Bus Frequency Divider** — Selects the amount to divide down the clock source selected by the CLKS bits. This controls the bus frequency.<br>00 Encoding 0 — Divides selected clock by 1<br>01 Encoding 1 — Divides selected clock by 2 (reset default)<br>10 Encoding 2 — Divides selected clock by 4<br>11 Encoding 3 — Divides selected clock by 8 |
| 5<br>RANGE | **Frequency Range Select** — Selects the frequency range for the external oscillator.<br>1 High frequency range selected for the external oscillator<br>0 Low frequency range selected for the external oscillator |
| 4<br>HGO | **High Gain Oscillator Select** — The HGO bit controls the external oscillator mode of operation.<br>1 Configure external oscillator for high gain operation<br>0 Configure external oscillator for low power operation |
| 3<br>LP | **Low Power Select** — The LP bit controls whether the FLL is disabled in FLL bypassed modes.<br>1 FLL is disabled in bypass modes unless BDM is active<br>0 FLL is not disabled in bypass mode |
| 2<br>EREFS | **External Reference Select** — The EREFS bit selects the source for the external reference clock.<br>1 Oscillator requested<br>0 External Clock Source requested |
| 1<br>ERCLKEN | **External Reference Enable** — The ERCLKEN bit enables the external reference clock for use as ICSERCLK.<br>1 ICSERCLK active<br>0 ICSERCLK inactive |
| 0<br>EREFSTEN | **External Reference Stop Enable** — The EREFSTEN bit controls whether or not the external reference clock remains enabled when the ICS enters stop mode.<br>1 External reference clock stays enabled in stop if ERCLKEN is set or if ICS is in FEE, FBE, or FBELP mode before entering stop<br>0 External reference clock is disabled in stop |

## 11.3.3 ICS Trim Register (ICSTRM)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | TRIM | | | | | | | |
| POR: | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset: | U | U | U | U | U | U | U | U |

**Figure 11-5. ICS Trim Register (ICSTRM)**

**Table 11-4. ICS Trim Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>TRIM | **ICS Trim Setting** — The TRIM bits control the internal reference clock frequency by controlling the internal reference clock period. The bits' effect are binary weighted (i.e., bit 1 will adjust twice as much as bit 0). Increasing the binary value in TRIM will increase the period, and decreasing the value will decrease the period.<br><br>An additional fine trim bit is available in ICSSC as the FTRIM bit. |

## 11.3.4 ICS Status and Control (ICSSC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | IREFST | CLKST | | OSCINIT | FTRIM |
| W | | | | | | | | |
| POR: | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Reset: | 0 | 0 | 0 | 1 | 0 | 0 | 0 | U |

**Figure 11-6. ICS Status and Control Register (ICSSC)**

**Table 11-5. ICS Status and Control Register Field Descriptions**

| Field | Description |
|---|---|
| 7:5 | Reserved, should be cleared. |
| 4<br>IREFST | **Internal Reference Status** — The IREFST bit indicates the current source for the reference clock. The IREFST bit does not update immediately after a write to the IREFS bit due to internal synchronization between clock domains.<br>0 Source of reference clock is external clock.<br>1 Source of reference clock is internal clock. |
| 3-2<br>CLKST | **Clock Mode Status** — The CLKST bits indicate the current clock mode. The CLKST bits don't update immediately after a write to the CLKS bits due to internal synchronization between clock domains.<br>00 Output of FLL is selected.<br>01 FLL Bypassed, Internal reference clock is selected.<br>10 FLL Bypassed, External reference clock is selected.<br>11 Reserved. |

**Table 11-5. ICS Status and Control Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1 | **OSC Initialization** — If the external reference clock is selected by ERCLKEN or by the ICS being in FEE, FBE, or FBELP mode, and if EREFS is set, then this bit is set after the initialization cycles of the external oscillator clock have completed. This bit is only cleared when either ERCLKEN or EREFS are cleared. |
| 0 | **ICS Fine Trim** — The FTRIM bit controls the smallest adjustment of the internal reference clock frequency. Setting FTRIM will increase the period and clearing FTRIM will decrease the period by the smallest amount possible. |

## 11.4 Functional Description

### 11.4.1 Operational Modes

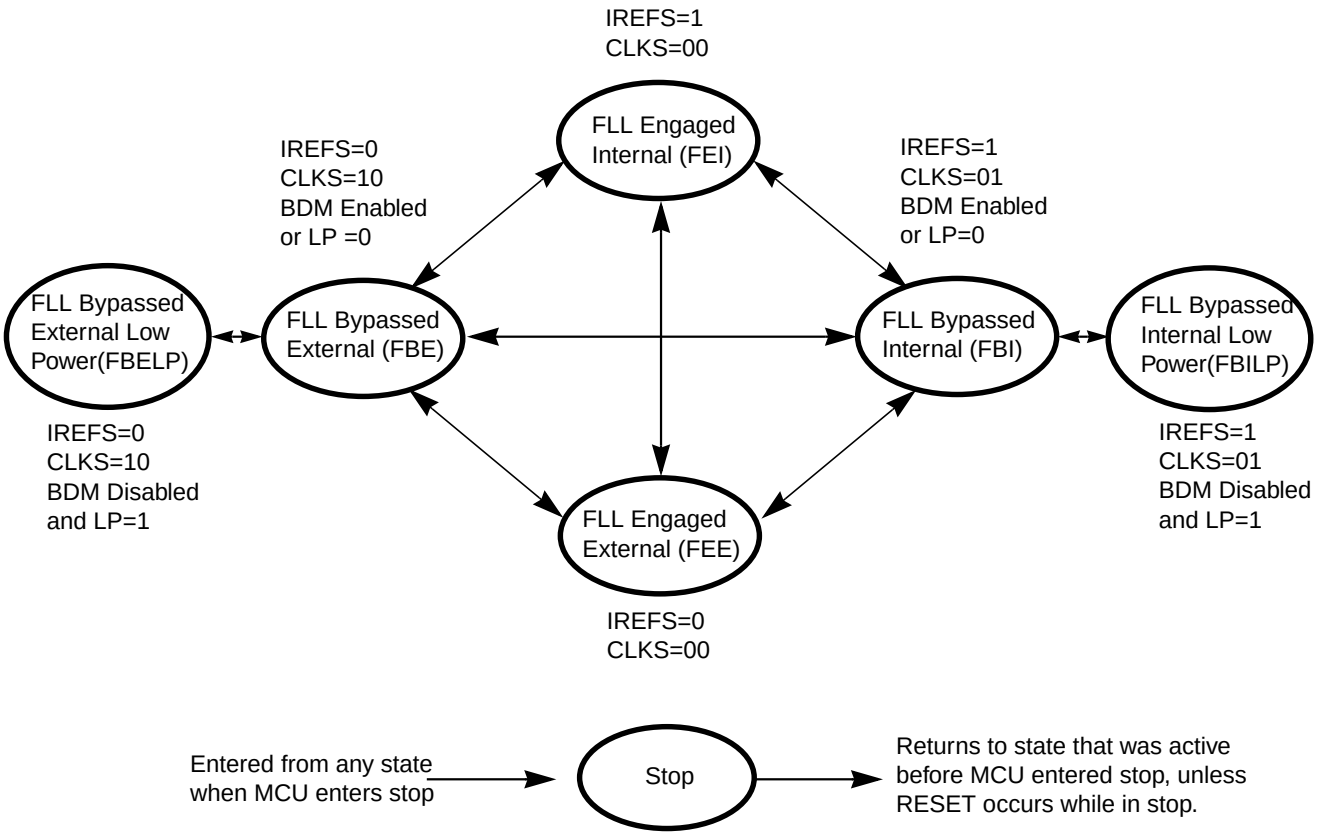



**Figure 11-7. Clock Switching Modes**

The seven states of the ICS are shown as a state diagram and are described below. The arrows indicate the allowed movements between the states.

#### 11.4.1.1 FLL Engaged Internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

#### 11.4.1.2 FLL Engaged External (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock.The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

#### 11.4.1.3 FLL Bypassed Internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is active or LP bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

#### 11.4.1.4 FLL Bypassed Internal Low Power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is not active and LP bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

#### 11.4.1.5 FLL Bypassed External (FBE)

The FLL bypassed external (FBE) mode is entered when all the following conditions occur:

- CLKS bits are written to 10.
- IREFS bit is written to 0.
- BDM mode is active or LP bit is written to 0.

In FLL bypassed external mode, the ICSOUT clock is derived from the external reference clock. The FLL clock is controlled by the external reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits, so that the ICSLCLK will be available for BDC communications, and the external reference clock is enabled.

#### 11.4.1.6 FLL Bypassed External Low Power (FBELP)

The FLL bypassed external low power (FBELP) mode is entered when all the following conditions occur:

- CLKS bits are written to 10.
- IREFS bit is written to 0.
- BDM mode is not active and LP bit is written to 1.

In FLL bypassed external low power mode, the ICSOUT clock is derived from the external reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications. The external reference clock is enabled.

#### 11.4.1.7 Stop

Stop mode is entered whenever the MCU enters a STOP state. In this mode, all ICS clock signals are static except in the following cases:

ICSIRCLK will be active in stop mode when all the following conditions occur:

- IRCLKEN bit is written to 1
- IREFSTEN bit is written to 1

ICSERCLK will be active in stop mode when all the following conditions occur:

- ERCLKEN bit is written to 1
- EREFSTEN bit is written to 1

### 11.4.2 Mode Switching

When switching between FLL engaged internal (FEI) and FLL engaged external (FEE) modes the IREFS bit can be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. After a change in the IREFS value the FLL will begin locking again after a few full cycles of the resulting divided reference frequency. The completion of the switch is shown by the IREFST bit.

The CLKS bits can also be changed at anytime, but the RDIV bits must be changed simultaneously so that the resulting frequency stays in the range of 31.25 kHz to 39.0625 kHz. The actual switch to the newly selected clock will not occur until after a few full cycles of the new clock. If the newly selected clock is not available, the previous clock will remain selected.

### 11.4.3 Bus Frequency Divider

The BDIV bits can be changed at anytime and the actual switch to the new frequency will occur immediately.

### 11.4.4 Low Power Bit Usage

The low power bit (LP) is provided to allow the FLL to be disabled and thus conserve power when it is not being used. However, in some applications it may be desirable to enable the FLL and allow it to lock for maximum accuracy before switching to an FLL engaged mode. Do this by writing the LP bit to 0.

### 11.4.5 Internal Reference Clock

When IRCLKEN is set the internal reference clock signal will be presented as ICSIRCLK, which can be used as an additional clock source. The ICSIRCLK frequency can be re-targeted by trimming the period of the internal reference clock. This can be done by writing a new value to the TRIM bits in the ICSTRM register. Writing a larger value will slow down the ICSIRCLK frequency, and writing a smaller value to the ICSTRM register will speed up the ICSIRCLK frequency. The TRIM bits will effect the ICSOUT frequency if the ICS is in FLL engaged internal (FEI), FLL bypassed internal (FBI), or FLL bypassed internal low power (FBILP) mode. The TRIM and FTRIM value will not be affected by a reset.

Until ICSIRCLK is trimmed, programming low reference divider (RDIV) factors may result in ICSOUT frequencies that exceed the maximum chip-level frequency and violate the chip-level clock timing specifications (see the Device Overview chapter).

If IREFSTEN is set and the IRCLKEN bit is written to 1, the internal reference clock will keep running during stop mode in order to provide a fast recovery upon exiting stop.

All MCU devices are factory programmed with a trim value in a reserved memory location (NVTRIM:NVFTRIM). This value can be copied to the ICSTRM register during reset initialization. The factory trim value includes the FTRIM bit. For finer precision, the user can trim the internal oscillator in the application to take in account small differences between the factory test setup and actual application conditions.

### 11.4.6 Optional External Reference Clock

The ICS module can support an external reference clock with frequencies between 31.25 kHz to 5 MHz in all modes. When the ERCLKEN is set, the external reference clock signal will be presented as ICSERCLK, which can be used as an additional clock source. When IREFS = 1, the external reference clock will not be used by the FLL and will only be used as ICSERCLK. In these modes, the frequency can be equal to the maximum frequency the chip-level timing specifications will support (see the Device Overview chapter).

If EREFSTEN is set and the ERCLKEN bit is written to 1, the external reference clock will keep running during stop mode in order to provide a fast recovery upon exiting stop.

### 11.4.7 Fixed Frequency Clock

The ICS presents the divided FLL reference clock as ICSFFCLK for use as an additional clock source for peripheral modules. The ICS provides an output signal (ICSFFE) which indicates when the ICS is providing ICSOUT frequencies four times or greater than the divided FLL reference clock (ICSFFCLK). In FLL Engaged mode (FEI and FEE) this is always true and ICSFFE is always high. In ICS Bypass modes, ICSFFE will get asserted for the following combinations of BDIV and RDIV values:

- BDIV=00 (divide by 1), RDIV ≥ 010
- BDIV=01 (divide by 2), RDIV ≥ 011
- BDIV=10 (divide by 4), RDIV ≥ 100
- BDIV=11 (divide by 8), RDIV ≥ 101

# Chapter 12
# Modulo Timer (S08MTIMV1)

## 12.1 Introduction

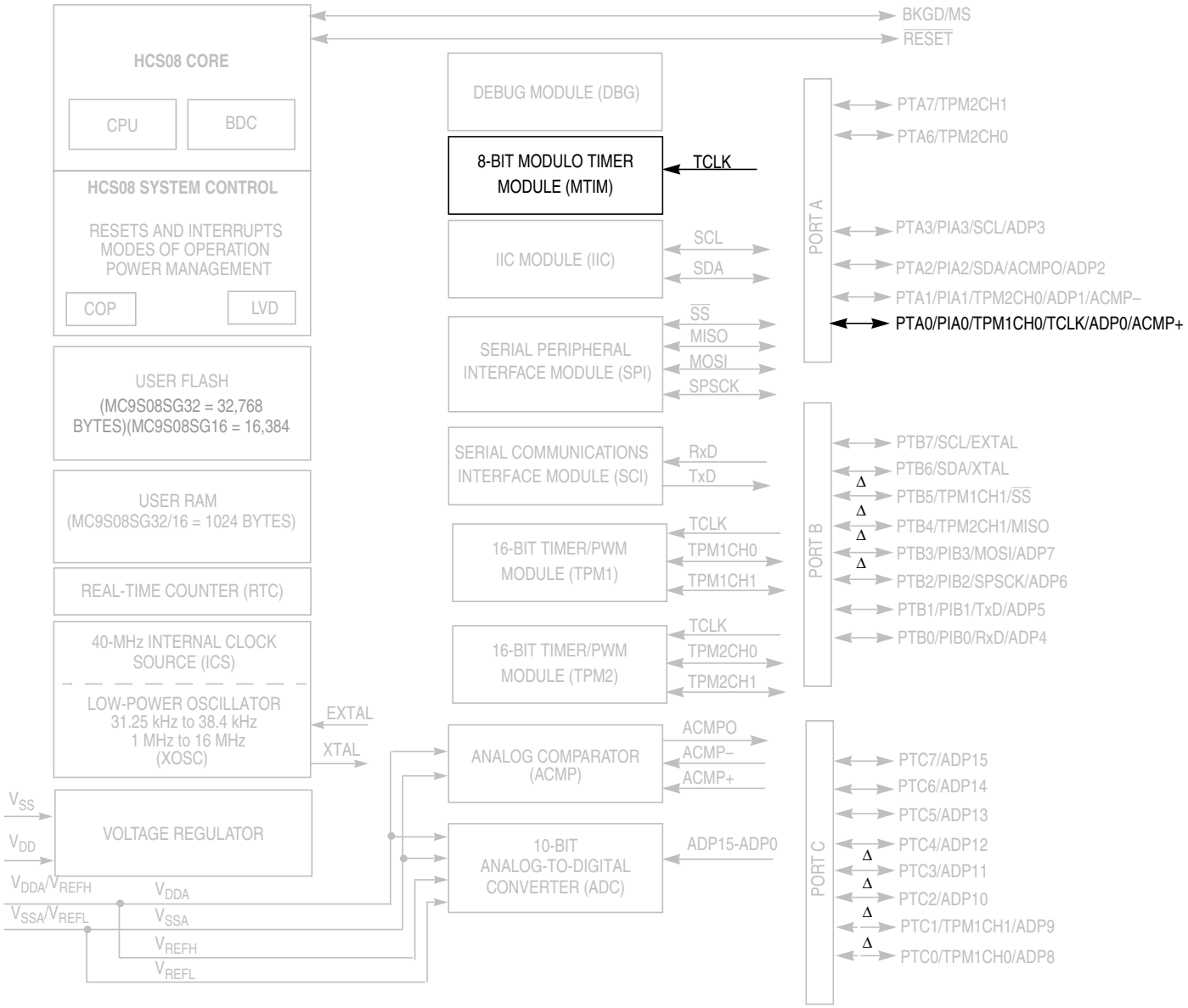
The MTIM is a simple 8-bit timer with several software selectable clock sources and a programmable interrupt.

The central component of the MTIM is the 8-bit counter, which can operate as a free-running counter or a modulo counter. A timer overflow interrupt can be enabled to generate periodic interrupts for time-based software loops.

Figure 12-1 shows the MC9S08SG32 Series block diagram with the MTIM highlighted.

### 12.1.1 MTIM Configuration Information

The external clock for the MTIM module, TCLK, is selected by setting CLKS = 1:1 or 1:0 in MTIMCLK, which selects the TCLK pin input. The TCLK input can be enabled as external clock inputs to both the MTIM and TPM modules simultaneously.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 12-1. MC9S08SG32 Series Block Diagram Highlighting MTIM Block and Pins**

### 12.1.2 Features

Timer system features include:

- 8-bit up-counter
  - — Free-running or 8-bit modulo limit
  - — Software controllable interrupt on overflow
  - — Counter reset bit (TRST)
  - — Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - — System bus clock — rising edge
  - — Fixed frequency clock (XCLK) — rising edge
  - — External clock source on the TCLK pin — rising edge
  - — External clock source on the TCLK pin — falling edge
- Nine selectable clock prescale values:
  - — Clock source divide by 1, 2, 4, 8, 16, 32, 64, 128, or 256

### 12.1.3 Modes of Operation

This section defines the MTIM's operation in stop, wait and background debug modes.

#### 12.1.3.1 MTIM in Wait Mode

The MTIM continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the MTIM can be used to bring the MCU out of wait mode if the timer overflow interrupt is enabled. For lowest possible current consumption, the MTIM should be stopped by software if not needed as an interrupt source during wait mode.

#### 12.1.3.2 MTIM in Stop Modes

The MTIM is disabled in all stop modes, regardless of the settings before executing the STOP instruction. Therefore, the MTIM cannot be used as a wake up source from stop modes.

Waking from stop2 mode, the MTIM will be put into its reset state. If stop3 is exited with a reset, the MTIM will be put into its reset state. If stop3 is exited with an interrupt, the MTIM continues from the state it was in when stop3 was entered. If the counter was active upon entering stop3, the count will resume from the current value.

#### 12.1.3.3 MTIM in Active Background Mode

The MTIM suspends all counting until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as an MTIM reset did not occur (TRST written to a 1 or MTIMMOD written).

### 12.1.4 Block Diagram

The block diagram for the modulo timer module is shown Figure 12-2.

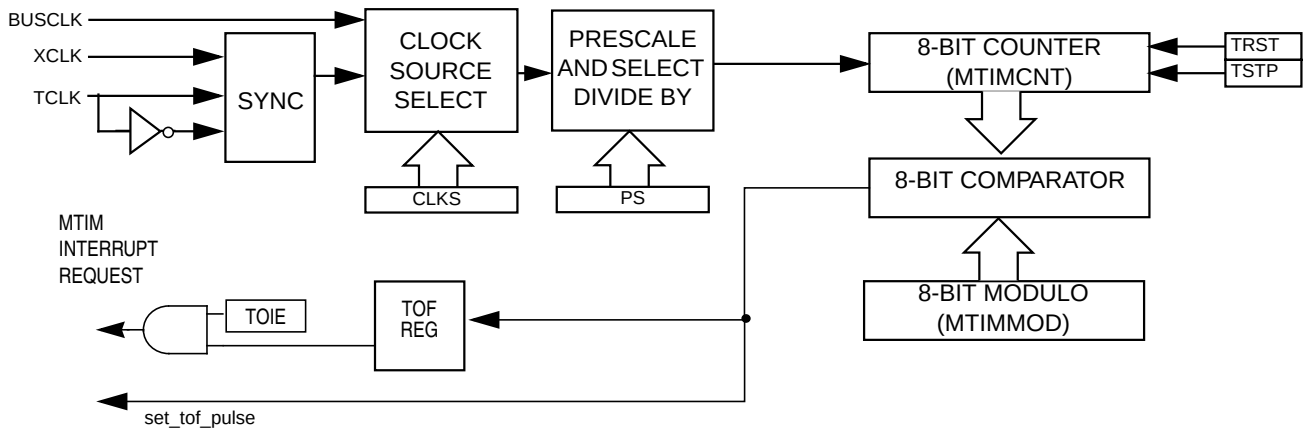



**Figure 12-2. Modulo Timer (MTIM) Block Diagram**

## 12.2 External Signal Description

The MTIM includes one external signal, TCLK, used to input an external clock when selected as the MTIM clock source. The signal properties of TCLK are shown in Table 12-1.

**Table 12-1. Signal Properties**

| Signal | Function | I/O |
|---|---|---|
| TCLK | External clock source input into MTIM | I |

The TCLK input must be synchronized by the bus clock. Also, variations in duty cycle and clock jitter must be accommodated. Therefore, the TCLK signal must be limited to one-fourth of the bus frequency.

The TCLK pin can be muxed with a general-purpose port pin. See the Pins and Connections chapter for the pin location and priority of this function.

## 12.3 Register Definition

Figure 12-3 is a summary of MTIM registers.

| Name | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| MTIMSC | R | TOF | TOIE | 0 | TSTP | 0 | 0 | 0 | 0 |
| | W | | | TRST | | | | | |
| MTIMCLK | R | 0 | 0 | CLKS | | PS | | | |
| | W | | | | | | | | |
| MTIMCNT | R | COUNT | | | | | | | |
| | W | | | | | | | | |
| MTIMMOD | R | MOD | | | | | | | |
| | W | | | | | | | | |

**Figure 12-3. MTIM Register Summary**

Each MTIM includes four registers:

- An 8-bit status and control register
- An 8-bit clock configuration register
- An 8-bit counter register
- An 8-bit modulo register

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all MTIM registers.This section refers to registers and control bits only by their names and relative address offsets.

Some MCUs may have more than one MTIM, so register names include placeholder characters to identify which MTIM is being referenced.

## 12.3.1 MTIM Status and Control Register (MTIMSC)

MTIMSC contains the overflow status flag and control bits which are used to configure the interrupt enable, reset the counter, and stop the counter.

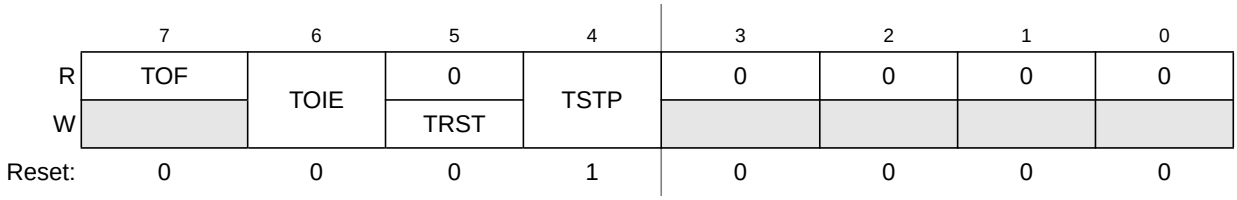



**Figure 12-4. MTIM Status and Control Register**

**Table 12-2. MTIM Status and Control Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TOF | **MTIM Overflow Flag** — This read-only bit is set when the MTIM counter register overflows to $00 after reaching the value in the MTIM modulo register. Clear TOF by reading the MTIMSC register while TOF is set, then writing a 0 to TOF. TOF is also cleared when TRST is written to a 1 or when any value is written to the MTIMMOD register.<br>0 MTIM counter has not reached the overflow value in the MTIM modulo register.<br>1 MTIM counter has reached the overflow value in the MTIM modulo register. |
| 6<br>TOIE | **MTIM Overflow Interrupt Enable** — This read/write bit enables MTIM overflow interrupts. If TOIE is set, then an interrupt is generated when TOF = 1. Reset clears TOIE. Do not set TOIE if TOF = 1. Clear TOF first, then set TOIE.<br>0 TOF interrupts are disabled. Use software polling.<br>1 TOF interrupts are enabled. |
| 5<br>TRST | **MTIM Counter Reset** — When a 1 is written to this write-only bit, the MTIM counter register resets to $00 and TOF is cleared. Reading this bit always returns 0.<br>0 No effect. MTIM counter remains at current state.<br>1 MTIM counter is reset to $00. |
| 4<br>TSTP | **MTIM Counter Stop** — When set, this read/write bit stops the MTIM counter at its current value. Counting resumes from the current value when TSTP is cleared. Reset sets TSTP to prevent the MTIM from counting.<br>0 MTIM counter is active.<br>1 MTIM counter is stopped. |
| 3:0 | Unused register bits, always read 0. |

## 12.3.2 MTIM Clock Configuration Register (MTIMCLK)

MTIMCLK contains the clock select bits (CLKS) and the prescaler select bits (PS).

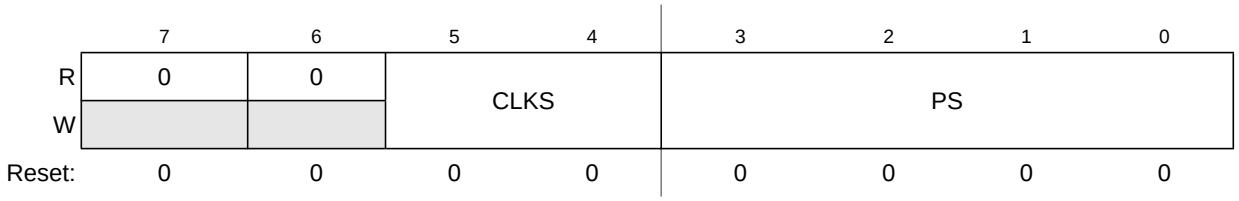



**Figure 12-5. MTIM Clock Configuration Register**

**Table 12-3. MTIM Clock Configuration Register Field Description**

| Field | Description |
|---|---|
| 7:6 | Unused register bits, always read 0. |
| 5:4<br>CLKS | **Clock Source Select** — These two read/write bits select one of four different clock sources as the input to the MTIM prescaler. Changing the clock source while the counter is active does not clear the counter. The count continues with the new clock source. Reset clears CLKS to 000.<br>00 Encoding 0. Bus clock (BUSCLK)<br>01 Encoding 1. Fixed-frequency clock (XCLK)<br>10 Encoding 3. External source (TCLK pin), falling edge<br>11 Encoding 4. External source (TCLK pin), rising edge<br>All other encodings default to the bus clock (BUSCLK). |
| 3:0<br>PS | **Clock Source Prescaler** — These four read/write bits select one of nine outputs from the 8-bit prescaler. Changing the prescaler value while the counter is active does not clear the counter. The count continues with the new prescaler value. Reset clears PS to 0000.<br>0000 Encoding 0. MTIM clock source ÷ 1<br>0001 Encoding 1. MTIM clock source ÷ 2<br>0010 Encoding 2. MTIM clock source ÷ 4<br>0011 Encoding 3. MTIM clock source ÷ 8<br>0100 Encoding 4. MTIM clock source ÷ 16<br>0101 Encoding 5. MTIM clock source ÷ 32<br>0110 Encoding 6. MTIM clock source ÷ 64<br>0111 Encoding 7. MTIM clock source ÷ 128<br>1000 Encoding 8. MTIM clock source ÷ 256<br>All other encodings default to MTIM clock source ÷ 256. |

### 12.3.3 MTIM Counter Register (MTIMCNT)

MTIMCNT is the read-only value of the current MTIM count of the 8-bit counter.

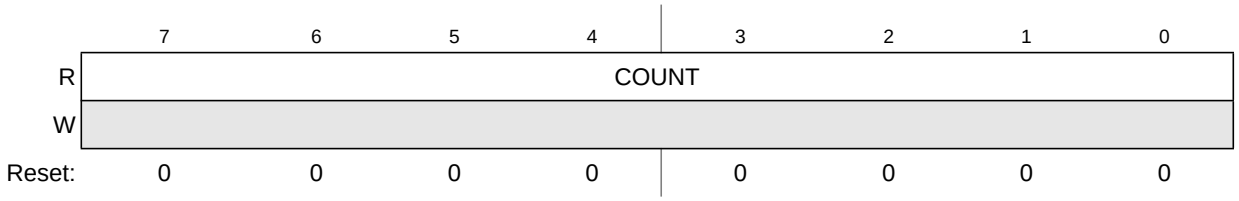



**Figure 12-6. MTIM Counter Register**

**Table 12-4. MTIM Counter Register Field Description**

| Field | Description |
|---|---|
| 7:0<br>COUNT | **MTIM Count** — These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset clears the count to $00. |

### 12.3.4 MTIM Modulo Register (MTIMMOD)

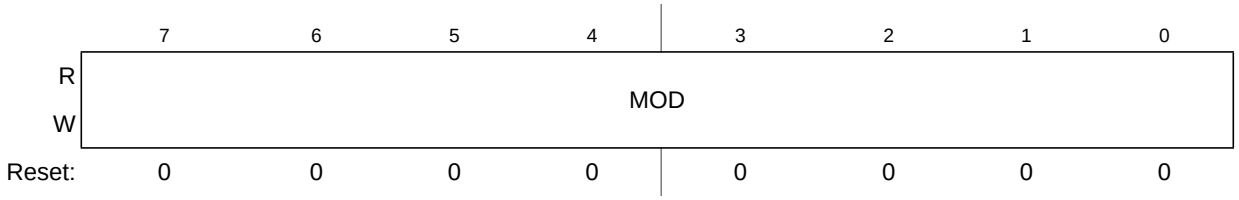



**Figure 12-7. MTIM Modulo Register**

**Table 12-5. MTIM Modulo Register Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>MOD | **MTIM Modulo** — These eight read/write bits contain the modulo value used to reset the count and set TOF. A value of $00 puts the MTIM in free-running mode. Writing to MTIMMOD resets the COUNT to $00 and clears TOF. Reset sets the modulo to $00. |

## 12.4 Functional Description

The MTIM is composed of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with nine selectable values. The module also contains software selectable interrupt logic.

The MTIM counter (MTIMCNT) has three modes of operation: stopped, free-running, and modulo. Out of reset, the counter is stopped. If the counter is started without writing a new value to the modulo register, then the counter will be in free-running mode. The counter is in modulo mode when a value other than $00 is in the modulo register while the counter is running.

After any MCU reset, the counter is stopped and reset to $00, and the modulus is set to $00. The bus clock is selected as the default clock source and the prescale value is divide by 1. To start the MTIM in free-running mode, simply write to the MTIM status and control register (MTIMSC) and clear the MTIM stop bit (TSTP).

Four clock sources are software selectable: the internal bus clock, the fixed frequency clock (XCLK), and an external clock on the TCLK pin, selectable as incrementing on either rising or falling edges. The MTIM clock select bits (CLKS1:CLKS0) in MTIMSC are used to select the desired clock source. If the counter is active (TSTP = 0) when a new clock source is selected, the counter will continue counting from the previous value using the new clock source.

Nine prescale values are software selectable: clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256. The prescaler select bits (PS[3:0]) in MTIMSC select the desired prescale value. If the counter is active (TSTP = 0) when a new prescaler value is selected, the counter will continue counting from the previous value using the new prescaler value.

The MTIM modulo register (MTIMMOD) allows the overflow compare value to be set to any value from $01 to $FF. Reset clears the modulo value to $00, which results in a free running counter.

When the counter is active (TSTP = 0), the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter overflows to $00 and continues counting. The MTIM overflow flag (TOF) is set whenever the counter overflows. The flag sets on the transition from the modulo value to $00. Writing to MTIMMOD while the counter is active resets the counter to $00 and clears TOF.

Clearing TOF is a two-step process. The first step is to read the MTIMSC register while TOF is set. The second step is to write a 0 to TOF. If another overflow occurs between the first and second steps, the clearing process is reset and TOF will remain set after the second step is performed. This will prevent the second occurrence from being missed. TOF is also cleared when a 1 is written to TRST or when any value is written to the MTIMMOD register.

The MTIM allows for an optional interrupt to be generated whenever TOF is set. To enable the MTIM overflow interrupt, set the MTIM overflow interrupt enable bit (TOIE) in MTIMSC. TOIE should never be written to a 1 while TOF = 1. Instead, TOF should be cleared first, then the TOIE can be set to 1.

### 12.4.1 MTIM Operation Example

This section shows an example of the MTIM operation as the counter reaches a matching value from the modulo register.

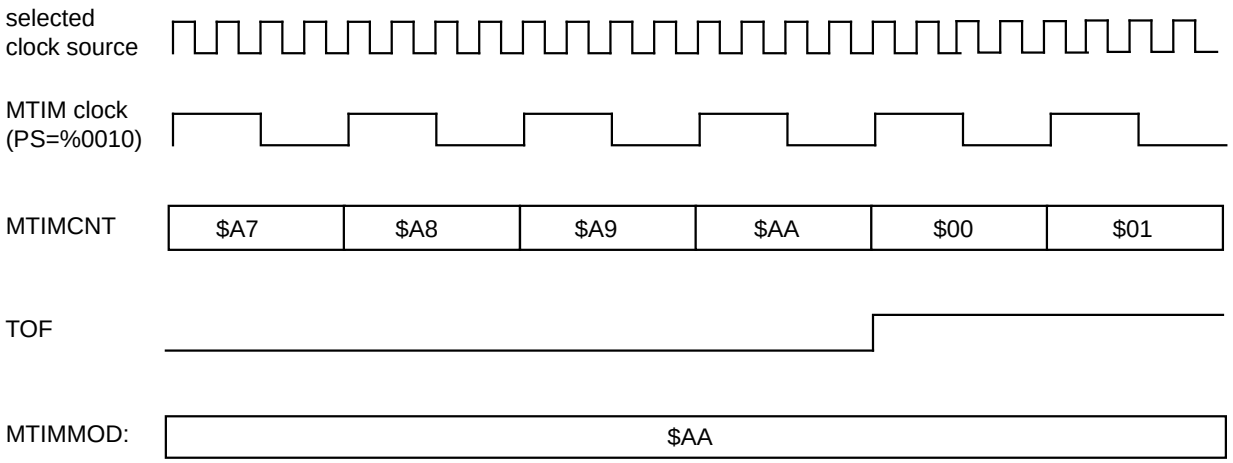



**Figure 12-8. MTIM counter overflow example**

In the example of Figure 12-8, the selected clock source could be any of the five possible choices. The prescaler is set to PS = %0010 or divide-by-4. The modulo value in the MTIMMOD register is set to $AA. When the counter, MTIMCNT, reaches the modulo value of $AA, the counter overflows to $00 and continues counting. The timer overflow flag, TOF, sets when the counter value changes from $AA to $00. An MTIM overflow interrupt is generated when TOF is set, if TOIE = 1.

# Chapter 13
# Real-Time Counter (S08RTCV1)

## 13.1 Introduction

The RTC module consists of one 8-bit counter, one 8-bit comparator, several binary-based and decimal-based prescaler dividers, two clock sources, and one programmable periodic interrupt. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wake up from low power modes without the need of external components.

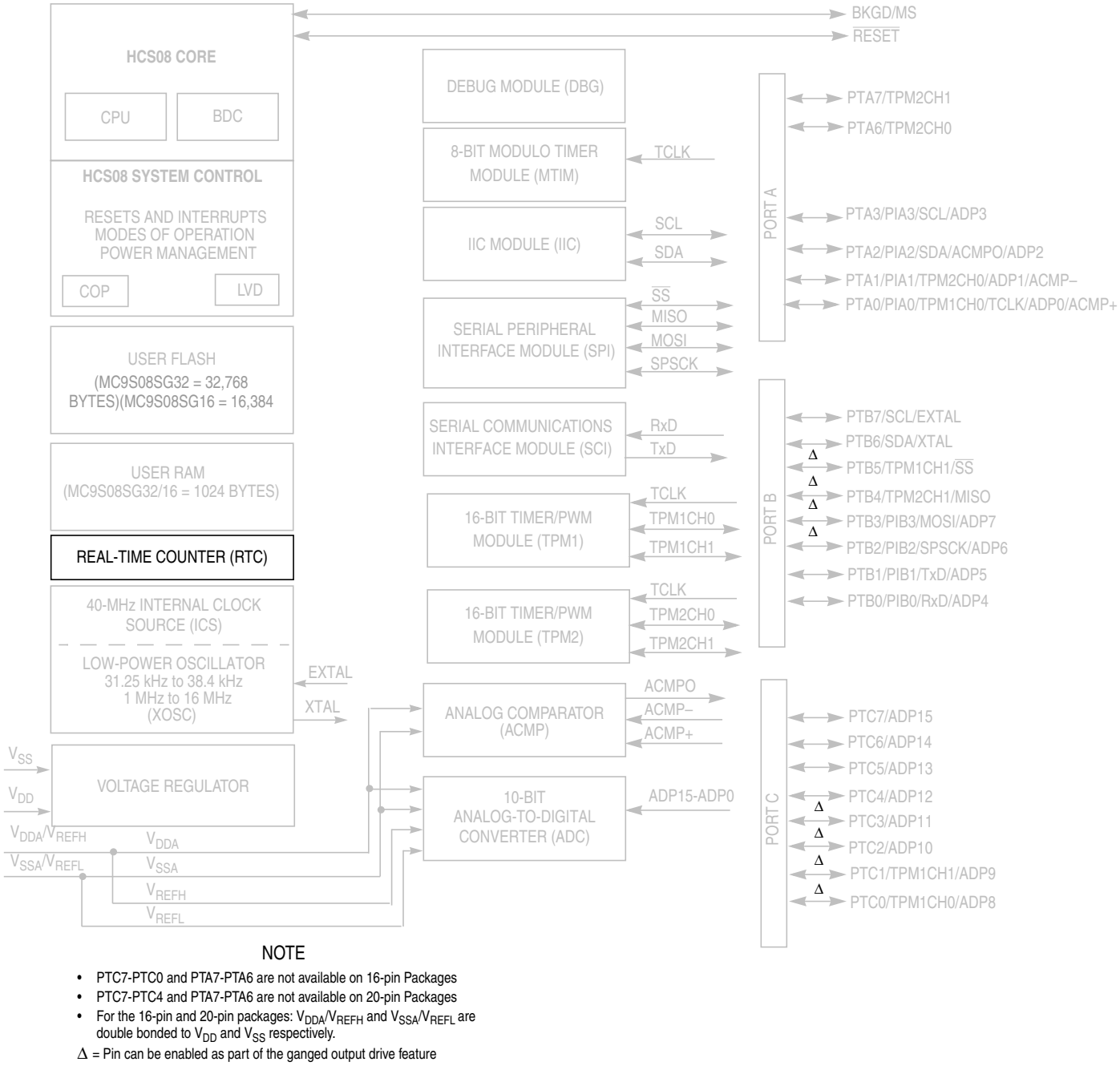



**Figure 13-1. MC9S08SG32 Series Block Diagram Highlighting RTC Block and Pins**

### 13.1.1 Features

Features of the RTC module include:

- 8-bit up-counter
  - 8-bit modulo match limit
  - Software controllable periodic interrupt on match
- Three software selectable clock sources for input to prescaler with selectable binary-based and decimal-based divider values
  - 1-kHz internal low-power oscillator (LPO)
  - External clock (ERCLK)
  - 32-kHz internal clock (IRCLK)

### 13.1.2 Modes of Operation

This section defines the operation in stop, wait and background debug modes.

#### 13.1.2.1 Wait Mode

The RTC continues to run in wait mode if enabled before executing the appropriate instruction. Therefore, the RTC can bring the MCU out of wait mode if the real-time interrupt is enabled. For lowest possible current consumption, the RTC should be stopped by software if not needed as an interrupt source during wait mode.

#### 13.1.2.2 Stop Modes

The RTC continues to run in stop2 or stop3 mode if the RTC is enabled before executing the STOP instruction. Therefore, the RTC can bring the MCU out of stop modes with no external components, if the real-time interrupt is enabled.

The LPO clock can be used in stop2 and stop3 modes. ERCLK and IRCLK clocks are only available in stop3 mode.

Power consumption is lower when all clock sources are disabled, but in that case, the real-time interrupt cannot wake up the MCU from stop modes.

#### 13.1.2.3 Active Background Mode

The RTC suspends all counting during active background mode until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as the RTCMOD register is not written and the RTCPS and RTCLKS bits are not altered.

### 13.1.3 Block Diagram

The block diagram for the RTC module is shown in Figure 13-2.

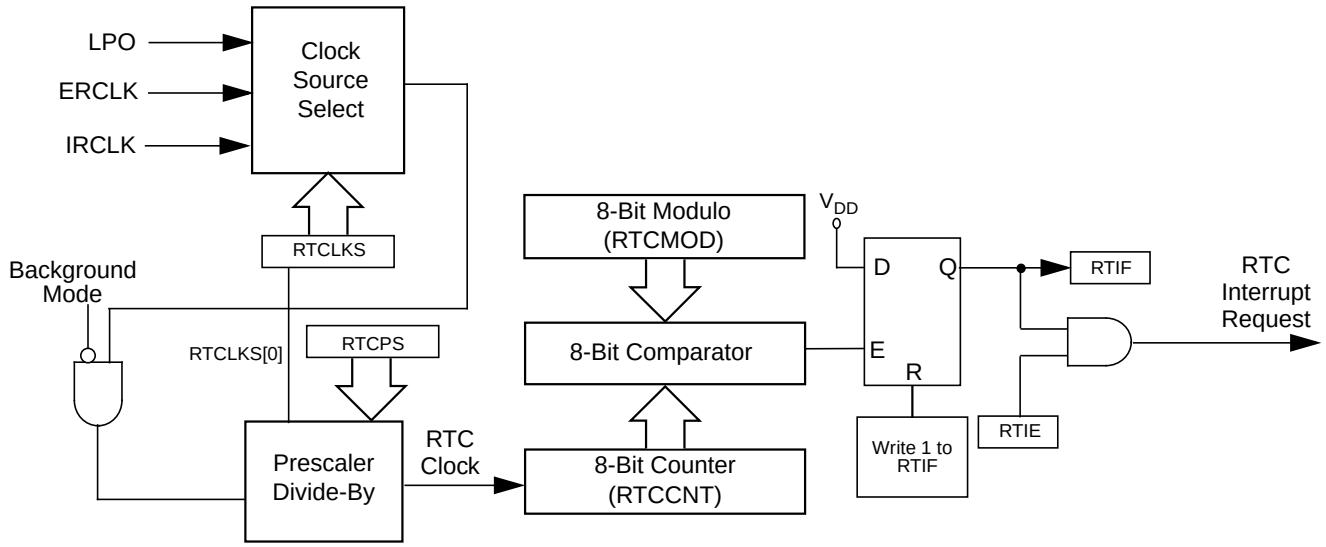



**Figure 13-2. Real-Time Counter (RTC) Block Diagram**

## 13.2 External Signal Description

The RTC does not include any off-chip signals.

## 13.3 Register Definition

The RTC includes a status and control register, an 8-bit counter register, and an 8-bit modulo register.

Refer to the direct-page register summary in the memory section of this document for the absolute address assignments for all RTC registers.This section refers to registers and control bits only by their names and relative address offsets.

Table 13-1 is a summary of RTC registers.

**Table 13-1. RTC Register Summary**

| Name | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| RTCSC | R | RTIF | RTCLKS | | RTIE | RTCPS | | | |
| | W | | | | | | | | |
| RTCCNT | R | RTCCNT | | | | | | | |
| | W | | | | | | | | |
| RTCMOD | R | RTCMOD | | | | | | | |
| | W | | | | | | | | |

### 13.3.1 RTC Status and Control Register (RTCSC)

RTCSC contains the real-time interrupt status flag (RTIF), the clock select bits (RTCLKS), the real-time interrupt enable bit (RTIE), and the prescaler select bits (RTCPS).

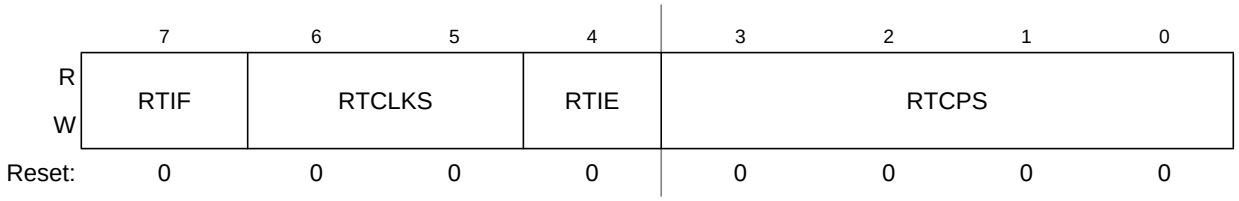



**Figure 13-3. RTC Status and Control Register (RTCSC)**

**Table 13-2. RTCSC Field Descriptions**

| Field | Description |
|---|---|
| 7<br>RTIF | Real-Time Interrupt Flag This status bit indicates the RTC counter register reached the value in the RTC modulo register. Writing a logic 0 has no effect. Writing a logic 1 clears the bit and the real-time interrupt request. Reset clears RTIF.<br>0 RTC counter has not reached the value in the RTC modulo register.<br>1 RTC counter has reached the value in the RTC modulo register. |
| 6–5<br>RTCLKS | Real-Time Clock Source Select. These two read/write bits select the clock source input to the RTC prescaler. Changing the clock source clears the prescaler and RTCCNT counters. When selecting a clock source, ensure that the clock source is properly enabled (if applicable) to ensure correct operation of the RTC. Reset clears RTCLKS.<br>00 Real-time clock source is the 1-kHz low power oscillator (LPO)<br>01 Real-time clock source is the external clock (ERCLK)<br>1x Real-time clock source is the internal clock (IRCLK) |
| 4<br>RTIE | Real-Time Interrupt Enable. This read/write bit enables real-time interrupts. If RTIE is set, then an interrupt is generated when RTIF is set. Reset clears RTIE.<br>0 Real-time interrupt requests are disabled. Use software polling.<br>1 Real-time interrupt requests are enabled. |
| 3–0<br>RTCPS | Real-Time Clock Prescaler Select. These four read/write bits select binary-based or decimal-based divide-by values for the clock source. See Table 13-3. Changing the prescaler value clears the prescaler and RTCCNT counters. Reset clears RTCPS. |

**Table 13-3. RTC Prescaler Divide-by values**

| RTCLKS[0] | RTCPS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| **0** | Off | $2^3$ | $2^5$ | $2^6$ | $2^7$ | $2^8$ | $2^9$ | $2^{10}$ | 1 | 2 | $2^2$ | 10 | $2^4$ | $10^2$ | $5x10^2$ | $10^3$ |
| **1** | Off | $2^{10}$ | $2^{11}$ | $2^{12}$ | $2^{13}$ | $2^{14}$ | $2^{15}$ | $2^{16}$ | $10^3$ | $2x10^3$ | $5x10^3$ | $10^4$ | $2x10^4$ | $5x10^4$ | $10^5$ | $2x10^5$ |

### 13.3.2 RTC Counter Register (RTCCNT)

RTCCNT is the read-only value of the current RTC count of the 8-bit counter.

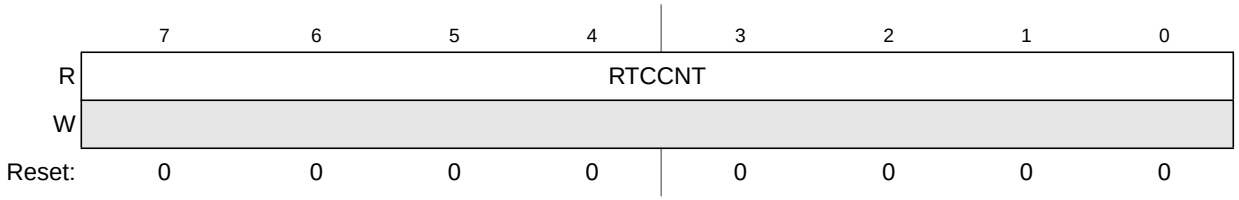



**Figure 13-4. RTC Counter Register (RTCCNT)**

**Table 13-4. RTCCNT Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>RTCCNT | RTC Count. These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset, writing to RTCMOD, or writing different values to RTCLKS and RTCPS clear the count to 0x00. |

### 13.3.3 RTC Modulo Register (RTCMOD)

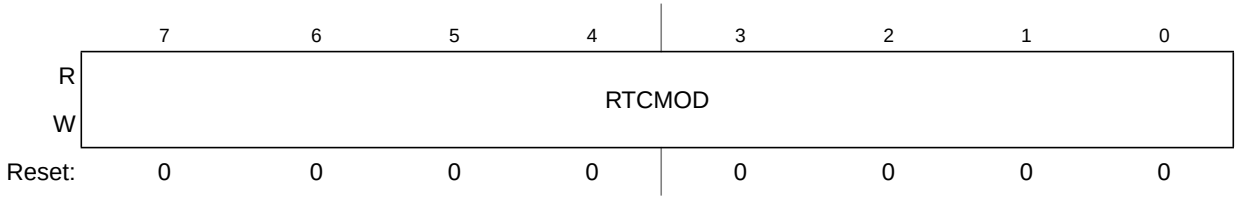



**Figure 13-5. RTC Modulo Register (RTCMOD)**

**Table 13-5. RTCMOD Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>RTCMOD | RTC Modulo. These eight read/write bits contain the modulo value used to reset the count to 0x00 upon a compare match and set the RTIF status bit. A value of 0x00 sets the RTIF bit on each rising edge of the prescaler output. Writing to RTCMOD resets the prescaler and the RTCCNT counters to 0x00. Reset sets the modulo to 0x00. |

## 13.4 Functional Description

The RTC is composed of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with binary-based and decimal-based selectable values. The module also contains software selectable interrupt logic.

After any MCU reset, the counter is stopped and reset to 0x00, the modulus register is set to 0x00, and the prescaler is off. The 1-kHz internal oscillator clock is selected as the default clock source. To start the prescaler, write any value other than zero to the prescaler select bits (RTCPS).

Three clock sources are software selectable: the low power oscillator clock (LPO), the external clock (ERCLK), and the internal clock (IRCLK). The RTC clock select bits (RTCLKS) select the desired clock source. If a different value is written to RTCLKS, the prescaler and RTCCNT counters are reset to 0x00.

RTCPS and the RTCLKS[0] bit select the desired divide-by value. If a different value is written to RTCPS, the prescaler and RTCCNT counters are reset to 0x00. Table 13-6 shows different prescaler period values.

**Table 13-6. Prescaler Period**

| RTCPS | 1-kHz Internal Clock (RTCLKS = 00) | 1-MHz External Clock (RTCLKS = 01) | 32-kHz Internal Clock (RTCLKS = 10) | 32-kHz Internal Clock (RTCLKS = 11) |
|---|---|---|---|---|
| 0000 | Off | Off | Off | Off |
| 0001 | 8 ms | 1.024 ms | 250 µs | 32 ms |
| 0010 | 32 ms | 2.048 ms | 1 ms | 64 ms |
| 0011 | 64 ms | 4.096 ms | 2 ms | 128 ms |
| 0100 | 128 ms | 8.192 ms | 4 ms | 256 ms |
| 0101 | 256 ms | 16.4 ms | 8 ms | 512 ms |
| 0110 | 512 ms | 32.8 ms | 16 ms | 1.024 s |
| 0111 | 1.024 s | 65.5 ms | 32 ms | 2.048 s |
| 1000 | 1 ms | 1 ms | 31.25 µs | 31.25 ms |
| 1001 | 2 ms | 2 ms | 62.5 µs | 62.5 ms |
| 1010 | 4 ms | 5 ms | 125 µs | 156.25 ms |
| 1011 | 10 ms | 10 ms | 312.5 µs | 312.5 ms |
| 1100 | 16 ms | 20 ms | 0.5 ms | 0.625 s |
| 1101 | 0.1 s | 50 ms | 3.125 ms | 1.5625 s |
| 1110 | 0.5 s | 0.1 s | 15.625 ms | 3.125 s |
| 1111 | 1 s | 0.2 s | 31.25 ms | 6.25 s |

The RTC modulo register (RTCMOD) allows the compare value to be set to any value from 0x00 to 0xFF. When the counter is active, the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter resets to 0x00 and continues counting. The real-time interrupt flag (RTIF) is set when a match occurs. The flag sets on the transition from the modulo value to 0x00. Writing to RTCMOD resets the prescaler and the RTCCNT counters to 0x00.

The RTC allows for an interrupt to be generated when RTIF is set. To enable the real-time interrupt, set the real-time interrupt enable bit (RTIE) in RTCSC. RTIF is cleared by writing a 1 to RTIF.

### 13.4.1 RTC Operation Example

This section shows an example of the RTC operation as the counter reaches a matching value from the modulo register.

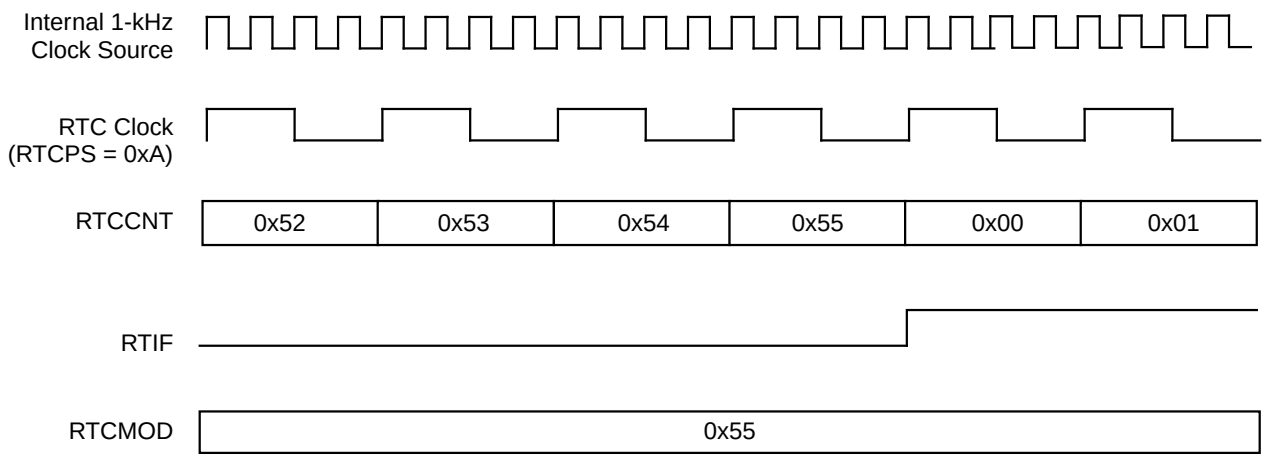



**Figure 13-6. RTC Counter Overflow Example**

In the example of Figure 13-6, the selected clock source is the 1-kHz internal oscillator clock source. The prescaler (RTCPS) is set to 0xA or divide-by-4. The modulo value in the RTCMOD register is set to 0x55. When the counter, RTCCNT, reaches the modulo value of 0x55, the counter overflows to 0x00 and continues counting. The real-time interrupt flag, RTIF, sets when the counter value changes from 0x55 to 0x00. A real-time interrupt is generated when RTIF is set, if RTIE is set.

## 13.5 Initialization/Application Information

This section provides example code to give some basic direction to a user on how to initialize and configure the RTC module. The example software is implemented in C language.

The example below shows how to implement time of day with the RTC using the 1-kHz clock source to achieve the lowest possible power consumption. Because the 1-kHz clock source is not as accurate as a crystal, software can be added for any adjustments. For accuracy without adjustments at the expense of additional power consumption, the external clock (ERCLK) or the internal clock (IRCLK) can be selected with appropriate prescaler and modulo values.

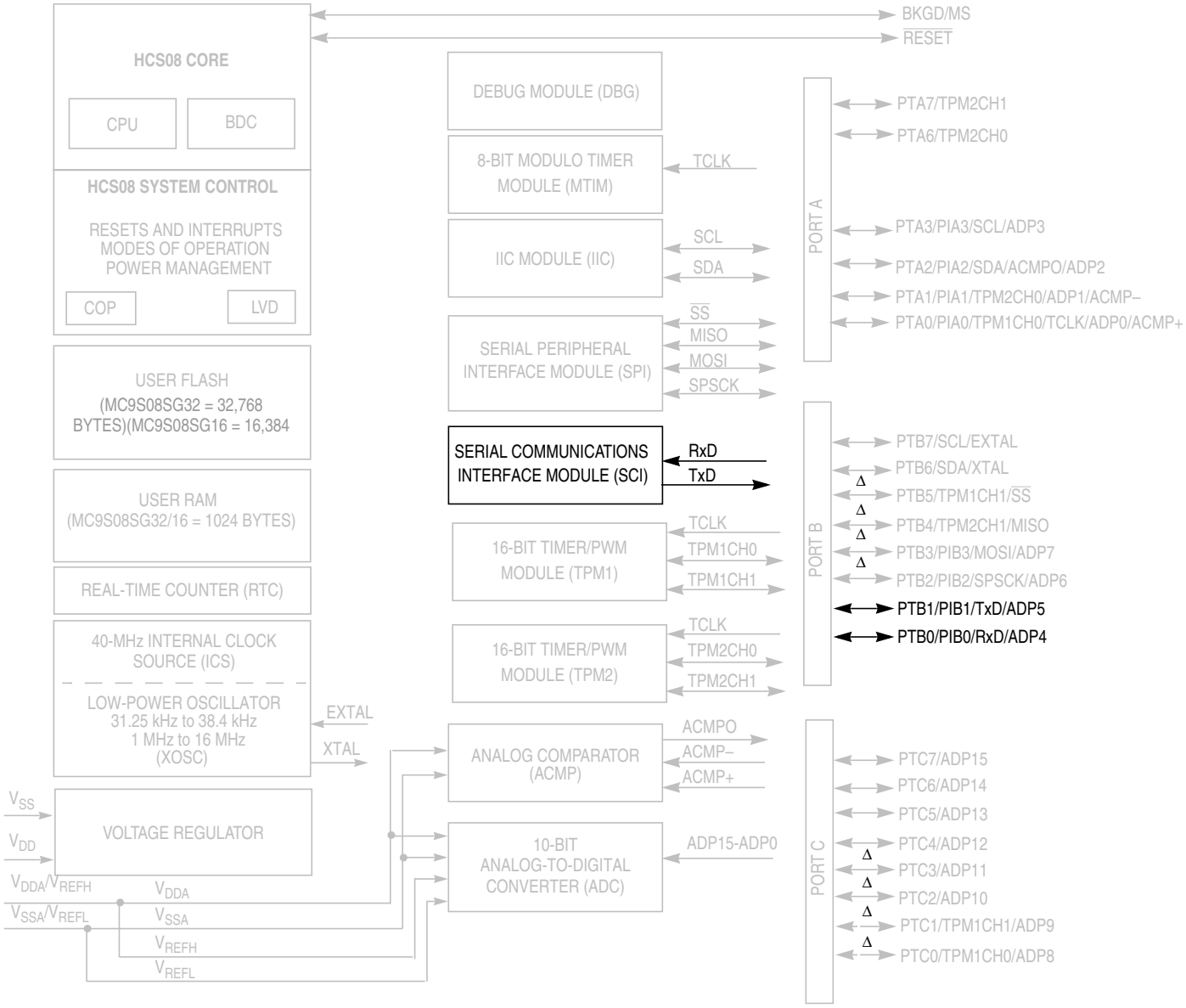
```
/* Initialize the elapsed time counters */
Seconds = 0;
Minutes = 0;
Hours = 0;
Days=0;

/* Configure RTC to interrupt every 1 second from 1-kHz clock source */
RTCMOD.byte = 0x00;
RTCSC.byte = 0x1F;

/*********************************************************************
Function Name : RTC_ISR
Notes : Interrupt service routine for RTC module.
*********************************************************************/
#pragma TRAP_PROC
void RTC_ISR(void)
{
        /* Clear the interrupt flag */
```

```
        RTCSC.byte = RTCSC.byte | 0x80;
        /* RTC interrupts every 1 Second */
        Seconds++;
        /* 60 seconds in a minute */
        if (Seconds > 59){
        Minutes++;
        Seconds = 0;
        }
        /* 60 minutes in an hour */
        if (Minutes > 59){
        Hours++;
        Minutes = 0;
        }
        /* 24 hours in a day */
        if (Hours > 23){
        Days ++;
        Hours = 0;
        }
}
```

# Chapter 14
# Serial Communications Interface (S08SCIV4)

## 14.1 Introduction

Figure 14-1 shows the MC9S08SG32 Series block diagram with the SCI module highlighted.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 14-1. MC9S08SG32 Series Block Diagram Highlighting SCI Block and Pins**

### 14.1.1 Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

### 14.1.2 Modes of Operation

See Section 14.3, “Functional Description,” For details concerning SCI operation in these modes:

- 8- and 9-bit data modes
- Stop mode operation
- Loop mode
- Single-wire mode

### 14.1.3 Block Diagram

Figure 14-2 shows the transmitter portion of the SCI.

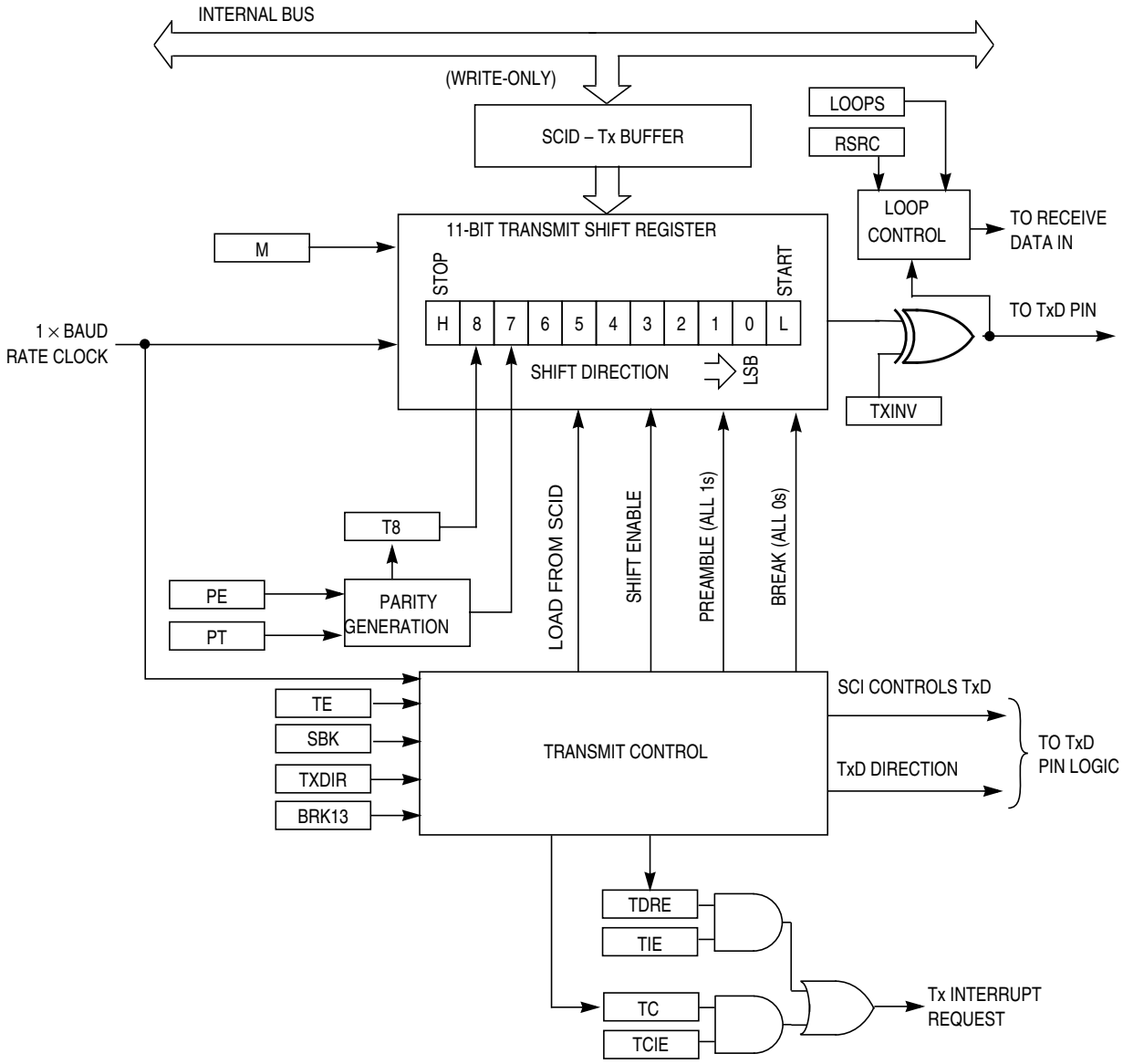



**Figure 14-2. SCI Transmitter Block Diagram**

Figure 14-3 shows the receiver portion of the SCI.

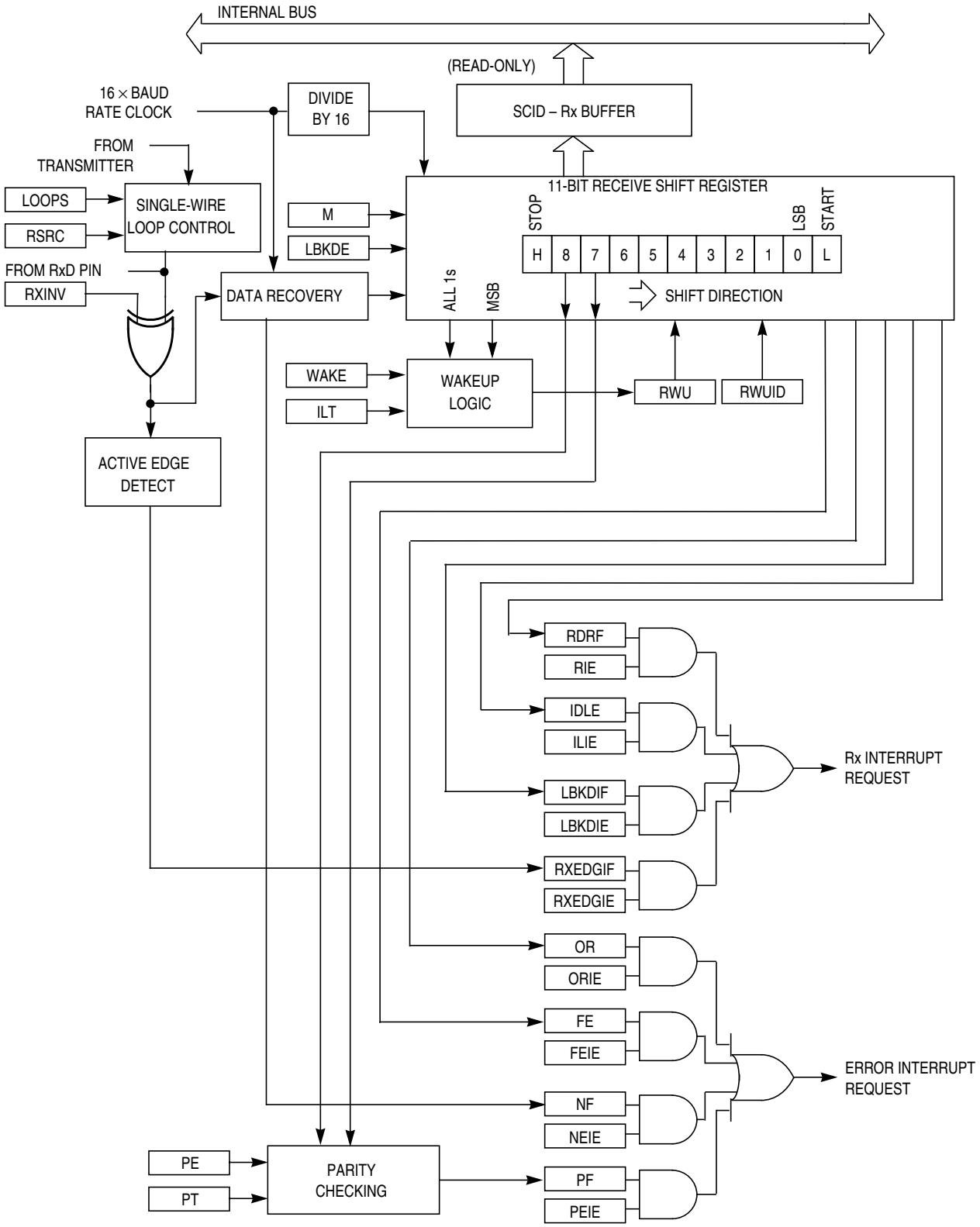



**Figure 14-3. SCI Receiver Block Diagram**

## 14.2 Register Definition

The SCI has eight 8-bit registers to control baud rate, select SCI options, report SCI status, and for transmit/receive data.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all SCI registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

### 14.2.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

This pair of registers controls the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCIBDH to buffer the high half of the new value and then write to SCIBDL. The working value in SCIBDH does not change until SCIBDL is written.

SCIBDL is reset to a non-zero value, so after reset the baud rate generator remains disabled until the first time the receiver or transmitter is enabled (RE or TE bits in SCIC2 are written to 1).

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | LBKDIE | RXEDGIE | 0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 14-4. SCI Baud Rate Register (SCIBDH)**

**Table 14-1. SCIBDH Field Descriptions**

| Field | Description |
|---|---|
| 7<br>LBKDIE | **LIN Break Detect Interrupt Enable (for LBKDIF)**<br>0 Hardware interrupts from LBKDIF disabled (use polling).<br>1 Hardware interrupt requested when LBKDIF flag is 1. |
| 6<br>RXEDGIE | **RxD Input Active Edge Interrupt Enable (for RXEDGIF)**<br>0 Hardware interrupts from RXEDGIF disabled (use polling).<br>1 Hardware interrupt requested when RXEDGIF flag is 1. |
| 4:0<br>SBR[12:8] | **Baud Rate Modulo Divisor** — The 13 bits in SBR[12:0] are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR = 0, the SCI baud rate generator is disabled to reduce supply current. When BR = 1 to 8191, the SCI baud rate = BUSCLK/(16×BR). See also BR bits in Table 14-2. |

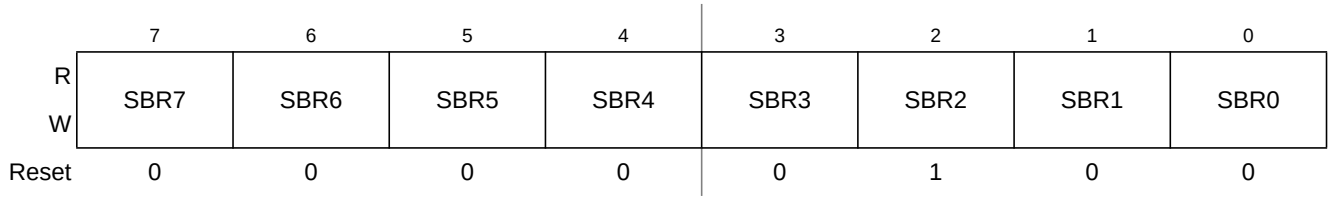



**Figure 14-5. SCI Baud Rate Register (SCIBDL)**

**Table 14-2. SCIBDL Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>SBR[7:0] | **Baud Rate Modulo Divisor** — These 13 bits in SBR[12:0] are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR = 0, the SCI baud rate generator is disabled to reduce supply current. When BR = 1 to 8191, the SCI baud rate = BUSCLK/(16×BR). See also BR bits in Table 14-1. |

## 14.2.2 SCI Control Register 1 (SCIC1)

This read/write register is used to control various optional features of the SCI system.

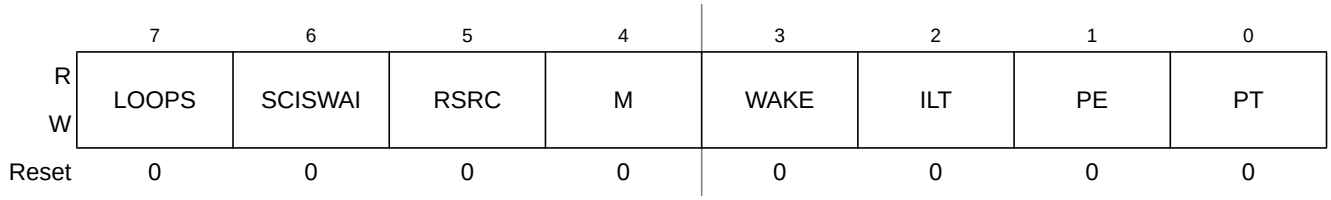



**Figure 14-6. SCI Control Register 1 (SCIC1)**

**Table 14-3. SCIC1 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>LOOPS | **Loop Mode Select** — Selects between loop back modes and normal 2-pin full-duplex modes. When LOOPS = 1, the transmitter output is internally connected to the receiver input.<br>0 Normal operation — RxD and TxD use separate pins.<br>1 Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input. (See RSRC bit.) RxD pin is not used by SCI. |
| 6<br>SCISWAI | **SCI Stops in Wait Mode**<br>0 SCI clocks continue to run in wait mode so the SCI can be the source of an interrupt that wakes up the CPU.<br>1 SCI clocks freeze while CPU is in wait mode. |
| 5<br>RSRC | **Receiver Source Select** — This bit has no meaning or effect unless the LOOPS bit is set to 1. When LOOPS = 1, the receiver input is internally connected to the TxD pin and RSRC determines whether this connection is also connected to the transmitter output.<br>0 Provided LOOPS = 1, RSRC = 0 selects internal loop back mode and the SCI does not use the RxD pins.<br>1 Single-wire SCI mode where the TxD pin is connected to the transmitter output and receiver input. |
| 4<br>M | **9-Bit or 8-Bit Mode Select**<br>0 Normal — start + 8 data bits (LSB first) + stop.<br>1 Receiver and transmitter use 9-bit data characters start + 8 data bits (LSB first) + 9th data bit + stop. |

**Table 14-3. SCIC1 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 3<br>WAKE | **Receiver Wakeup Method Select** — Refer to Section 14.3.3.2, “Receiver Wakeup Operation” for more information.<br>0 Idle-line wakeup.<br>1 Address-mark wakeup. |
| 2<br>ILT | **Idle Line Type Select** — Setting this bit to 1 ensures that the stop bit and logic 1 bits at the end of a character do not count toward the 10 or 11 bit times of logic high level needed by the idle line detection logic. Refer to Section 14.3.3.2.1, “Idle-Line Wakeup” for more information.<br>0 Idle character bit count starts after start bit.<br>1 Idle character bit count starts after stop bit. |
| 1<br>PE | **Parity Enable** — Enables hardware parity generation and checking. When parity is enabled, the most significant bit (MSB) of the data character (eighth or ninth data bit) is treated as the parity bit.<br>0 No hardware parity generation or checking.<br>1 Parity enabled. |
| 0<br>PT | **Parity Type** — Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even.<br>0 Even parity.<br>1 Odd parity. |

## 14.2.3 SCI Control Register 2 (SCIC2)

This register can be read or written at any time.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 14-7. SCI Control Register 2 (SCIC2)**

**Table 14-4. SCIC2 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TIE | **Transmit Interrupt Enable (for TDRE)**<br>0 Hardware interrupts from TDRE disabled (use polling).<br>1 Hardware interrupt requested when TDRE flag is 1. |
| 6<br>TCIE | **Transmission Complete Interrupt Enable (for TC)**<br>0 Hardware interrupts from TC disabled (use polling).<br>1 Hardware interrupt requested when TC flag is 1. |
| 5<br>RIE | **Receiver Interrupt Enable (for RDRF)**<br>0 Hardware interrupts from RDRF disabled (use polling).<br>1 Hardware interrupt requested when RDRF flag is 1. |
| 4<br>ILIE | **Idle Line Interrupt Enable (for IDLE)**<br>0 Hardware interrupts from IDLE disabled (use polling).<br>1 Hardware interrupt requested when IDLE flag is 1. |

**Table 14-4. SCIC2 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 3<br>TE | **Transmitter Enable**<br>0 Transmitter off.<br>1 Transmitter on.<br>TE must be 1 in order to use the SCI transmitter. When TE = 1, the SCI forces the TxD pin to act as an output for the SCI system.<br>When the SCI is configured for single-wire operation (LOOPS = RSRC = 1), TXDIR controls the direction of traffic on the single SCI communication line (TxD pin).<br>TE also can be used to queue an idle character by writing TE = 0 then TE = 1 while a transmission is in progress. Refer to Section 14.3.2.1, “Send Break and Queued Idle” for more details.<br>When TE is written to 0, the transmitter keeps control of the port TxD pin until any data, queued idle, or queued break character finishes transmitting before allowing the pin to revert to a general-purpose I/O pin. |
| 2<br>RE | **Receiver Enable** — When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS = 1 the RxD pin reverts to being a general-purpose I/O pin even if RE = 1.<br>0 Receiver off.<br>1 Receiver on. |
| 1<br>RWU | **Receiver Wakeup Control** — This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is either an idle line between messages (WAKE = 0, idle-line wakeup), or a logic 1 in the most significant data bit in a character (WAKE = 1, address-mark wakeup). Application software sets RWU and (normally) a selected hardware condition automatically clears RWU. Refer to Section 14.3.3.2, “Receiver Wakeup Operation” for more details.<br>0 Normal SCI receiver operation.<br>1 SCI receiver in standby waiting for wakeup condition. |
| 0<br>SBK | **Send Break** — Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 (13 or 14 if BRK13 = 1) bit times of logic 0 are queued as long as SBK = 1. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. Refer to Section 14.3.2.1, “Send Break and Queued Idle” for more details.<br>0 Normal transmitter operation.<br>1 Queue break character(s) to be sent. |

## 14.2.4 SCI Status Register 1 (SCIS1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| W | | | | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 14-8. SCI Status Register 1 (SCIS1)**

**Table 14-5. SCIS1 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TDRE | **Transmit Data Register Empty Flag** — TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCIS1 with TDRE = 1 and then write to the SCI data register (SCID).<br>0 Transmit data register (buffer) full.<br>1 Transmit data register (buffer) empty. |
| 6<br>TC | **Transmission Complete Flag** — TC is set out of reset and when TDRE = 1 and no data, preamble, or break character is being transmitted.<br>0 Transmitter active (sending data, a preamble, or a break).<br>1 Transmitter idle (transmission activity complete).<br>TC is cleared automatically by reading SCIS1 with TC = 1 and then doing one of the following three things:<br>• Write to the SCI data register (SCID) to transmit new data<br>• Queue a preamble by changing TE from 0 to 1<br>• Queue a break character by writing 1 to SBK in SCIC2 |
| 5<br>RDRF | **Receive Data Register Full Flag** — RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCID). To clear RDRF, read SCIS1 with RDRF = 1 and then read the SCI data register (SCID).<br>0 Receive data register empty.<br>1 Receive data register full. |
| 4<br>IDLE | **Idle Line Flag** — IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT = 0, the receiver starts counting idle bit times after the start bit. So if the receive character is all 1s, these bit times and the stop bit time count toward the full character time of logic high (10 or 11 bit times depending on the M control bit) needed for the receiver to detect an idle line. When ILT = 1, the receiver doesn't start counting idle bit times until after the stop bit. So the stop bit and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line.<br>To clear IDLE, read SCIS1 with IDLE = 1 and then read the SCI data register (SCID). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE will get set only once even if the receive line remains idle for an extended period.<br>0 No idle line detected.<br>1 Idle line was detected. |
| 3<br>OR | **Receiver Overrun Flag** — OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCID yet. In this case, the new character (and all associated error information) is lost because there is no room to move it into SCID. To clear OR, read SCIS1 with OR = 1 and then read the SCI data register (SCID).<br>0 No overrun.<br>1 Receive overrun (new SCI data lost). |
| 2<br>NF | **Noise Flag** — The advanced sampling technique used in the receiver takes seven samples during the start bit and three samples in each data bit and the stop bit. If any of these samples disagrees with the rest of the samples within any bit time in the frame, the flag NF will be set at the same time as the flag RDRF gets set for the character. To clear NF, read SCIS1 and then read the SCI data register (SCID).<br>0 No noise detected.<br>1 Noise detected in the received character in SCID. |

**Table 14-5. SCIS1 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>FE | **Framing Error Flag** — FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bit was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCIS1 with FE = 1 and then read the SCI data register (SCID).<br>0 No framing error detected. This does not guarantee the framing is correct.<br>1 Framing error. |
| 0<br>PF | **Parity Error Flag** — PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCIS1 and then read the SCI data register (SCID).<br>0 No parity error.<br>1 Parity error. |

## 14.2.5 SCI Status Register 2 (SCIS2)

This register has one read-only status flag.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | LBKDIF | RXEDGIF | 0 | RXINV | RWUID | BRK13 | LBKDE | RAF |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 14-9. SCI Status Register 2 (SCIS2)**

**Table 14-6. SCIS2 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>LBKDIF | **LIN Break Detect Interrupt Flag** — LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a “1” to it.<br>0 No LIN break character has been detected.<br>1 LIN break character has been detected. |
| 6<br>RXEDGIF | **RxD Pin Active Edge Interrupt Flag** — RXEDGIF is set when an active edge (falling if RXINV = 0, rising if RXINV=1) on the RxD pin occurs. RXEDGIF is cleared by writing a “1” to it.<br>0 No active edge on the receive pin has occurred.<br>1 An active edge on the receive pin has occurred. |
| 4<br>RXINV[1] | **Receive Data Inversion** — Setting this bit reverses the polarity of the received data input.<br>0 Receive data not inverted<br>1 Receive data inverted |
| 3<br>RWUID | **Receive Wake Up Idle Detect**— RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit.<br>0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character.<br>1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character. |
| 2<br>BRK13 | **Break Character Generation Length** — BRK13 is used to select a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit.<br>0 Break character is transmitted with length of 10 bit times (11 if M = 1)<br>1 Break character is transmitted with length of 13 bit times (14 if M = 1) |

**Table 14-6. SCIS2 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>LBKDE | **LIN Break Detection Enable**— LBKDE is used to select a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting.<br>0 Break character is detected at length of 10 bit times (11 if M = 1).<br>1 Break character is detected at length of 11 bit times (12 if M = 1). |
| 0<br>RAF | **Receiver Active Flag** — RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode.<br>0 SCI receiver idle waiting for a start bit.<br>1 SCI receiver active (RxD input not idle). |

[1] Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle.

When using an internal oscillator in a LIN system, it is necessary to raise the break detection threshold by one bit time. Under the worst case timing conditions allowed in LIN, it is possible that a 0x00 data character can appear to be 10.26 bit times long at a slave which is running 14% faster than the master. This would trigger normal break detection circuitry which is designed to detect a 10 bit break symbol. When the LBKDE bit is set, framing errors are inhibited and the break detection threshold changes from 10 bits to 11 bits, preventing false detection of a 0x00 data character as a LIN break symbol.

## 14.2.6 SCI Control Register 3 (SCIC3)

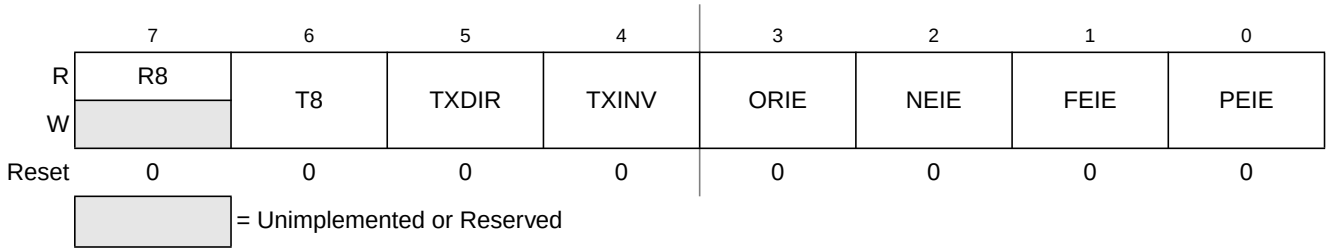



**Figure 14-10. SCI Control Register 3 (SCIC3)**

**Table 14-7. SCIC3 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>R8 | **Ninth Data Bit for Receiver** — When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the MSB of the buffered data in the SCID register. When reading 9-bit data, read R8 before reading SCID because reading SCID completes automatic flag clearing sequences which could allow R8 and SCID to be overwritten with new data. |
| 6<br>T8 | **Ninth Data Bit for Transmitter** — When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the MSB of the data in the SCID register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCID is written so T8 should be written (if it needs to change from its previous value) before SCID is written. If T8 does not need to change in the new value (such as when it is used to generate mark or space parity), it need not be written each time SCID is written. |
| 5<br>TXDIR | **TxD Pin Direction in Single-Wire Mode** — When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin.<br>0 TxD pin is an input in single-wire mode.<br>1 TxD pin is an output in single-wire mode. |

**Table 14-7. SCIC3 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 4<br>TXINV[1] | **Transmit Data Inversion** — Setting this bit reverses the polarity of the transmitted data output.<br>0 Transmit data not inverted<br>1 Transmit data inverted |
| 3<br>ORIE | **Overrun Interrupt Enable** — This bit enables the overrun flag (OR) to generate hardware interrupt requests.<br>0 OR interrupts disabled (use polling).<br>1 Hardware interrupt requested when OR = 1. |
| 2<br>NEIE | **Noise Error Interrupt Enable** — This bit enables the noise flag (NF) to generate hardware interrupt requests.<br>0 NF interrupts disabled (use polling).<br>1 Hardware interrupt requested when NF = 1. |
| 1<br>FEIE | **Framing Error Interrupt Enable** — This bit enables the framing error flag (FE) to generate hardware interrupt requests.<br>0 FE interrupts disabled (use polling).<br>1 Hardware interrupt requested when FE = 1. |
| 0<br>PEIE | **Parity Error Interrupt Enable** — This bit enables the parity error flag (PF) to generate hardware interrupt requests.<br>0 PF interrupts disabled (use polling).<br>1 Hardware interrupt requested when PF = 1. |

1 Setting TXINV inverts the TxD output for all cases: data bits, start and stop bits, break, and idle.

## 14.2.7 SCI Data Register (SCID)

This register is actually two separate registers. Reads return the contents of the read-only receive data buffer and writes go to the write-only transmit data buffer. Reads and writes of this register are also involved in the automatic flag clearing mechanisms for the SCI status flags.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| W | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 14-11. SCI Data Register (SCID)**

# 14.3 Functional Description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs. The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. The following describes each of the blocks of the SCI.

## 14.3.1 Baud Rate Generation

As shown in Figure 14-12, the clock source for the SCI baud rate generator is the bus-rate clock.

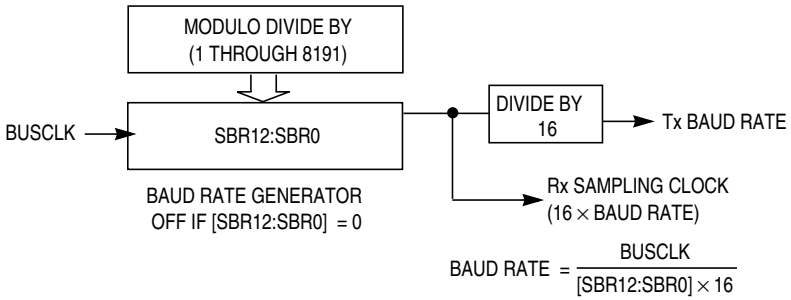



**Figure 14-12. SCI Baud Rate Generation**

SCI communications require the transmitter and receiver (which typically derive baud rates from independent clock sources) to use the same baud rate. Allowed tolerance on this baud frequency depends on the details of how the receiver synchronizes to the leading edge of the start bit and how bit sampling is performed.

The MCU resynchronizes to bit boundaries on every high-to-low transition, but in the worst case, there are no such transitions in the full 10- or 11-bit time character frame so any mismatch in baud rate is accumulated for the whole character time. For a Freescale Semiconductor SCI system whose bus frequency is driven by a crystal, the allowed baud rate mismatch is about 4.5percent for 8-bit data format and about 4 percent for 9-bit data format. Although baud rate modulo divider settings do not always produce baud rates that exactly match standard rates, it is normally possible to get within a few percent, which is acceptable for reliable communications.

## 14.3.2 Transmitter Functional Description

This section describes the overall block diagram for the SCI transmitter, as well as specialized functions for sending break and idle characters. The transmitter block diagram is shown in Figure 14-2.

The transmitter output (TxD) idle state defaults to logic high (TXINV = 0 following reset). The transmitter output is inverted by setting TXINV = 1. The transmitter is enabled by setting the TE bit in SCIC2. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the SCI data register (SCID).

The central element of the SCI transmitter is the transmit shift register that is either 10 or 11 bits long depending on the setting in the M control bit. For the remainder of this section, we will assume M = 0, selecting the normal 8-bit data mode. In 8-bit data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new SCI character, the value waiting in the transmit data register is transferred to the shift register (synchronized with the baud rate clock) and the transmit data register empty (TDRE) status flag is set to indicate another character may be written to the transmit data buffer at SCID.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD high, waiting for more characters to transmit.

Writing 0 to TE does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity that is in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

#### 14.3.2.1 Send Break and Queued Idle

The SBK control bit in SCIC2 is used to send break characters which were originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0 (10 bit times including the start and stop bits). A longer break of 13 bit times can be enabled by setting BRK13 = 1. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 1 and then write 0 to the SBK bit. This action queues a break character to be sent as soon as the shifter is available. If SBK is still 1 when the queued break moves into the shifter (synchronized to the baud rate clock), an additional break character is queued. If the receiving device is another Freescale Semiconductor SCI, the break characters will be received as 0s in all eight data bits and a framing error (FE = 1) occurs.

When idle-line wakeup is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the TE bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while TE = 0, the SCI transmitter never actually releases control of the TxD pin. If there is a possibility of the shifter finishing while TE = 0, set the general-purpose I/O controls so the pin that is shared with TxD is an output driving a logic 1. This ensures that the TxD line will look like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to TE.

The length of the break character is affected by the BRK13 and M bits as shown below.

**Table 14-8. Break Character Length**

| BRK13 | M | Break Character Length |
|---|---|---|
| 0 | 0 | 10 bit times |
| 0 | 1 | 11 bit times |
| 1 | 0 | 13 bit times |
| 1 | 1 | 14 bit times |

### 14.3.3 Receiver Functional Description

In this section, the receiver block diagram (Figure 14-3) is used as a guide for the overall receiver functional description. Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, two variations of the receiver wakeup function are explained.

The receiver input is inverted by setting RXINV = 1. The receiver is enabled by setting the RE bit in SCIC2. Character frames consist of a start bit of logic 0, eight (or nine) data bits (LSB first), and a stop bit of logic 1. For information about 9-bit data mode, refer to Section 14.3.5.1, “8- and 9-Bit Data Modes.” For the remainder of this discussion, we assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (RDRF) status

flag is set. If RDRF was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after RDRF is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared automatically by a 2-step sequence which is normally satisfied in the course of the user's program that handles receive data. Refer to Section 14.3.4, "Interrupts and Status Flags" for more details about flag clearing.

#### 14.3.3.1 Data Sampling Technique

The SCI receiver uses a 16× baud rate clock for sampling. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock is used to divide the bit time into 16 segments labeled RT1 through RT16. When a falling edge is located, three more samples are taken at RT3, RT5, and RT7 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at RT8, RT9, and RT10 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at RT3, RT5, and RT7 are 0 even if one or all of the samples taken at RT8, RT9, and RT10 are 1s. If any sample in any bit time (including the start and stop bits) in a character frame fails to agree with the logic level for that bit, the noise flag (NF) will be set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges, and if an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if FE is still set.

#### 14.3.3.2 Receiver Wakeup Operation

Receiver wakeup is a hardware mechanism that allows an SCI receiver to ignore the characters in a message that is intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up (RWU) control bit in SCIC2. When RWU bit is set, the status flags associated with the receiver (with the exception of the idle bit, IDLE, when RWUID bit is set) are inhibited from setting, thus eliminating the software overhead for handling the unimportant message

characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.

#### 14.3.3.2.1 Idle-Line Wakeup

When WAKE = 0, the receiver is configured for idle-line wakeup. In this mode, RWU is cleared automatically when the receiver detects a full character time of the idle-line level. The M control bit selects 8-bit or 9-bit data mode that determines how many bit times of idle are needed to constitute a full character time (10 or 11 bit times because of the start and stop bits).

When RWU is one and RWUID is zero, the idle condition that wakes up the receiver does not set the IDLE flag. The receiver wakes up and waits for the first data character of the next message which will set the RDRF flag and generate an interrupt if enabled. When RWUID is one, any idle condition sets the IDLE flag and generates an interrupt if enabled, regardless of whether RWU is zero or one.

The idle-line type (ILT) control bit selects one of two ways to detect an idle line. When ILT = 0, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When ILT = 1, the idle bit counter does not start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

#### 14.3.3.2.2 Address-Mark Wakeup

When WAKE = 1, the receiver is configured for address-mark wakeup. In this mode, RWU is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character (eighth bit in M = 0 mode and ninth bit in M = 1 mode).

Address-mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames. The logic 1 MSB of an address frame clears the RWU bit before the stop bit is received and sets the RDRF flag. In this case the character with the MSB set is received even though the receiver was sleeping during most of this character time.

### 14.3.4 Interrupts and Status Flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt. One interrupt vector is associated with the transmitter for TDRE and TC events. Another interrupt vector is associated with the receiver for RDRF, IDLE, RXEDGIF and LBKDIF events, and a third vector is used for OR, NF, FE, and PF error conditions. Each of these ten interrupt sources can be separately masked by local interrupt enable masks. The flags can still be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that optionally can generate hardware interrupt requests. Transmit data register empty (TDRE) indicates when there is room in the transmit data buffer to write another transmit character to SCID. If the transmit interrupt enable (TIE) bit is set, a hardware interrupt will be requested whenever TDRE = 1. Transmit complete (TC) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (TCIE) bit is set, a hardware interrupt will be requested whenever TC = 1.

Instead of hardware interrupts, software polling may be used to monitor the TDRE and TC status flags if the corresponding TIE or TCIE local interrupt masks are 0s.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared by reading SCIS1 while RDRF = 1 and then reading SCID.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCIS1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD line remains idle for an extended period of time. IDLE is cleared by reading SCIS1 while IDLE = 1 and then reading SCID. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled (RE = 1).

## 14.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

### 14.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCID to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

#### 14.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop2 mode, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note, because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

#### 14.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general-purpose port I/O pin.

#### 14.3.5.4 Single-Wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general-purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

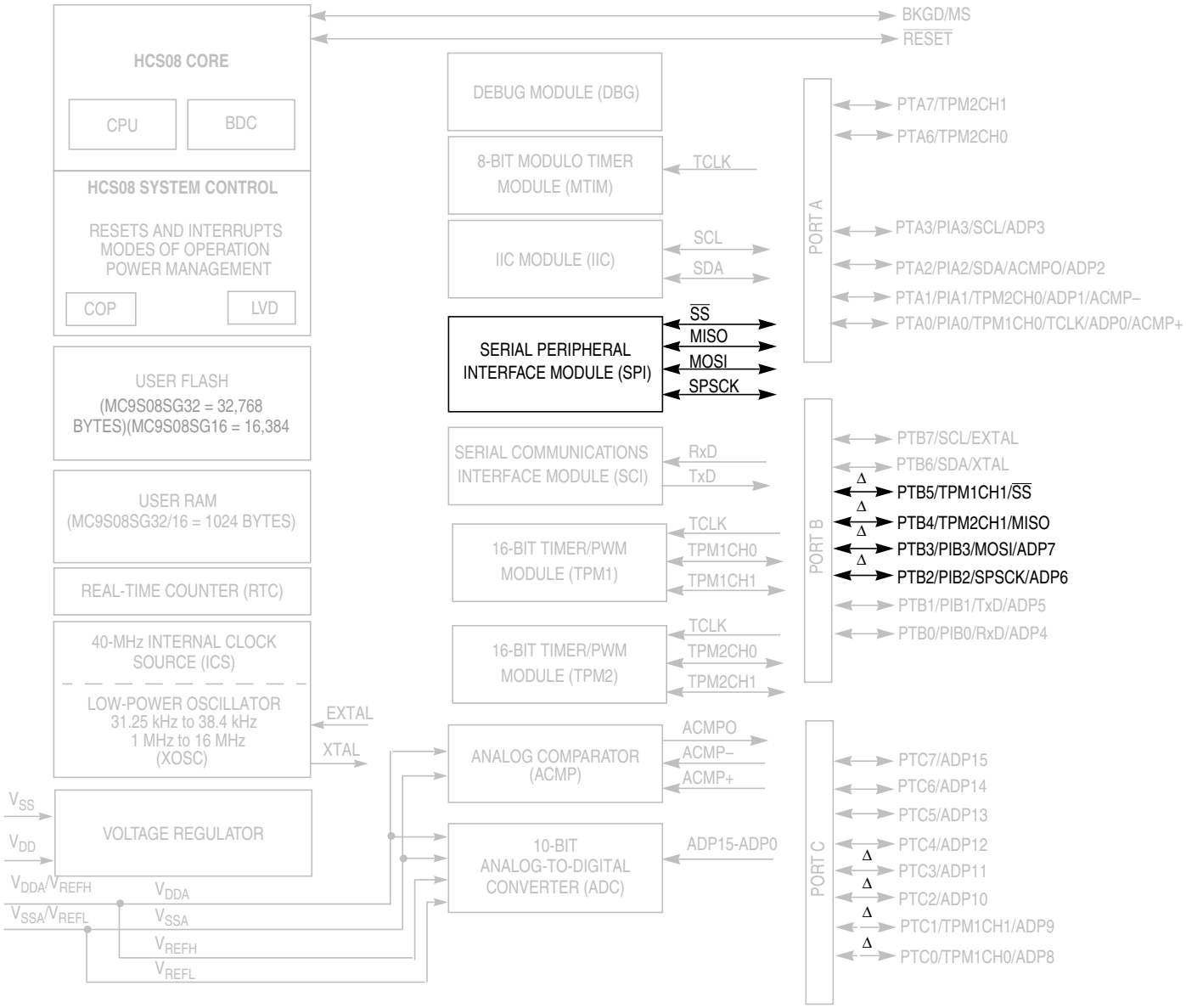
# Chapter 15
# Serial Peripheral Interface (S08SPIV3)

## 15.1 Introduction

The serial peripheral interface (SPI) module provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, memories, and so forth.

The SPI runs at a baud rate up to that of the bus clock divided by two in master mode and bus clock divided by four in slave mode. The SPI operation can be interrupt driven or software can poll the status flags.

All devices in the MC9S08SG32 Series MCUs contain one SPI module, as shown in the following block diagram. Figure 15-1 shows the MC9S08SG32 Series block diagram with the SPI modules highlighted.




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 15-1. MC9S08SG32 Series Block Diagram Highlighting SPI Block and Pin**

### 15.1.1 Features

Features of the SPI module include:

- Master or slave mode operation
- Full-duplex or single-wire bidirectional option
- Programmable transmit bit rate
- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting

### 15.1.2 Block Diagrams

This section includes block diagrams showing SPI system connections, the internal organization of the SPI module, and the SPI clock dividers that control the master mode bit rate.

#### 15.1.2.1 SPI System Block Diagram

Figure 15-2 shows the SPI modules of two MCUs connected in a master-slave arrangement. The master device initiates all SPI data transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. The transfer effectively exchanges the data that was in the SPI shift registers of the two SPI systems. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input ($\overline{SS}$ pin). In this system, the master device has configured its $\overline{SS}$ pin as an optional slave select output.

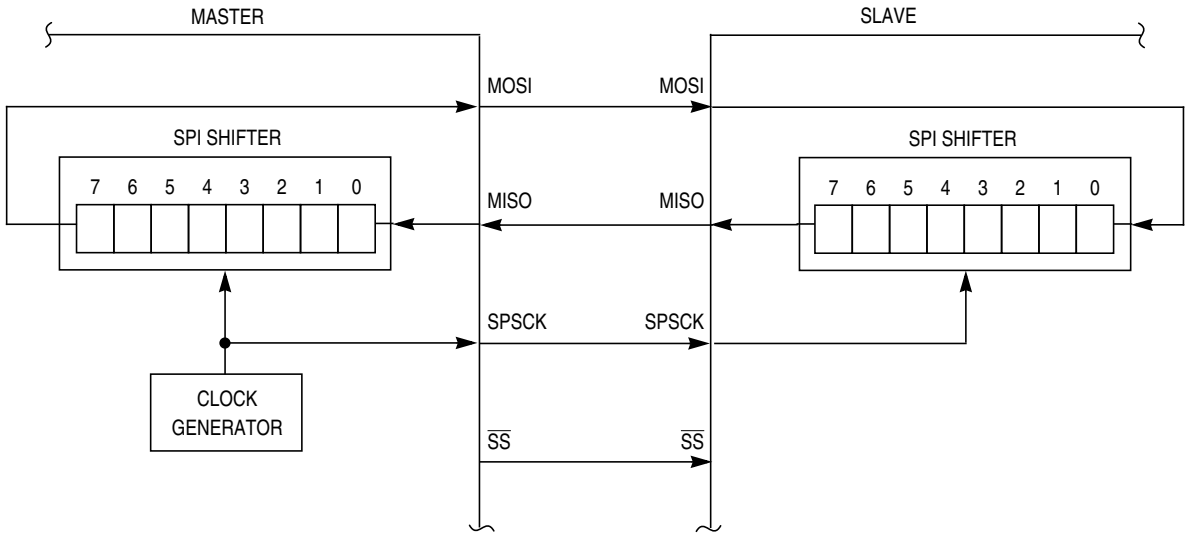



**Figure 15-2. SPI System Connections**

The most common uses of the SPI system include connecting simple shift registers for adding input or output ports or connecting small peripheral devices such as serial A/D or D/A converters. Although Figure 15-2 shows a system where data is exchanged between two MCUs, many practical systems involve simpler connections where data is unidirectionally transferred from the master MCU to a slave or from a slave to the master MCU.

#### 15.1.2.2 SPI Module Block Diagram

Figure 15-3 is a block diagram of the SPI module. The central element of the SPI is the SPI shift register. Data is written to the double-buffered transmitter (write to SPID) and gets transferred to the SPI shift register at the start of a data transfer. After shifting in a byte of data, the data is transferred into the double-buffered receiver where it can be read (read from SPID). Pin multiplexing logic controls connections between MCU pins and the SPI module.

When the SPI is configured as a master, the clock output is routed to the SPSCK pin, the shifter output is routed to MOSI, and the shifter input is routed from the MISO pin.

When the SPI is configured as a slave, the SPSCK pin is routed to the clock input of the SPI, the shifter output is routed to MISO, and the shifter input is routed from the MOSI pin.

In the external SPI system, simply connect all SPSCK pins to each other, all MISO pins together, and all MOSI pins together. Peripheral devices often use slightly different names for these pins.

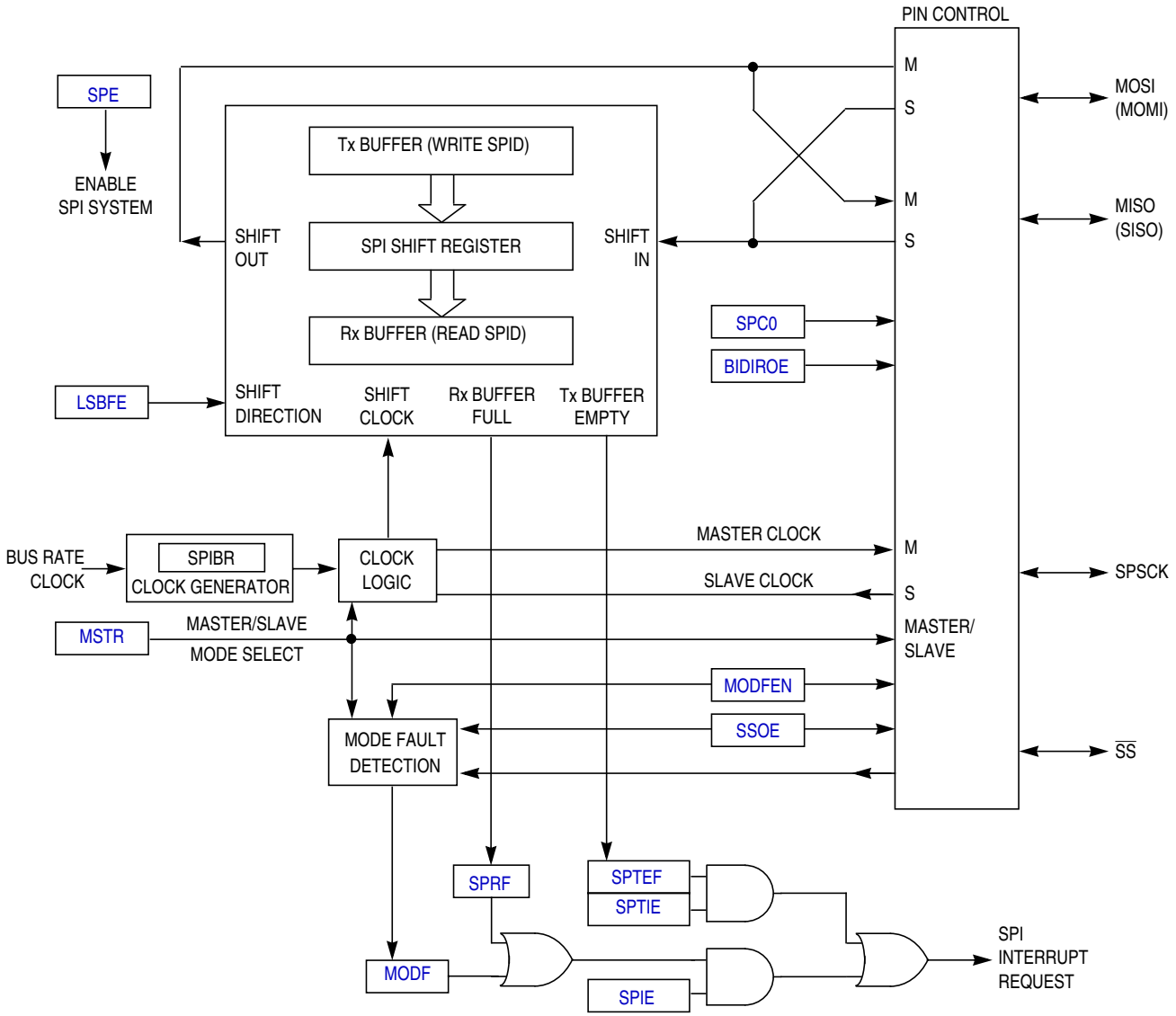



**Figure 15-3. SPI Module Block Diagram**

## 15.1.3 SPI Baud Rate Generation

As shown in Figure 15-4, the clock source for the SPI baud rate generator is the bus clock. The three prescale bits (SPPR2:SPPR1:SPPR0) choose a prescale divisor of 1, 2, 3, 4, 5, 6, 7, or 8. The three rate select bits (SPR2:SPR1:SPR0) divide the output of the prescaler stage by 2, 4, 8, 16, 32, 64, 128, or 256 to get the internal SPI master mode bit-rate clock.

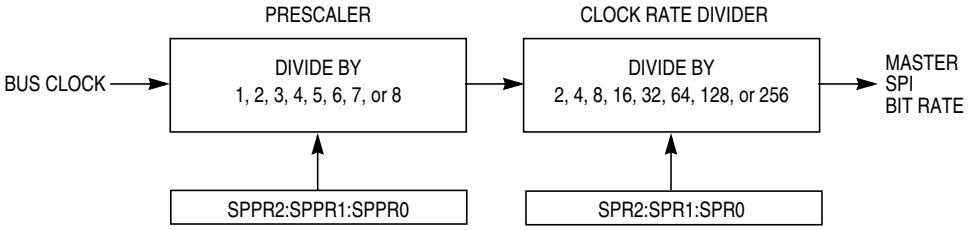



**Figure 15-4. SPI Baud Rate Generation**

## 15.2 External Signal Description

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to being general-purpose port I/O pins that are not controlled by the SPI.

### 15.2.1 SPSCK — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

### 15.2.2 MOSI — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data input. If SPC0 = 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and slave mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

### 15.2.3 MISO — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 = 0, this pin is the serial data output. If SPC0 = 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO) and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE = 0) or an output (BIDIROE = 1). If SPC0 = 1 and master mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

### 15.2.4 $\overline{SS}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN = 0), this pin is not used by the SPI and reverts to being a general-purpose port I/O pin. When the SPI is enabled as a master and MODFEN = 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE = 0) or as the slave select output (SSOE = 1).

## 15.3 Modes of Operation

### 15.3.1 SPI in Stop Modes

The SPI is disabled in all stop modes, regardless of the settings before executing the STOP instruction. During stop2 mode, the SPI module will be fully powered down. Upon wake-up from stop2 mode, the SPI module will be in the reset state. During stop3 mode, clocks to the SPI module are halted. No registers are affected. If stop3 is exited with a reset, the SPI will be put into its reset state. If stop3 is exited with an interrupt, the SPI continues from the state it was in when stop3 was entered.

## 15.4 Register Definition

The SPI has five 8-bit registers to select SPI options, control baud rate, report SPI status, and for transmit/receive data.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all SPI registers. This section refers to registers and control bits only by their names, and a Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

### 15.4.1 SPI Control Register 1 (SPIC1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Figure 15-5. SPI Control Register 1 (SPIC1)**

**Table 15-1. SPIC1 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>SPIE | **SPI Interrupt Enable (for SPRF and MODF)** — This is the interrupt enable for SPI receive buffer full (SPRF) and mode fault (MODF) events.<br>0 Interrupts from SPRF and MODF inhibited (use polling)<br>1 When SPRF or MODF is 1, request a hardware interrupt |
| 6<br>SPE | **SPI System Enable** — Disabling the SPI halts any transfer that is in progress, clears data buffers, and initializes internal state machines. SPRF is cleared and SPTEF is set to indicate the SPI transmit data buffer is empty.<br>0 SPI system inactive<br>1 SPI system enabled |
| 5<br>SPTIE | **SPI Transmit Interrupt Enable** — This is the interrupt enable bit for SPI transmit buffer empty (SPTEF).<br>0 Interrupts from SPTEF inhibited (use polling)<br>1 When SPTEF is 1, hardware interrupt requested |

**Table 15-1. SPIC1 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 4<br>MSTR | **Master/Slave Mode Select**<br>0 SPI module configured as a slave SPI device<br>1 SPI module configured as a master SPI device |
| 3<br>CPOL | **Clock Polarity** — This bit effectively places an inverter in series with the clock signal from a master SPI or to a slave SPI device. Refer to Section 15.5.1, “SPI Clock Formats” for more details.<br>0 Active-high SPI clock (idles low)<br>1 Active-low SPI clock (idles high) |
| 2<br>CPHA | **Clock Phase** — This bit selects one of two clock formats for different kinds of synchronous serial peripheral devices. Refer to Section 15.5.1, “SPI Clock Formats” for more details.<br>0 First edge on SPSCK occurs at the middle of the first cycle of an 8-cycle data transfer<br>1 First edge on SPSCK occurs at the start of the first cycle of an 8-cycle data transfer |
| 1<br>SSOE | **Slave Select Output Enable** — This bit is used in combination with the mode fault enable (MODFEN) bit in SPCR2 and the master/slave (MSTR) control bit to determine the function of the $\overline{SS}$ pin as shown in Table 15-2. |
| 0<br>LSBFE | **LSB First (Shifter Direction)**<br>0 SPI serial data transfers start with most significant bit<br>1 SPI serial data transfers start with least significant bit |

**Table 15-2. $\overline{SS}$ Pin Function**

| MODFEN | SSOE | Master Mode | Slave Mode |
|---|---|---|---|
| 0 | 0 | General-purpose I/O (not SPI) | Slave select input |
| 0 | 1 | General-purpose I/O (not SPI) | Slave select input |
| 1 | 0 | $\overline{SS}$ input for mode fault | Slave select input |
| 1 | 1 | Automatic $\overline{SS}$ output | Slave select input |

**NOTE**

Ensure that the SPI should not be disabled (SPE=0) at the same time as a bit change to the CPHA bit. These changes should be performed as separate operations or unexpected behavior may occur.

## 15.4.2 SPI Control Register 2 (SPIC2)

This read/write register is used to control optional features of the SPI system. Bits 7, 6, 5, and 2 are not implemented and always read 0.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 15-6. SPI Control Register 2 (SPIC2)**

**Table 15-3. SPIC2 Register Field Descriptions**

| Field | Description |
|---|---|
| 4<br>MODFEN | **Master Mode-Fault Function Enable** — When the SPI is configured for slave mode, this bit has no meaning or effect. (The $\overline{SS}$ pin is the slave select input.) In master mode, this bit determines how the $\overline{SS}$ pin is used (refer to Table 15-2 for more details).<br>0 Mode fault function disabled, master $\overline{SS}$ pin reverts to general-purpose I/O not controlled by SPI<br>1 Mode fault function enabled, master $\overline{SS}$ pin acts as the mode fault input or the slave select output |
| 3<br>BIDIROE | **Bidirectional Mode Output Enable** — When bidirectional mode is enabled by SPI pin control 0 (SPC0) = 1, BIDIROE determines whether the SPI data output driver is enabled to the single bidirectional SPI I/O pin. Depending on whether the SPI is configured as a master or a slave, it uses either the MOSI (MOMI) or MISO (SISO) pin, respectively, as the single SPI data I/O pin. When SPC0 = 0, BIDIROE has no meaning or effect.<br>0 Output driver disabled so SPI data I/O pin acts as an input<br>1 SPI I/O pin enabled as an output |
| 1<br>SPISWAI | **SPI Stop in Wait Mode**<br>0 SPI clocks continue to operate in wait mode<br>1 SPI clocks stop when the MCU enters wait mode |
| 0<br>SPC0 | **SPI Pin Control 0** — The SPC0 bit chooses single-wire bidirectional mode. If MSTR = 0 (slave mode), the SPI uses the MISO (SISO) pin for bidirectional SPI data transfers. If MSTR = 1 (master mode), the SPI uses the MOSI (MOMI) pin for bidirectional SPI data transfers. When SPC0 = 1, BIDIROE is used to enable or disable the output driver for the single bidirectional SPI I/O pin.<br>0 SPI uses separate pins for data input and data output<br>1 SPI configured for single-wire bidirectional operation |

## 15.4.3 SPI Baud Rate Register (SPIBR)

This register is used to set the prescaler and bit rate divisor for an SPI master. This register may be read or written at any time.

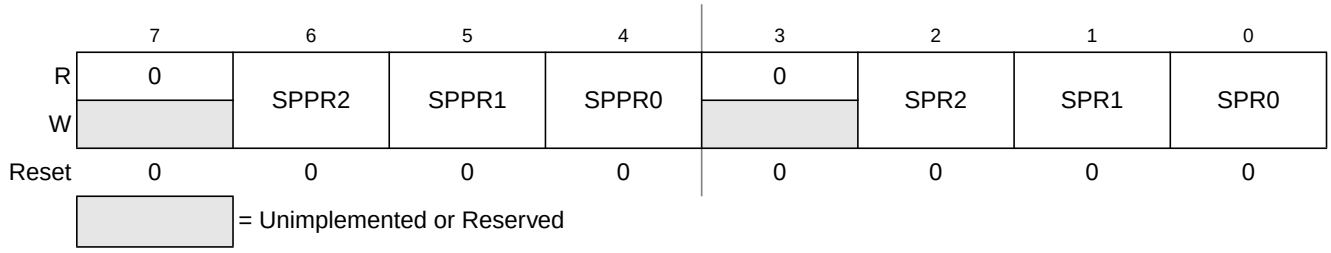



**Figure 15-7. SPI Baud Rate Register (SPIBR)**

**Table 15-4. SPIBR Register Field Descriptions**

| Field | Description |
|---|---|
| 6:4<br>SPPR[2:0] | **SPI Baud Rate Prescale Divisor** — This 3-bit field selects one of eight divisors for the SPI baud rate prescaler as shown in Table 15-5. The input to this prescaler is the bus rate clock (BUSCLK). The output of this prescaler drives the input of the SPI baud rate divider (see Figure 15-4). |
| 2:0<br>SPR[2:0] | **SPI Baud Rate Divisor** — This 3-bit field selects one of eight divisors for the SPI baud rate divider as shown in Table 15-6. The input to this divider comes from the SPI baud rate prescaler (see Figure 15-4). The output of this divider is the SPI bit rate clock for master mode. |

**Table 15-5. SPI Baud Rate Prescaler Divisor**

| SPPR2:SPPR1:SPPR0 | Prescaler Divisor |
|---|---|
| 0:0:0 | 1 |
| 0:0:1 | 2 |
| 0:1:0 | 3 |
| 0:1:1 | 4 |
| 1:0:0 | 5 |
| 1:0:1 | 6 |
| 1:1:0 | 7 |
| 1:1:1 | 8 |

**Table 15-6. SPI Baud Rate Divisor**

| SPR2:SPR1:SPR0 | Rate Divisor |
|---|---|
| 0:0:0 | 2 |
| 0:0:1 | 4 |
| 0:1:0 | 8 |
| 0:1:1 | 16 |
| 1:0:0 | 32 |
| 1:0:1 | 64 |
| 1:1:0 | 128 |
| 1:1:1 | 256 |

## 15.4.4 SPI Status Register (SPIS)

This register has three read-only status bits. Bits 6, 3, 2, 1, and 0 are not implemented and always read 0. Writes have no meaning or effect.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | SPRF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 15-8. SPI Status Register (SPIS)**

**Table 15-7. SPIS Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>SPRF | **SPI Read Buffer Full Flag** — SPRF is set at the completion of an SPI transfer to indicate that received data may be read from the SPI data register (SPID). SPRF is cleared by reading SPRF while it is set, then reading the SPI data register.<br>0 No data available in the receive data buffer<br>1 Data available in the receive data buffer |
| 5<br>SPTEF | **SPI Transmit Buffer Empty Flag** — This bit is set when there is room in the transmit data buffer. It is cleared by reading SPIS with SPTEF set, followed by writing a data value to the transmit buffer at SPID. SPIS must be read with SPTEF = 1 before writing data to SPID or the SPID write will be ignored. SPTEF generates an SPTEF CPU interrupt request if the SPTIE bit in the SPIC1 is also set. SPTEF is automatically set when a data byte transfers from the transmit buffer into the transmit shift register. For an idle SPI (no data in the transmit buffer or the shift register and no transfer in progress), data written to SPID is transferred to the shifter almost immediately so SPTEF is set within two bus cycles allowing a second 8-bit data value to be queued into the transmit buffer. After completion of the transfer of the value in the shift register, the queued value from the transmit buffer will automatically move to the shifter and SPTEF will be set to indicate there is room for new data in the transmit buffer. If no new data is waiting in the transmit buffer, SPTEF simply remains set and no data moves from the buffer to the shifter.<br>0 SPI transmit buffer not empty<br>1 SPI transmit buffer empty |
| 4<br>MODF | **Master Mode Fault Flag** — MODF is set if the SPI is configured as a master and the slave select input goes low, indicating some other SPI device is also configured as a master. The $\overline{SS}$ pin acts as a mode fault error input only when MSTR = 1, MODFEN = 1, and SSOE = 0; otherwise, MODF will never be set. MODF is cleared by reading MODF while it is 1, then writing to SPI control register 1 (SPIC1).<br>0 No mode fault error<br>1 Mode fault error detected |

## 15.4.5 SPI Data Register (SPID)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 15-9. SPI Data Register (SPID)**

Reads of this register return the data read from the receive data buffer. Writes to this register write data to the transmit data buffer. When the SPI is configured as a master, writing data to the transmit data buffer initiates an SPI transfer.

Data should not be written to the transmit data buffer unless the SPI transmit buffer empty flag (SPTEF) is set, indicating there is room in the transmit buffer to queue a new transmit byte.

Data may be read from SPID any time after SPRF is set and before another transfer is finished. Failure to read the data out of the receive data buffer before a new transfer ends causes a receive overrun condition and the data from the new transfer is lost.

## 15.5 Functional Description

An SPI transfer is initiated by checking for the SPI transmit buffer empty flag (SPTEF = 1) and then writing a byte of data to the SPI data register (SPID) in the master SPI device. When the SPI shift register is available, this byte of data is moved from the transmit data buffer to the shifter, SPTEF is set to indicate there is room in the buffer to queue another transmit character if desired, and the SPI serial transfer starts.

During the SPI transfer, data is sampled (read) on the MISO pin at one SPSCK edge and shifted, changing the bit value on the MOSI pin, one-half SPSCK cycle later. After eight SPSCK cycles, the data that was in the shift register of the master has been shifted out the MOSI pin to the slave while eight bits of data were shifted in the MISO pin into the master's shift register. At the end of this transfer, the received data byte is moved from the shifter into the receive data buffer and SPRF is set to indicate the data can be read by reading SPID. If another byte of data is waiting in the transmit buffer at the end of a transfer, it is moved into the shifter, SPTEF is set, and a new transfer is started.

Normally, SPI data is transferred most significant bit (MSB) first. If the least significant bit first enable (LSBFE) bit is set, SPI data is shifted LSB first.

When the SPI is configured as a slave, its $\overline{SS}$ pin must be driven low before a transfer starts and $\overline{SS}$ must stay low throughout the transfer. If a clock format where CPHA = 0 is selected, $\overline{SS}$ must be driven to a logic 1 between successive transfers. If CPHA = 1, $\overline{SS}$ may remain low between successive transfers. See Section 15.5.1, "SPI Clock Formats" for more details.

Because the transmitter and receiver are double buffered, a second byte, in addition to the byte currently being shifted out, can be queued into the transmit data buffer, and a previously received character can be in the receive data buffer while a new character is being shifted in. The SPTEF flag indicates when the transmit buffer has room for a new character. The SPRF flag indicates when a received character is available in the receive data buffer. The received character must be read out of the receive buffer (read SPID) before the next transfer is finished or a receive overrun error results.

In the case of a receive overrun, the new data is lost because the receive buffer still held the previous character and was not ready to accept the new data. There is no indication for such an overrun condition so the application system designer must ensure that previous data has been read from the receive buffer before a new transfer is initiated.

### 15.5.1 SPI Clock Formats

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the SPI system has a clock polarity (CPOL) bit and a clock phase (CPHA) control bit to select one of four clock formats for data transfers. CPOL selectively inserts an inverter in series with the clock. CPHA chooses between two different clock phase relationships between the clock and data.

Figure 15-10 shows the clock formats when CPHA = 1. At the top of the figure, the eight bit times are shown for reference with bit 1 starting at the first SPSCK edge and bit 8 ending one-half SPSCK cycle after the sixteenth SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output

pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

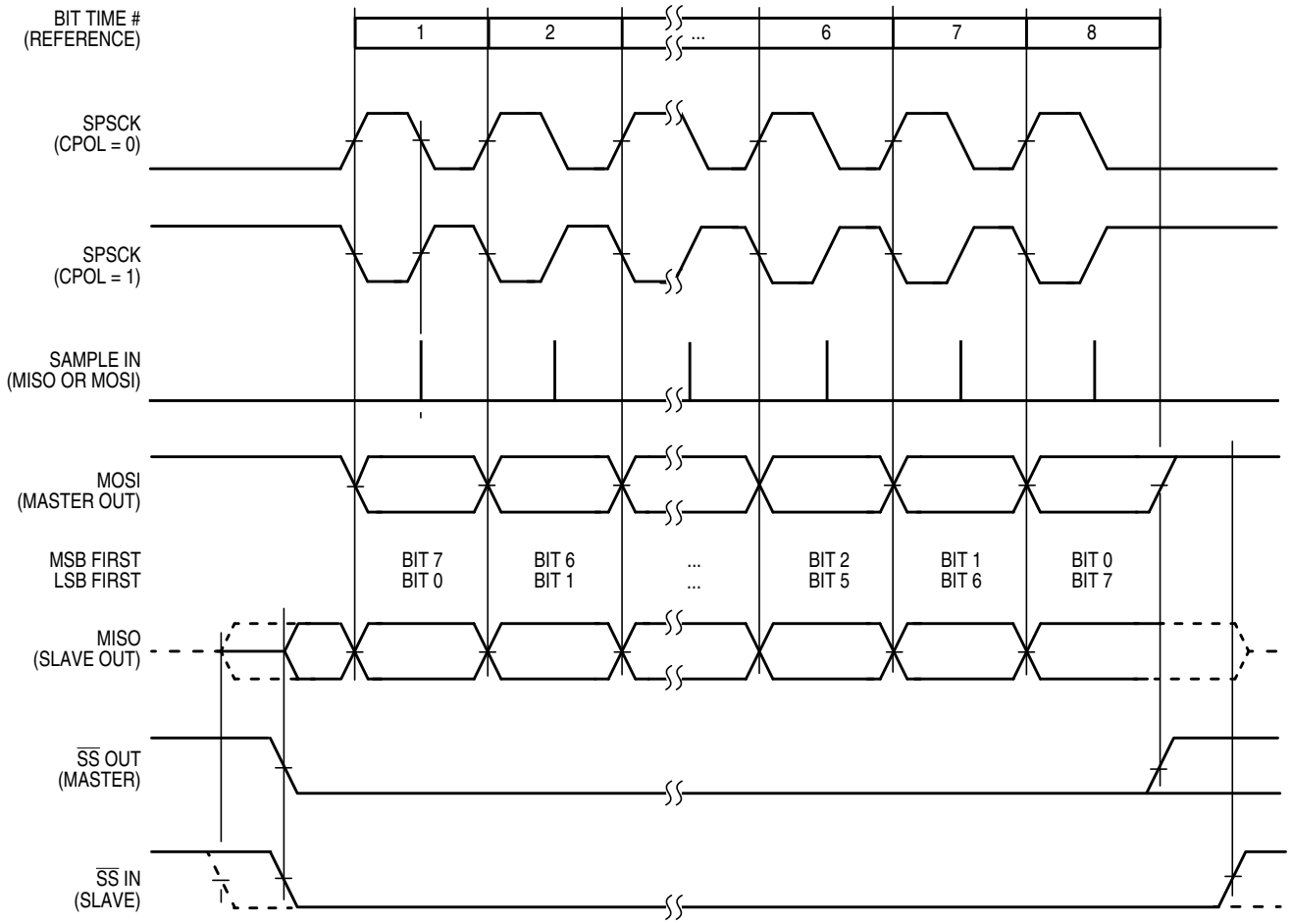



**Figure 15-10. SPI Clock Formats (CPHA = 1)**

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CHPA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers.

Figure 15-11 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected ($\overline{SS}$ IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting

in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

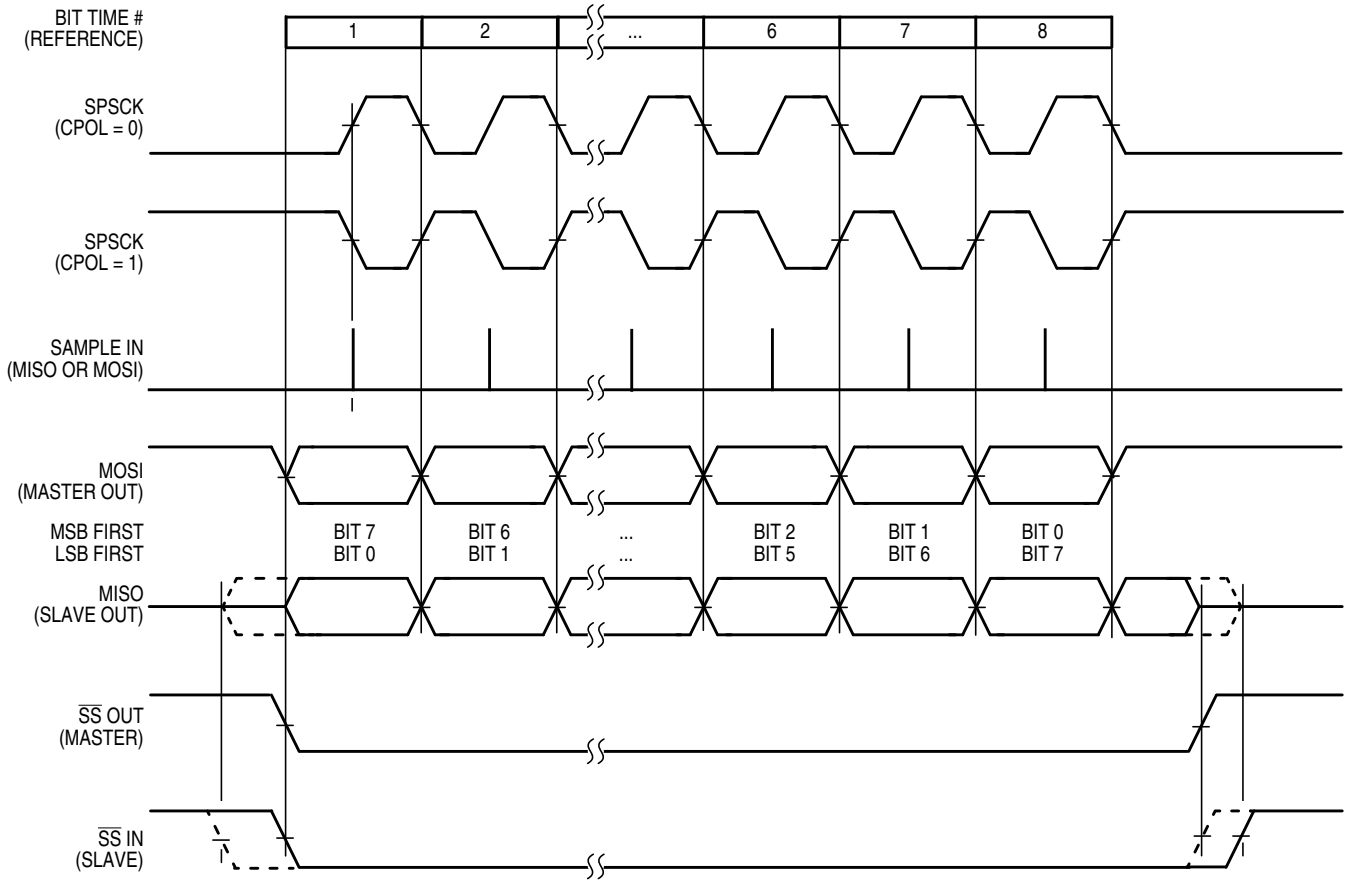



**Figure 15-11. SPI Clock Formats (CPHA = 0)**

When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when $\overline{SS}$ goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's $\overline{SS}$ input must go to its inactive high level between transfers.

### 15.5.2 SPI Interrupts

There are three flag bits, two interrupt mask bits, and one interrupt vector associated with the SPI system. The SPI interrupt enable mask (SPIE) enables interrupts from the SPI receiver full flag (SPRF) and mode fault flag (MODF). The SPI transmit interrupt enable mask (SPTIE) enables interrupts from the SPI transmit buffer empty flag (SPTEF). When one of the flag bits is set, and the associated interrupt mask bit is set, a hardware interrupt request is sent to the CPU. If the interrupt mask bits are cleared, software can poll the associated flag bits instead of using interrupts. The SPI interrupt service routine (ISR) should check the flag bits to determine what event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

### 15.5.3 Mode Fault Detection

A mode fault occurs and the mode fault flag (MODF) becomes set when a master SPI device detects an error on the $\overline{SS}$ pin (provided the $\overline{SS}$ pin is configured as the mode fault input signal). The $\overline{SS}$ pin is configured to be the mode fault input signal when MSTR = 1, mode fault enable is set (MODFEN = 1), and slave select output enable is clear (SSOE = 0).

The mode fault detection feature can be used in a system where more than one SPI device might become a master at the same time. The error is detected when a master's $\overline{SS}$ pin is low, indicating that some other SPI device is trying to address this master as if it were a slave. This could indicate a harmful output driver conflict, so the mode fault logic is designed to disable all SPI output drivers when such an error is detected.

When a mode fault is detected, MODF is set and MSTR is cleared to change the SPI configuration back to slave mode. The output drivers on the SPSCK, MOSI, and MISO (if not bidirectional mode) are disabled.

MODF is cleared by reading it while it is set, then writing to the SPI control register 1 (SPIC1). User software should verify the error condition has been corrected before changing the SPI back to master mode.

# Chapter 16
# Timer Pulse-Width Modulator (S08TPMV3)

## 16.1 Introduction

The TPM uses one input/output (I/O) pin per channel, TPMxCHn where x is the TPM number (for example, 1 or 2) and n is the channel number (for example, 0–1). The TPM shares its I/O pins with general-purpose I/O port pins (refer to the Pins and Connections chapter for more information).

All MC9S08SG32 Series MCUs have two TPM modules.

Figure 16-1 shows the MC9S08SG32 Series block diagram with the TPM modules highlighted.

### 16.1.1 TPM Configuration Information

The external clock for the MTIM module, TCLK, is selected by setting CLKS = 1:1 or 1:0 in MTIMCLK, which selects the TCLK pin input. The TCLK input can be enabled as external clock inputs to both the MTIM and TPM modules simultaneously.

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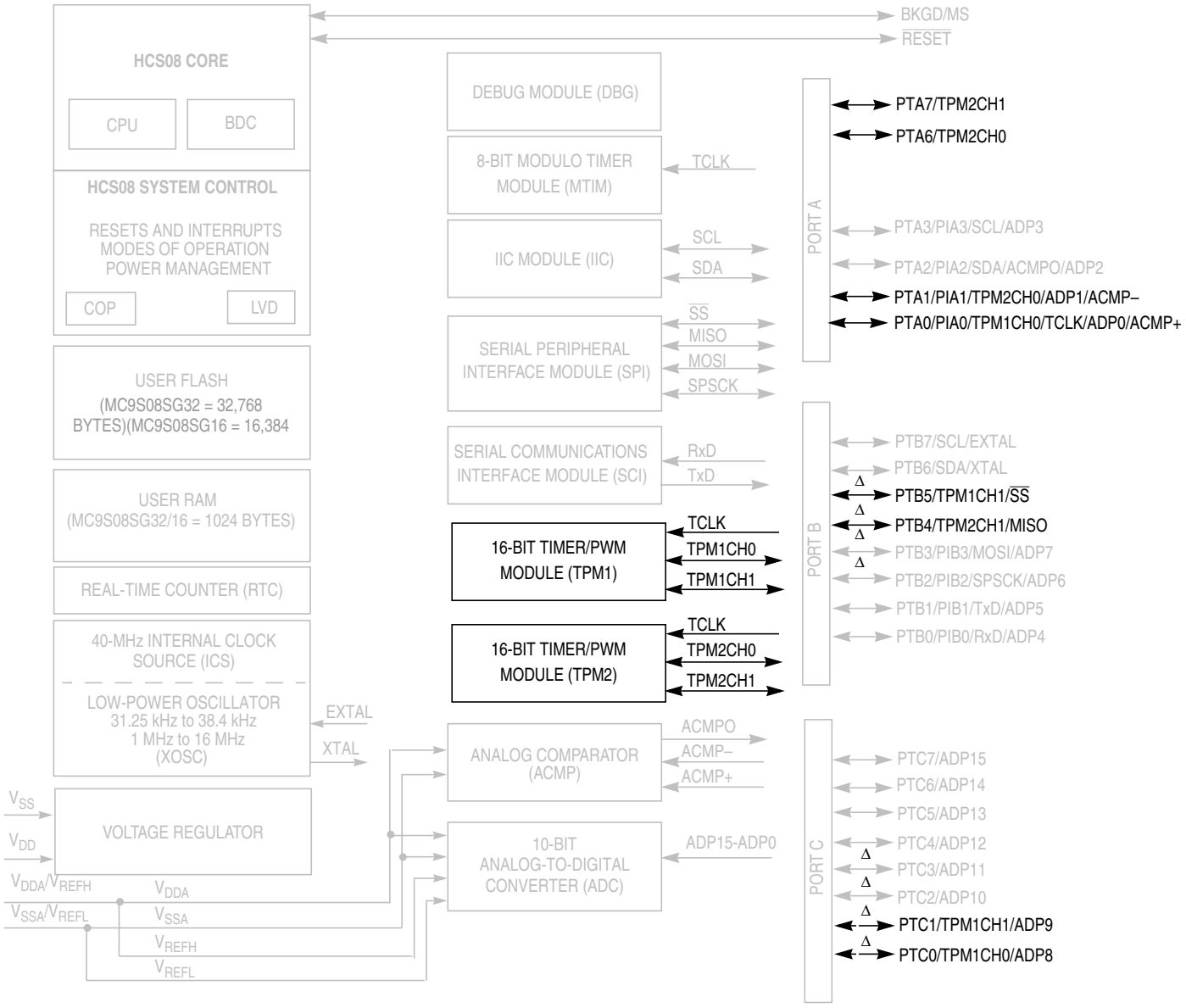
### 16.1.2 TPM Pin Repositioning

The TPM modules pins, TPM1CHx and TPM2CHx can be repositioned under software control using TxCHnPS bits in SOPT2 as shown in Table 16-1.

**Table 16-1. TPM Position Options**

| TxCHxPS in SOPT2 | Port Pin for TPM2CH1 | Port Pin for TPM2CH0 | Port Pin for TPM1CH1 | Port Pin for TPM1CH0 |
|---|---|---|---|---|
| 0 (default) | PTB4 | PTA1 | PTB5 | PTA0 |
| 1 | PTA7 | PTA6 | PTC1 | PTC0 |




NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: $V_{DDA}/V_{REFH}$ and $V_{SSA}/V_{REFL}$ are double bonded to $V_{DD}$ and $V_{SS}$ respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

**Figure 16-1. MC9S08SG32 Series Block Diagram Highlighting TPM Block and Pins**

### 16.1.3 Features

The TPM includes these distinctive features:

- One to eight channels:
  - Each channel may be input capture, output compare, or edge-aligned PWM
  - Rising-Edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs
- Module may be configured for buffered, center-aligned pulse-width-modulation (CPWM) on all channels
- Timer clock source selectable as prescaled bus clock, fixed system clock, or an external clock pin
  - Prescale taps for divide-by 1, 2, 4, 8, 16, 32, 64, or 128
  - Fixed system clock source are synchronized to the bus clock by an on-chip synchronization circuit
  - External clock pin may be shared with any timer channel pin or a separated input pin
- 16-bit free-running or modulo up/down count operation
- Timer system enable
- One interrupt per channel plus terminal count interrupt

### 16.1.4 Modes of Operation

In general, TPM channels may be independently configured to operate in input capture, output compare, or edge-aligned PWM modes. A control bit allows the whole TPM (all channels) to switch to center-aligned PWM mode. When center-aligned PWM mode is selected, input capture, output compare, and edge-aligned PWM functions are not available on any channels of this TPM module.

When the microcontroller is in active BDM background or BDM foreground mode, the TPM temporarily suspends all counting until the microcontroller returns to normal user operating mode. During stop mode, all system clocks, including the main oscillator, are stopped; therefore, the TPM is effectively disabled until clocks resume. During wait mode, the TPM continues to operate normally. Provided the TPM does not need to produce a real time reference or provide the interrupt source(s) needed to wake the MCU from wait mode, the user can save power by disabling TPM functions before entering wait mode.

- Input capture mode

  When a selected edge event occurs on the associated MCU pin, the current value of the 16-bit timer counter is captured into the channel value register and an interrupt flag bit is set. Rising edges, falling edges, any edge, or no edge (disable channel) may be selected as the active edge which triggers the input capture.
- Output compare mode

  When the value in the timer counter register matches the channel value register, an interrupt flag bit is set, and a selected output action is forced on the associated MCU pin. The output compare action may be selected to force the pin to zero, force the pin to one, toggle the pin, or ignore the pin (used for software timing functions).

- Edge-aligned PWM mode

  The value of a 16-bit modulo register plus 1 sets the period of the PWM output signal. The channel value register sets the duty cycle of the PWM output signal. The user may also choose the polarity of the PWM output signal. Interrupts are available at the end of the period and at the duty-cycle transition point. This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within a TPM.
- Center-aligned PWM mode

  Twice the value of a 16-bit modulo register sets the period of the PWM output, and the channel-value register sets the half-duty-cycle duration. The timer counter counts up until it reaches the modulo value and then counts down until it reaches zero. As the count matches the channel value register while counting down, the PWM output becomes active. When the count matches the channel value register while counting up, the PWM output becomes inactive. This type of PWM signal is called center-aligned because the centers of the active duty cycle periods for all channels are aligned with a count value of zero. This type of PWM is required for types of motors used in small appliances.

This is a high-level description only. Detailed descriptions of operating modes are in later sections.

### 16.1.5 Block Diagram

The TPM uses one input/output (I/O) pin per channel, TPMxCHn (timer channel n) where n is the channel number (1-8). The TPM shares its I/O pins with general purpose I/O port pins (refer to I/O pin descriptions in full-chip specification for the specific chip implementation).

Figure 16-2 shows the TPM structure. The central component of the TPM is the 16-bit counter that can operate as a free-running counter or a modulo up/down counter. The TPM counter (when operating in normal up-counting mode) provides the timing reference for the input capture, output compare, and edge-aligned PWM functions. The timer counter modulo registers, TPMxMODH:TPMxMODL, control the modulo value of the counter (the values 0x0000 or 0xFFFF effectively make the counter free running). Software can read the counter value at any time without affecting the counting sequence. Any write to either half of the TPMxCNT counter resets the counter, regardless of the data value written.

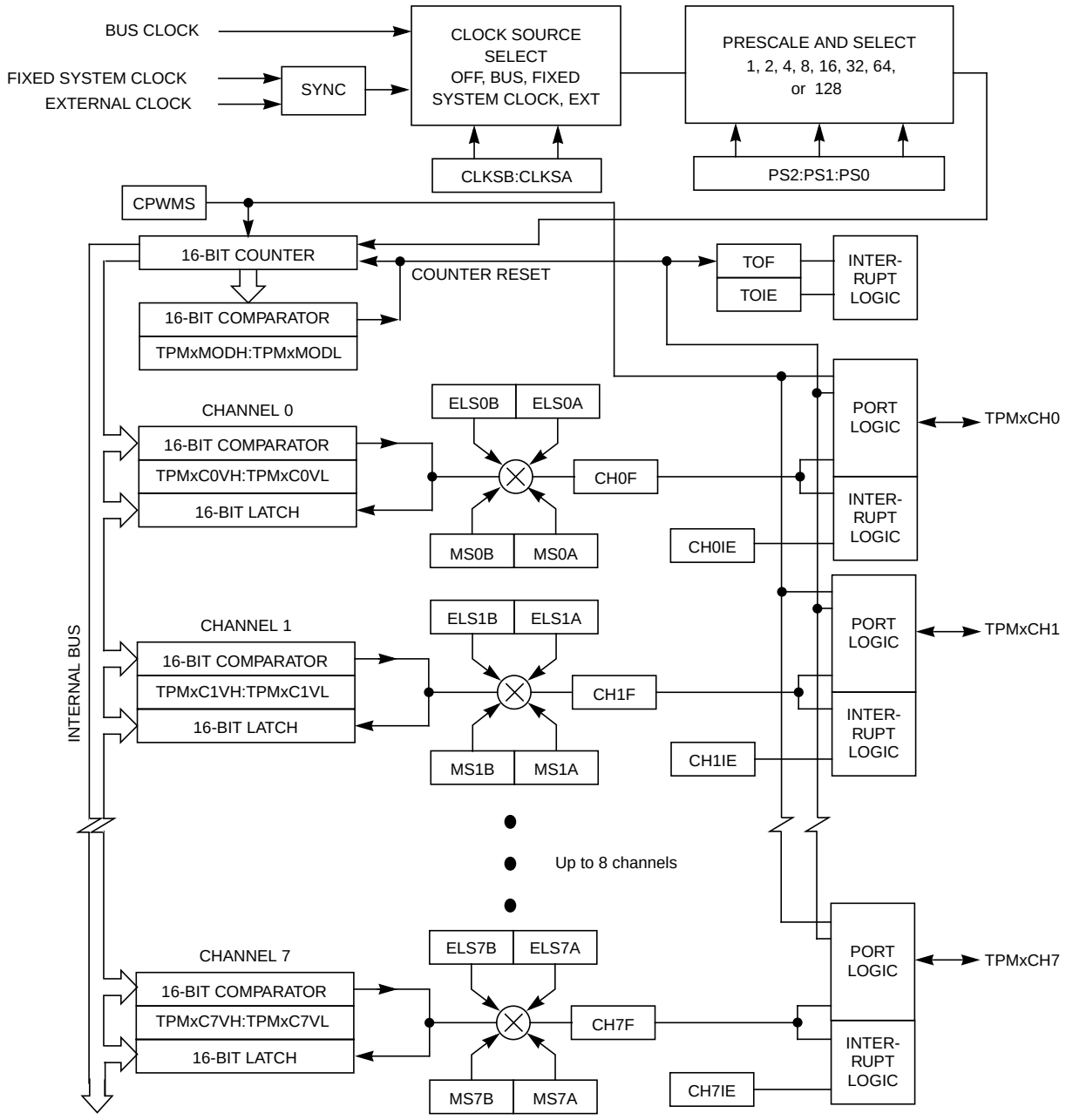



**Figure 16-2. TPM Block Diagram**

The TPM channels are programmable independently as input capture, output compare, or edge-aligned PWM channels. Alternately, the TPM can be configured to produce CPWM outputs on all channels. When the TPM is configured for CPWMs, the counter operates as an up/down counter; input capture, output compare, and EPWM functions are not practical.

If a channel is configured as input capture, an internal pullup device may be enabled for that channel. The details of how a module interacts with pin controls depends upon the chip implementation because the I/O pins and associated general purpose I/O controls are not part of the module. Refer to the discussion of the I/O port logic in a full-chip specification.

Because center-aligned PWMs are usually used to drive 3-phase AC-induction motors and brushless DC motors, they are typically used in sets of three or six channels.

## 16.2 Signal Description

Table 16-2 shows the user-accessible signals for the TPM. The number of channels may be varied from one to eight. When an external clock is included, it can be shared with the same pin as any TPM channel; however, it could be connected to a separate input pin. Refer to the I/O pin descriptions in full-chip specification for the specific chip implementation.

**Table 16-2. Signal Properties**

| Name | Function |
|---|---|
| EXTCLK[1] | External clock source which may be selected to drive the TPM counter. |
| TPMxCHn[2] | I/O pin associated with TPM channel n |

1 When preset, this signal can share any channel pin; however depending upon full-chip implementation, this signal could be connected to a separate external pin.

2 n=channel number (1 to 8)

Refer to documentation for the full-chip for details about reset states, port connections, and whether there is any pullup device on these pins.

TPM channel pins can be associated with general purpose I/O pins and have passive pullup devices which can be enabled with a control bit when the TPM or general purpose I/O controls have configured the associated pin as an input. When no TPM function is enabled to use a corresponding pin, the pin reverts to being controlled by general purpose I/O controls, including the port-data and data-direction registers. Immediately after reset, no TPM functions are enabled, so all associated pins revert to general purpose I/O control.

### 16.2.1 Detailed Signal Descriptions

This section describes each user-accessible pin signal in detail. Although Table 16-2 grouped all channel pins together, any TPM pin can be shared with the external clock source signal. Since I/O pin logic is not part of the TPM, refer to full-chip documentation for a specific derivative for more details about the interaction of TPM pin functions and general purpose I/O controls including port data, data direction, and pullup controls.

#### 16.2.1.1 EXTCLK — External Clock Source

Control bits in the timer status and control register allow the user to select nothing (timer disable), the bus-rate clock (the normal default source), a crystal-related clock, or an external clock as the clock which drives the TPM prescaler and subsequently the 16-bit TPM counter. The external clock source is synchronized in the TPM. The bus clock clocks the synchronizer; the frequency of the external source must be no more than one-fourth the frequency of the bus-rate clock, to meet Nyquist criteria and allowing for jitter.

The external clock signal shares the same pin as a channel I/O pin, so the channel pin will not be usable for channel I/O function when selected as the external clock source. It is the user's responsibility to avoid such settings. If this pin is used as an external clock source (CLKSB:CLKSA = 1:1), the channel can still be used in output compare mode as a software timer (ELSnB:ELSnA = 0:0).

#### 16.2.1.2 TPMxCHn — TPM Channel n I/O Pin(s)

Each TPM channel is associated with an I/O pin on the MCU. The function of this pin depends on the channel configuration. The TPM pins share with general purpose I/O pins, where each pin has a port data register bit, and a data direction control bit, and the port has optional passive pullups which may be enabled whenever a port pin is acting as an input.

The TPM channel does not control the I/O pin when (ELSnB:ELSnA = 0:0) or when (CLKSB:CLKSA = 0:0) so it normally reverts to general purpose I/O control. When CPWMS = 1 (and ELSnB:ELSnA not = 0:0), all channels within the TPM are configured for center-aligned PWM and the TPMxCHn pins are all controlled by the TPM system. When CPWMS=0, the MSnB:MSnA control bits determine whether the channel is configured for input capture, output compare, or edge-aligned PWM.

When a channel is configured for input capture (CPWMS=0, MSnB:MSnA = 0:0 and ELSnB:ELSnA not = 0:0), the TPMxCHn pin is forced to act as an edge-sensitive input to the TPM. ELSnB:ELSnA control bits determine what polarity edge or edges will trigger input-capture events. A synchronizer based on the bus clock is used to synchronize input edges to the bus clock. This implies the minimum pulse width—that can be reliably detected—on an input capture pin is four bus clock periods (with ideal clock pulses as near as two bus clocks can be detected). TPM uses this pin as an input capture input to override the port data and data direction controls for the same pin.

When a channel is configured for output compare (CPWMS=0, MSnB:MSnA = 0:1 and ELSnB:ELSnA not = 0:0), the associated data direction control is overridden, the TPMxCHn pin is considered an output controlled by the TPM, and the ELSnB:ELSnA control bits determine how the pin is controlled. The remaining three combinations of ELSnB:ELSnA determine whether the TPMxCHn pin is toggled, cleared, or set each time the 16-bit channel value register matches the timer counter.

When the output compare toggle mode is initially selected, the previous value on the pin is driven out until the next output compare event—then the pin is toggled.

When a channel is configured for edge-aligned PWM (CPWMS=0, MSnB=1 and ELSnB:ELSnA not = 0:0), the data direction is overridden, the TPMxCHn pin is forced to be an output controlled by the TPM, and ELSnA controls the polarity of the PWM output signal on the pin. When ELSnB:ELSnA=1:0, the TPMxCHn pin is forced high at the start of each new period (TPMxCNT=0x0000), and the pin is forced low when the channel value register matches the timer counter. When ELSnA=1, the TPMxCHn pin is forced low at the start of each new period (TPMxCNT=0x0000), and the pin is forced high when the channel value register matches the timer counter.

TPMxMODH:TPMxMODL = 0x0008
TPMxCnVH:TPMxCnVL = 0x0005

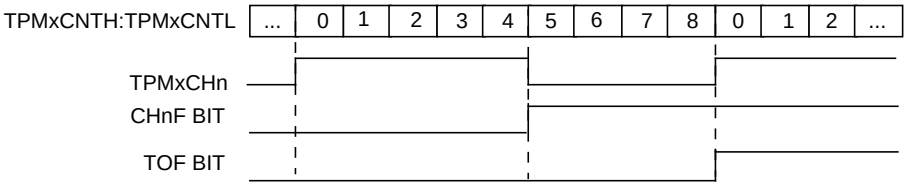



**Figure 16-3. High-True Pulse of an Edge-Aligned PWM**

TPMxMODH:TPMxMODL = 0x0008
TPMxCnVH:TPMxCnVL = 0x0005

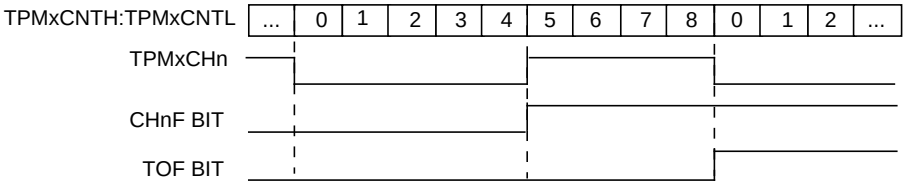



**Figure 16-4. Low-True Pulse of an Edge-Aligned PWM**

When the TPM is configured for center-aligned PWM (and ELSnB:ELSnA not = 0:0), the data direction for all channels in this TPM are overridden, the TPMxCHn pins are forced to be outputs controlled by the TPM, and the ELSnA bits control the polarity of each TPMxCHn output. If ELSnB:ELSnA=1:0, the corresponding TPMxCHn pin is cleared when the timer counter is counting up, and the channel value register matches the timer counter; the TPMxCHn pin is set when the timer counter is counting down, and the channel value register matches the timer counter. If ELSnA=1, the corresponding TPMxCHn pin is set when the timer counter is counting up and the channel value register matches the timer counter; the TPMxCHn pin is cleared when the timer counter is counting down and the channel value register matches the timer counter.

TPMxMODH:TPMxMODL = 0x0008
TPMxCnVH:TPMxCnVL = 0x0005

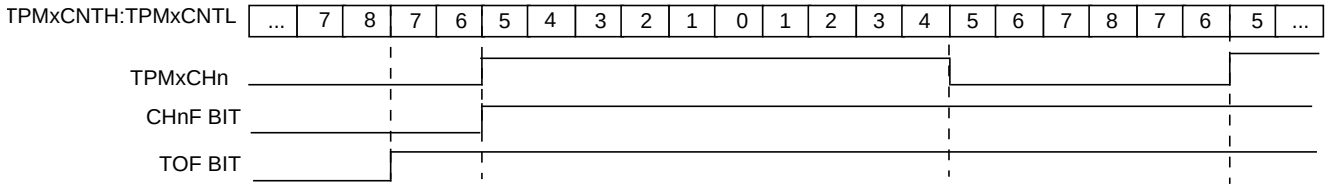



**Figure 16-5. High-True Pulse of a Center-Aligned PWM**

TPMxMODH:TPMxMODL = 0x0008
TPMxCnVH:TPMxCnVL = 0x0005

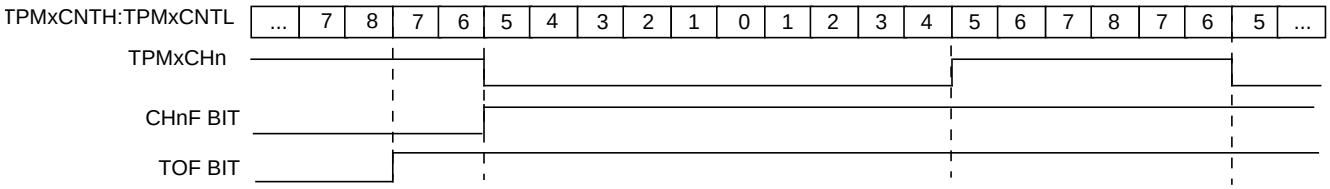



**Figure 16-6. Low-True Pulse of a Center-Aligned PWM**

## 16.3 Register Definition

This section consists of register descriptions in address order.

### 16.3.1 TPM Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits used to configure the interrupt enable, TPM configuration, clock source, and prescale factor. These controls relate to all channels within this timer module.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | TOF | TOIE | CPWMS | CLKSB | CLKSA | PS2 | PS1 | PS0 |
| W | 0 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-7. TPM Status and Control Register (TPMxSC)**

**Table 16-3. TPMxSC Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TOF | Timer overflow flag. This read/write flag is set when the TPM counter resets to 0x0000 after reaching the modulo value programmed in the TPM counter modulo registers. Clear TOF by reading the TPM status and control register when TOF is set and then writing a logic 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. This is done so a TOF interrupt request cannot be lost during the clearing sequence for a previous TOF. Reset clears TOF. Writing a logic 1 to TOF has no effect.<br>0 TPM counter has not reached modulo value or overflow<br>1 TPM counter has overflowed |
| 6<br>TOIE | Timer overflow interrupt enable. This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals one. Reset clears TOIE.<br>0 TOF interrupts inhibited (use for software polling)<br>1 TOF interrupts enabled |
| 5<br>CPWMS | Center-aligned PWM select. When present, this read/write bit selects CPWM operating mode. By default, the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up/down counting mode for CPWM functions. Reset clears CPWMS.<br>0 All channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register.<br>1 All channels operate in center-aligned PWM mode. |
| 4–3<br>CLKS[B:A] | Clock source selects. As shown in Table 16-4, this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The fixed system clock source is only meaningful in systems with a PLL-based or FLL-based system clock. When there is no PLL or FLL, the fixed-system clock source is the same as the bus rate clock. The external source is synchronized to the bus clock by TPM module, and the fixed system clock source (when a PLL or FLL is present) is synchronized to the bus clock by an on-chip synchronization circuit. When a PLL or FLL is present but not enabled, the fixed-system clock source is the same as the bus-rate clock. |
| 2–0<br>PS[2:0] | Prescale factor select. This 3-bit field selects one of 8 division factors for the TPM clock input as shown in Table 16-5. This prescaler is located after any clock source synchronization or clock source selection so it affects the clock source selected to drive the TPM system. The new prescale factor will affect the clock source on the next system clock cycle after the new value is updated into the register bits. |

**Table 16-4. TPM-Clock-Source Selection**

| CLKSB:CLKSA | TPM Clock Source to Prescaler Input |
|---|---|
| 00 | No clock selected (TPM counter disable) |
| 01 | Bus rate clock |
| 10 | Fixed system clock |
| 11 | External source |

**Table 16-5. Prescale Factor Selection**

| PS2:PS1:PS0 | TPM Clock Source Divided-by |
|---|---|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |

## 16.3.2 TPM-Counter Registers (TPMxCNTH:TPMxCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMxCNTH or TPMxCNTL) latches the contents of both bytes into a buffer where they remain latched until the other half is read. This allows coherent 16-bit reads in either big-endian or little-endian order which makes this more friendly to various compiler implementations. The coherency mechanism is automatically restarted by an MCU reset or any write to the timer status/control register (TPMxSC).

Reset clears the TPM counter registers. Writing any value to TPMxCNTH or TPMxCNTL also clears the TPM counter (TPMxCNTH:TPMxCNTL) and resets the coherency mechanism, regardless of the data involved in the write.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| W | Any write to TPMxCNTH clears the 16-bit counter | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-8. TPM Counter Register High (TPMxCNTH)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| W | Any write to TPMxCNTL clears the 16-bit counter | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-9. TPM Counter Register Low (TPMxCNTL)**

When BDM is active, the timer counter is frozen (this is the value that will be read by user); the coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both counter halves are read while BDM is active. This assures that if the user was in the middle of reading a 16-bit register when BDM became active, it will read the appropriate value from the other half of the 16-bit value after returning to normal execution.

In BDM mode, writing any value to TPMxSC, TPMxCNTH or TPMxCNTL registers resets the read coherency mechanism of the TPMxCNTH:L registers, regardless of the data involved in the write.

## 16.3.3 TPM Counter Modulo Registers (TPMxMODH:TPMxMODL)

The read/write TPM modulo registers contain the modulo value for the TPM counter. After the TPM counter reaches the modulo value, the TPM counter resumes counting from 0x0000 at the next clock, and the overflow flag (TOF) becomes set. Writing to TPMxMODH or TPMxMODL inhibits the TOF bit and overflow interrupts until the other byte is written. Reset sets the TPM counter modulo registers to 0x0000 which results in a free running timer counter (modulo disabled).

Writing to either byte (TPMxMODH or TPMxMODL) latches the value into a buffer and the registers are updated with the value of their write buffer according to the value of CLKSB:CLKSA bits, so:

- If (CLKSB:CLKSA = 0:0), then the registers are updated when the second byte is written
- If (CLKSB:CLKSA not = 0:0), then the registers are updated after both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter, the update is made when the TPM counter changes from 0xFFFE to 0xFFFF

The latching mechanism may be manually reset by writing to the TPMxSC address (whether BDM is active or not).

When BDM is active, the coherency mechanism is frozen (unless reset by writing to TPMxSC register) such that the buffer latches remain in the state they were in when the BDM became active, even if one or both halves of the modulo register are written while BDM is active. Any write to the modulo registers bypasses the buffer latches and directly writes to the modulo register while BDM is active.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-10. TPM Counter Modulo Register High (TPMxMODH)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset the TPM counter before writing to the TPM modulo registers to avoid confusion about when the first counter overflow will occur.

## 16.3.4 TPM Channel n Status and Control Register (TPMxCnSC)

TPMxCnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | CHnF | CHnIE | MSnB | MSnA | ELSnB | ELSnA | 0 | 0 |
| W | 0 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 16-12. TPM Channel n Status and Control Register (TPMxCnSC)**

**Table 16-6. TPMxCnSC Field Descriptions**

| Field | Description |
|---|---|
| 7<br>CHnF | Channel n flag. When channel n is an input-capture channel, this read/write bit is set when an active edge occurs on the channel n pin. When channel n is an output compare or edge-aligned/center-aligned PWM channel, CHnF is set when the value in the TPM counter registers matches the value in the TPM channel n value registers. When channel n is an edge-aligned/center-aligned PWM channel and the duty cycle is set to 0% or 100%, CHnF will not be set even when the value in the TPM counter registers matches the value in the TPM channel n value registers.<br>A corresponding interrupt is requested when CHnF is set and interrupts are enabled (CHnIE = 1). Clear CHnF by reading TPMxCnSC while CHnF is set and then writing a logic 0 to CHnF. If another interrupt request occurs before the clearing sequence is complete, the sequence is reset so CHnF remains set after the clear sequence completed for the earlier CHnF. This is done so a CHnF interrupt request cannot be lost due to clearing a previous CHnF.<br>Reset clears the CHnF bit. Writing a logic 1 to CHnF has no effect.<br>0 No input capture or output compare event occurred on channel n<br>1 Input capture or output compare event on channel n |
| 6<br>CHnIE | Channel n interrupt enable. This read/write bit enables interrupts from channel n. Reset clears CHnIE.<br>0 Channel n interrupt requests disabled (use for software polling)<br>1 Channel n interrupt requests enabled |
| 5<br>MSnB | Mode select B for TPM channel n. When CPWMS=0, MSnB=1 configures TPM channel n for edge-aligned PWM mode. Refer to the summary of channel mode and setup controls in Table 16-7. |

**Table 16-6. TPMxCnSC Field Descriptions (continued)**

| Field | Description |
|---|---|
| 4<br>MSnA | Mode select A for TPM channel n. When CPWMS=0 and MSnB=0, MSnA configures TPM channel n for input-capture mode or output compare mode. Refer to Table 16-7 for a summary of channel mode and setup controls.<br>**Note:** If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger. |
| 3–2<br>ELSnB<br>ELSnA | Edge/level select bits. Depending upon the operating mode for the timer channel as set by CPWMS:MSnB:MSnA and shown in Table 16-7, these bits select the polarity of the input edge that triggers an input capture event, select the level that will be driven in response to an output compare match, or select the polarity of the PWM output. Setting ELSnB:ELSnA to 0:0 configures the related timer pin as a general purpose I/O pin not related to any timer functions. This function is typically used to temporarily disable an input capture channel or to make the timer pin available as a general purpose I/O pin when the associated timer channel is set up as a software timer that does not require the use of a pin. |

**Table 16-7. Mode, Edge, and Level Selection**

| CPWMS | MSnB:MSnA | ELSnB:ELSnA | Mode | Configuration |
|---|---|---|---|---|
| X | XX | 00 | Pin not used for TPM - revert to general purpose I/O or other peripheral control | |
| 0 | 00 | 01 | Input capture | Capture on rising edge only |
| | | 10 | | Capture on falling edge only |
| | | 11 | | Capture on rising or falling edge |
| | 01 | 00 | Output compare | Software compare only |
| | | 01 | | Toggle output on compare |
| | | 10 | | Clear output on compare |
| | | 11 | | Set output on compare |
| | 1X | 10 | Edge-aligned PWM | High-true pulses (clear output on compare) |
| | | X1 | | Low-true pulses (set output on compare) |
| 1 | XX | 10 | Center-aligned PWM | High-true pulses (clear output on compare-up) |
| | | X1 | | Low-true pulses (set output on compare-up) |

## 16.3.5 TPM Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel registers are cleared by reset.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-13. TPM Channel Value Register High (TPMxCnVH)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 16-14. TPM Channel Value Register Low (TPMxCnVL)**

In input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain latched until the other half is read. This latching mechanism also resets (becomes unlatched) when the TPMxCnSC register is written (whether BDM mode is active or not). Any write to the channel registers will be ignored during the input capture mode.

When BDM is active, the coherency mechanism is frozen (unless reset by writing to TPMxCnSC register) such that the buffer latches remain in the state they were in when the BDM became active, even if one or both halves of the channel register are read while BDM is active. This assures that if the user was in the middle of reading a 16-bit register when BDM became active, it will read the appropriate value from the other half of the 16-bit value after returning to normal execution. The value read from the TPMxCnVH and TPMxCnVL registers in BDM mode is the value of these registers and not the value of their read buffer.

In output compare or PWM modes, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer. After both bytes are written, they are transferred as a coherent 16-bit value into the timer-channel registers according to the value of CLKSB:CLKSA bits and the selected mode, so:

- If (CLKSB:CLKSA = 0:0), then the registers are updated when the second byte is written.
- If (CLKSB:CLKSA not = 0:0 and in output compare mode) then the registers are updated after the second byte is written and on the next change of the TPM counter (end of the prescaler counting).
- If (CLKSB:CLKSA not = 0:0 and in EPWM or CPWM modes), then the registers are updated after the both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter then the update is made when the TPM counter changes from 0xFFFE to 0xFFFF.

The latching mechanism may be manually reset by writing to the TPMxCnSC register (whether BDM mode is active or not). This latching mechanism allows coherent 16-bit writes in either big-endian or little-endian order which is friendly to various compiler implementations.

When BDM is active, the coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active even if one or both halves of the channel register are written while BDM is active. Any write to the channel registers bypasses the buffer latches and directly write to the channel register while BDM is active. The values written to the channel register while BDM is active

are used for PWM & output compare operation once normal execution resumes. Writes to the channel registers while BDM is active do not interfere with partial completion of a coherency sequence. After the coherency mechanism has been fully exercised, the channel registers are updated using the buffered values written (while BDM was not active) by the user.

## 16.4 Functional Description

All TPM functions are associated with a central 16-bit counter which allows flexible selection of the clock source and prescale factor. There is also a 16-bit modulo register associated with the main counter.

The CPWMS control bit chooses between center-aligned PWM operation for all channels in the TPM (CPWMS=1) or general purpose timing functions (CPWMS=0) where each channel can independently be configured to operate in input capture, output compare, or edge-aligned PWM mode. The CPWMS control bit is located in the main TPM status and control register because it affects all channels within the TPM and influences the way the main counter operates. (In CPWM mode, the counter changes to an up/down mode rather than the up-counting mode used for general purpose timer functions.)

The following sections describe the main counter and each of the timer operating modes (input capture, output compare, edge-aligned PWM, and center-aligned PWM). Because details of pin operation and interrupt activity depend upon the operating mode, these topics will be covered in the associated mode explanation sections.

### 16.4.1 Counter

All timer functions are based on the main 16-bit counter (TPMxCNTH:TPMxCNTL). This section discusses selection of the clock source, end-of-count overflow, up-counting vs. up/down counting, and manual counter reset.

#### 16.4.1.1 Counter Clock Source

The 2-bit field, CLKSB:CLKSA, in the timer status and control register (TPMxSC) selects one of three possible clock sources or OFF (which effectively disables the TPM). See Table 16-4. After any MCU reset, CLKSB:CLKSA=0:0 so no clock source is selected, and the TPM is in a very low power state. These control bits may be read or written at any time and disabling the timer (writing 00 to the CLKSB:CLKSA field) does not affect the values in the counter or other timer registers.

**Table 16-8. TPM Clock Source Selection**

| CLKSB:CLKSA | TPM Clock Source to Prescaler Input |
|---|---|
| 00 | No clock selected (TPM counter disabled) |
| 01 | Bus rate clock |
| 10 | Fixed system clock |
| 11 | External source |

The bus rate clock is the main system bus clock for the MCU. This clock source requires no synchronization because it is the clock that is used for all internal MCU activities including operation of the CPU and buses.

In MCUs that have no PLL and FLL or the PLL and FLL are not engaged, the fixed system clock source is the same as the bus-rate-clock source, and it does not go through a synchronizer. When a PLL or FLL is present and engaged, a synchronizer is required between the crystal divided-by two clock source and the timer counter so counter transitions will be properly aligned to bus-clock transitions. A synchronizer will be used at chip level to synchronize the crystal-related source clock to the bus clock.

The external clock source may be connected to any TPM channel pin. This clock source always has to pass through a synchronizer to assure that counter transitions are properly aligned to bus clock transitions. The bus-rate clock drives the synchronizer; therefore, to meet Nyquist criteria even with jitter, the frequency of the external clock source must not be faster than the bus rate divided-by four. With ideal clocks the external clock can be as fast as bus clock divided by four.

When the external clock source shares the TPM channel pin, this pin should not be used for other channel timing functions. For example, it would be ambiguous to configure channel 0 for input capture when the TPM channel 0 pin was also being used as the timer external clock source. (It is the user's responsibility to avoid such settings.) The TPM channel could still be used in output compare mode for software timing functions (pin controls set not to affect the TPM channel pin).

### 16.4.1.2 Counter Overflow and Modulo Reset

An interrupt flag and enable are associated with the 16-bit main counter. The flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE=0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE=1) where a static hardware interrupt is generated whenever the TOF flag is equal to one.

The conditions causing TOF to become set depend on whether the TPM is configured for center-aligned PWM (CPWMS=1). In the simplest mode, there is no modulus limit and the TPM is not in CPWMS=1 mode. In this case, the 16-bit timer counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the TPM is in center-aligned PWM mode (CPWMS=1), the TOF flag gets set as the counter changes direction at the end of the count value set in the modulus register (that is, at the transition from the value set in the modulus register to the next lower count value). This corresponds to the end of a PWM period (the 0x0000 count value corresponds to the center of a period).

#### 16.4.1.3 Counting Modes

The main timer counter has two counting modes. When center-aligned PWM is selected (CPWMS=1), the counter operates in up/down counting mode. Otherwise, the counter operates as a simple up counter. As an up counter, the timer counter counts from 0x0000 through its terminal count and then continues with 0x0000. The terminal count is 0xFFFF or a modulus value in TPMxMODH:TPMxMODL.

When center-aligned PWM operation is specified, the counter counts up from 0x0000 through its terminal count and then down to 0x0000 where it changes back to up counting. Both 0x0000 and the terminal count value are normal length counts (one timer clock period long). In this mode, the timer overflow flag (TOF) becomes set at the end of the terminal-count period (as the count changes to the next lower count value).

#### 16.4.1.4 Manual Counter Reset

The main timer counter can be manually reset at any time by writing any value to either half of TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only half of the counter was read before resetting the count.

### 16.4.2 Channel Mode Selection

Provided CPWMS=0, the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and edge-aligned PWM.

#### 16.4.2.1 Input Capture Mode

With the input-capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input-capture channel, the TPM latches the contents of the TPM counter into the channel-value registers (TPMxCnVH:TPMxCnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

In input capture mode, the TPMxCnVH and TPMxCnVL registers are read only.

When either half of the 16-bit capture register is read, the other half is latched into a buffer to support coherent 16-bit accesses in big-endian or little-endian order. The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An input capture event sets a flag bit (CHnF) which may optionally generate a CPU interrupt request.

While in BDM, the input capture function works as configured by the user. When an external event occurs, the TPM latches the contents of the TPM counter (which is frozen because of the BDM mode) into the channel value registers and sets the flag bit.

#### 16.4.2.2 Output Compare Mode

With the output-compare function, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter reaches the value in the channel-value registers of an output-compare channel, the TPM can set, clear, or toggle the channel pin.

In output compare mode, values are transferred to the corresponding timer channel registers only after both 8-bit halves of a 16-bit register have been written and according to the value of CLKSB:CLKSA bits, so:

- If (CLKSB:CLKSA = 0:0), the registers are updated when the second byte is written
- If (CLKSB:CLKSA not = 0:0), the registers are updated at the next change of the TPM counter (end of the prescaler counting) after the second byte is written.

The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An output compare event sets a flag bit (CHnF) which may optionally generate a CPU-interrupt request.

### 16.4.2.3 Edge-Aligned PWM Mode

This type of PWM output uses the normal up-counting mode of the timer counter (CPWMS=0) and can be used when other channels in the same TPM are configured for input capture or output compare functions. The period of this PWM signal is determined by the value of the modulus register (TPMxMODH:TPMxMODL) plus 1. The duty cycle is determined by the setting in the timer channel register (TPMxCnVH:TPMxCnVL). The polarity of this PWM signal is determined by the setting in the ELSnA control bit. 0% and 100% duty cycle cases are possible.

The output compare value in the TPM channel registers determines the pulse width (duty cycle) of the PWM signal (Figure 16-15). The time between the modulus overflow and the output compare is the pulse width. If ELSnA=0, the counter overflow forces the PWM signal high, and the output compare forces the PWM signal low. If ELSnA=1, the counter overflow forces the PWM signal low, and the output compare forces the PWM signal high.

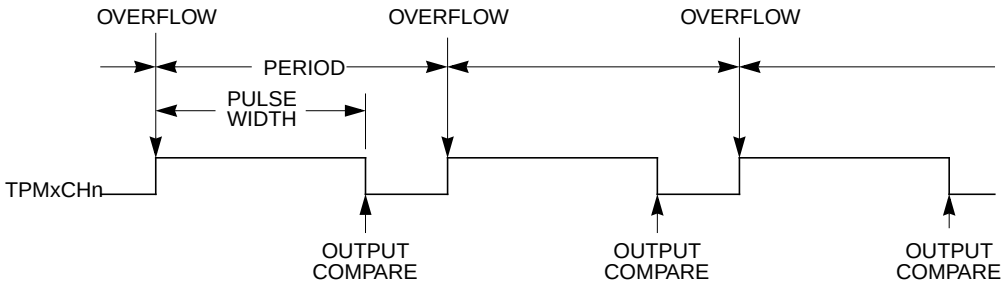



**Figure 16-15. PWM Period and Pulse Width (ELSnA=0)**

When the channel value register is set to 0x0000, the duty cycle is 0%. 100% duty cycle can be achieved by setting the timer-channel register (TPMxCnVH:TPMxCnVL) to a value greater than the modulus setting. This implies that the modulus setting must be less than 0xFFFF in order to get 100% duty cycle.

Because the TPM may be used in an 8-bit MCU, the settings in the timer channel registers are buffered to ensure coherent 16-bit updates and to avoid unexpected PWM pulse widths. Writes to any of the registers TPMxCnVH and TPMxCnVL, actually write to buffer registers. In edge-aligned PWM mode, values are transferred to the corresponding timer-channel registers according to the value of CLKSB:CLKSA bits, so:

- If (CLKSB:CLKSA = 0:0), the registers are updated when the second byte is written
- If (CLKSB:CLKSA not = 0:0), the registers are updated after the both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If

the TPM counter is a free-running counter then the update is made when the TPM counter changes from 0xFFFE to 0xFFFF.

### 16.4.2.4 Center-Aligned PWM Mode

This type of PWM output uses the up/down counting mode of the timer counter (CPWMS=1). The output compare value in TPMxCnVH:TPMxCnVL determines the pulse width (duty cycle) of the PWM signal while the period is determined by the value in TPMxMODH:TPMxMODL. TPMxMODH:TPMxMODL should be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results. ELSnA will determine the polarity of the CPWM output.

pulse width = 2 x (TPMxCnVH:TPMxCnVL)

period = 2 x (TPMxMODH:TPMxMODL); TPMxMODH:TPMxMODL=0x0001-0x7FFF

If the channel-value register TPMxCnVH:TPMxCnVL is zero or negative (bit 15 set), the duty cycle will be 0%. If TPMxCnVH:TPMxCnVL is a positive value (bit 15 clear) and is greater than the (non-zero) modulus setting, the duty cycle will be 100% because the duty cycle compare will never occur. This implies the usable range of periods set by the modulus register is 0x0001 through 0x7FFE (0x7FFF if you do not need to generate 100% duty cycle). This is not a significant limitation. The resulting period would be much longer than required for normal applications.

TPMxMODH:TPMxMODL=0x0000 is a special case that should not be used with center-aligned PWM mode. When CPWMS=0, this case corresponds to the counter running free from 0x0000 through 0xFFFF, but when CPWMS=1 the counter needs a valid match to the modulus register somewhere other than at 0x0000 in order to change directions from up-counting to down-counting.

The output compare value in the TPM channel registers (times 2) determines the pulse width (duty cycle) of the CPWM signal (Figure 16-16). If ELSnA=0, a compare occurred while counting up forces the CPWM output signal low and a compare occurred while counting down forces the output high. The counter counts up until it reaches the modulo setting in TPMxMODH:TPMxMODL, then counts down until it reaches zero. This sets the period equal to two times TPMxMODH:TPMxMODL.

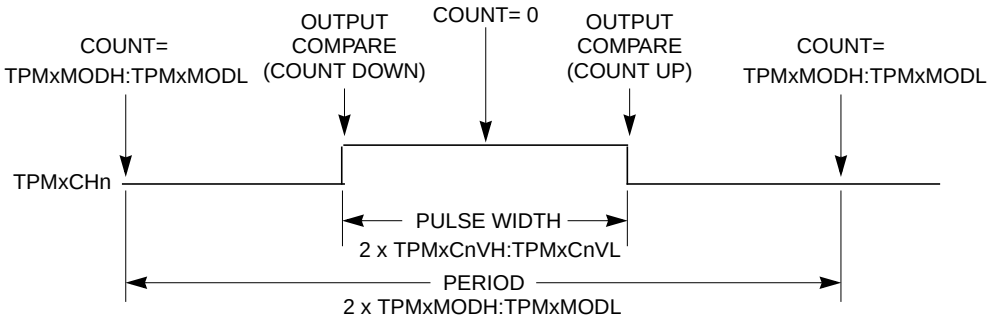



**Figure 16-16. CPWM Period and Pulse Width (ELSnA=0)**

Center-aligned PWM outputs typically produce less noise than edge-aligned PWMs because fewer I/O pin transitions are lined up at the same system clock edge. This type of PWM is also required for some types of motor drives.

Input capture, output compare, and edge-aligned PWM functions do not make sense when the counter is operating in up/down counting mode so this implies that all active channels within a TPM must be used in CPWM mode when CPWMS=1.

The TPM may be used in an 8-bit MCU. The settings in the timer channel registers are buffered to ensure coherent 16-bit updates and to avoid unexpected PWM pulse widths. Writes to any of the registers TPMxMODH, TPMxMODL, TPMxCnVH, and TPMxCnVL, actually write to buffer registers.

In center-aligned PWM mode, the TPMxCnVH:L registers are updated with the value of their write buffer according to the value of CLKSB:CLKSA bits, so:

- If (CLKSB:CLKSA = 0:0), the registers are updated when the second byte is written
- If (CLKSB:CLKSA not = 0:0), the registers are updated after the both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter, the update is made when the TPM counter changes from 0xFFFE to 0xFFFF.

When TPMxCNTH:TPMxCNTL=TPMxMODH:TPMxMODL, the TPM can optionally generate a TOF interrupt (at the end of this count).

Writing to TPMxSC cancels any values written to TPMxMODH and/or TPMxMODL and resets the coherency mechanism for the modulo registers. Writing to TPMxCnSC cancels any values written to the channel value registers and resets the coherency mechanism for TPMxCnVH:TPMxCnVL.

## 16.5 Reset Overview

### 16.5.1 General

The TPM is reset whenever any MCU reset occurs.

### 16.5.2 Description of Reset Operation

Reset clears the TPMxSC register which disables clocks to the TPM and disables timer overflow interrupts (TOIE=0). CPWMS, MSnB, MSnA, ELSnB, and ELSnA are all cleared which configures all TPM channels for input-capture operation with the associated pins disconnected from I/O pin logic (so all MCU pins related to the TPM revert to general purpose I/O pins).

## 16.6 Interrupts

### 16.6.1 General

The TPM generates an optional interrupt for the main counter overflow and an interrupt for each channel. The meaning of channel interrupts depends on each channel’s mode of operation. If the channel is configured for input capture, the interrupt flag is set each time the selected input capture edge is recognized. If the channel is configured for output compare or PWM modes, the interrupt flag is set each time the main timer counter matches the value in the 16-bit channel value register.

All TPM interrupts are listed in Table 16-9 which shows the interrupt name, the name of any local enable that can block the interrupt request from leaving the TPM and getting recognized by the separate interrupt processing logic.

**Table 16-9. Interrupt Summary**

| Interrupt | Local Enable | Source | Description |
|---|---|---|---|
| TOF | TOIE | Counter overflow | Set each time the timer counter reaches its terminal count (at transition to next count value which is usually 0x0000) |
| CHnF | CHnIE | Channel event | An input capture or output compare event took place on channel n |

The TPM module will provide a high-true interrupt signal. Vectors and priorities are determined at chip integration time in the interrupt module so refer to the user's guide for the interrupt module or to the chip's complete documentation for details.

## 16.6.2 Description of Interrupt Operation

For each interrupt source in the TPM, a flag bit is set upon recognition of the interrupt condition such as timer overflow, channel-input capture, or output-compare events. This flag may be read (polled) by software to determine that the action has occurred, or an associated enable bit (TOIE or CHnIE) can be set to enable hardware interrupt generation. While the interrupt enable bit is set, a static interrupt will generate whenever the associated interrupt flag equals one. The user's software must perform a sequence of steps to clear the interrupt flag before returning from the interrupt-service routine.

TPM interrupt flags are cleared by a two-step process including a read of the flag bit while it is set (1) followed by a write of zero (0) to the bit. If a new event is detected between these two steps, the sequence is reset and the interrupt flag remains set after the second step to avoid the possibility of missing the new event.

### 16.6.2.1 Timer Overflow Interrupt (TOF) Description

The meaning and details of operation for TOF interrupts varies slightly depending upon the mode of operation of the TPM system (general purpose timing functions versus center-aligned PWM operation). The flag is cleared by the two step sequence described above.

#### 16.6.2.1.1 Normal Case

Normally TOF is set when the timer counter changes from 0xFFFF to 0x0000. When the TPM is not configured for center-aligned PWM (CPWMS=0), TOF gets set when the timer counter changes from the terminal count (the value in the modulo register) to 0x0000. This case corresponds to the normal meaning of counter overflow.

#### 16.6.2.1.2 Center-Aligned PWM Case

When CPWMS=1, TOF gets set when the timer counter changes direction from up-counting to down-counting at the end of the terminal count (the value in the modulo register). In this case the TOF corresponds to the end of a PWM period.

### 16.6.2.2 Channel Event Interrupt Description

The meaning of channel interrupts depends on the channel's current mode (input-capture, output-compare, edge-aligned PWM, or center-aligned PWM).

#### 16.6.2.2.1 Input Capture Events

When a channel is configured as an input capture channel, the ELSnB:ELSnA control bits select no edge (off), rising edges, falling edges or any edge as the edge which triggers an input capture event. When the selected edge is detected, the interrupt flag is set. The flag is cleared by the two-step sequence described in Section 16.6.2, "Description of Interrupt Operation."

#### 16.6.2.2.2 Output Compare Events

When a channel is configured as an output compare channel, the interrupt flag is set each time the main timer counter matches the 16-bit value in the channel value register. The flag is cleared by the two-step sequence described Section 16.6.2, "Description of Interrupt Operation."

#### 16.6.2.2.3 PWM End-of-Duty-Cycle Events

For channels configured for PWM operation there are two possibilities. When the channel is configured for edge-aligned PWM, the channel flag gets set when the timer counter matches the channel value register which marks the end of the active duty cycle period. When the channel is configured for center-aligned PWM, the timer count matches the channel value register twice during each PWM cycle. In this CPWM case, the channel flag is set at the start and at the end of the active duty cycle period which are the times when the timer counter matches the channel value register. The flag is cleared by the two-step sequence described Section 16.6.2, "Description of Interrupt Operation."

## 16.7 The Differences from TPM v2 to TPM v3

1. Write to TPMxCNTH:L registers (Section 16.3.2, "TPM-Counter Registers (TPMxCNTH:TPMxCNTL)) [SE110-TPM case 7]

   Any write to TPMxCNTH or TPMxCNTL registers in TPM v3 clears the TPM counter (TPMxCNTH:L) and the prescaler counter. Instead, in the TPM v2 only the TPM counter is cleared in this case.

2. Read of TPMxCNTH:L registers (Section 16.3.2, "TPM-Counter Registers (TPMxCNTH:TPMxCNTL))

   — In TPM v3, any read of TPMxCNTH:L registers during BDM mode returns the value of the TPM counter that is frozen. In TPM v2, if only one byte of the TPMxCNTH:L registers was read before the BDM mode became active, then any read of TPMxCNTH:L registers during

BDM mode returns the latched value of TPMxCNTH:L from the read buffer instead of the frozen TPM counter value.

— This read coherency mechanism is cleared in TPM v3 in BDM mode if there is a write to TPMxSC, TPMxCNTH or TPMxCNTL. Instead, in these conditions the TPM v2 does not clear this read coherency mechanism.

3. Read of TPMxCnVH:L registers (Section 16.3.5, “TPM Channel Value Registers (TPMxCnVH:TPMxCnVL)”)

— In TPM v3, any read of TPMxCnVH:L registers during BDM mode returns the value of the TPMxCnVH:L register. In TPM v2, if only one byte of the TPMxCnVH:L registers was read before the BDM mode became active, then any read of TPMxCnVH:L registers during BDM mode returns the latched value of TPMxCNTH:L from the read buffer instead of the value in the TPMxCnVH:L registers.

— This read coherency mechanism is cleared in TPM v3 in BDM mode if there is a write to TPMxCnSC. Instead, in this condition the TPM v2 does not clear this read coherency mechanism.

4. Write to TPMxCnVH:L registers

— Input Capture Mode (Section 16.4.2.1, “Input Capture Mode)

In this mode the TPM v3 does not allow the writes to TPMxCnVH:L registers. Instead, the TPM v2 allows these writes.

— Output Compare Mode (Section 16.4.2.2, “Output Compare Mode)

In this mode and if (CLKSB:CLKSA not = 0:0), the TPM v3 updates the TPMxCnVH:L registers with the value of their write buffer at the next change of the TPM counter (end of the prescaler counting) after the second byte is written. Instead, the TPM v2 always updates these registers when their second byte is written.

The following procedure can be used in the TPM v3 to verify if the TPMxCnVH:L registers were updated with the new value that was written to these registers (value in their write buffer).

...

write the new value to TPMxCnVH:L;

read TPMxCnVH and TPMxCnVL registers;

while (the read value of TPMxCnVH:L is different from the new value written to TPMxCnVH:L)

begin

read again TPMxCnVH and TPMxCnVL;

end

...

In this point, the TPMxCnVH:L registers were updated, so the program can continue and, for example, write to TPMxC0SC without cancelling the previous write to TPMxCnVH:L registers.

— Edge-Aligned PWM (Section 16.4.2.3, “Edge-Aligned PWM Mode)

In this mode and if (CLKSB:CLKSA not = 00), the TPM v3 updates the TPMxCnVH:L registers with the value of their write buffer after that the both bytes were written and when the

TPM counter changes from (TPMxMODH:L - 1) to (TPMxMODH:L). If the TPM counter is a free-running counter, then this update is made when the TPM counter changes from $FFFE to $FFFF. Instead, the TPM v2 makes this update after that the both bytes were written and when the TPM counter changes from TPMxMODH:L to $0000.

— Center-Aligned PWM (Section 16.4.2.4, “Center-Aligned PWM Mode)

In this mode and if (CLKSB:CLKSA not = 00), the TPM v3 updates the TPMxCnVH:L registers with the value of their write buffer after that the both bytes were written and when the TPM counter changes from (TPMxMODH:L - 1) to (TPMxMODH:L). If the TPM counter is a free-running counter, then this update is made when the TPM counter changes from $FFFE to $FFFF. Instead, the TPM v2 makes this update after that the both bytes were written and when the TPM counter changes from TPMxMODH:L to (TPMxMODH:L - 1).

5. Center-Aligned PWM (Section 16.4.2.4, “Center-Aligned PWM Mode)
   — TPMxCnVH:L = TPMxMODH:L [SE110-TPM case 1]

   In this case, the TPM v3 produces 100% duty cycle. Instead, the TPM v2 produces 0% duty cycle.

   — TPMxCnVH:L = (TPMxMODH:L - 1) [SE110-TPM case 2]

   In this case, the TPM v3 produces almost 100% duty cycle. Instead, the TPM v2 produces 0% duty cycle.

   — TPMxCnVH:L is changed from 0x0000 to a non-zero value [SE110-TPM case 3 and 5]

   In this case, the TPM v3 waits for the start of a new PWM period to begin using the new duty cycle setting. Instead, the TPM v2 changes the channel output at the middle of the current PWM period (when the count reaches 0x0000).

   — TPMxCnVH:L is changed from a non-zero value to 0x0000 [SE110-TPM case 4]

   In this case, the TPM v3 finishes the current PWM period using the old duty cycle setting. Instead, the TPM v2 finishes the current PWM period using the new duty cycle setting.

6. Write to TPMxMODH:L registers in BDM mode (Section 16.3.3, “TPM Counter Modulo Registers (TPMxMODH:TPMxMODL))

   In the TPM v3 a write to TPMxSC register in BDM mode clears the write coherency mechanism of TPMxMODH:L registers. Instead, in the TPM v2 this coherency mechanism is not cleared when there is a write to TPMxSC register.

7. Update of EPWM signal when CLKSB:CLKSA = 00

   In the TPM v3 if CLKSB:CLKSA = 00, then the EPWM signal in the channel output is not update (it is frozen while CLKSB:CLKSA = 00). Instead, in the TPM v2 the EPWM signal is updated at the next rising edge of bus clock after a write to TPMxCnSC register.

   The Figure 16-17 and Figure 16-18 show when the EPWM signals generated by TPM v2 and TPM v3 after the reset (CLKSB:CLKSA = 00) and if there is a write to TPMxCnSC register.

EPWM mode
TPMxMODH:TPMxMODL = 0x0007
TPMxCnVH:TPMxCnVL = 0x0005

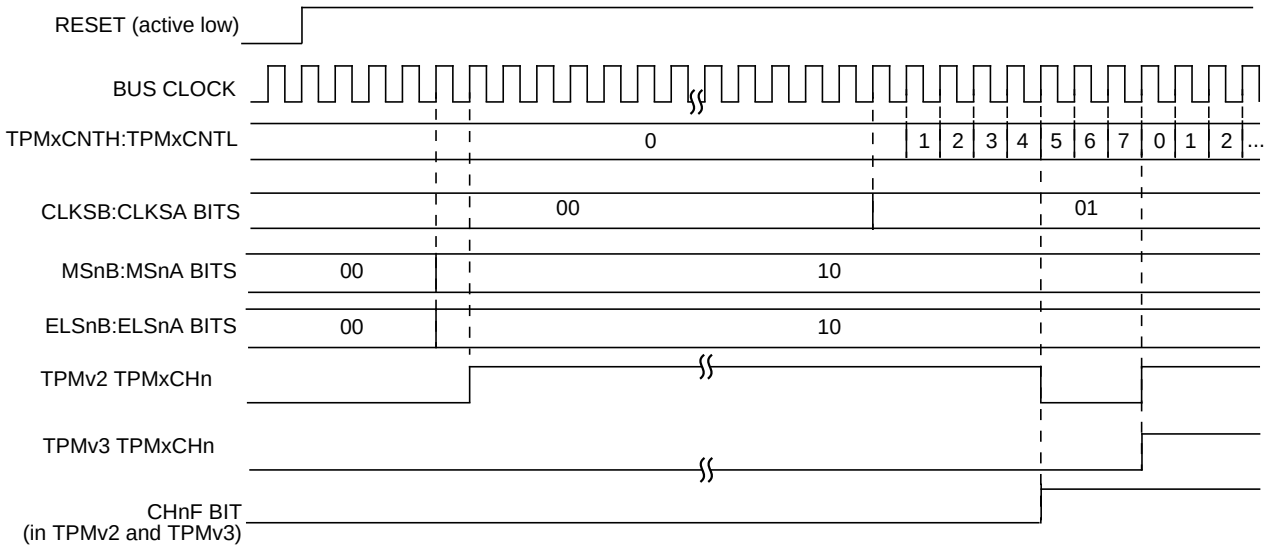



**Figure 16-17. Generation of high-true EPWM signal by TPM v2 and v3 after the reset**

EPWM mode
TPMxMODH:TPMxMODL = 0x0007
TPMxCnVH:TPMxCnVL = 0x0005

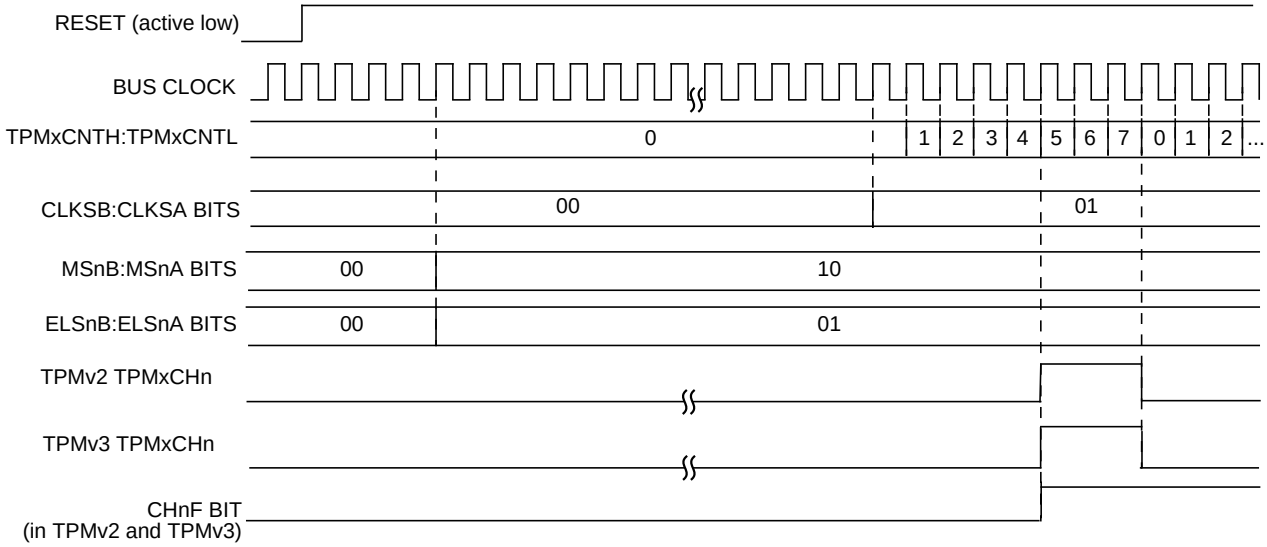



**Figure 16-18. Generation of low-true EPWM signal by TPM v2 and v3 after the reset**

The following procedure can be used in TPM v3 (when the channel pin is also a port pin) to emulate the high-true EPWM generated by TPM v2 after the reset.

...
configure the channel pin as output port pin and set the output pin;
configure the channel to generate the EPWM signal but keep ELSnB:ELSnA as 00;
configure the other registers (TPMxMODH, TPMxMODL, TPMxCnVH, TPMxCnVL, ...);
configure CLKSB:CLKSA bits (TPM v3 starts to generate the high-true EPWM signal, however TPM does not control the channel pin, so the EPWM signal is not available);
wait until the TOF is set (or use the TOF interrupt);
enable the channel output by configuring ELSnB:ELSnA bits (now EPWM signal is available);
...

# Chapter 17
# Development Support

## 17.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip FLASH and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

### 17.1.1 Forcing Active Background

The method for forcing active background mode depends on the specific HCS08 derivative. For the MC9S08SG32 Series, you can force active background after a power-on reset by holding the BKGD pin low as the device exits the reset condition. You can also force active background by driving BKGD low immediately after a serial background command that writes a one to the BDFR bit in the SBDFR register. Other causes of reset including an external pin reset or an internally generated error reset ignore the state of the BKGD pin and reset into normal user mode. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.

### 17.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

Features of the ICE system include:

- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
  - Change-of-flow addresses or
  - Event-only data
- Two types of breakpoints:
  - Tag breakpoints for instruction opcodes
  - Force breakpoints for any address access
- Nine trigger modes:
  - Basic: A-only, A OR B
  - Sequence: A then B
  - Full: A AND B data, A AND NOT B data
  - Event (store data): Event-only B, A then event-only B
  - Range: Inside range ($A \leq address \leq B$), outside range ($address < A$ or $address > B$)

## 17.2 Background Debug Controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.

- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, $\overline{\text{RESET}}$, and sometimes $V_{DD}$. An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes $V_{DD}$ can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

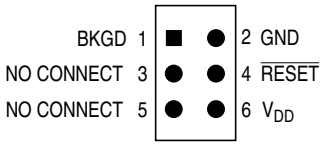



**Figure 17-1. BDM Tool Connector**

## 17.2.1 BKGD Pin Description

BKGD is the single-wire background debug interface pin. The primary function of this pin is for bidirectional serial communication of active background mode commands and data. During reset, this pin is used to select between starting in active background mode or starting the user's application program. This pin is also used to request a timed sync response pulse to allow a host development tool to determine the correct clock frequency for background debug serial communications.

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to Section 17.2.2, "Communication Details."

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Section 17.2.2, "Communication Details," for more detail.

When no debugger pod is connected to the 6-pin BDM interface connector, the internal pullup on BKGD chooses normal operating mode. When a debug pod is connected to BKGD it is possible to force the MCU into active background mode after reset. The specific conditions for forcing active background depend upon the HCS08 derivative (refer to the introduction to this Development Support section). It is not necessary to reset the target MCU to communicate with it through the background debug interface.

### 17.2.2 Communication Details

The BDC serial interface requires the external controller to generate a falling edge on the BKGD pin to indicate the start of each bit time. The external controller provides this falling edge whether data is transmitted or received.

BKGD is a pseudo-open-drain pin that can be driven either by an external controller or by the MCU. Data is transferred MSB first at 16 BDC clock cycles per bit (nominal speed). The interface times out if 512 BDC clock cycles occur between falling edges from the host. Any BDC command that was in progress when this timeout occurs is aborted without affecting the memory or operating mode of the target MCU system.

The custom serial protocol requires the debug pod to know the target BDC communication clock speed.

The clock switch (CLKSW) control bit in the BDC status and control register allows the user to select the BDC clock source. The BDC clock source can either be the bus or the alternate BDC clock source.

The BKGD pin can receive a high or low level or transmit a high or low level. The following diagrams show timing for each of these cases. Interface timing is synchronous to clocks in the target BDC, but asynchronous to the external host. The internal BDC clock signal is shown for reference in counting cycles.

Figure 17-2 shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target HCS08 MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target transmission period, there is no need to treat the line as an open-drain signal during this period.

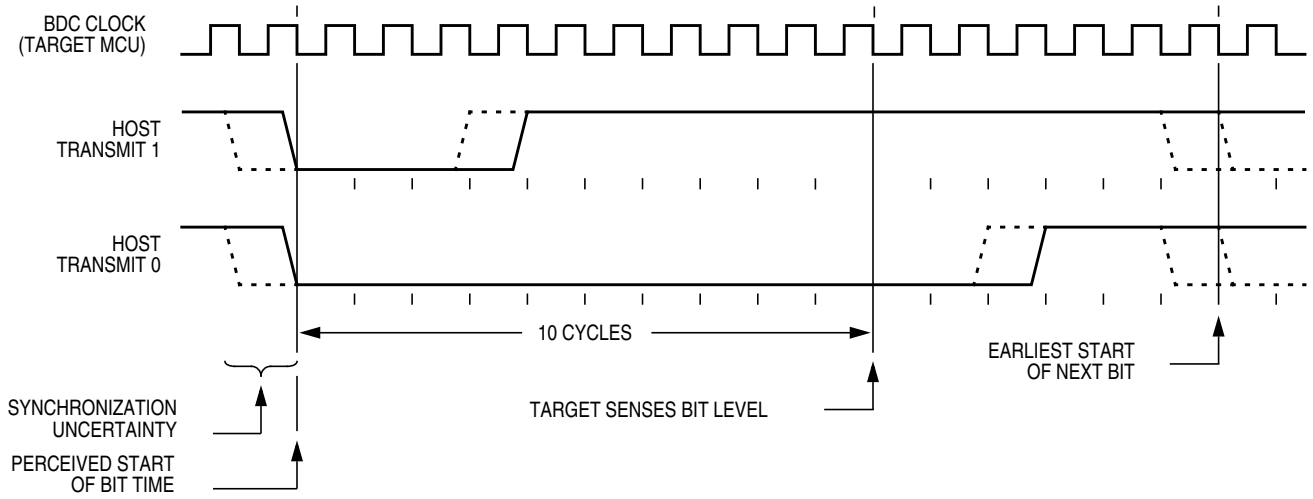



**Figure 17-2. BDC Host-to-Target Serial Bit Timing**

Figure 17-3 shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.

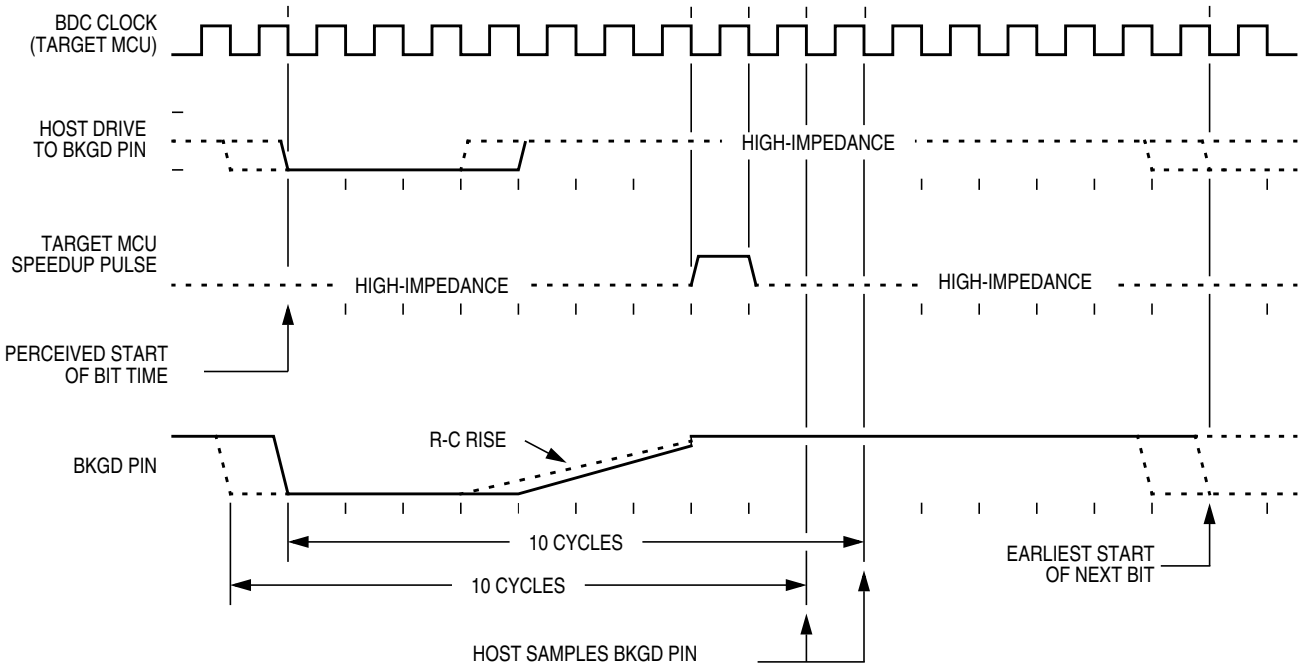



**Figure 17-3. BDC Target-to-Host Serial Bit Timing (Logic 1)**

Figure 17-4 shows the host receiving a logic 0 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target MCU. The host initiates the bit time but the target HCS08 finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 BDC clock cycles, then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 cycles after starting the bit time.

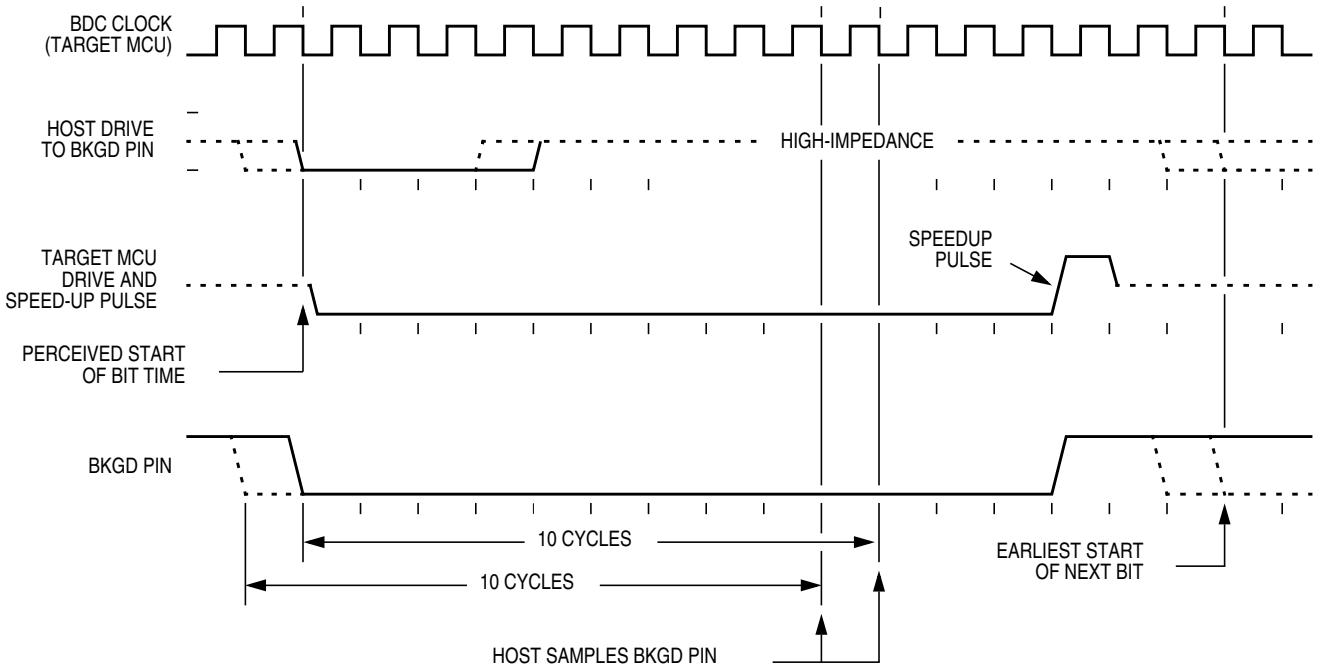



**Figure 17-4. BDM Target-to-Host Serial Bit Timing (Logic 0)**

## 17.2.3 BDC Commands

BDC commands are sent serially from a host computer to the BKGD pin of the target HCS08 MCU. All commands and data are sent MSB-first using a custom BDC communications protocol. Active background mode commands require that the target MCU is currently in the active background mode while non-intrusive commands may be issued at any time whether the target MCU is in active background mode or running a user application program.

Table 17-1 shows all HCS08 BDC commands, a shorthand description of their coding structure, and the meaning of each command.

### Coding Structure Nomenclature

This nomenclature is used in Table 17-1 to describe the coding structure of the BDC commands.

| | | |
|---|---|---|
| | | Commands begin with an 8-bit hexadecimal command code in the host-to-target direction (most significant bit first) |
| / | = | separates parts of the command |
| d | = | delay 16 target BDC clock cycles |
| AAAA | = | a 16-bit address in the host-to-target direction |
| RD | = | 8 bits of read data in the target-to-host direction |
| WD | = | 8 bits of write data in the host-to-target direction |
| RD16 | = | 16 bits of read data in the target-to-host direction |
| WD16 | = | 16 bits of write data in the host-to-target direction |
| SS | = | the contents of BDCSCR in the target-to-host direction (STATUS) |
| CC | = | 8 bits of write data for BDCSCR in the host-to-target direction (CONTROL) |
| RBKP | = | 16 bits of read data in the target-to-host direction (from BDCBKPT breakpoint register) |
| WBKP | = | 16 bits of write data in the host-to-target direction (for BDCBKPT breakpoint register) |

**Table 17-1. BDC Command Summary**

| Command Mnemonic | Active BDM/ Non-intrusive | Coding Structure | Description |
|---|---|---|---|
| SYNC | Non-intrusive | n/a[1] | Request a timed reference pulse to determine target BDC communication speed |
| ACK_ENABLE | Non-intrusive | D5/d | Enable acknowledge protocol. Refer to Freescale document order no. HCS08RMv1/D. |
| ACK_DISABLE | Non-intrusive | D6/d | Disable acknowledge protocol. Refer to Freescale document order no. HCS08RMv1/D. |
| BACKGROUND | Non-intrusive | 90/d | Enter active background mode if enabled (ignore if ENBDM bit equals 0) |
| READ_STATUS | Non-intrusive | E4/SS | Read BDC status from BDCSCR |
| WRITE_CONTROL | Non-intrusive | C4/CC | Write BDC controls in BDCSCR |
| READ_BYTE | Non-intrusive | E0/AAAA/d/RD | Read a byte from target memory |
| READ_BYTE_WS | Non-intrusive | E1/AAAA/d/SS/RD | Read a byte and report status |
| READ_LAST | Non-intrusive | E8/SS/RD | Re-read byte from address just read and report status |
| WRITE_BYTE | Non-intrusive | C0/AAAA/WD/d | Write a byte to target memory |
| WRITE_BYTE_WS | Non-intrusive | C1/AAAA/WD/d/SS | Write a byte and report status |
| READ_BKPT | Non-intrusive | E2/RBKP | Read BDCBKPT breakpoint register |
| WRITE_BKPT | Non-intrusive | C2/WBKP | Write BDCBKPT breakpoint register |
| GO | Active BDM | 08/d | Go to execute the user application program starting at the address currently in the PC |
| TRACE1 | Active BDM | 10/d | Trace 1 user instruction at the address in the PC, then return to active background mode |
| TAGGO | Active BDM | 18/d | Same as GO but enable external tagging (HCS08 devices have no external tagging pin) |
| READ_A | Active BDM | 68/d/RD | Read accumulator (A) |
| READ_CCR | Active BDM | 69/d/RD | Read condition code register (CCR) |
| READ_PC | Active BDM | 6B/d/RD16 | Read program counter (PC) |
| READ_HX | Active BDM | 6C/d/RD16 | Read H and X register pair (H:X) |
| READ_SP | Active BDM | 6F/d/RD16 | Read stack pointer (SP) |
| READ_NEXT | Active BDM | 70/d/RD | Increment H:X by one then read memory byte located at H:X |
| READ_NEXT_WS | Active BDM | 71/d/SS/RD | Increment H:X by one then read memory byte located at H:X. Report status and data. |
| WRITE_A | Active BDM | 48/WD/d | Write accumulator (A) |
| WRITE_CCR | Active BDM | 49/WD/d | Write condition code register (CCR) |
| WRITE_PC | Active BDM | 4B/WD16/d | Write program counter (PC) |
| WRITE_HX | Active BDM | 4C/WD16/d | Write H and X register pair (H:X) |
| WRITE_SP | Active BDM | 4F/WD16/d | Write stack pointer (SP) |
| WRITE_NEXT | Active BDM | 50/WD/d | Increment H:X by one, then write memory byte located at H:X |
| WRITE_NEXT_WS | Active BDM | 51/WD/d/SS | Increment H:X by one, then write memory byte located at H:X. Also report status. |

[1] The SYNC command is a special operation that does not have a command code.

The SYNC command is unlike other BDC commands because the host does not necessarily know the correct communications speed to use for BDC communications until after it has analyzed the response to the SYNC command.

To issue a SYNC command, the host:

- Drives the BKGD pin low for at least 128 cycles of the slowest possible BDC clock (The slowest clock is normally the reference oscillator/64 or the self-clocked rate/64.)
- Drives BKGD high for a brief speedup pulse to get a fast rise time (This speedup pulse is typically one cycle of the fastest clock in the system.)
- Removes all drive to the BKGD pin so it reverts to high impedance
- Monitors the BKGD pin for the sync response pulse

The target, upon detecting the SYNC request from the host (which is a much longer low time than would ever occur during normal BDC communications):

- Waits for BKGD to return to a logic high
- Delays 16 cycles to allow the host to stop driving the high speedup pulse
- Drives BKGD low for 128 BDC clock cycles
- Drives a 1-cycle high speedup pulse to force a fast rise time on BKGD
- Removes all drive to the BKGD pin so it reverts to high impedance

The host measures the low time of this 128-cycle sync response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

### 17.2.4 BDC Hardware Breakpoint

The BDC includes one relatively simple hardware breakpoint that compares the CPU address bus to a 16-bit match value in the BDCBKPT register. This breakpoint can generate a forced breakpoint or a tagged breakpoint. A forced breakpoint causes the CPU to enter active background mode at the first instruction boundary following any access to the breakpoint address. The tagged breakpoint causes the instruction opcode at the breakpoint address to be tagged so that the CPU will enter active background mode rather than executing that instruction if and when it reaches the end of the instruction queue. This implies that tagged breakpoints can only be placed at the address of an instruction opcode while forced breakpoints can be set at any address.

The breakpoint enable (BKPTEN) control bit in the BDC status and control register (BDCSCR) is used to enable the breakpoint logic (BKPTEN = 1). When BKPTEN = 0, its default value after reset, the breakpoint logic is disabled and no BDC breakpoints are requested regardless of the values in other BDC breakpoint registers and control bits. The force/tag select (FTS) control bit in BDCSCR is used to select forced (FTS = 1) or tagged (FTS = 0) type breakpoints.

The on-chip debug module (DBG) includes circuitry for two additional hardware breakpoints that are more flexible than the simple breakpoint in the BDC module.

## 17.3 On-Chip Debug System (DBG)

Because HCS08 devices do not have external address and data buses, the most important functions of an in-circuit emulator have been built onto the chip with the MCU. The debug system consists of an 8-stage FIFO that can store address or data bus information, and a flexible trigger system to decide when to capture bus information and what information to capture. The system relies on the single-wire background debug system to access debug control registers and to read results out of the eight stage FIFO.

The debug module includes control and status registers that are accessible in the user's memory map. These registers are located in the high register space to avoid using valuable direct page memory space.

Most of the debug module's functions are used during development, and user programs rarely access any of the control and status registers for the debug module. The one exception is that the debug system can provide the means to implement a form of ROM patching. This topic is discussed in greater detail in Section 17.3.6, "Hardware Breakpoints."

### 17.3.1 Comparators A and B

Two 16-bit comparators (A and B) can optionally be qualified with the R/W signal and an opcode tracking circuit. Separate control bits allow you to ignore R/W for each comparator. The opcode tracking circuitry optionally allows you to specify that a trigger will occur only if the opcode at the specified address is actually executed as opposed to only being read from memory into the instruction queue. The comparators are also capable of magnitude comparisons to support the inside range and outside range trigger modes. Comparators are disabled temporarily during all BDC accesses.

The A comparator is always associated with the 16-bit CPU address. The B comparator compares to the CPU address or the 8-bit CPU data bus, depending on the trigger mode selected. Because the CPU data bus is separated into a read data bus and a write data bus, the RWAEN and RWA control bits have an additional purpose, in full address plus data comparisons they are used to decide which of these buses to use in the comparator B data bus comparisons. If RWAEN = 1 (enabled) and RWA = 0 (write), the CPU's write data bus is used. Otherwise, the CPU's read data bus is used.

The currently selected trigger mode determines what the debugger logic does when a comparator detects a qualified match condition. A match can cause:

- Generation of a breakpoint to the CPU
- Storage of data bus values into the FIFO
- Starting to store change-of-flow addresses into the FIFO (begin type trace)
- Stopping the storage of change-of-flow addresses into the FIFO (end type trace)

### 17.3.2 Bus Capture Information and FIFO Operation

The usual way to use the FIFO is to setup the trigger mode and other control options, then arm the debugger. When the FIFO has filled or the debugger has stopped storing data into the FIFO, you would read the information out of it in the order it was stored into the FIFO. Status bits indicate the number of words of valid information that are in the FIFO as data is stored into it. If a trace run is manually halted by writing 0 to ARM before the FIFO is full (CNT = 1:0:0:0), the information is shifted by one position and

the host must perform ((8 – CNT) – 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Section 17.3.5, “Trigger Modes”), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

### 17.3.3 Change-of-Flow Information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

### 17.3.4 Tag vs. Force Breakpoints and Triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

A force-type breakpoint waits for the current instruction to finish and then acts upon the breakpoint request. The usual action in response to a breakpoint is to go to active background mode rather than continuing to the next instruction in the user application program.

The tag vs. force terminology is used in two contexts within the debug module. The first context refers to breakpoint requests from the debug module to the CPU. The second refers to match signals from the comparators to the debugger control logic. When a tag-type break request is sent to the CPU, a signal is entered into the instruction queue along with the opcode so that if/when this opcode ever executes, the CPU will effectively replace the tagged opcode with a BGND opcode so the CPU goes to active background mode rather than executing the tagged instruction. When the TRGSEL control bit in the DBGT register is set to select tag-type operation, the output from comparator A or B is qualified by a block of logic in the debug module that tracks opcodes and only produces a trigger to the debugger if the opcode at the compare address is actually executed. There is separate opcode tracking logic for each comparator so more than one compare event can be tracked through the instruction queue at a time.

### 17.3.5 Trigger Modes

The trigger mode controls the overall behavior of a debug run. The 4-bit TRG field in the DBGT register selects one of nine trigger modes. When TRGSEL = 1 in the DBGT register, the output of the comparator must propagate through an opcode tracking circuit before triggering FIFO actions. The BEGIN bit in DBGT chooses whether the FIFO begins storing data when the qualified trigger is detected (begin trace), or the FIFO stores data in a circular fashion from the time it is armed until the qualified trigger is detected (end trigger).

A debug run is started by writing a 1 to the ARM bit in the DBGC register, which sets the ARMF flag and clears the AF and BF flags and the CNT bits in DBGS. A begin-trace debug run ends when the FIFO gets full. An end-trace run ends when the selected trigger event occurs. Any debug run can be stopped manually by writing a 0 to ARM or DBGEN in DBGC.

In all trigger modes except event-only modes, the FIFO stores change-of-flow addresses. In event-only trigger modes, the FIFO stores data in the low-order eight bits of the FIFO.

The BEGIN control bit is ignored in event-only trigger modes and all such debug runs are begin type traces. When TRGSEL = 1 to select opcode fetch triggers, it is not necessary to use R/W in comparisons because opcode tags would only apply to opcode fetches that are always read cycles. It would also be unusual to specify TRGSEL = 1 while using a full mode trigger because the opcode value is normally known at a particular address.

The following trigger mode descriptions only state the primary comparator conditions that lead to a trigger. Either comparator can usually be further qualified with R/W by setting RWAEN (RWBEN) and the corresponding RWA (RWB) value to be matched against R/W. The signal from the comparator with optional R/W qualification is used to request a CPU breakpoint if BRKEN = 1 and TAG determines whether the CPU request will be a tag request or a force request.

**A-Only** — Trigger when the address matches the value in comparator A

**A OR B** — Trigger when the address matches either the value in comparator A or the value in comparator B

**A Then B** — Trigger when the address matches the value in comparator B but only after the address for another cycle matched the value in comparator A. There can be any number of cycles after the A match and before the B match.

**A AND B Data (Full Mode)** — This is called a full mode because address, data, and R/W (optionally) must match within the same bus cycle to cause a trigger event. Comparator A checks address, the low byte of comparator B checks data, and R/W is checked against RWA if RWAEN = 1. The high-order half of comparator B is not used.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

**A AND NOT B Data (Full Mode)** — Address must match comparator A, data must not match the low half of comparator B, and R/W must match RWA if RWAEN = 1. All three conditions must be met within the same bus cycle to cause a trigger.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

**Event-Only B (Store Data)** — Trigger events occur each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

**A Then Event-Only B (Store Data)** — After the address has matched the value in comparator A, a trigger event occurs each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

**Inside Range (A ≤ Address ≤ B)** — A trigger occurs when the address is greater than or equal to the value in comparator A and less than or equal to the value in comparator B at the same time.

**Outside Range (Address < A or Address > B)** — A trigger occurs when the address is either less than the value in comparator A or greater than the value in comparator B.

### 17.3.6 Hardware Breakpoints

The BRKEN control bit in the DBGC register may be set to 1 to allow any of the trigger conditions described in Section 17.3.5, “Trigger Modes,” to be used to generate a hardware breakpoint request to the CPU. TAG in DBGC controls whether the breakpoint request will be treated as a tag-type breakpoint or a force-type breakpoint. A tag breakpoint causes the current opcode to be marked as it enters the instruction queue. If a tagged opcode reaches the end of the pipe, the CPU executes a BGND instruction to go to active background mode rather than executing the tagged opcode. A force-type breakpoint causes the CPU to finish the current instruction and then go to active background mode.

If the background mode has not been enabled (ENBDM = 1) by a serial WRITE_CONTROL command through the BKGD pin, the CPU will execute an SWI instruction instead of going to active background mode.

## 17.4 Register Definition

This section contains the descriptions of the BDC and DBG registers and control bits.

Refer to the high-page register summary in the device overview chapter of this data sheet for the absolute address assignments for all DBG registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

### 17.4.1 BDC Registers and Control Bits

The BDC has two registers:

- The BDC status and control register (BDCSCR) is an 8-bit register containing control and status bits for the background debug controller.
- The BDC breakpoint match register (BDCBKPT) holds a 16-bit breakpoint match address.

These registers are accessed with dedicated serial BDC commands and are not located in the memory space of the target MCU (so they do not have addresses and cannot be accessed by user programs).

Some of the bits in the BDCSCR have write limitations; otherwise, these registers may be read or written at any time. For example, the ENBDM control bit may not be written while the MCU is in active background mode. (This prevents the ambiguous condition of the control bit forbidding active background mode while the MCU is already in active background mode.) Also, the four status bits (BDMACT, WS, WSF, and DVF) are read-only status indicators and can never be written by the WRITE_CONTROL serial BDC command. The clock switch (CLKSW) control bit may be read or written at any time.

### 17.4.1.1 BDC Status and Control Register (BDCSCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | ENBDM | BDMACT | BKPTEN | FTS | CLKSW | WS | WSF | DVF |
| W | | | | | | | | |
| Normal Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset inActive BDM: | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 17-5. BDC Status and Control Register (BDCSCR)**

**Table 17-2. BDCSCR Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ENBDM | **Enable BDM (Permit Active Background Mode)** — Typically, this bit is written to 1 by the debug host shortly after the beginning of a debug session or whenever the debug host resets the target and remains 1 until a normal reset clears it.<br>0 BDM cannot be made active (non-intrusive commands still allowed)<br>1 BDM can be made active to allow active background mode commands |
| 6<br>BDMACT | **Background Mode Active Status** — This is a read-only status bit.<br>0 BDM not active (user application program running)<br>1 BDM active and waiting for serial commands |
| 5<br>BKPTEN | **BDC Breakpoint Enable** — If this bit is clear, the BDC breakpoint is disabled and the FTS (force tag select) control bit and BDCBKPT match register are ignored.<br>0 BDC breakpoint disabled<br>1 BDC breakpoint enabled |
| 4<br>FTS | **Force/Tag Select** — When FTS = 1, a breakpoint is requested whenever the CPU address bus matches the BDCBKPT match register. When FTS = 0, a match between the CPU address bus and the BDCBKPT register causes the fetched opcode to be tagged. If this tagged opcode ever reaches the end of the instruction queue, the CPU enters active background mode rather than executing the tagged opcode.<br>0 Tag opcode at breakpoint address and enter active background mode if CPU attempts to execute that instruction<br>1 Breakpoint match forces active background mode at next instruction boundary (address need not be an opcode) |
| 3<br>CLKSW | **Select Source for BDC Communications Clock** — CLKSW defaults to 0, which selects the alternate BDC clock source.<br>0 Alternate BDC clock source<br>1 MCU bus clock |

**Table 17-2. BDCSCR Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 2<br>WS | **Wait or Stop Status** — When the target CPU is in wait or stop mode, most BDC commands cannot function. However, the BACKGROUND command can be used to force the target CPU out of wait or stop and into active background mode where all BDC commands work. Whenever the host forces the target MCU into active background mode, the host should issue a READ_STATUS command to check that BDMACT = 1 before attempting other BDC commands.<br>0 Target CPU is running user application code or in active background mode (was not in wait or stop mode when background became active)<br>1 Target CPU is in wait or stop mode, or a BACKGROUND command was used to change from wait or stop to active background mode |
| 1<br>WSF | **Wait or Stop Failure Status** — This status bit is set if a memory access command failed due to the target CPU executing a wait or stop instruction at or about the same time. The usual recovery strategy is to issue a BACKGROUND command to get out of wait or stop mode into active background mode, repeat the command that failed, then return to the user program. (Typically, the host would restore CPU registers and stack values and re-execute the wait or stop instruction.)<br>0 Memory access did not conflict with a wait or stop instruction<br>1 Memory access command failed because the CPU entered wait or stop mode |
| 0<br>DVF | **Data Valid Failure Status** — This status bit is not used in the MC9S08SG32 Series because it does not have any slow access memory.<br>0 Memory access did not conflict with a slow memory access<br>1 Memory access command failed because CPU was not finished with a slow memory access |

#### 17.4.1.2 BDC Breakpoint Match Register (BDCBKPT)

This 16-bit register holds the address for the hardware breakpoint in the BDC. The BKPTEN and FTS control bits in BDCSCR are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDCBKPT register but is not accessible to user programs because it is not located in the normal memory map of the MCU. Breakpoints are normally set while the target MCU is in active background mode before running the user application program. For additional information about setup and use of the hardware breakpoint logic in the BDC, refer to Section 17.2.4, “BDC Hardware Breakpoint.”

### 17.4.2 System Background Debug Force Reset Register (SBDFR)

This register contains a single write-only control bit. A serial background mode command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | | | | | | | | BDFR[1] |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

1 BDFR is writable only through serial background mode debug commands, not from user programs.

**Figure 17-6. System Background Debug Force Reset Register (SBDFR)**

**Table 17-3. SBDFR Register Field Description**

| Field | Description |
|---|---|
| 0<br>BDFR | **Background Debug Force Reset** — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program. |

## 17.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

### 17.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

### 17.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

### 17.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

### 17.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

#### 17.4.3.5 Debug FIFO High Register (DBGFH)

This register provides read-only access to the high-order eight bits of the FIFO. Writes to this register have no meaning or effect. In the event-only trigger modes, the FIFO only stores data into the low-order byte of each FIFO word, so this register is not used and will read 0x00.

Reading DBGFH does not cause the FIFO to shift to the next word. When reading 16-bit words out of the FIFO, read DBGFH before reading DBGFL because reading DBGFL causes the FIFO to advance to the next word of information.

#### 17.4.3.6 Debug FIFO Low Register (DBGFL)

This register provides read-only access to the low-order eight bits of the FIFO. Writes to this register have no meaning or effect.

Reading DBGFL causes the FIFO to shift to the next available word of information. When the debug module is operating in event-only modes, only 8-bit data is stored into the FIFO (high-order half of each FIFO word is unused). When reading 8-bit words out of the FIFO, simply read DBGFL repeatedly to get successive bytes of data from the FIFO. It isn’t necessary to read DBGFH in this case.

Do not attempt to read data from the FIFO while it is still armed (after arming but before the FIFO is filled or ARMF is cleared) because the FIFO is prevented from advancing during reads of DBGFL. This can interfere with normal sequencing of reads from the FIFO.

Reading DBGFL while the debugger is not armed causes the address of the most-recently fetched opcode to be stored to the last location in the FIFO. By reading DBGFH then DBGFL periodically, external host software can develop a profile of program execution. After eight reads from the FIFO, the ninth read will return the information that was stored as a result of the first read. To use the profiling feature, read the FIFO eight times without using the data to prime the sequence and then begin using the data to get a delayed picture of what addresses were being executed. The information stored into the FIFO on reads of DBGFL (while the FIFO is not armed) is the address of the most-recently fetched opcode.

### 17.4.3.7 Debug Control Register (DBGC)

This register can be read or written at any time.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | DBGEN | ARM | TAG | BRKEN | RWA | RWAEN | RWB | RWBEN |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 17-7. Debug Control Register (DBGC)**

**Table 17-4. DBGC Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>DBGEN | **Debug Module Enable** — Used to enable the debug module. DBGEN cannot be set to 1 if the MCU is secure.<br>0 DBG disabled<br>1 DBG enabled |
| 6<br>ARM | **Arm Control** — Controls whether the debugger is comparing and storing information in the FIFO. A write is used to set this bit (and ARMF) and completion of a debug run automatically clears it. Any debug run can be manually stopped by writing 0 to ARM or to DBGEN.<br>0 Debugger not armed<br>1 Debugger armed |
| 5<br>TAG | **Tag/Force Select** — Controls whether break requests to the CPU will be tag or force type requests. If BRKEN = 0, this bit has no meaning or effect.<br>0 CPU breaks requested as force type requests<br>1 CPU breaks requested as tag type requests |
| 4<br>BRKEN | **Break Enable** — Controls whether a trigger event will generate a break request to the CPU. Trigger events can cause information to be stored in the FIFO without generating a break request to the CPU. For an end trace, CPU break requests are issued to the CPU when the comparator(s) and R/W meet the trigger requirements. For a begin trace, CPU break requests are issued when the FIFO becomes full. TRGSEL does not affect the timing of CPU break requests.<br>0 CPU break requests not enabled<br>1 Triggers cause a break request to the CPU |
| 3<br>RWA | **R/W Comparison Value for Comparator A** — When RWAEN = 1, this bit determines whether a read or a write access qualifies comparator A. When RWAEN = 0, RWA and the R/W signal do not affect comparator A.<br>0 Comparator A can only match on a write cycle<br>1 Comparator A can only match on a read cycle |
| 2<br>RWAEN | **Enable R/W for Comparator A** — Controls whether the level of R/W is considered for a comparator A match.<br>0 R/W is not used in comparison A<br>1 R/W is used in comparison A |
| 1<br>RWB | **R/W Comparison Value for Comparator B** — When RWBEN = 1, this bit determines whether a read or a write access qualifies comparator B. When RWBEN = 0, RWB and the R/W signal do not affect comparator B.<br>0 Comparator B can match only on a write cycle<br>1 Comparator B can match only on a read cycle |
| 0<br>RWBEN | **Enable R/W for Comparator B** — Controls whether the level of R/W is considered for a comparator B match.<br>0 R/W is not used in comparison B<br>1 R/W is used in comparison B |

### 17.4.3.8 Debug Trigger Register (DBGT)

This register can be read any time, but may be written only if ARM = 0, except bits 4 and 5 are hard-wired to 0s.

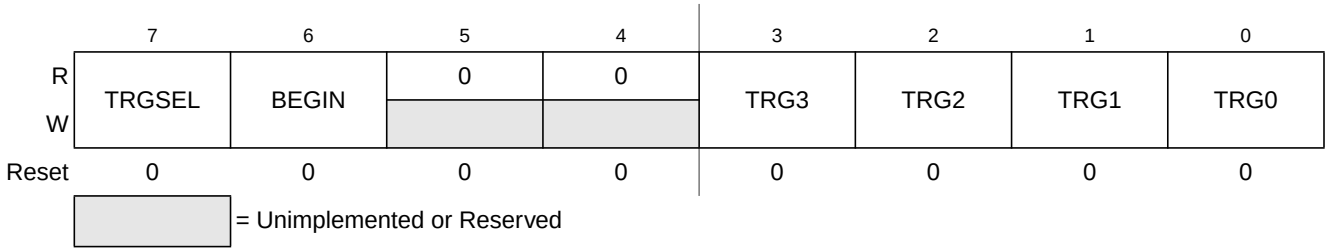



**Figure 17-8. Debug Trigger Register (DBGT)**

**Table 17-5. DBGT Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>TRGSEL | **Trigger Type** — Controls whether the match outputs from comparators A and B are qualified with the opcode tracking logic in the debug module. If TRGSEL is set, a match signal from comparator A or B must propagate through the opcode tracking logic and a trigger event is only signalled to the FIFO logic if the opcode at the match address is actually executed.<br>0 Trigger on access to compare address (force)<br>1 Trigger if opcode at compare address is executed (tag) |
| 6<br>BEGIN | **Begin/End Trigger Select** — Controls whether the FIFO starts filling at a trigger or fills in a circular manner until a trigger ends the capture of information. In event-only trigger modes, this bit is ignored and all debug runs are assumed to be begin traces.<br>0 Data stored in FIFO until trigger (end trace)<br>1 Trigger initiates data storage (begin trace) |
| 3:0<br>TRG[3:0] | **Select Trigger Mode** — Selects one of nine triggering modes, as described below.<br>0000 A-only<br>0001 A OR B<br>0010 A Then B<br>0011 Event-only B (store data)<br>0100 A then event-only B (store data)<br>0101 A AND B data (full mode)<br>0110 A AND NOT B data (full mode)<br>0111 Inside range: A ≤ address ≤ B<br>1000 Outside range: address < A or address > B<br>1001 – 1111 (No trigger) |

### 17.4.3.9 Debug Status Register (DBGS)

This is a read-only status register.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | AF | BF | ARMF | 0 | CNT3 | CNT2 | CNT1 | CNT0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 17-9. Debug Status Register (DBGS)**

**Table 17-6. DBGS Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>AF | **Trigger Match A Flag** — AF is cleared at the start of a debug run and indicates whether a trigger match A condition was met since arming.<br>0 Comparator A has not matched<br>1 Comparator A match |
| 6<br>BF | **Trigger Match B Flag** — BF is cleared at the start of a debug run and indicates whether a trigger match B condition was met since arming.<br>0 Comparator B has not matched<br>1 Comparator B match |
| 5<br>ARMF | **Arm Flag** — While DBGEN = 1, this status bit is a read-only image of ARM in DBGC. This bit is set by writing 1 to the ARM control bit in DBGC (while DBGEN = 1) and is automatically cleared at the end of a debug run. A debug run is completed when the FIFO is full (begin trace) or when a trigger event is detected (end trace). A debug run can also be ended manually by writing 0 to ARM or DBGEN in DBGC.<br>0 Debugger not armed<br>1 Debugger armed |
| 3:0<br>CNT[3:0] | **FIFO Valid Count** — These bits are cleared at the start of a debug run and indicate the number of words of valid data in the FIFO at the end of a debug run. The value in CNT does not decrement as data is read out of the FIFO. The external debug host is responsible for keeping track of the count as information is read out of the FIFO.<br>0000 Number of valid words in FIFO = No valid data<br>0001 Number of valid words in FIFO = 1<br>0010 Number of valid words in FIFO = 2<br>0011 Number of valid words in FIFO = 3<br>0100 Number of valid words in FIFO = 4<br>0101 Number of valid words in FIFO = 5<br>0110 Number of valid words in FIFO = 6<br>0111 Number of valid words in FIFO = 7<br>1000 Number of valid words in FIFO = 8 |

# Appendix A
# Electrical Characteristics

## A.1 Introduction

This section contains electrical and timing specifications for the MC9S08SG32 Series of microcontrollers available at the time of publication. The MC9S08SG32 Series includes both:

- Standard (STD)— devices that are *standard-temperature* rated. Table rows marked with a ♦ indicate electrical characteristics that apply to these devices.
- AEC Grade 0 — devices that are *high-temperature* rated. Table rows marked with a ♦ indicate electrical characteristics that apply to AEC Grade 0 devices.

## A.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table A-1. Parameter Classifications**

| | |
|---|---|
| **P** | Those parameters are guaranteed during production testing on each individual device. |
| **C** | Those parameters are achieved through the design characterization by measuring a statistically relevant sample size across process variations. |
| **T** | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| **D** | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## A.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pull-up resistor associated with the pin is enabled.

**Table A-2. Absolute Maximum Ratings**

| # | Rating | Symbol | Value | Unit | Temp Rated | |
|---|---|---|---|---|---|---|
| | | | | | Standard | AEC Grade 0 |
| 1 | Supply voltage | $V_{DD}$ | –0.3 to +5.8 | V | ♦ | ♦ |
| 2 | Maximum current into $V_{DD}$ | $I_{DD}$ | 120 | mA | ♦ | ♦ |
| 3 | Digital input voltage | $V_{In}$ | –0.3 to $V_{DD}$ + 0.3 | V | ♦ | ♦ |
| 4 | Instantaneous maximum current<br>Single pin limit (applies to all port pins)[1, 2, 3] | $I_D$ | ± 25 | mA | ♦ | ♦ |
| 5 | Storage temperature range | $T_{stg}$ | –55 to 150 | °C | ♦ | ♦ |

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ($V_{DD}$) and negative ($V_{SS}$) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins except $\overline{\text{RESET}}$ are internally clamped to $V_{SS}$ and $V_{DD}$.

3 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

## A.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

**Table A-3. Thermal Characteristics**

| # | C | Rating | Symbol | Value | | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Standard | AEC Grade 0 |
| 1 | — | Operating temperature range (packaged) | | | | | | |
| | | Temperature Code W | $T_A$ | –40 to 150 | | °C | — | ♦ |
| | | Temperature Code J | | –40 to 140 | | | — | ♦ |
| | | Temperature Code M | | –40 to 125 | | | ♦ | — |
| | | Temperature Code V | | –40 to 105 | | | ♦ | — |
| | | Temperature Code C | | –40 to 85 | | | ♦ | — |
| 2 | D | Thermal resistance, Single-layer board | | | | | | |
| | | | | Airflow @200 ft/min | Natural Convection | | | |
| | | 28-pin TSSOP | $\theta_{JA}$ | 71 | 91 | °C/W | ♦ | ♦ |
| | | 20-pin TSSOP | | 94 | 114 | | ♦ | — |
| | | 16-pin TSSOP | | 108 | 133 | | ♦ | ♦ |
| 3 | D | Thermal resistance, Four-layer board | | | | | | |
| | | | | Airflow @200 ft/min | Natural Convection | | | |
| | | 28-pin TSSOP | $\theta_{JA}$ | 51 | 58 | °C/W | ♦ | ♦ |
| | | 20-pin TSSOP | | 68 | 75 | | ♦ | — |
| | | 16-pin TSSOP | | 78 | 92 | | ♦ | ♦ |
| 4 | D | Maximum junction temperature | $T_J$ | 135 | | °C | ♦ | — |
| | | | | 155 | | | — | ♦ |

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. A-1}$$

where:

$T_A$ = Ambient temperature, °C
$\theta_{JA}$ = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. A-2}$$

Solving Equation A-1 and Equation A-2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. A-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving Equation A-1 and Equation A-2 iteratively for any value of $T_A$.

## A.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-4. ESD and Latch-up Test Conditions**

| Model | Description | Symbol | Value | Unit |
|---|---|---|---|---|
| Human Body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | — |
| Latch-up | Minimum input voltage limit | — | – 2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

**Table A-5. ESD and Latch-Up Protection Characteristics**

| No. | Rating[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Human body model (HBM) | $V_{HBM}$ | ± 2000 | — | V |
| 2 | Charge device model (CDM) | $V_{CDM}$ | ± 500 | — | V |
| 3 | Latch-up current at $T_A$ = 125°C | $I_{LAT}$ | ± 100 | — | mA |

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## A.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table A-6. DC Characteristics**

| # | C | Characteristic | Symbol | Condition | Min | Typ[1] | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 |
| 1 | — | Operating Voltage | $V_{DD}$ | — | 2.7 | — | 5.5 | V | ♦ | ♦ |
| 2 | C | Output high voltage — All I/O pins, low-drive strength | $V_{OH}$ | 5 V, $I_{Load}$ = –4 mA | $V_{DD}$ – 1.5 | — | — | V | ♦ | ♦ |
| | P | | | 5 V, $I_{Load}$ = –2 mA | $V_{DD}$ – 0.8 | — | — | V | ♦ | ♦ |
| | C | | | 3 V, $I_{Load}$ = –1 mA | $V_{DD}$ – 0.8 | — | — | V | ♦ | ♦ |
| | C | Output high voltage — All I/O pins, high-drive strength | | 5 V, $I_{Load}$ = –20 mA | $V_{DD}$ – 1.5 | — | — | V | ♦ | ♦ |
| | P | | | 5 V, $I_{Load}$ = –10 mA | $V_{DD}$ – 0.8 | — | — | V | ♦ | ♦ |
| | C | | | 3 V, $I_{Load}$ = –5 mA | $V_{DD}$ – 0.8 | — | — | V | ♦ | ♦ |
| 3 | D | Output high current — Max total $I_{OH}$ for all ports | $I_{OHT}$ | $V_{OUT} < V_{DD}$ | 0 | — | –100 | mA | ♦ | — |
| | | | | | 0 | — | –50 | mA | — | ♦ |
| 4 | C | Output low voltage — All I/O pins, low-drive strength | $V_{OL}$ | 5 V, $I_{Load}$ = 4 mA | — | — | 1.5 | V | ♦ | ♦ |
| | P | | | 5 V, $I_{Load}$ = 2 mA | — | — | 0.8 | V | ♦ | ♦ |
| | C | | | 3 V, $I_{Load}$ = 1 mA | — | — | 0.8 | V | ♦ | ♦ |
| | C | Output low voltage — AllI/O pins, high-drive strength | | 5 V, $I_{Load}$ = 20 mA | — | — | 1.5 | V | ♦ | ♦ |
| | P | | | 5 V, $I_{Load}$ = 10 mA | — | — | 0.8 | V | ♦ | ♦ |
| | C | | | 3 V, $I_{Load}$ = 5 mA | — | — | 0.8 | V | ♦ | ♦ |
| 5 | D | Output low current — Max total $I_{OL}$ for all ports | $I_{OLT}$ | $V_{OUT} > V_{SS}$ | 0 | — | 100 | mA | ♦ | — |
| | | | | | 0 | — | 50 | mA | — | ♦ |
| 6 | P | Input high voltage; all digital inputs | $V_{IH}$ | 5V | 0.65 x $V_{DD}$ | — | — | V | ♦ | ♦ |
| | C | | | 3V | 0.7 x $V_{DD}$ | — | — | V | ♦ | ♦ |
| 7 | P | Input low voltage; all digital inputs | $V_{IL}$ | 5V | — | — | 0.35 x $V_{DD}$ | V | ♦ | ♦ |
| | C | | | 3V | — | — | 0.35 x $V_{DD}$ | V | ♦ | ♦ |
| 8 | C | Input hysteresis | $V_{hys}$ | — | 0.06 x $V_{DD}$ | — | — | V | ♦ | ♦ |

**Table A-6. DC Characteristics (continued)**

| # | C | Characteristic | Symbol | Condition | Min | Typ[1] | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 |
| 9 | P | Input leakage current (per pin) | $\|I_{In}\|$ | $V_{In} = V_{DD}$ or $V_{SS}$ | — | — | 1 | µA | ♦ | — |
| | | | | temperature > 125 C | — | — | 2 | µA | — | ♦ |
| 10 | P | Hi-Z (off-state) leakage current (per pin) input/output port pins | $\|I_{OZ}\|$ | $V_{In} = V_{DD}$ or $V_{SS}$; temperature | — | — | 1 | µA | ♦ | — |
| | | $\overline{\text{RESET}}$ | | $V_{In} = V_{DD}$ or $V_{SS}$ | — | — | 2 | µA | ♦ | — |
| | | Input/Output Port pins | | $V_{In} = V_{DD}$ or $V_{SS}$; temperature > 125 C | — | 0.2 | 2 | µA | — | ♦ |
| 11 | P | Pullup or Pulldown[2] resistors; when enabled I/O pins | $R_{PU}$,$R_{PD}$ | — | 17 | 37 | 52 | kΩ | ♦ | ♦ |
| | C | $\overline{\text{RESET}}$[3] | $R_{PU}$ | — | 17 | 37 | 52 | kΩ | ♦ | ♦ |
| 12 | D | DC injection current [4, 5, 6, 7] | $I_{IC}$ | | | | | | ♦ | ♦ |
| | | Single pin limit | | $V_{IN} > V_{DD}$ | 0 | — | 2 | mA | ♦ | ♦ |
| | | | | $V_{IN} < V_{SS}$, | 0 | — | –0.2 | mA | ♦ | ♦ |
| | | Total MCU limit, includes sum of all stressed pins | | $V_{IN} > V_{DD}$ | 0 | — | 25 | mA | ♦ | ♦ |
| | | | | $V_{IN} < V_{SS}$, | 0 | — | –5 | mA | ♦ | ♦ |
| 13 | D | Input Capacitance, all pins | $C_{In}$ | — | — | — | 8 | pF | ♦ | ♦ |
| 14 | D | RAM retention voltage | $V_{RAM}$ | — | — | 0.6 | 1.0 | V | ♦ | ♦ |
| 15 | D | POR re-arm voltage[8] | $V_{POR}$ | — | 0.9 | 1.4 | 2.0 | V | ♦ | ♦ |
| 16 | D | POR re-arm time[9] | $t_{POR}$ | — | 10 | — | — | µs | ♦ | ♦ |
| 17 | P | Low-voltage detection threshold — high range $V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVD1}$ | — | 3.9<br>4.0 | 4.0<br>4.1 | 4.1<br>4.2 | V | ♦ | — |
| | | | | — | 3.88<br>3.98 | 4.0<br>4.1 | 4.12<br>4.22 | V | — | ♦ |

**Table A-6. DC Characteristics (continued)**

| # | C | Characteristic | Symbol | Condition | Min | Typ[1] | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 |
| 18 | P | Low-voltage detection threshold — low range<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVD0}$ | — | 2.48<br>2.54 | 2.56<br>2.62 | 2.64<br>2.70 | V | ♦ | ♦ |
| 19 | P | Low-voltage warning threshold — high range 1<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW3}$ | — | 4.5<br>4.6 | 4.6<br>4.7 | 4.7<br>4.8 | V | ♦ | — |
| | | | | | 4.48<br>4.58 | 4.6<br>4.7 | 4.72<br>4.82 | V | — | ♦ |
| 20 | P | Low-voltage warning threshold — high range 0<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW2}$ | — | 4.2<br>4.3 | 4.3<br>4.4 | 4.4<br>4.5 | V | ♦ | — |
| | | | | | 4.18<br>4.28 | 4.3<br>4.4 | 4.42<br>4.52 | V | — | ♦ |
| 21 | P | Low-voltage warning threshold low range 1<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW1}$ | — | 2.84<br>2.90 | 2.92<br>2.98 | 3.00<br>3.06 | V | ♦ | ♦ |
| 22 | P | Low-voltage warning threshold — low range 0<br>$V_{DD}$ falling<br>$V_{DD}$ rising | $V_{LVW0}$ | — | 2.66<br>2.72 | 2.74<br>2.80 | 2.82<br>2.88 | V | ♦ | ♦ |
| 23 | T | Low-voltage inhibit reset/recover hysteresis | $V_{hys}$ | 5 V | — | 100 | — | mV | ♦ | ♦ |
| | | | | 3 V | — | 60 | — | mV | ♦ | ♦ |
| 24 | P | Bandgap Voltage Reference[10] | $V_{BG}$ | — | 1.18 | 1.202 | 1.21 | V | ♦ | — |
| | | | | | 1.17 | 1.202 | 1.22 | V | — | ♦ |

1 Typical values are measured at 25°C. Characterized, not tested

2 When IRQ or a pin interrupt is configured to detect rising edges, pulldown resistors are used in place of pullup resistors.

3 The specified resistor value is the actual value internal to the device. The pullup value may measure higher when measured externally on the pin.

4 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

5 All functional non-supply pins except $\overline{\text{RESET}}$ are internally clamped to $V_{SS}$ and $V_{DD}$.

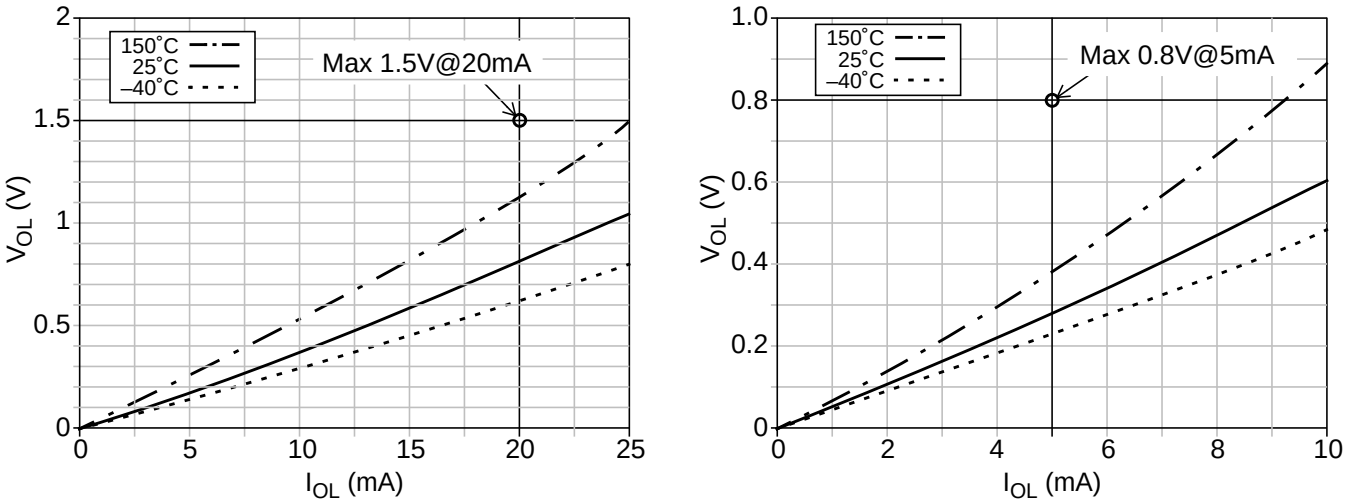
6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The $\overline{\text{RESET}}$ pin does not have a clamp diode to $V_{DD}$. Do not drive this pin above $V_{DD}$.

8 Maximum is highest voltage that POR is guaranteed.

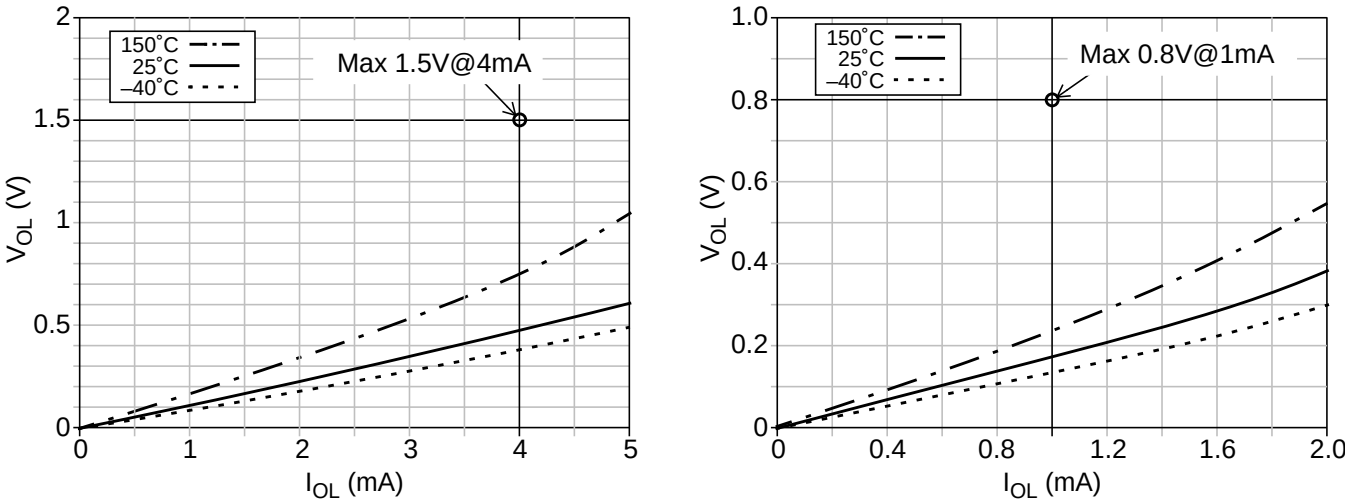
9 Simulated, not tested.

10 Factory trimmed at $V_{DD}$ = 5.0 V, Temp = 25°C.



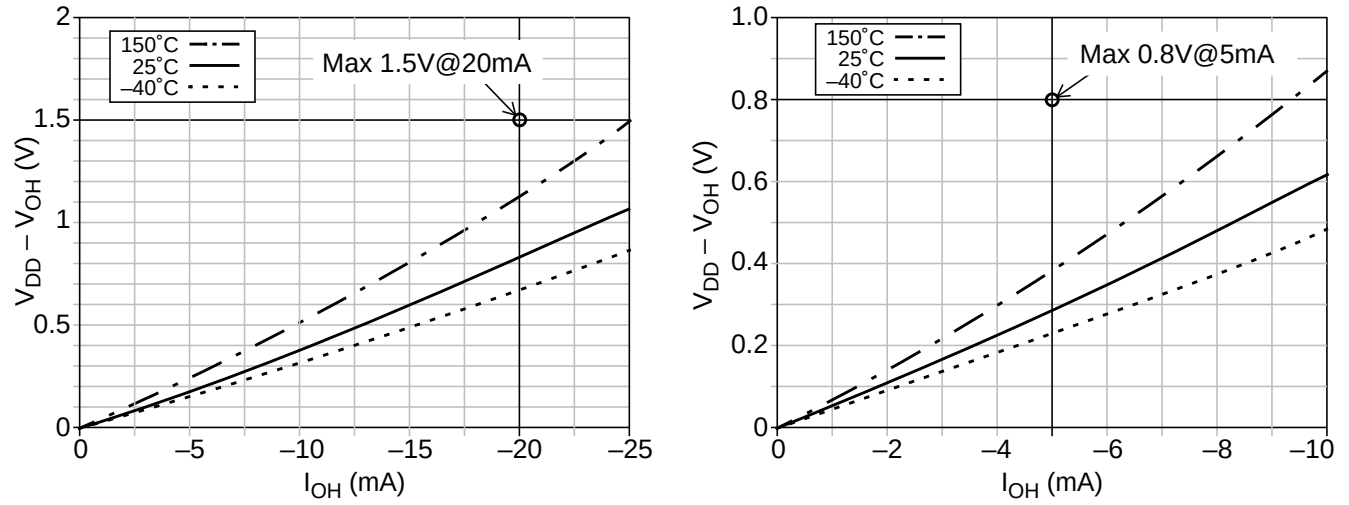

**a) $V_{DD}$ = 5V, High Drive** **b) $V_{DD}$ = 3V, High Drive**

**Figure A-1. Typical $V_{OL}$ vs $I_{OL}$, High Drive Strength**



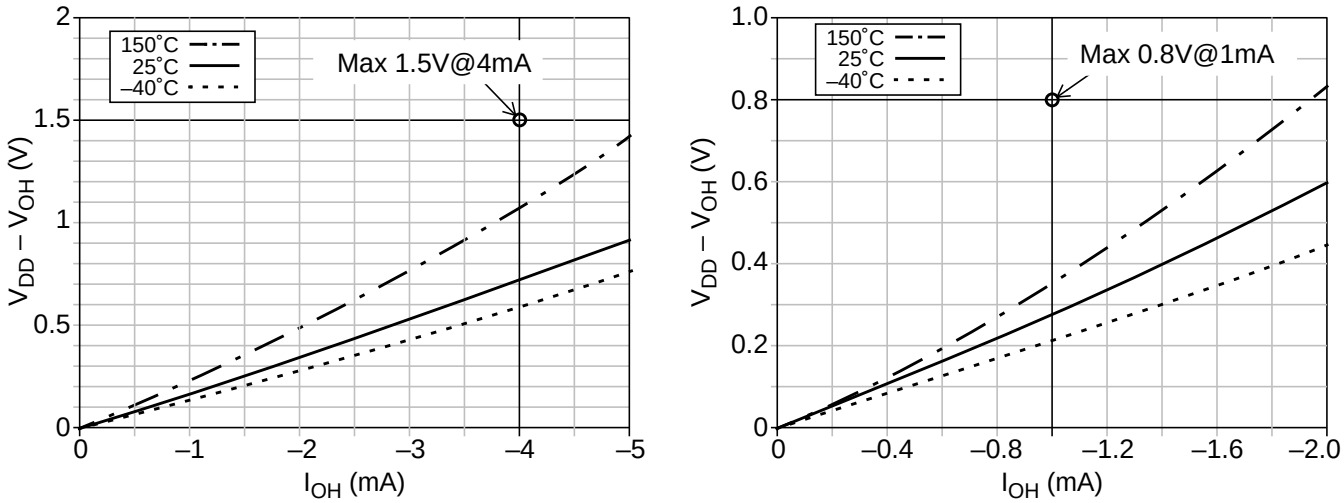

**a) $V_{DD}$ = 5V, Low Drive** **b) $V_{DD}$ = 3V, Low Drive**

**Figure A-2. Typical $V_{OL}$ vs $I_{OL}$, Low Drive Strength**




**a) $V_{DD}$ = 5V, High Drive** **b) $V_{DD}$ = 3V, High Drive**

**Figure A-3. Typical $V_{DD} - V_{OH}$ vs $I_{OH}$, High Drive Strength**




**a) $V_{DD}$ = 5V, Low Drive**

**b) $V_{DD}$ = 3V, Low Drive**

**Figure A-4. Typical $V_{DD} – V_{OH}$ vs $I_{OH}$, Low Drive Strength**

## A.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

**Table A-7. Supply Current Characteristics**

| # | C | Parameter | Symbol | $V_{DD}$ (V) | Typ[1] | Max[2] | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | C | Run supply current[3] measured at (CPU clock = 4 MHz, $f_{Bus}$ = 2 MHz) | $RI_{DD}$ | 5 | 1.4 | 3 | mA | ♦ | ♦ |
| | C | | | 3 | 1.3 | 2.5 | mA | ♦ | ♦ |
| 2 | P | Run supply current[3] measured at (CPU clock = 16 MHz, $f_{Bus}$ = 8 MHz) | $RI_{DD}$ | 5 | 4.7 | 7.5 | mA | ♦ | ♦ |
| | C | | | 3 | 4.6 | 7 | mA | ♦ | ♦ |
| 3 | C | Run supply current[4] measured at (CPU clock = 32 MHz, $f_{Bus}$ = 16MHz) | $RI_{DD}$ | 5 | 8.9 | 10 | mA | ♦ | ♦ |
| | C | | | 3 | 8.7 | 9.6 | mA | ♦ | ♦ |
| 4 | | Stop3 mode supply current | | | | | | | |
| | C | –40°C (C,V, and M suffix) | $S3I_{DD}$ | 5 | 0.96 | – | µA | ♦ | — |
| | P | 25°C (All parts) | | | 1.3 | – | µA | ♦ | — |
| | P[5] | 85°C (C suffix only) | | | 16.9 | 35 | µA | ♦ | — |
| | P[5] | 105°C (V suffix only) | | | 37 | 90 | µA | ♦ | — |
| | P[5] | 125°C (M suffix only) | | | 84 | 150 | µA | ♦ | — |
| | C | –40°C (C,V, and M suffix) | | 3 | 0.85 | – | µA | ♦ | — |
| | P | 25°C (All parts) | | | 1.2 | – | µA | ♦ | — |
| | P[5] | 85°C (C suffix only) | | | 14.8 | 30 | µA | ♦ | — |
| | P[5] | 105°C (V suffix only) | | | 32.7 | 80 | µA | ♦ | — |
| | P[5] | 125°C (M suffix only) | | | 75 | 130 | µA | ♦ | — |

**Table A-7. Supply Current Characteristics (continued)**

| # | C | Parameter | Symbol | $V_{DD}$ (V) | Typ[1] | Max[2] | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 5 | | Stop2 mode supply current | | | | | | | |
| | C | –40°C (C,M, and V suffix) | $S2I_{DD}$ | 5 | 0.94 | – | µA | ♦ | — |
| | P | 25°C (All parts) | | | 1.25 | – | µA | ♦ | — |
| | P[5] | 85°C (C suffix only) | | | 13.4 | 30 | µA | ♦ | — |
| | P[5] | 105°C (V suffix only) | | | 30 | 65 | µA | ♦ | — |
| | P[5] | 125°C (M suffix only) | | | 65 | 120 | µA | ♦ | — |
| | C | –40°C (C,M, and V suffix) | | 3 | 0.83 | – | µA | ♦ | — |
| | P | 25°C (All parts) | | | 1.1 | – | µA | ♦ | — |
| | P[5] | 85°C (C suffix only) | | | 11.5 | 25 | µA | ♦ | — |
| | P[5] | 105°C (V suffix only) | | | 25 | 55 | µA | ♦ | — |
| | P[5] | 125°C (M suffix only) | | | 57 | 100 | µA | ♦ | — |
| 6 | C | RTC adder to stop2 or stop3[6] | $S23I_{DDRTI}$ | 5 | 300 | 500 | nA | ♦ | — |
| | | | | 3 | 300 | 500 | nA | ♦ | — |
| 7 | C | LVD adder to stop3 (LVDE = LVDSE = 1) | $S3I_{DDLVD}$ | 5 | 110 | 180 | µA | ♦ | — |
| | | | | 3 | 90 | 160 | µA | ♦ | — |
| 8 | C | Adder to stop3 for oscillator enabled[7] (EREFSTEN =1) | $S3I_{DDOSC}$ | 5,3 | 5 | 8 | µA | ♦ | — |

1 Typical values are based on characterization data at 25°C. See Figure A-5 through Figure A-7 for typical curves across temperature and voltage.

2 Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

3 All modules except ADC active, ICS configured for FBELP, and does not include any dc loads on port pins

4 All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins

5 Stop Currents are tested in production for 25 Con all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

6 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

7 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal and low power mode (HGO = 0).

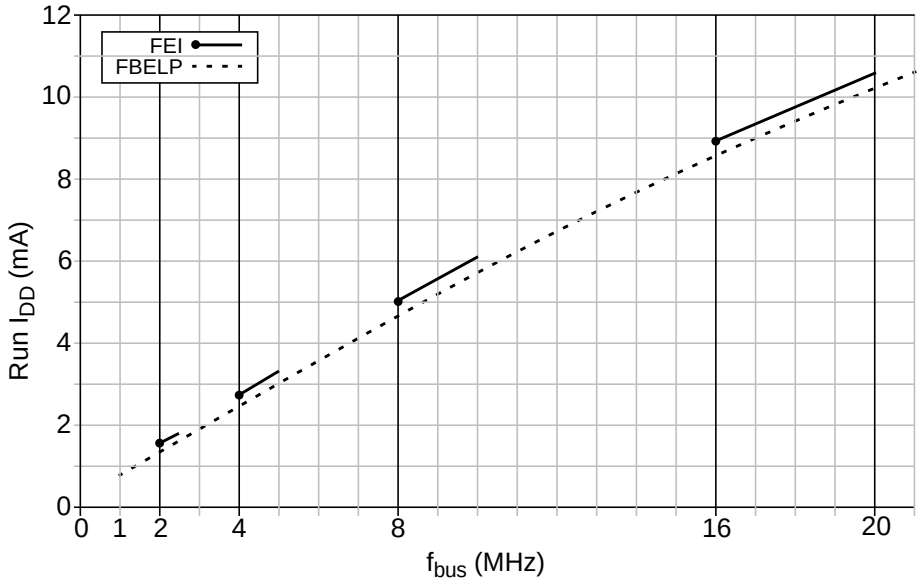



**Figure A-5. Typical Run $I_{DD}$ vs. Bus Frequency ($V_{DD}$ = 5V)**

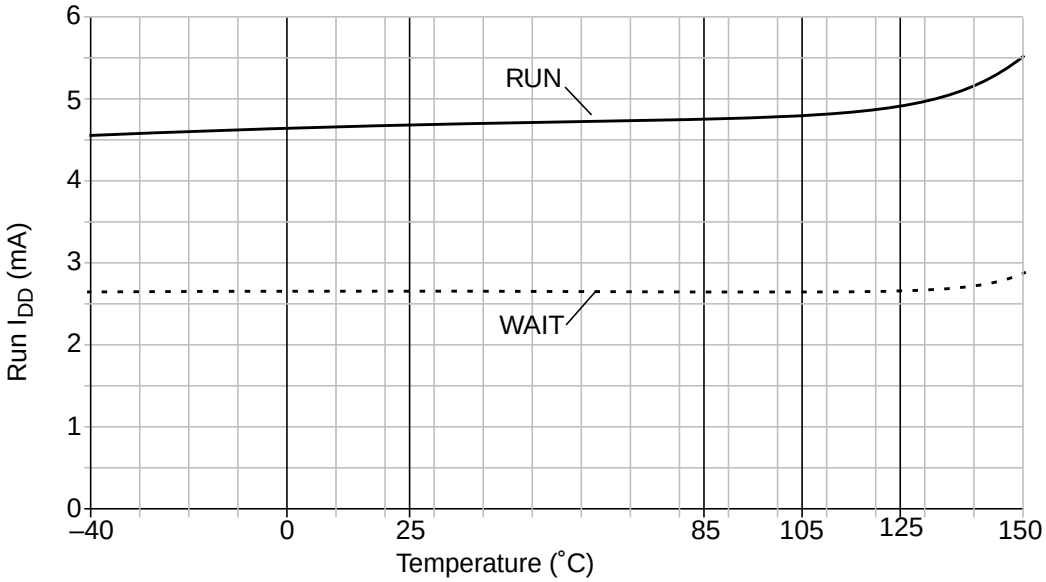



**Figure A-6. Typical Run and Wait $I_{DD}$ vs. Temperature ($V_{DD}$ = 5V; $f_{bus}$ = 8MHz)**

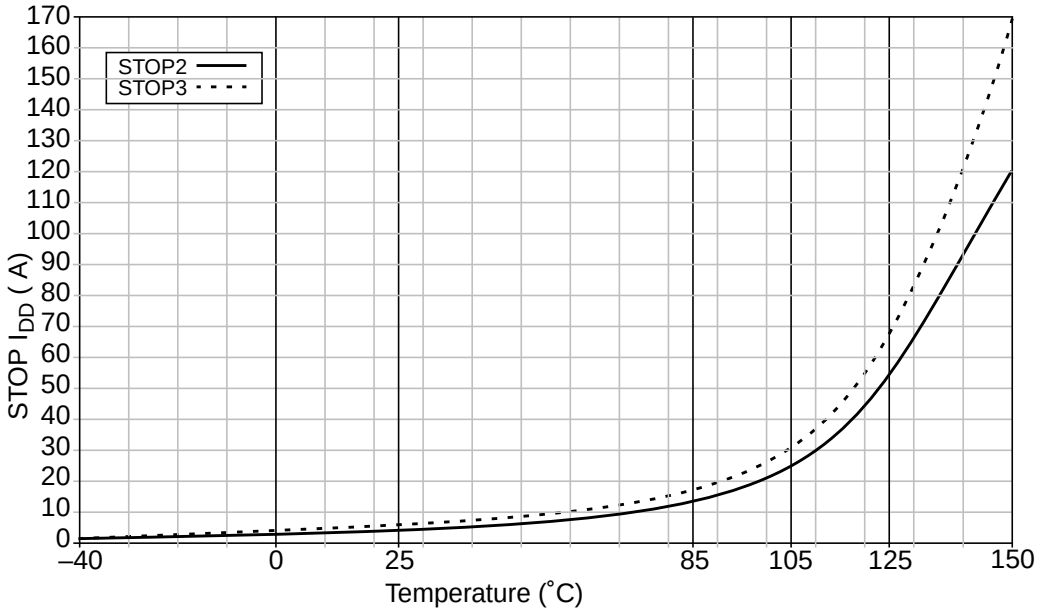


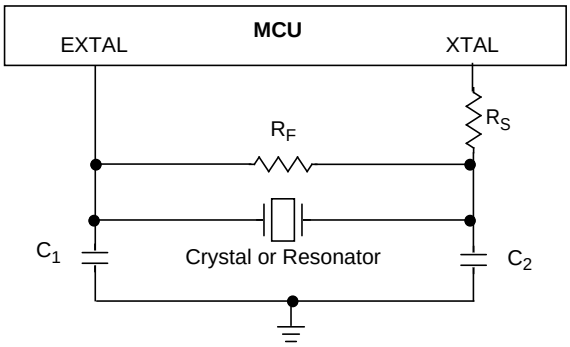

**Figure A-7. Typical Stop $I_{DD}$ vs. Temperature ($V_{DD}$ = 5V)**

# A.8 External Oscillator (XOSC) Characteristics

**Table A-8. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)**

| # | C | Rating | Symbol | Min | Typ[1] | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | | | | | | | |
| | | Low range (RANGE = 0) | $f_{lo}$ | 32 | — | 38.4 | kHz | ♦ | ♦ |
| | | High range (RANGE = 1) FEE or FBE mode [2] | $f_{hi}$ | 1 | — | 5 | MHz | ♦ | ♦ |
| | | High range (RANGE = 1, HGO = 1) FBELP mode | $f_{hi-hgo}$ | 1 | — | 16 | MHz | ♦ | ♦ |
| | | High range (RANGE = 1, HGO = 0) FBELP mode | $f_{hi-lp}$ | 1 | — | 8 | MHz | ♦ | ♦ |
| 2 | — | Load capacitors | $C_1$, $C_2$ | See crystal or resonator manufacturer's recommendation. | | | | | |
| 3 | — | Feedback resistor | | | | | | | |
| | | Low range (32 kHz to 100 kHz) | $R_F$ | — | 10 | — | MΩ | ♦ | ♦ |
| | | High range (1 MHz to 16 MHz) | | — | 1 | — | MΩ | ♦ | ♦ |
| 4 | — | Series resistor | | | | | | | |
| | | Low range, low gain (RANGE = 0, HGO = 0) | $R_S$ | — | 0 | — | kΩ | ♦ | ♦ |
| | | Low range, high gain (RANGE = 0, HGO = 1) | | — | 100 | — | kΩ | ♦ | ♦ |
| | | High range, low gain (RANGE = 1, HGO = 0) | | — | 0 | — | kΩ | ♦ | ♦ |
| | | High range, high gain (RANGE = 1, HGO = 1) | | | | | | | |
| | | ≥ 8 MHz | | — | 0 | 0 | kΩ | ♦ | ♦ |
| | | 4 MHz | | — | 0 | 10 | kΩ | ♦ | ♦ |
| | | 1 MHz | | — | 0 | 20 | kΩ | ♦ | ♦ |
| 5 | T | Crystal start-up time [3] | | | | | | | |
| | | Low range, low gain (RANGE = 0, HGO = 0) | $t_{CSTL-LP}$ | — | 200 | — | ms | ♦ | ♦ |
| | | Low range, high gain (RANGE = 0, HGO = 1) | $t_{CSTL-HGO}$ | — | 400 | — | ms | ♦ | ♦ |
| | | High range, low gain (RANGE = 1, HGO = 0)[4] | $t_{CSTH-LP}$ | — | 5 | — | ms | ♦ | ♦ |
| | | High range, high gain (RANGE = 1, HGO = 1)[4] | $t_{CSTH-HGO}$ | — | 20 | — | ms | ♦ | ♦ |
| 6 | T | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) | | | | | | | |
| | | FEE or FBE mode [2] | $f_{extal}$ | 0.03125 | — | 5 | MHz | ♦ | ♦ |
| | | FBELP mode | | 0 | — | 40 | MHz | ♦ | — |
| | | FBELP mode | | 0 | — | 36 | MHz | — | ♦ |

1 Typical data was characterized at 5.0 V, 25°C or is recommended value.
2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3 Characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.
4 4 MHz crystal



# A.9 Internal Clock Source (ICS) Characteristics

**Table A-9. ICS Frequency Specifications (Temperature Range = –40 to 125°C Ambient)**

| # | C | Rating | Symbol | Min | Typical | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | P | Internal reference frequency — factory trimmed at $V_{DD}$ = 5 V and temperature = 25°C | $f_{int_ft}$ | — | 31.25 | — | kHz | ♦ | ♦ |
| 2 | T | Internal reference frequency — untrimmed[1] | $f_{int_ut}$ | 25 | 36 | 41.66 | kHz | ♦ | ♦ |
| 3 | P | Internal reference frequency — trimmed | $f_{int_t}$ | 31.25 | — | 39.0625 | kHz | ♦ | ♦ |
| 4 | D | Internal reference startup time | $t_{irefst}$ | — | 55 | 100 | µs | ♦ | ♦ |
| 5 | — | DCO output frequency range — untrimmed[1] value provided for reference: $f_{dco_ut}$ = 1024 x $f_{int_ut}$ | $f_{dco_ut}$ | 25.6 | 36.86 | 42.66 | MHz | ♦ | ♦ |
| 6 | D | DCO output frequency range — trimmed | $f_{dco_t}$ | 32 | — | 40 | MHz | ♦ | — |
| | | | | 32 | — | 36 | MHz | — | ♦ |
| 7 | D | Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) | $\Delta f_{dco_res_t}$ | — | ± 0.1 | ± 0.2 | $\%f_{dco}$ | ♦ | ♦ |
| 8 | D | Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) | $\Delta f_{dco_res_t}$ | — | ± 0.2 | ± 0.4 | $\%f_{dco}$ | ♦ | ♦ |
| 9 | P | Total deviation of trimmed DCO output frequency over voltage and temperature | $\Delta f_{dco_t}$ | — | + 0.5 – 1.0 | ± 1.5 | $\%f_{dco}$ | ♦ | — |
| | | | | — | + 0.5 – 1.0 | ± 3 | $\%f_{dco}$ | — | ♦ |
| 10 | D | Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C | $\Delta f_{dco_t}$ | — | ± 0.5 | ± 1 | $\%f_{dco}$ | ♦ | ♦ |
| 11 | D | FLL acquisition time [2] | $t_{acquire}$ | — | | 1 | ms | ♦ | ♦ |
| 12 | D | DCO output clock long term jitter (over 2 ms interval) [3] | $C_{Jitter}$ | — | 0.02 | 0.2 | $\%f_{dco}$ | ♦ | ♦ |

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{BUS}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

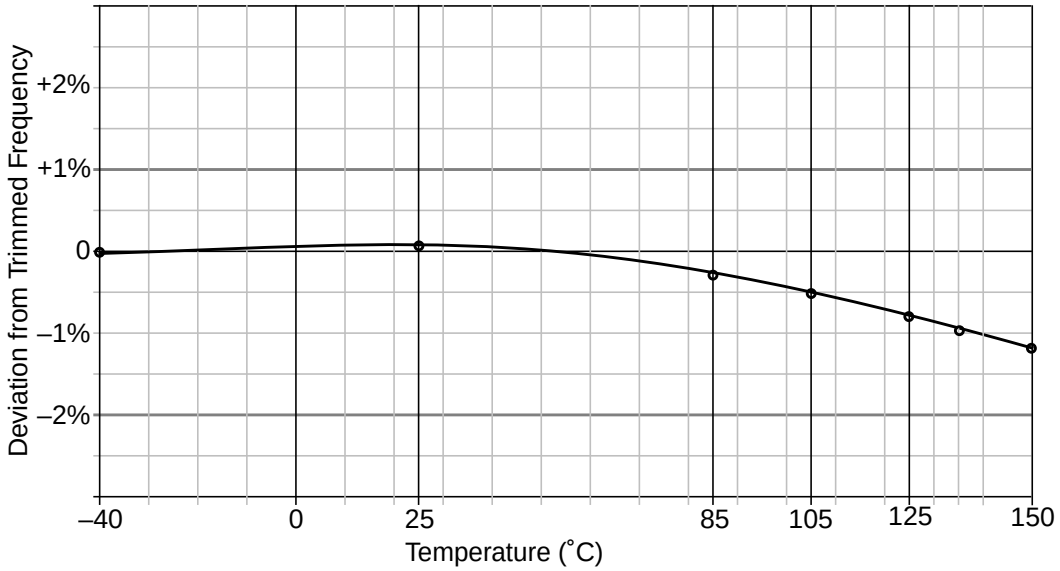



**Figure A-8. Typical Frequency Deviation vs Temperature (ICS Trimmed to 16MHz bus@25˚C, 5V, FEI)[1]**

## A.10 Analog Comparator (ACMP) Electricals

**Table A-10. Analog Comparator Electrical Specifications**

| # | C | Rating | Symbol | Min | Typical | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | — | Supply voltage | $V_{DD}$ | 2.7 | — | 5.5 | V | ♦ | ♦ |
| 2 | C/T | Supply current (active) | $I_{DDAC}$ | — | 20 | 35 | µA | ♦ | ♦ |
| 3 | D | Analog input voltage | $V_{AIN}$ | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V | ♦ | ♦ |
| 4 | D | Analog input offset voltage | $V_{AIO}$ | — | 20 | 40 | mV | ♦ | ♦ |
| 5 | D | Analog Comparator hysteresis | $V_H$ | 3.0 | 6.0 | 20.0 | mV | ♦ | ♦ |
| 6 | D | Analog input leakage current | $I_{ALKG}$ | — | — | 1.0 | µA | ♦ | ♦ |
| 7 | D | Analog Comparator initialization delay | $t_{AINIT}$ | — | — | 1.0 | µs | ♦ | ♦ |

1. Based on the average of several hundred units from a typical characterization lot.

# A.11 ADC Characteristics

**Table A-11. ADC Operating Conditions**

| # | Characteristic | Conditions | Symb | Min | Typ[1] | Max | Unit | Temp Rated | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 | |
| 1 | Supply voltage | Absolute | $V_{DDAD}$ | 2.7 | — | 5.5 | V | ♦ | ♦ | |
| 2 | Input Voltage | | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | ♦ | ♦ | |
| 3 | Input Capacitance | | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | ♦ | ♦ | |
| 4 | Input Resistance | | $R_{ADIN}$ | — | 3 | 5 | kΩ | ♦ | ♦ | |
| 5 | Analog Source Resistance | 10 bit mode<br>$f_{ADCK}$ > 4MHz<br>$f_{ADCK}$ < 4MHz | $R_{AS}$ | —<br>— | —<br>— | 5<br>10 | kΩ | ♦ | ♦ | External to MCU |
| | | 8 bit mode (all valid $f_{ADCK}$) | | — | — | 10 | kΩ | ♦ | ♦ | |
| 6 | ADC Conversion Clock Freq. | High Speed (ADLPC=0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | ♦ | ♦ | |
| | | Low Power (ADLPC=1) | | 0.4 | — | 4.0 | MHz | ♦ | ♦ | |

1 Typical values assume $V_{DDAD}$ = $V_{DD}$ = 5.0V, Temp = 25°C, $f_{ADCK}$=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

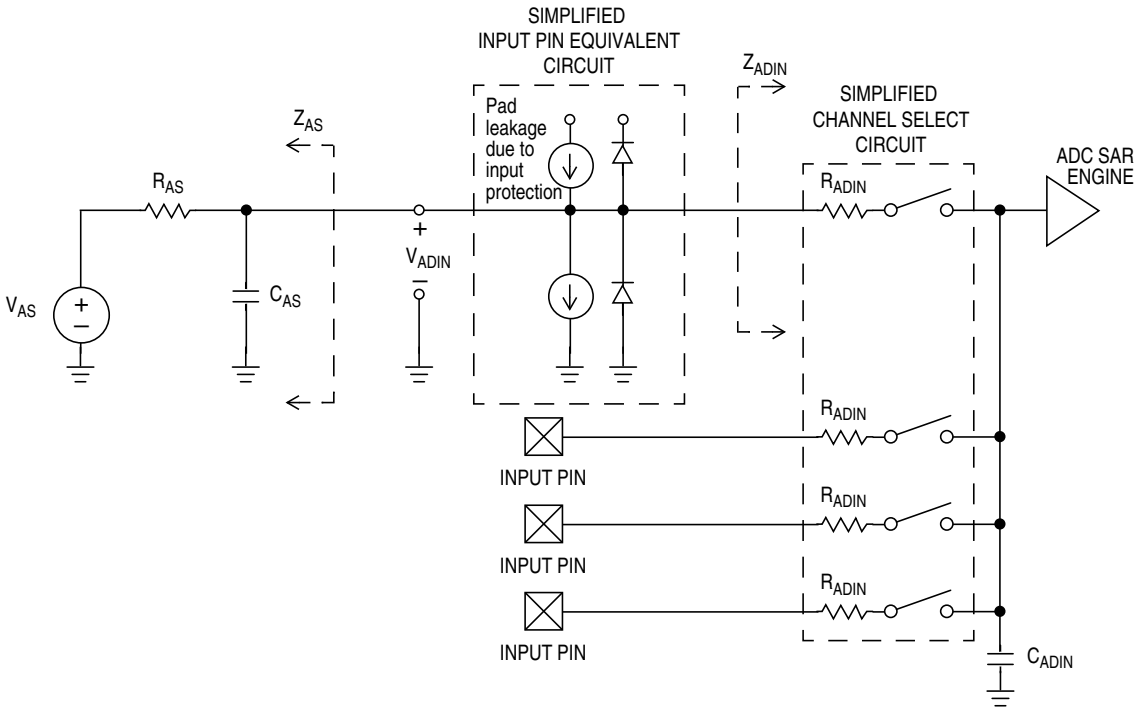



**Figure A-9. ADC Input Impedance Equivalency Diagram**

## Table A-12. ADC Characteristics

| # | Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit | Temp Rated | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 | |
| 1 | Supply current | ADLPC=1<br>ADLSMP=1<br>ADCO=1 | T | $I_{DD}$ + $I_{DDAD}$ | — | 133 | — | µA | ♦ | ♦ | ADC current only |
| | | ADLPC=1<br>ADLSMP=0<br>ADCO=1 | T | $I_{DD}$ + $I_{DDAD}$ | — | 218 | — | µA | ♦ | ♦ | ADC current only |
| | | ADLPC=0<br>ADLSMP=1<br>ADCO=1 | T | $I_{DD}$ + $I_{DDAD}$ | — | 327 | — | µA | ♦ | ♦ | ADC current only |
| | | ADLPC=0<br>ADLSMP=0<br>ADCO=1 | P | $I_{DD}$ + $I_{DDAD}$ | — | 0.582 | 1 | mA | ♦ | ♦ | ADC current only |
| 2 | ADC asynchronous clock source | High speed (ADLPC=0) | P | $f_{ADACK}$ | 2 | 3.3 | 5 | MHz | ♦ | ♦ | $t_{ADACK}$ = $1/f_{ADACK}$ |
| | | Low power (ADLPC=1) | | | 1.25 | 2 | 3.3 | | ♦ | ♦ | |
| 3 | Conversion time (including sample time) | Short sample (ADLSMP=0) | D | $t_{ADC}$ | — | 20 | — | ADCK cycles | ♦ | ♦ | See ADC Chapter for conversion time variances |
| | | Long sample (ADLSMP=1) | | | — | 40 | — | | ♦ | ♦ | |
| 4 | Sample time | Short sample (ADLSMP=0) | D | $t_{ADS}$ | — | 3.5 | — | ADCK cycles | ♦ | ♦ | |
| | | Long sample (ADLSMP=1) | | | — | 23.5 | — | | ♦ | ♦ | |

**Table A-12. ADC Characteristics (continued)**

| # | Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit | Temp Rated | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 | |
| 5 | Total unadjusted error (includes quantization) | 28-pin packages only | | | | | | | | | |
| | | 10-bit mode | P | $E_{TUE}$ | — | ±1 | ±2.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.5 | ±1 | | ♦ | ♦ | |
| | | 20-pin packages | | | | | | | | | |
| | | 10-bit mode | P | $E_{TUE}$ | — | ±.5 | ±3.5 | LSB[2] | ♦ | — | |
| | | 8-bit mode | | | — | ±0.7 | ±1.5 | | ♦ | — | |
| | | 16-pin and packages | | | | | | | | | |
| | | 10-bit mode | P | $E_{TUE}$ | — | ±.5 | ±3.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.7 | ±1.5 | | ♦ | ♦ | |
| 6 | Differential Non-Linearity | 10-bit mode | P | DNL | — | ±0.5 | ±1.0 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.3 | ±0.5 | | ♦ | ♦ | |
| | | Monotonicity and No-Missing-Codes guaranteed | | | | | | | | | |
| 7 | Integral non-linearity | 10-bit mode | T | INL | — | ±0.5 | ±1.0 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.3 | ±0.5 | | ♦ | ♦ | |

**Table A-12. ADC Characteristics (continued)**

| # | Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit | Temp Rated | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 | |
| 8 | Zero-scale error | 28-pin packages only | | | | | | | | | |
| | | 10-bit mode | P | $E_{ZS}$ | — | ±0.5 | ±1.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.5 | ±0.5 | | ♦ | ♦ | |
| | | 20-pin packages | | | | | | | | | |
| | | 10-bit mode | P | $E_{ZS}$ | — | ±1.5 | ±2.5 | LSB[2] | ♦ | — | |
| | | 8-bit mode | | | — | ±0.5 | ±0.7 | | ♦ | — | |
| | | 16-pin packages | | | | | | | | | |
| | | 10-bit mode | P | $E_{ZS}$ | — | ±1.5 | ±2.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | ±0.5 | ±0.7 | | ♦ | ♦ | |

**Table A-12. ADC Characteristics (continued)**

| # | Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit | Temp Rated | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Standard | AEC Grade 0 | |
| | Full-scale error | 28-pin packages only | | | | | | | | | |
| | | 10-bit mode | T | $E_{FS}$ | 0 | ±0.5 | ±1 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | 0 | ±0.5 | ±0.5 | LSB[2] | ♦ | ♦ | |
| | | 20-pin packages | | | | | | | | | |
| | | 10-bit mode | T | $E_{FS}$ | 0 | ±1.0 | ±1.5 | LSB[2] | ♦ | — | |
| | | 8-bit mode | | | 0 | ±0.5 | ±0.5 | LSB[2] | ♦ | — | |
| | | 16-pin packages | | | | | | | | | |
| | | 10-bit mode | T | $E_{FS}$ | 0 | ±1.0 | ±1.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | 0 | ±0.5 | ±0.5 | LSB[2] | ♦ | ♦ | |
| | Quantization error | 10-bit mode | D | $E_Q$ | — | — | ±0.5 | LSB[2] | ♦ | ♦ | |
| | | 8-bit mode | | | — | — | ±0.5 | LSB[2] | ♦ | ♦ | |
| | Input leakage error | 10-bit mode | D | $E_{IL}$ | 0 | ±0.2 | ±2.5 | LSB[2] | ♦ | ♦ | Pad leakage[3] * $R_{AS}$ |
| | | 8-bit mode | | | 0 | ±0.1 | ±1 | LSB[2] | ♦ | ♦ | |
| | Temp sensor slope | -40°C to 25°C | D | m | — | 3.266 | — | mV/°C | ♦ | ♦ | |
| | | 25°C to 125°C | | | — | 3.638 | — | mV/°C | ♦ | ♦ | |
| | Temp sensor voltage | 25°C | D | $V_{TEMP25}$ | — | 1.396 | — | V | ♦ | ♦ | |

1 Typical values assume $V_{DD}$ = 5.0 V, Temp = 25°C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

# A.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

## A.12.1 Control Timing

**Table A-13. Control Timing**

| Num | C | Rating | Symbol | Min | Typ[1] | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | D | Bus frequency ($t_{cyc}$ = 1/$f_{Bus}$) -40 C to 125 C | $f_{Bus}$ | dc | — | 20 | MHz | ♦ | — |
| | | > 125 C | | dc | — | 18 | MHz | — | ♦ |
| 2 | D | Internal low power oscillator period -40 C to 125 C | $t_{LPO}$ | 700 | | 1500 | µs | ♦ | — |
| | | > 125 C | | 600 | | 1500 | µs | — | ♦ |
| 3 | D | External reset pulse width[2] | $t_{extrst}$ | 100 | | — | ns | ♦ | ♦ |
| 4 | D | Reset low drive[3] | $t_{rstdrv}$ | 66 x $t_{cyc}$ | | — | ns | ♦ | ♦ |
| 5 | D | Pin interrupt pulse width Asynchronous path[2] / Synchronous path[4] | $t_{ILIH}$, $t_{IHIL}$ | 100 / 1.5 x $t_{cyc}$ | — | — | ns | ♦ | ♦ |
| 6 | C | Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] | | | | | | | |
| | | Slew rate control disabled (PTxSE = 0) | $t_{Rise}$, $t_{Fall}$ | — | 40 | — | ns | ♦ | ♦ |
| | | Slew rate control enabled (PTxSE = 1) | | — | 75 | — | | ♦ | ♦ |
| | | Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] | | | | | | | |
| | | Slew rate control disabled (PTxSE = 0) | $t_{Rise}$, $t_{Fall}$ | — | 11 | — | ns | ♦ | ♦ |
| | | Slew rate control enabled (PTxSE = 1) | $t_{Rise}$, $t_{Fall}$ | — | 35 | — | | ♦ | ♦ |

1 Typical values are based on characterization data at $V_{DD}$ = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 When any reset is initiated, internal circuitry drives the reset pin low for about 66 cycles of $t_{cyc}$. After POR reset, the bus clock frequency changes to the untrimmed DCO frequency ($f_{reset}$ = ($f_{dco_ut}$)/4) because TRIM is reset to 0x80 and FTRIM is reset to 0, and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets trim stays at the pre-reset value.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ levels. Temperature range –40°C to 125°C.

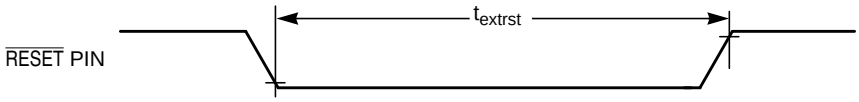



**Figure A-10. Reset Timing**

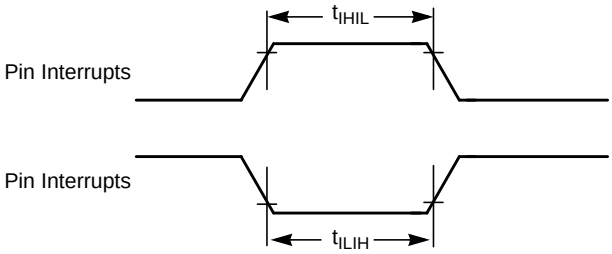



**Figure A-11. Pin Interrupt Timing**

## A.12.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table A-14. TPM Input Timing**

| # | C | Rating | Symbol | Min | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Standard | AEC Grade 0 |
| 1 | — | External clock frequency ($1/t_{TCLK}$) | $f_{TCLK}$ | dc | $f_{Bus}/4$ | MHz | ♦ | ♦ |
| 2 | — | External clock period | $t_{TCLK}$ | 4 | — | $t_{cyc}$ | ♦ | ♦ |
| 3 | — | External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ | ♦ | ♦ |
| 4 | — | External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ | ♦ | ♦ |
| 5 | — | Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ | ♦ | ♦ |

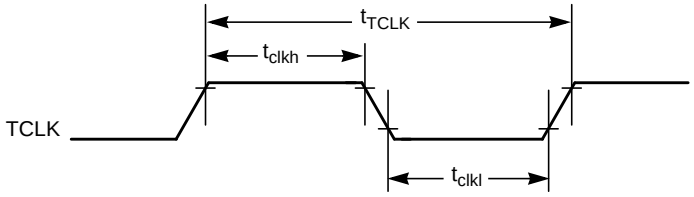



**Figure A-12. Timer External Clock**

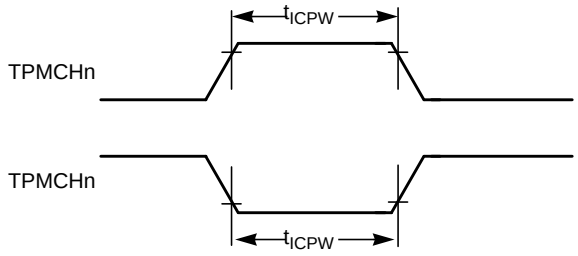



**Figure A-13. Timer Input Capture Pulse**

## A.12.3 SPI

Table A-15 and Figure A-14 through Figure A-17 describe the timing requirements for the SPI system.

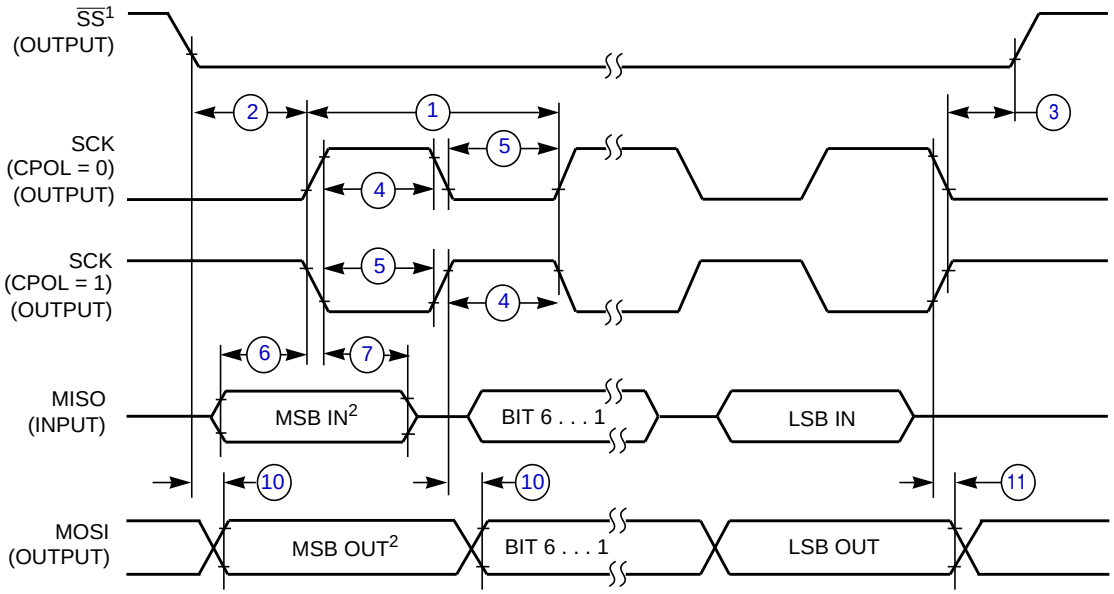
**Table A-15. SPI Electrical Characteristic**

| Num[1] | C | Rating[2] | Symbol | Min | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Standard | AEC Grade 0 |
| 1 | D | Cycle time<br>Master<br>Slave | $t_{SCK}$<br>$t_{SCK}$ | 2<br>4 | 2048<br>— | $t_{cyc}$<br>$t_{cyc}$ | ♦ | ♦ |
| 2 | D | Enable lead time<br>Master<br>Slave | $t_{Lead}$<br>$t_{Lead}$ | —<br>1/2 | 1/2<br>— | $t_{SCK}$<br>$t_{SCK}$ | ♦ | ♦ |
| 3 | D | Enable lag time<br>Master<br>Slave | $t_{Lag}$<br>$t_{Lag}$ | —<br>1/2 | 1/2<br>— | $t_{SCK}$<br>$t_{SCK}$ | ♦ | ♦ |
| 4 | D | Clock (SPSCK) high time<br>Master and Slave | $t_{SCKH}$ | 1/2 $t_{SCK}$ – 25 | — | ns | ♦ | ♦ |
| 5 | D | Clock (SPSCK) low time<br>Master and Slave | $t_{SCKL}$ | 1/2 $t_{SCK}$ – 25 | — | ns | ♦ | ♦ |
| 6 | D | Data setup time (inputs)<br>Master<br>Slave | $t_{SI(M)}$<br>$t_{SI(S)}$ | 30<br>30 | —<br>— | ns<br>ns | ♦ | ♦ |
| 7 | D | Data hold time (inputs)<br>Master<br>Slave | $t_{HI(M)}$<br>$t_{HI(S)}$ | 30<br>30 | —<br>— | ns<br>ns | ♦ | ♦ |
| 8 | D | Access time, slave[3] | $t_A$ | 0 | 40 | ns | ♦ | ♦ |
| 9 | D | Disable time, slave[4] | $t_{dis}$ | — | 40 | ns | ♦ | ♦ |
| 10 | D | Data setup time (outputs)<br>Master<br>Slave | $t_{SO}$<br>$t_{SO}$ | —<br>— | 25<br>25 | ns<br>ns | ♦ | ♦ |
| 11 | D | Data hold time (outputs)<br>Master<br>Slave | $t_{HO}$<br>$t_{HO}$ | –10<br>–10 | —<br>— | ns<br>ns | ♦ | ♦ |
| 12 | D | Operating frequency<br>Master<br>Slave | $f_{op}$<br>$f_{op}$ | $f_{Bus}$/2048<br>dc | $5^5$<br>$f_{Bus}$/4 | MHz | ♦ | ♦ |

1 Refer to Figure A-14 through Figure A-17.

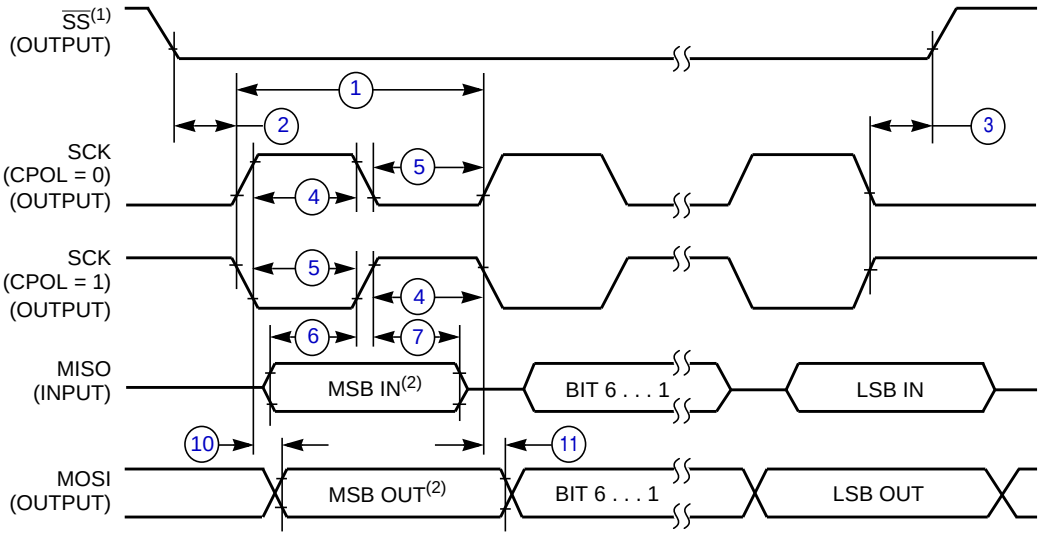
2 All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.
4 Hold time to high-impedance state.
5 Maximum baud rate must be limited to 5 MHz due to input filter characteristics.




NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

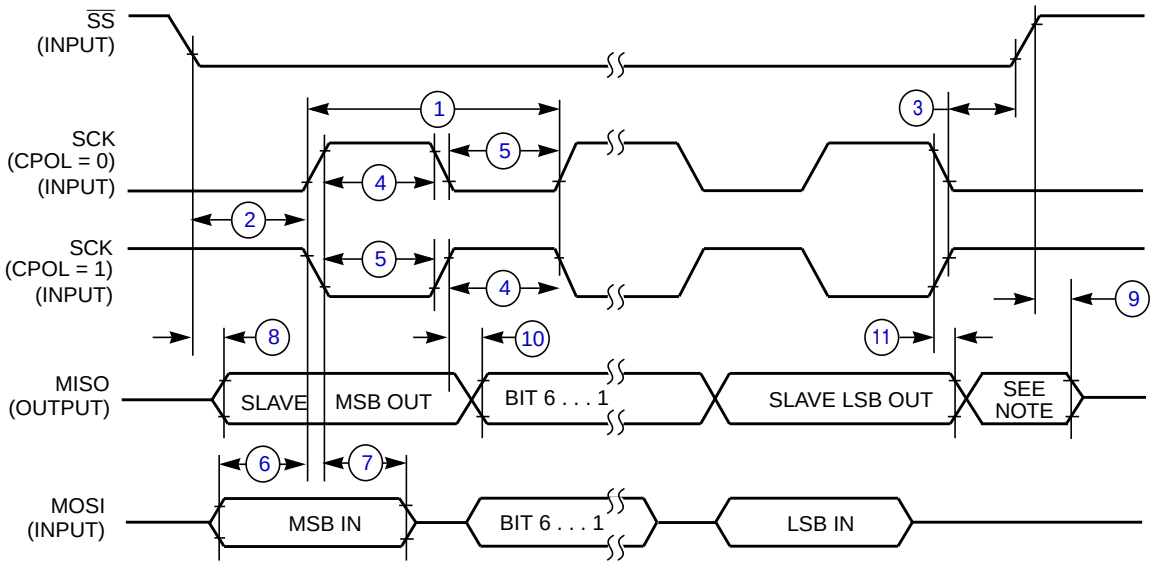
**Figure A-14. SPI Master Timing (CPHA = 0)**




NOTES:

1. SS output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

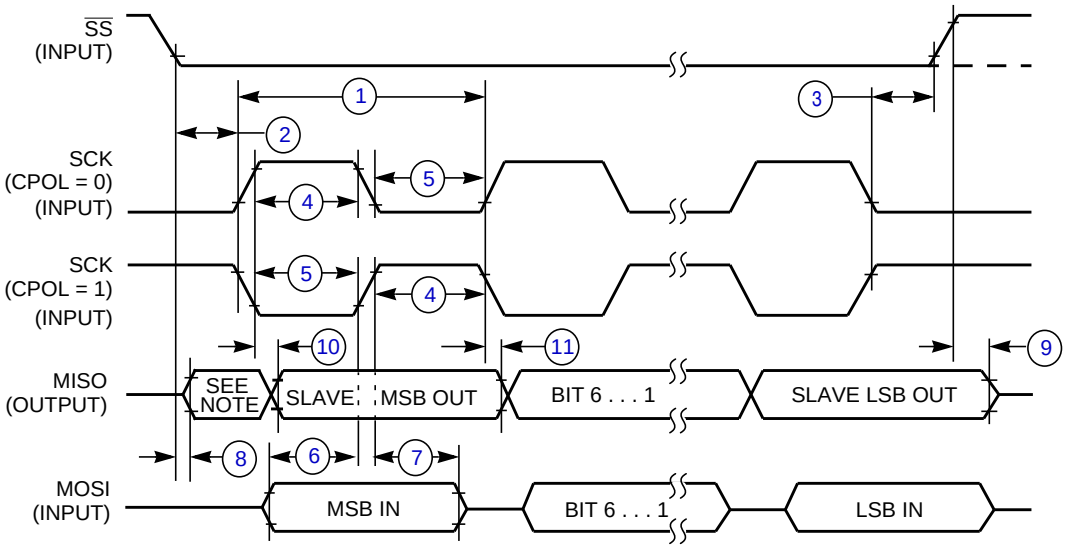
**Figure A-15. SPI Master Timing (CPHA = 1)**




NOTE:

1. Not defined but normally MSB of character just received

**Figure A-16. SPI Slave Timing (CPHA = 0)**




NOTE:
1. Not defined but normally LSB of character just received

**Figure A-17. SPI Slave Timing (CPHA = 1)**

## A.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal $V_{DD}$ supply. For more detailed information about program/erase operations, see the Memory section.

**Table A-16. Flash Characteristics**

| # | C | Characteristic | Symbol | Min | Typical | Max | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Standard | AEC Grade 0 |
| 1 | — | Supply voltage for program/erase | $V_{prog/erase}$ | 2.7 | — | 5.5 | V | ♦ | ♦ |
| 2 | — | Supply voltage for read operation | $V_{Read}$ | 2.7 | — | 5.5 | V | ♦ | ♦ |
| 3 | — | Internal FCLK frequency[1] | $f_{FCLK}$ | 150 | — | 200 | kHz | ♦ | ♦ |
| 4 | — | Internal FCLK period ($1/f_{FCLK}$) | $t_{Fcyc}$ | 5 | — | 6.67 | µs | ♦ | ♦ |
| 5 | — | Byte program time (random location)[2] | $t_{prog}$ | 9 | | | $t_{Fcyc}$ | ♦ | ♦ |
| 6 | — | Byte program time (burst mode)[2] | $t_{Burst}$ | 4 | | | $t_{Fcyc}$ | ♦ | ♦ |
| 7 | — | Page erase time[2] | $t_{Page}$ | 4000 | | | $t_{Fcyc}$ | ♦ | ♦ |
| 8 | — | Mass erase time[2] | $t_{Mass}$ | 20,000 | | | $t_{Fcyc}$ | | |
| 9 | C | Program/erase endurance[3] | $n_{FLPE}$ | | | | cycles | | |
| | | $T_L$ to $T_H$ = –40°C to +125°C | | 10,000 | — | — | | ♦ | — |
| | | $T_L$ to $T_H$ = –40°C to +150°C | | 10,000 | — | — | | — | ♦ |
| | | T = 25°C | | 10,000 | 100,000 | — | | ♦ | ♦ |
| 10 | C | Data retention[4] | $t_{D_ret}$ | 15 | 100 | — | years | ♦ | ♦ |

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for Flash** is based upon the intrinsic bit cell performance. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

## A.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### A.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table A-17. Radiated Emissions, Electric Field**

| Parameter | Symbol | Conditions | Frequency | $f_{OSC}/f_{BUS}$ | Level[1] (Max) | Unit | Temp Rated | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Standard | AEC Grade 0 |
| Radiated emissions, electric field | $V_{RE_TEM}$ | $V_{DD}$ = 5 V<br>$T_A$ = +25°C<br>package type 28 TSSOP | 0.15 – 50 MHz | 4 MHz crystal 20 MHz bus | 12 | dBµV | ♦ | ♦ |
| | | | 50 – 150 MHz | | 12 | | ♦ | ♦ |
| | | | 150 – 500 MHz | | 6 | | ♦ | ♦ |
| | | | 500 – 1000 MHz | | –8 | | ♦ | ♦ |
| | | | IEC Level[2] | | N | — | ♦ | ♦ |
| | | | SAE Level[3] | | 2 | — | ♦ | ♦ |

1 Data based on qualification test results.

2 IEC Level Maximums: N ≤ 12dBµV, L ≤ 24dBµV, I ≤ 36dBµV

3 SAE Level Maximums: 1 ≤ 10dBµV, 2 ≤ 20dBµV, 3 ≤ 30dBµV, 4 ≤ 40dBµV

# Appendix B
# Ordering Information and Mechanical Drawings

## B.1 Ordering Information

This section contains ordering information for MC9S08SG32 and MC9S08SG16 devices.

**Table B-1. Device Numbering System**

| Part Number[1] | Memory | | Temp Rated | | Available Packages[2] | | |
|---|---|---|---|---|---|---|---|
| | Flash | RAM | Standard | AEC Grade 0 | 28-Pin | 20-Pin | 16-Pin |
| MC9S08SG32 | 32K | 1K | ♦ | ♦ | 28 TSSOP | 20 TSSOP[3] | 16 TSSOP |
| MC9S08SG16 | 16K | | ♦ | ♦ | | | |

1 See Table 1-1 for a complete description of modules included on each device.

2 See Table B-2 for package information.

3 20-pin TSSOP package is not available on the AEC Grade 0 high-temperature rated devices.

### B.1.1 Device Numbering Scheme

This device uses a smart numbering system. Refer to the following diagram to understand what each element of the device number represents.

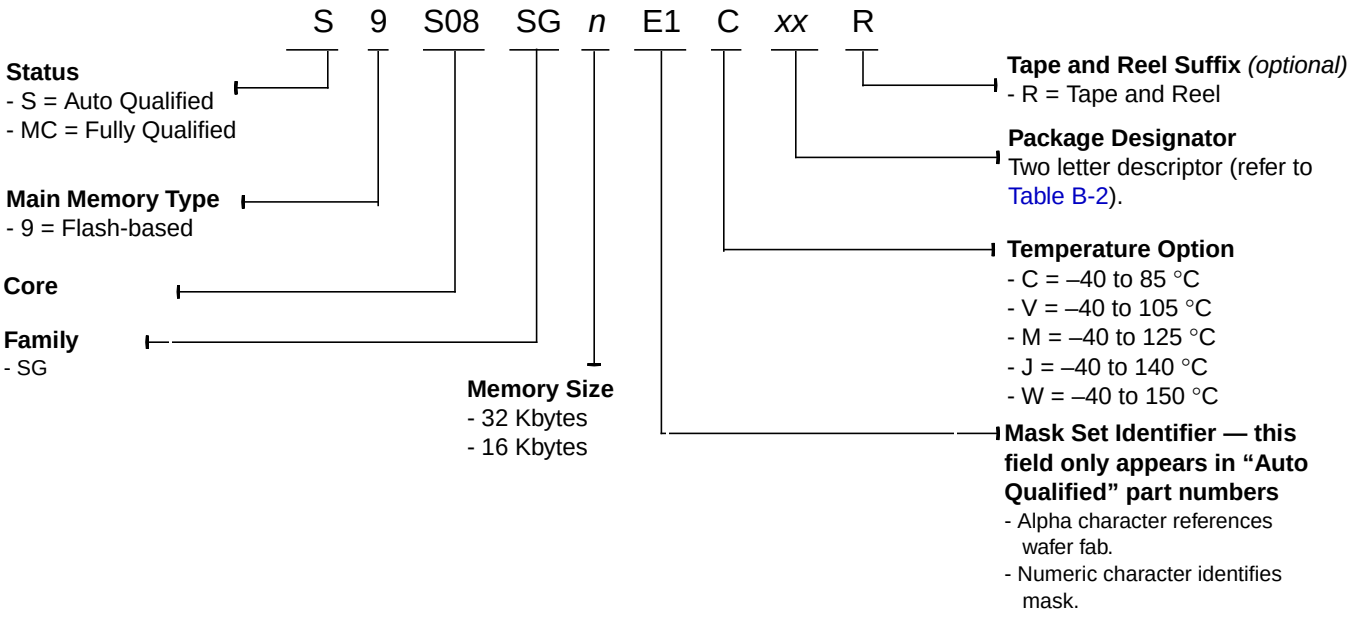



**Figure B-1. MC9S08SG32 Device Numbering Scheme**

## B.2 Package Information and Mechanical Drawings

Table B-2 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08SG32 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table B-2, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table B-2) in the “Enter Keyword” search box at the top of the page.

The following pages are mechanical specifications for MC9S08SG32 Series package options. See Table B-2 for the document number for each package type.

**Table B-2. Package Information**

| Pin Count | Type | Designator | Document No. |
|---|---|---|---|
| 28 | TSSOP | TL | 98ARS23923W |
| 20 | TSSOP | TJ | 98ASH70169A |
| 16 | TSSOP | TG | 98ASH70247A |

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Technical Information Center
Schatzbogen 7
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+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

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