Document Number: MMRF1009H
Rev. 0, 1/2014

RoHS

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

**MMRF1009HR5**
**MMRF1009HSR5**

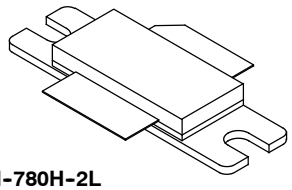
RF power transistors designed for applications operating at frequencies from 900 to 1215 MHz. These devices are suitable for use in defense and commercial pulse applications, such as IFF and DME.

- Typical Pulse Performance: $V_{DD}$ = 50 Vdc, $I_{DQ}$ = 200 mA, Pulse Width = 128 μsec, Duty Cycle = 10%

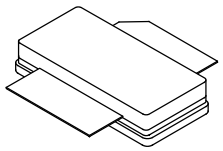
| Application | $P_{out}$ (W) | f (MHz) | $G_{ps}$ (dB) | $\eta_D$ (%) |
|---|---|---|---|---|
| Narrowband | 500 Peak | 1030 | 19.7 | 62.0 |
| Broadband | 500 Peak | 960-1215 | 18.5 | 57.0 |

- Capable of Handling 10:1 VSWR, @ 50 Vdc, 1030 MHz, 500 W Peak Power

**960-1215 MHz, 500 W, 50 V**
**PULSE**
**LATERAL N-CHANNEL**
**RF POWER MOSFETs**



**NI-780H-2L**
**MMRF1009HR5**



**NI-780S-2L**
**MMRF1009HSR5**

**Features**

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50 $V_{DD}$ Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- In Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | -0.5, +110 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | -6.0, +10 | Vdc |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Case Operating Temperature | $T_C$ | 150 | °C |
| Operating Junction Temperature (1) | $T_J$ | 225 | °C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value (2) | Unit |
|---|---|---|---|
| Thermal Impedance, Junction to Case<br>Case Temperature 80°C, 500 W Pulse, 128 μsec Pulse Width, 10% Duty Cycle | $Z_{\theta JC}$ | 0.044 | °C/W |

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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freescale

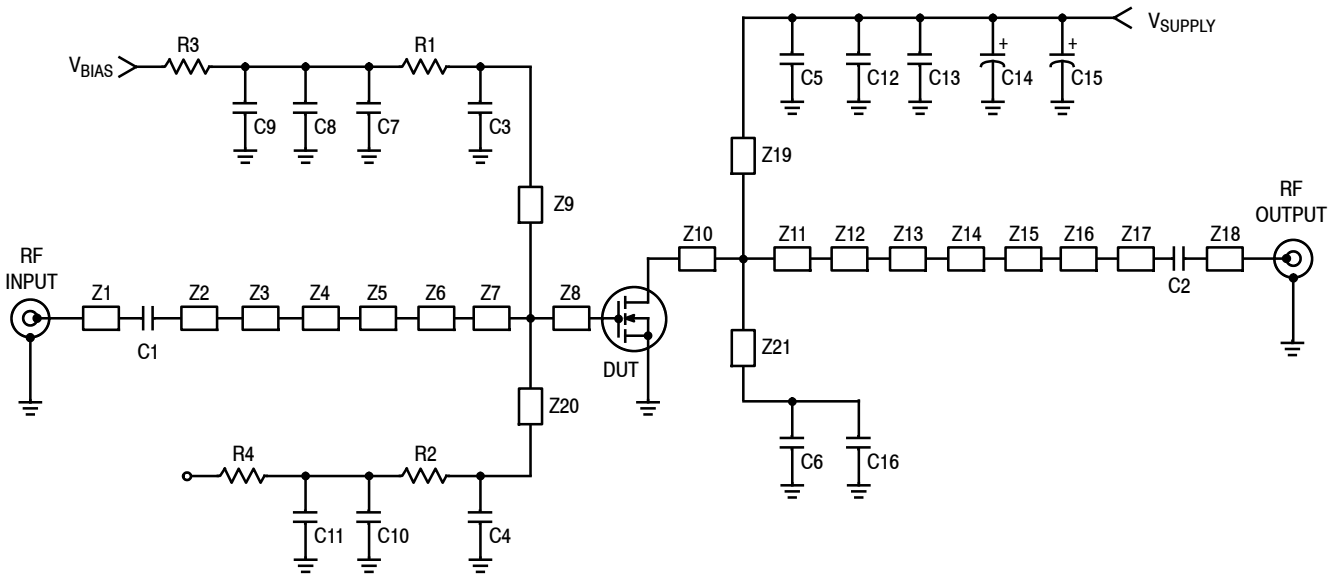
**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 2, passes 2600 V |
| Machine Model (per EIA/JESD22-A115) | B, passes 200 V |
| Charge Device Model (per JESD22-C101) | IV, passes 2000 V |

**Table 4. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics** | | | | | |
| Gate-Source Leakage Current ($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 10 | μAdc |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 200 mA) | $V_{(BR)DSS}$ | 110 | — | — | Vdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 20 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 90 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 200 | μAdc |
| **On Characteristics** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 1.32 mA) | $V_{GS(th)}$ | 0.9 | 1.7 | 2.4 | Vdc |
| Gate Quiescent Voltage ($V_{DD}$ = 50 Vdc, $I_D$ = 200 mAdc, Measured in Functional Test) | $V_{GS(Q)}$ | 1.7 | 2.4 | 3.2 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 3.26 Adc) | $V_{DS(on)}$ | — | 0.25 | — | Vdc |
| **Dynamic Characteristics** (1) | | | | | |
| Reverse Transfer Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{rss}$ | — | 0.2 | — | pF |
| Output Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{oss}$ | — | 697 | — | pF |
| Input Capacitance ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc ± 30 mV(rms)ac @ 1 MHz) | $C_{iss}$ | — | 1391 | — | pF |
| **Functional Tests** (In Freescale Narrowband Test Fixture, 50 ohm system) $V_{DD}$ = 50 Vdc, $I_{DQ}$ = 200 mA, $P_{out}$ = 500 W Peak (50 W Avg.), f = 1030 MHz, 128 μsec Pulse Width, 10% Duty Cycle | | | | | |
| Power Gain | $G_{ps}$ | 18.5 | 19.7 | 22.0 | dB |
| Drain Efficiency | $\eta_D$ | 58.0 | 62.0 | — | % |
| Input Return Loss | IRL | — | -18 | -9 | dB |
| **Typical Broadband Performance — 960-1215 MHz** (In Freescale 960-1215 MHz Test Fixture, 50 ohm system) $V_{DD}$ = 50 Vdc, $I_{DQ}$ = 200 mA, $P_{out}$ = 500 W Peak (50 W Avg.), f = 960-1215 MHz, 128 μsec Pulse Width, 10% Duty Cycle | | | | | |
| Power Gain | $G_{ps}$ | — | 18.5 | — | dB |
| Drain Efficiency | $\eta_D$ | — | 57.0 | — | % |

1. Part internally matched both on input and output.




| | | | |
|---|---|---|---|
| Z1 | 0.457″ x 0.080″ Microstrip | Z11 | 0.161” x 1.500″ Microstrip |
| Z2 | 0.250″ x 0.080″ Microstrip | Z12 | 0.613” x 1.281″ Microstrip |
| Z3 | 0.605″ x 0.040″ Microstrip | Z13 | 0.248” x 0.865″ Microstrip |
| Z4 | 0.080″ x 0.449″ Microstrip | Z14 | 0.087” x 0.425″ Microstrip |
| Z5 | 0.374″ x 0.608″ Microstrip | Z15 | 0.309” x 0.090″ Microstrip |
| Z6 | 0.118″ x 1.252″ Microstrip | Z16 | 0.193” x 0.516″ Microstrip |
| Z7 | 0.778″ x 1.710″ Microstrip | Z17 | 0.279” x 0.080″ Microstrip |
| Z8 | 0.095″ x 1.710″ Microstrip | Z18 | 0.731” x 0.080″ Microstrip |
| Z9, Z20 | 0.482″ x 0.050″ Microstrip | Z19, Z21 | 0.507” x 0.040″ Microstrip |
| Z10 | 0.138″ x 1.500″ Microstrip | PCB | Arlon CuClad 250GX-0300-55-22, 0.030″, $\varepsilon_r$ = 2.55 |

**Figure 1. MMRF1009HR5(HSR5) Test Circuit Schematic**

**Table 5. MMRF1009HR5(HSR5) Test Circuit Component Designations and Values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C2 | 5.1 pF Chip Capacitors | ATC100B5R1CT500XT | ATC |
| C3, C4, C5, C6 | 33 pF Chip Capacitors | ATC100B330JT500XT | ATC |
| C7, C10 | 10 μF, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C8, C11, C13, C16 | 2.2 μF, 100 V Chip Capacitors | 2225X7R225KT3AB | ATC |
| C9 | 22 μF, 25 V Chip Capacitor | TPSD226M025R0200 | AVX |
| C12 | 1 μF, 100 V Chip Capacitor | GRM31CR72A105KA01L | Murata |
| C14, C15 | 470 μF, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| R1, R2 | 56 Ω, 1/4 W Chip Resistors | CRCW120656R0FKEA | Vishay |
| R3, R4 | 0 Ω, 3 A Chip Resistors | CRCW12060000Z0EA | Vishay |

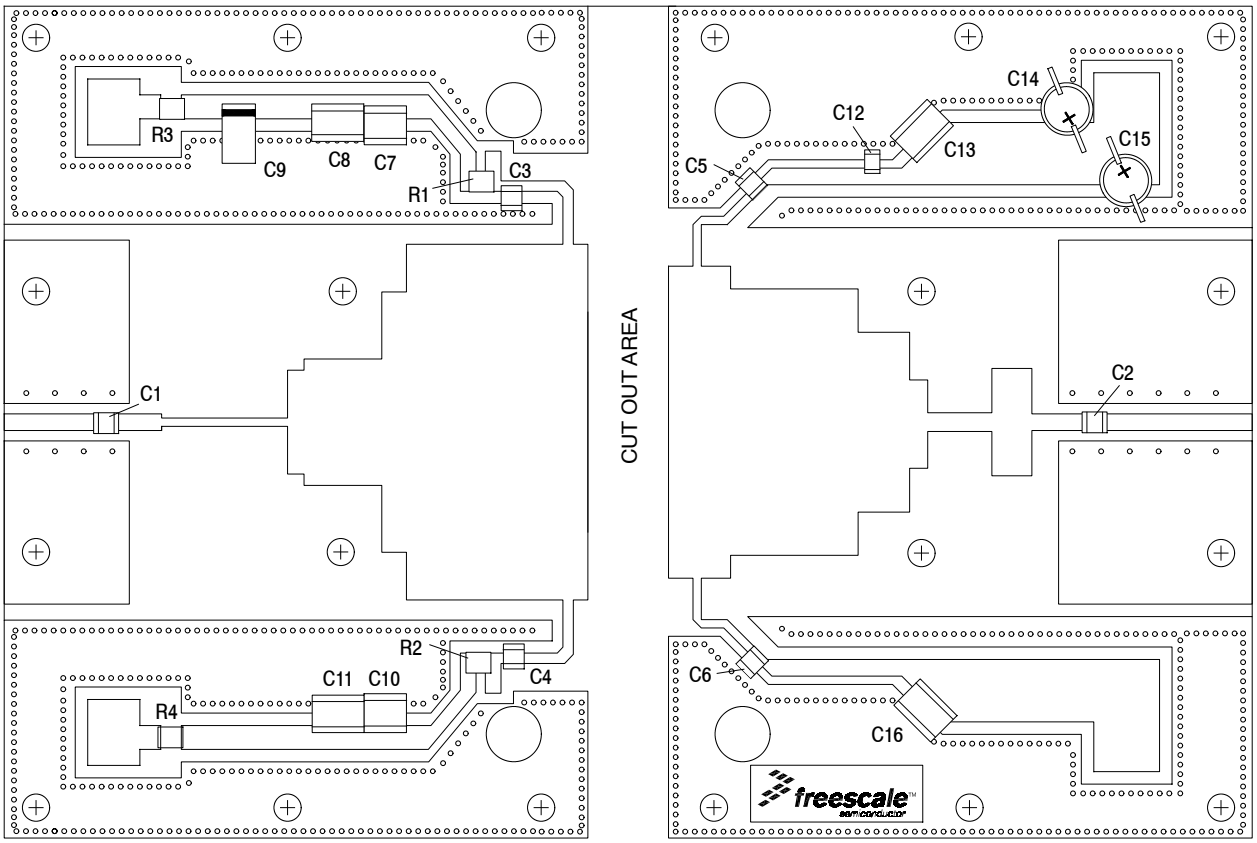



**Figure 2. MMRF1009HR5(HSR5) Test Circuit Component Layout**

## TYPICAL CHARACTERISTICS

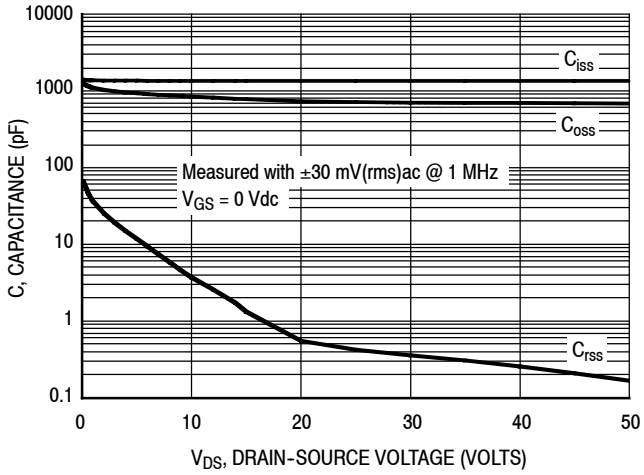



**Figure 3. Capacitance versus Drain-Source Voltage**

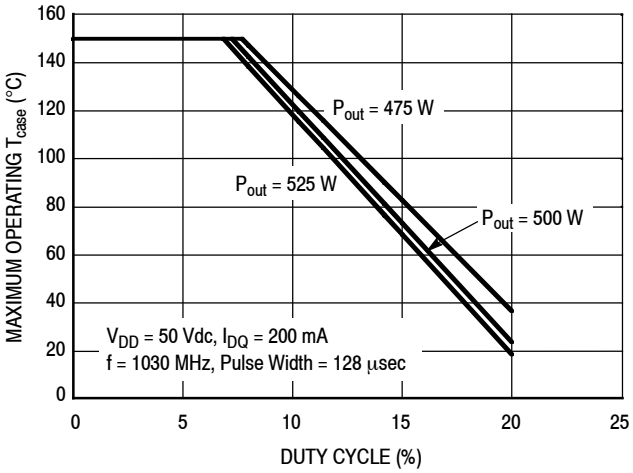



**Figure 4. Safe Operating Area**

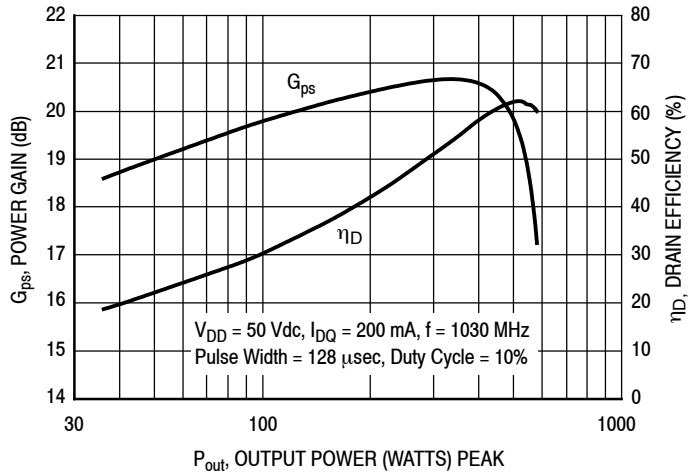



**Figure 5. Power Gain and Drain Efficiency versus Output Power**

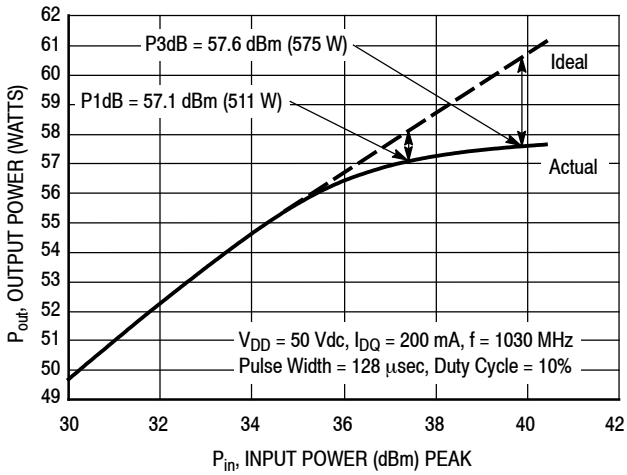



**Figure 6. Output Power versus Input Power**

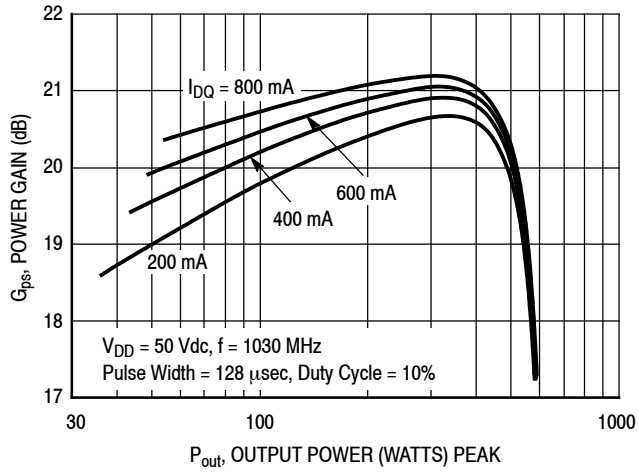



**Figure 7. Power Gain versus Output Power**

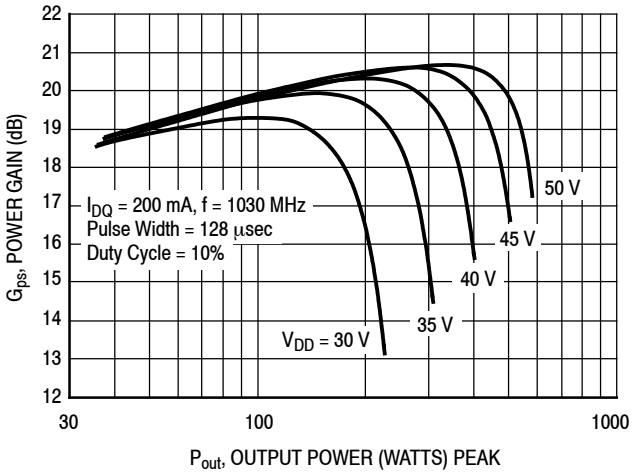



**Figure 8. Power Gain versus Output Power**

## TYPICAL CHARACTERISTICS

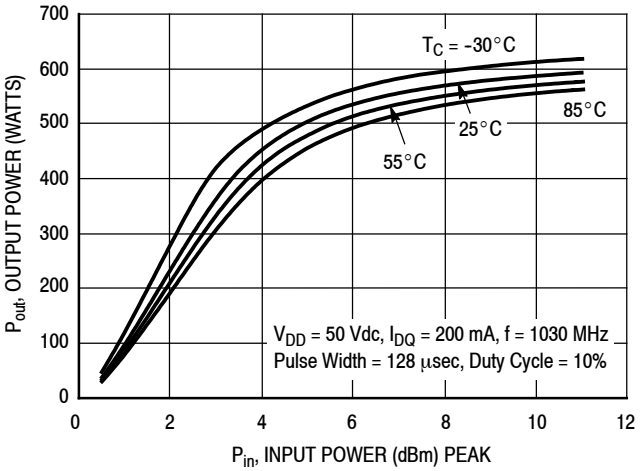



**Figure 9. Output Power versus Input Power**

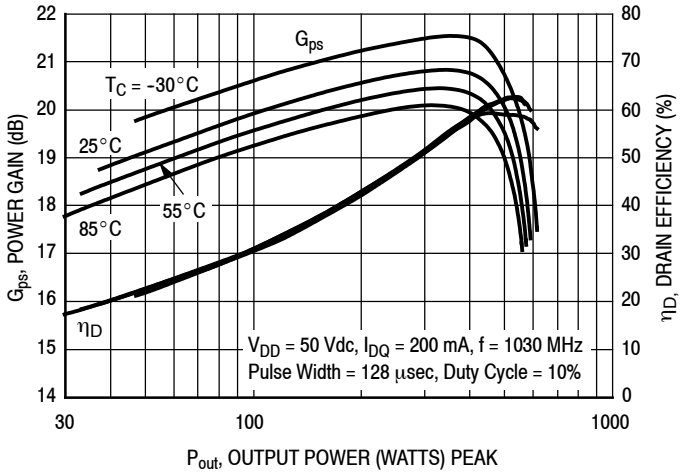
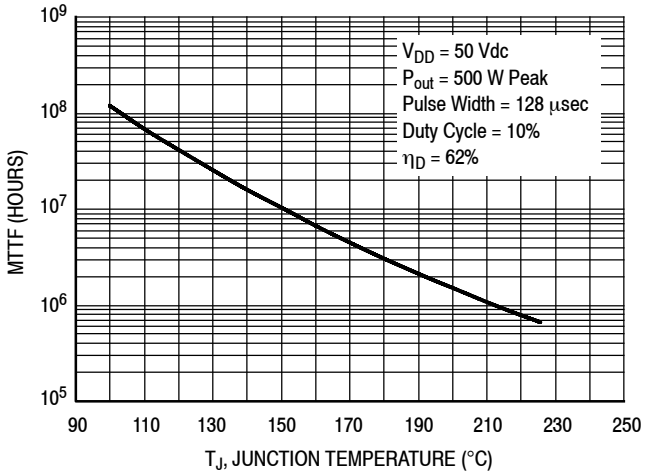



**Figure 10. Power Gain and Drain Efficiency versus Output Power**




MTTF calculator available at http:/www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 11. MTTF versus Junction Temperature**

$V_{DD}$ = 50 Vdc, $I_{DQ}$ = 200 mA, $P_{out}$ = 500 W Peak

| f MHz | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|
| 1030 | 1.36 - j1.27 | 2.50 - j0.17 |

$Z_{source}$ = Test circuit impedance as measured from gate to ground.

$Z_{load}$ = Test circuit impedance as measured from drain to ground.

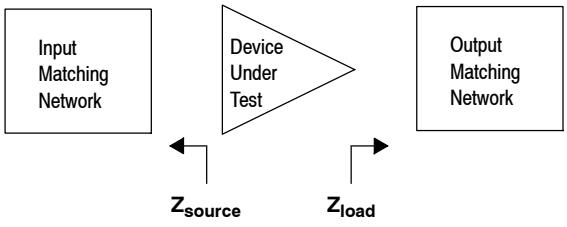



**Figure 12. Series Equivalent Source and Load Impedance**

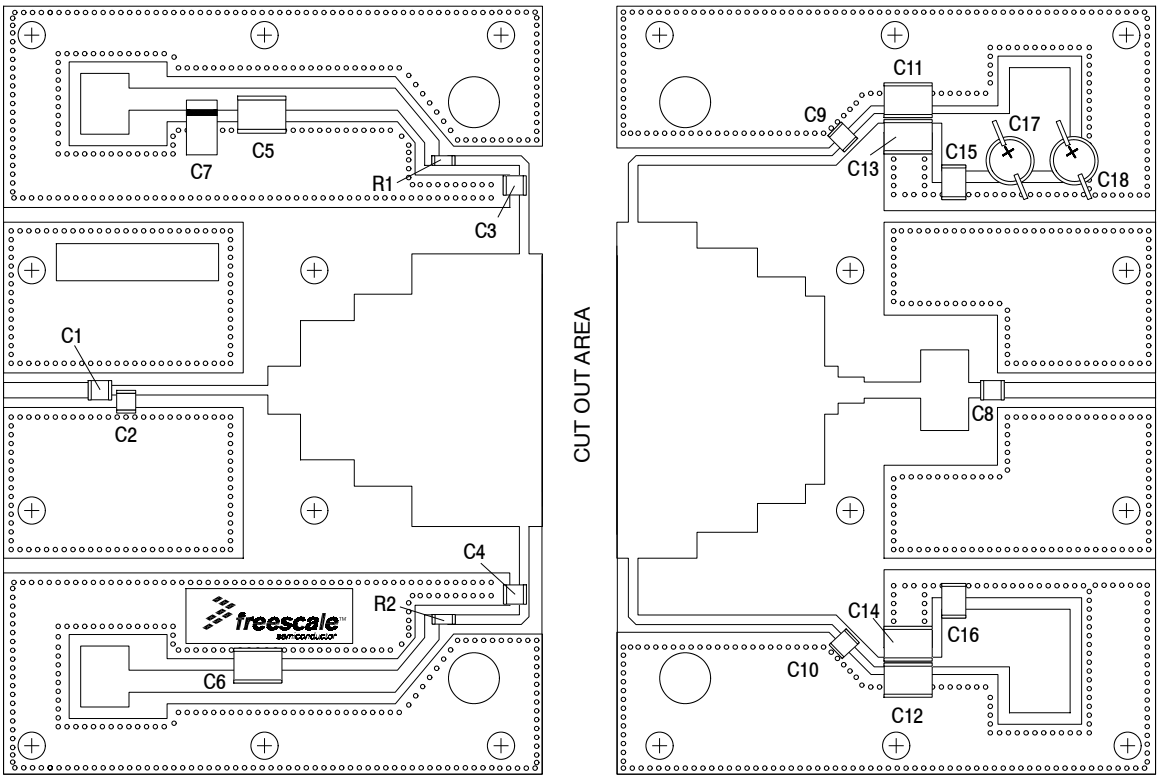



**Figure 13. MMRF1009HR5(HSR5) Test Circuit Component Layout — 960-1215 MHz**

**Table 6. MMRF1009HR5(HSR5) Test Circuit Component Designations and Values — 960-1215 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1 | 2.2 pF Chip Capacitor | ATC100B2R2JT500XT | ATC |
| C2 | 0.2 pF Chip Capacitor | ATC100B0R2BT500XT | ATC |
| C3, C4 | 33 pF Chip Capacitors | ATC100B330JT500XT | ATC |
| C5, C6, C11, C12 | 2.2 μF, 100 V Chip Capacitors | G2225X7R225KT3AB | ATC |
| C7 | 22 μF, 35 V Tantalum Capacitor | T491X226K035AT | Kemet |
| C8 | 8.2 pF Chip Capacitor | ATC100B8R2CT500XT | ATC |
| C9, C10 | 39 pF Chip Capacitors | ATC100B390JT500XT | ATC |
| C13, C14 | 0.022 μF, 100 V Chip Capacitors | C1825C223K1GAC | Kemet |
| C15, C16 | 0.10 μF, 100 V Chip Capacitors | C1812F104K1RAC | Kemet |
| C17, C18 | 470 μF, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| R1, R2 | 22 Ω, 1/4 W Chip Resistors | CRCW120622R0FKEA | Vishay |
| PCB | 0.030″, $\varepsilon_r$ = 2.55 | AD255A | Arlon |

## TYPICAL CHARACTERISTICS — 960–1215 MHz

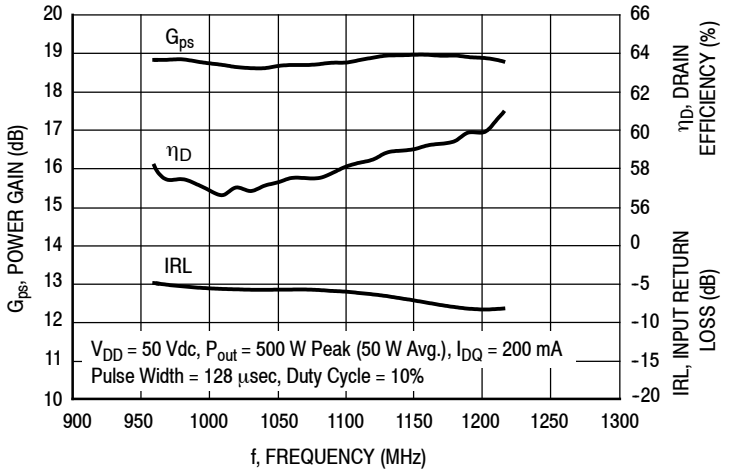



**Figure 14. Power Gain, Drain Efficiency and IRL versus Frequency**

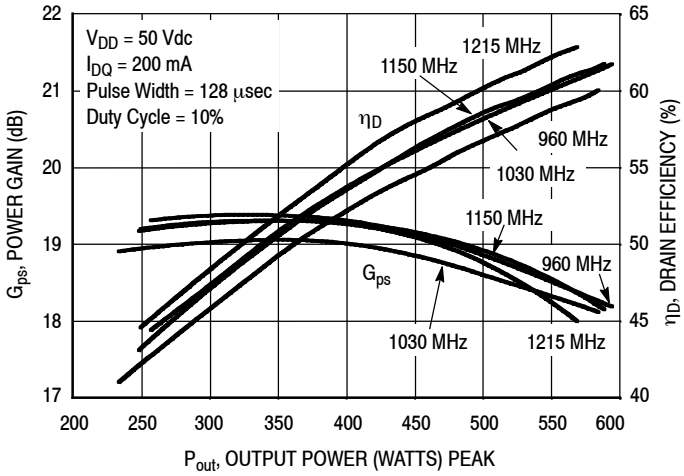
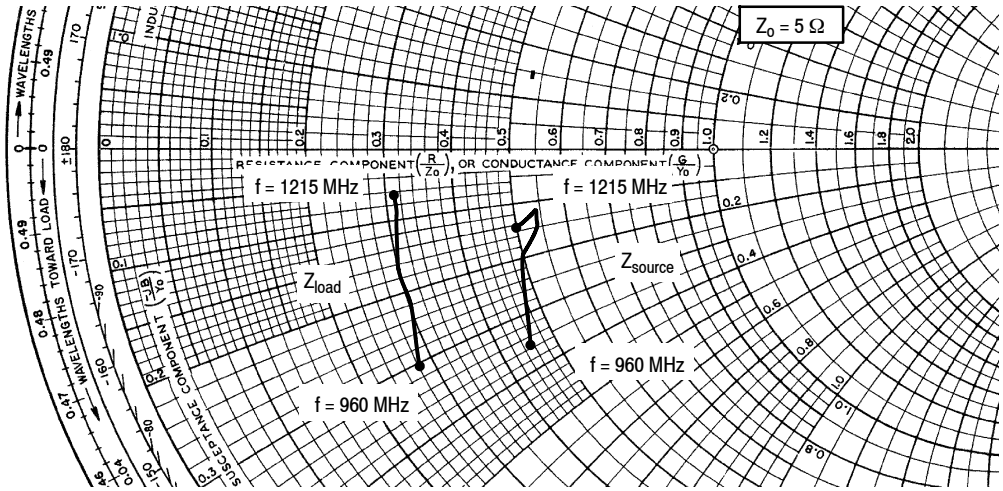



**Figure 15. Power Gain and Drain Efficiency versus Output Power**




$V_{DD}$ = 50 Vdc, $I_{DQ}$ = 200 mA, $P_{out}$ = 500 W Peak

| f MHz | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|
| 960 | 2.25 – j1.78 | 1.38 – j1.53 |
| 1030 | 2.51 – j1.02 | 1.48 – j1.11 |
| 1090 | 2.69 – j0.73 | 1.51 – j0.78 |
| 1150 | 2.71 – j0.65 | 1.53 – j0.49 |
| 1215 | 2.48 – j0.76 | 1.53 – j0.33 |

$Z_{source}$ = Test circuit impedance as measured from gate to ground.

$Z_{load}$ = Test circuit impedance as measured from drain to ground.

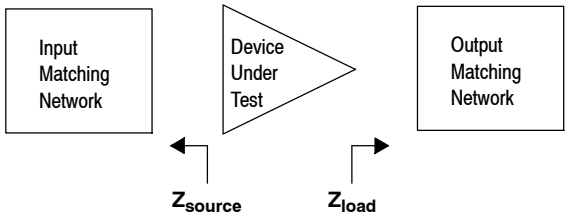
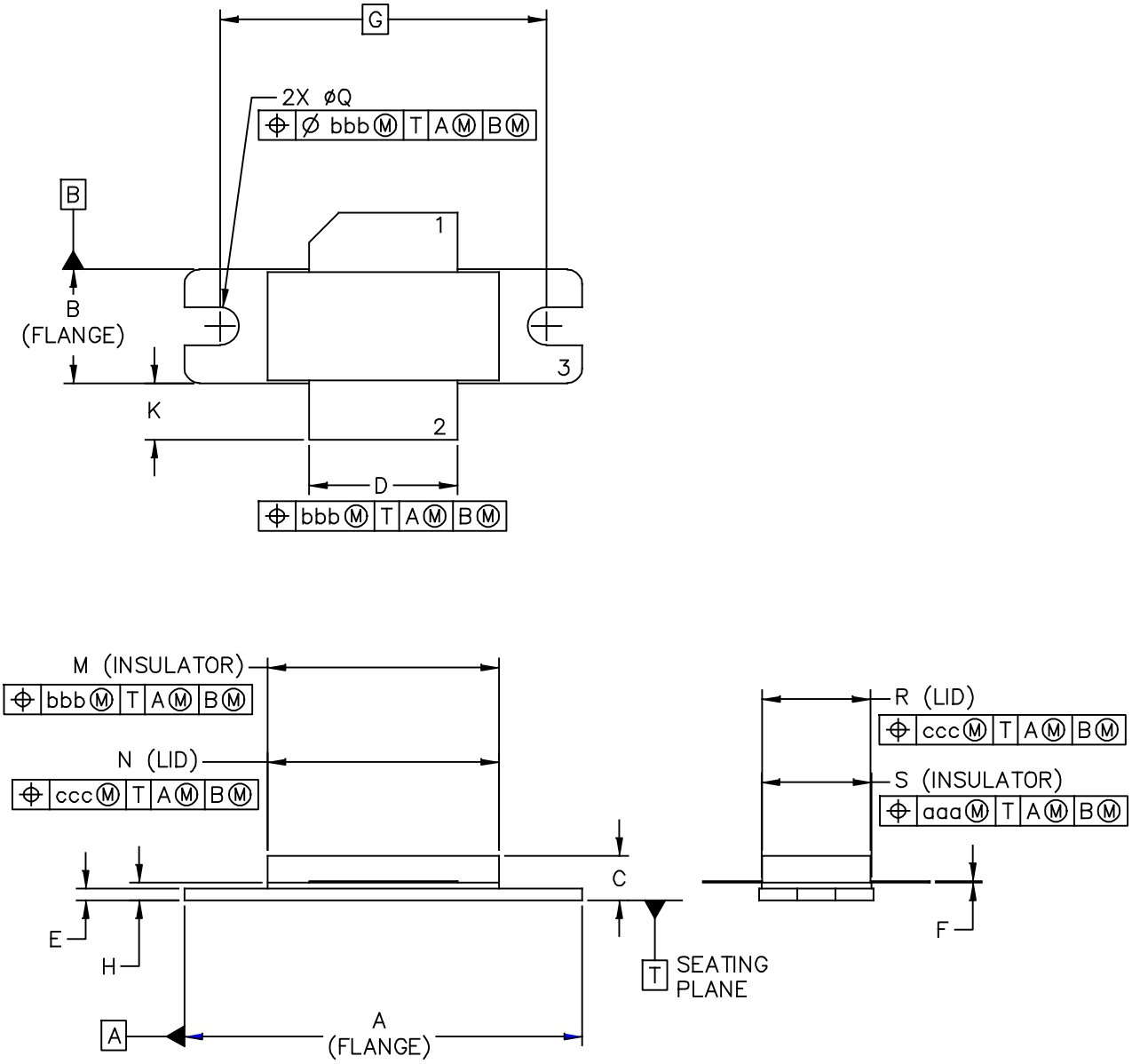



**Figure 16. Series Equivalent Source and Load Impedance — 960–1215 MHz**

## PACKAGE DIMENSIONS

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| TITLE: NI-780 | DOCUMENT NO: 98ASB15607C | REV: G |
| | CASE NUMBER: 465-06 | 31 MAR 2005 |
| | STANDARD: NON-JEDEC | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | 1.335 | 1.345 | 33.91 | 34.16 | R | .365 | .375 | 9.27 | 9.53 |
| B | .380 | .390 | 9.65 | 9.91 | S | .365 | .375 | 9.27 | 9.52 |
| C | .125 | .170 | 3.18 | 4.32 | aaa | — | .005 | — | 0.127 |
| D | .495 | .505 | 12.57 | 12.83 | bbb | — | .010 | — | 0.254 |
| E | .035 | .045 | 0.89 | 1.14 | ccc | — | .015 | — | 0.381 |
| F | .003 | .006 | 0.08 | 0.15 | — | — | — | — | — |
| G | 1.100 BSC | | 27.94 BSC | | — | — | — | — | — |
| H | .057 | .067 | 1.45 | 1.7 | — | — | — | — | — |
| K | .170 | .210 | 4.32 | 5.33 | — | — | — | — | — |
| M | .774 | .786 | 19.66 | 19.96 | — | — | — | — | — |
| N | .772 | .788 | 19.6 | 20 | — | — | — | — | — |
| Q | ø.118 | ø.138 | ø3 | ø3.51 | — | — | — | — | — |

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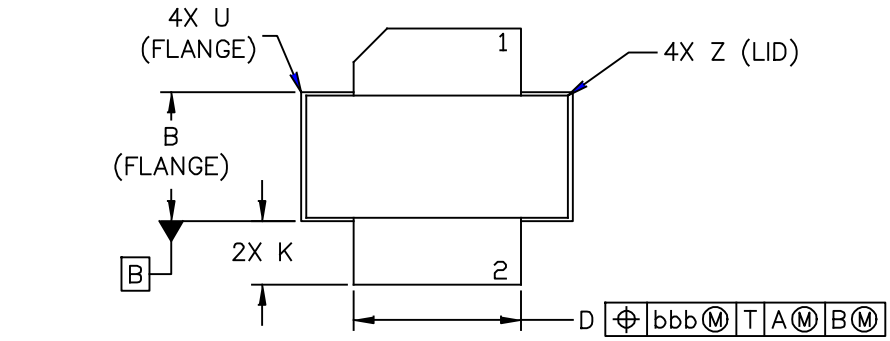
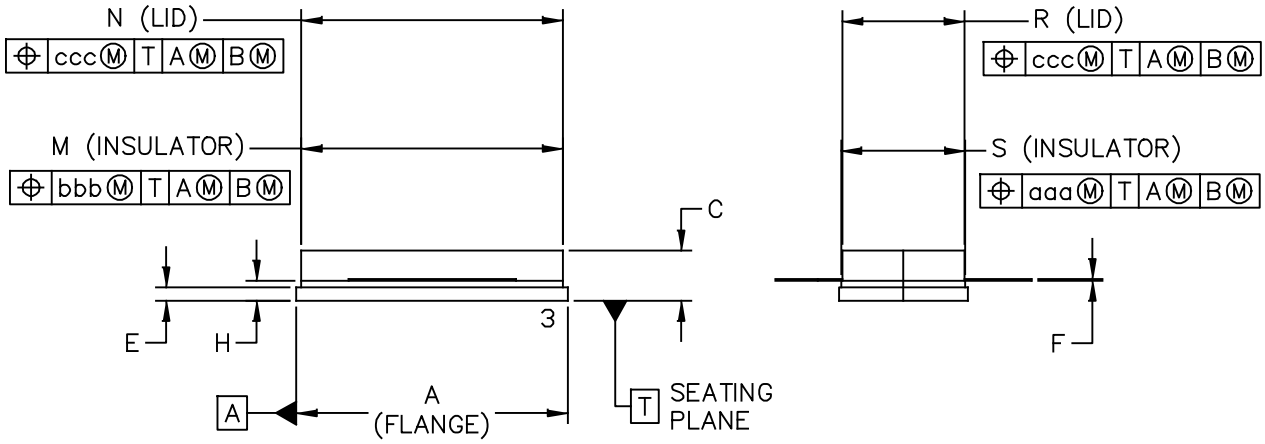
| NI–780 | CASE NUMBER: 465–06 | 31 MAR 2005 |
| | STANDARD: NON–JEDEC | |

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| TITLE: NI-780S | DOCUMENT NO: 98ASB16718C | REV: H |
| | CASE NUMBER: 465A-06 | 31 MAR 2005 |
| | STANDARD: NON-JEDEC | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH.

3. DELETED

4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .805 | .815 | 20.45 | 20.7 | U | – | .040 | – | 1.02 |
| B | .380 | .390 | 9.65 | 9.91 | Z | – | .030 | – | 0.76 |
| C | .125 | .170 | 3.18 | 4.32 | aaa | – | .005 | – | 0.127 |
| D | .495 | .505 | 12.57 | 12.83 | bbb | – | .010 | – | 0.254 |
| E | .035 | .045 | 0.89 | 1.14 | ccc | – | .015 | – | 0.381 |
| F | .003 | .006 | 0.08 | 0.15 | – | – | – | – | – |
| H | .057 | .067 | 1.45 | 1.7 | – | – | – | – | – |
| K | .170 | .210 | 4.32 | 5.33 | – | – | – | – | – |
| M | .774 | .786 | 19.61 | 20.02 | – | – | – | – | – |
| N | .772 | .788 | 19.61 | 20.02 | – | – | – | – | – |
| R | .365 | .375 | 9.27 | 9.53 | – | – | – | – | – |
| S | .365 | .375 | 9.27 | 9.52 | – | – | – | – | – |

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|---|---|---|
| NI–780S | CASE NUMBER: 465A–06 | 31 MAR 2005 |
| | STANDARD: NON–JEDEC | |

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

**Application Notes**

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | Jan. 2014 | • Initial Release of Data Sheet |

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