ACPL-33JT

Automotive 2.5 Amp Gate Drive Optocoupler with Integrated Flyback Controller for Isolated DC-DC Converter, Integrated IGBT Desat Over Current Sensing, Miller Current Clamping and UVLO Feedback

Data Sheet

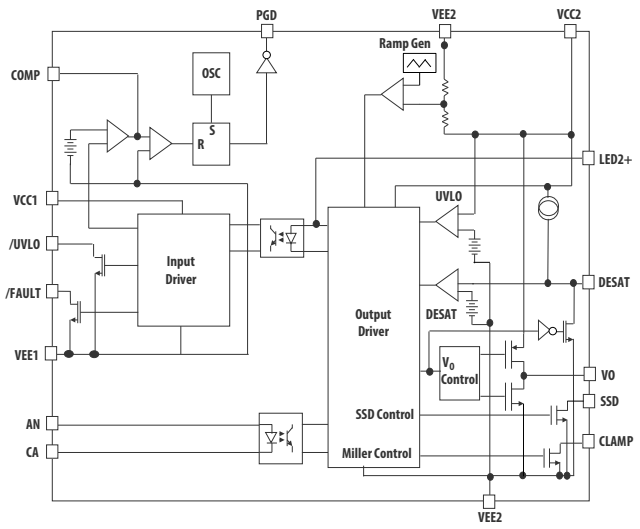
Description

The ACPL-33JT Automotive 2.5 Amp Gate Drive Optocoupler features integrated flyback controller for isolated DC-DC converter, IGBT desaturation sensing and fault feedback, Under-Voltage LockOut (UVLO) with soft-shutdown and fault feedback and active Miller current clamping. The fast propagation delay with excellent timing skew performance enables excellent timing control and efficiency. This full feature optocoupler comes in a compact, surface-mountable SO-16 package for space-savings, is suitable for traction power train inverter, power converter, battery charger, air-conditioner and oil pump motor drives in HEV and EV applications.

Avago R2Coupler® isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram

Figure 1 ACPL-33JT Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Integrated flyback controller for isolated DC-DC converter
- Regulated output voltage: 16 V
- Peak output current: 2.5 A max.
- Miller clamp sinking current: 2 A
- Input supply voltage range: 4.5 V to 5.5 V
- Common Mode Rejection (CMR): > 50 kV/µs at V_{CM} = 1500 V
- Propagation delay: 250 ns max.
- Integrated fail-safe IGBT protection
  - Desat sensing, "Soft" IGBT turn-off and Fault feedback
  - Under Voltage Lock-Out (UVLO) protection with feedback
- High Noise Immunity
  - Miller current clamping
  - Direct LED input with low input impedance and low noise sensitivity
- SO-16 package with 8mm clearance and creepage
- Regulatory approvals:
  - UL1577, CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive Isolated IGBT/MOSFET Inverter gate drive
- Automotive DC-DC Converter
- AC and brushless DC motor drives
- Hybrid and Plug-in hybrid power train inverter
- Un-interruptible Power Supplies (UPS)

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-33JT	–50JE	SO-16	X	X	X	850 per reel

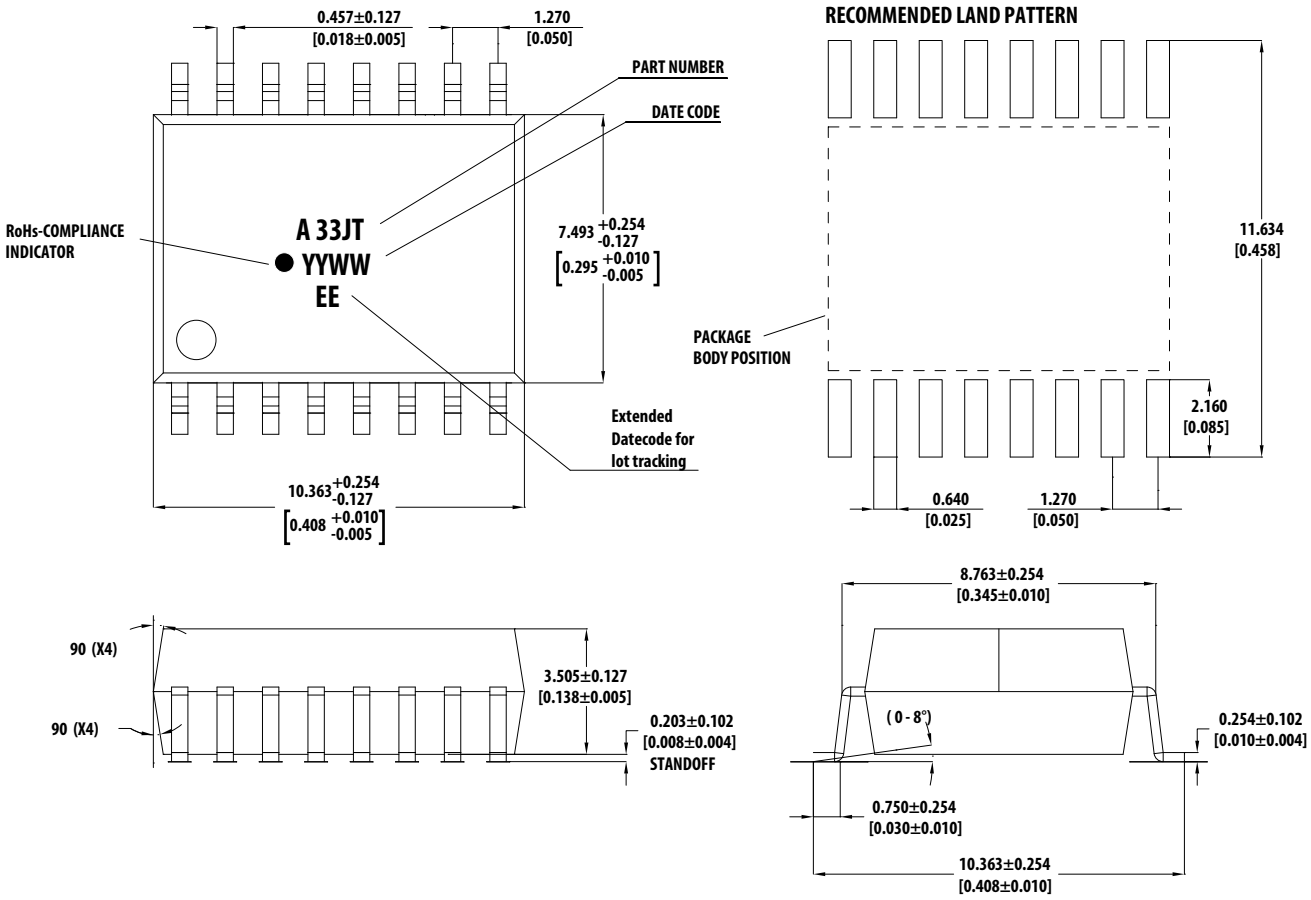
To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

Example:

ACPL-33JT-50JE to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings (16-Lead Surface Mount)



Dimensions in millimeters (inches)

NOTE

- Lead coplanarity = 0.10 mm (0.004 inches) Max
- Floating lead protrusion = 0.254 mm ([0.010 inches) Max
- Mold flash on each side = 0.254 mm (0.010 inches) Max

Recommended Lead-free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

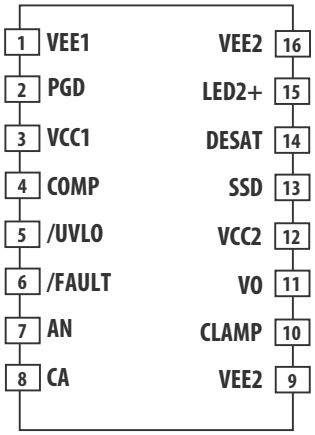
Non-halide flux should be used.

Product Overview Description

The ACPL-33JT (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, reliable, isolated IGBT gate drive circuit. It features a flyback controller for isolated DC-DC converter, a high current gate driver, Miller current clamping, IGBT desaturation sensing, IGBT soft shutdown (SSD), fault feeback and Under Voltage Lock-Out (UVLO) protection and feedback in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increases its noise immunity.

Package Pinout

Figure 2 Pin out of ACPL-33JT



Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	VEE1	Input IC common	16	VEE2	Output IC common and IGBT emitter reference
2	PGD	Primary gate drive for MOSFET	15	LED2+	No connection, for testing only
3	VCC1	Input power supply	14	DESAT	Desaturation over current sensing
4	COMP	Compensation network for Flyback Controller	13	SSD	Soft Shutdown
5	/UVLO	VCC2 Under Voltage Lock-Out feedback	12	VCC2	Output power supply
6	/FAULT	Over current fault feedback	11	VO	Driver output to IGBT gate
7	AN	Input LED anode	10	CLAMP	Miller current clamping output
8	CA	Input LED cathode	9	VEE2	Output IC common and IGBT emitter reference

Regulatory Information

The ACPL-33JT is approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to VISO = 5000 VRMS.
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN EN 60747-5-5	Approved under: IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5, IEC/EN/DIN EN60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 V_{rms} for rated mains voltage ≤ 300 V_{rm}s for rated mains voltage ≤ 600 V_{rms} for rated mains voltage ≤ 1000 V_{rms}		 I – IV I – IV I – IV I – III	
Climatic Classification[a]		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} ×1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Power Output Power	 T_S $P_{S,INPUT}$ $P_{S,OUTPUT}$	 175 400 1200	 °C mW mW
Insulation Resistance at T_S, VIO = 500V	RS	$> 10^9$	Ohm

a. Climatic classification denotes minimum operating temperature/ maximum operating temperature/ humidity test duration.

NOTE

1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC 60747-5-5, EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
Output IC Junction Temperature	T_J		150	°C	a
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		6.0	V	
Input Supply Voltage [b]	$V_{CC1} – V_{EE1}$	–0.5	6.0	V	
Primary Gate Drive Voltage[b]	$V_{PGD} – V_{EE1}$	–0.5	V_{CC1}	V	
COMP Pin Voltage [b]	$V_{COMP} – V_{EE1}$	–0.5	V_{CC1}	V	
/UVLO Output Current[c]	I/UVLO		10	mA	
/UVLO Pin Voltage[b]	V/UVLO – V_{EE1}	–0.5	6.0	V	d
/Fault Output Current[c]	I/FAULT		10	mA	
/Fault Pin Voltage[b]	V/FAULT – V_{EE1}	–0.5	6.0	V	d
Output Supply Voltage[b]	$V_{CC2} – V_{EE2}$	–0.5	25	V	
Peak Output Current[c]	$\|I_{O(peak)}\|$		2.5	A	e
Gate Drive Output Voltage [b]	$V_{O(peak)} – V_{EE2}$	–0.5	V_{CC2}+0.5	V	
Miller Clamping Pin Voltage[b]	$V_{CLAMP} – V_{EE2}$	–0.5	V_{CC2}+0.5	V	f
Desat Voltage[b]	$V_{DESAT} – V_{EE2}$	–0.5	V_{CC2}+0.5	V	g
Soft Shutdown Pin Voltage[b]	$V_{SSD} – V_{EE2}$	–0.5	V_{CC2}+0.5	V	
Output IC Power Dissipation	P_O		600	mW	a
Input IC Power Dissipation	P_I		150	mW	a

a. Input IC power dissipation is derated linearly above 10 0°C from 15 0mW to 100 mW at 125 °C for high effective thermal conductivity board. Output IC power dissipation is derated linearly above 100 °C from 600 mW to 350 mW at 125 °C for high effective thermal conductivity board; see Figure 5. For power derating with low effective thermal conductivity board, see Figure 4.

b. Absolute maximum voltage ratings imply transistor off state.

c. Absolute maximum current ratings imply transistor on state.

d. Duration of absolute maximum voltage applied to /UVLO or /Fault pin during the internal MOS turns ON is limited to maximum 10 µs with maximum 5% duty cycle.

e. Maximum pulse width=1 µs, maximum duty cycle=1%.

f. When CLAMP pin is turned on, maximum pulse width is limited to 1 µs, maximum duty cycle=2%.

g. Maximum pulse width=5 µs, maximum duty cycle=10%.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	–40	125	°C	
Input IC Supply Voltage	V_{CC1}	4.5	5.5	V	a
Total Output IC Supply Voltage	$V_{CC2} – V_{EE2}$	15.2	16.8	V	b
Input LED Turn on Current	$I_{F(ON)}$	10	16	mA	
Input LED Turn off Voltage (VAN–VCA)	$V_{F(OFF)}$	–5.5	0.8	V	
Maximum PWM Duty Cycle	D_{MAX}		50	%	
Input Pulse Width	$t_{ON(LED)}$	500		ns	

a. In most applications, V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that the input remains low until V_{CC1} reaches the proper operating voltage to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down).

b. 15.2V is the recommended minimum operating supply voltage ($V_{CC2} – V_{EE2}$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 14.5V.

Electrical Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1}, all voltages at output IC are referenced to V_{EE2}. All typical values at T_A = 25 °C, V_{CC1} = 5 V, $V_{CC2} – V_{EE2}$ = 16 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
DCDC Flyback Converter								
VCC1 MOS Threshold	V_{CC1_MOSTH}	0.4	1.2	1.7	V	I_{FAULT} = 2.0 mA		
VCC1 Turn on Threshold	V_{CC1_TH}	3.7	4.0	4.3	V			
VCC1 Turn on Threshold Hysteresis	$V_{CC1\_TH\_HYS}$	0.05	0.3	0.5	V			
PWM Switching Frequency	f_{PWM}	100	150	190	kHz			a
Primary Gate Drive Rise Time	t_{rPGD}	3	16	40	ns	C_{PGD} = 1 nF		
Primary Gate Drive Fall Time	t_{fPGD}	3	14	40	ns	C_{PGD} = 1 nF		
Maximum PWM Duty Cycle	D_{MAX}	50	55	60	%		8	
Regulated VCC2 Voltage	$V_{CC2} – V_{EE2}$	15.2	16.0	16.8	V			
VCC2 Over Voltage Protection Threshold	V_{OV_TH}	18.0	20.5	22.0	V			
VCC2 Over Voltage Protection Threshold Hysteresis	$V_{OV\_TH\_HYS}$	0.4	0.8	1.2	V			
IC Supply Current								
Input Supply Current	I_{CC1}		4.7	6.2	mA	V_{COMP} = 0 V	9	
Output Supply Current	I_{CC2}	6.5	10.30	14.20	mA	I_F = 0 mA	10	
Logic Input and Output								
LED Forward Voltage	V_F	1.25	1.55	1.85	V	I_F = 10 mA	11	
LED Reverse Breakdown Voltage	V_{BR}	6.0	11		V	I_F = 10 µA		

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}		90		pF			b
LED Turn on Current Threshold Low-to-High	I_{TH+}	0.5	2.7	7.5	mA	V_O= 5 V	12	
LED Turn on Current Threshold High-to-Low	I_{TH-}	0.3	2.3	7.0	mA	V_O = 5 V	12	
LED Turn on Current Hysteresis	I_{TH_HYS}		0.4		mA			
/FAULT Logic Low Output Current	I_{FAULT_L}	4	10	20	mA	V_{FAULT} = 0.4 V		
/FAULT Logic High Output Current	I_{FAULT_H}		0.01	2	uA	V_{FAULT} = 5V		
/UVLO Logic Low Output Current	I_{UVLO_L}	4	10	20	mA	V_{UVLO} = 0.4 V		
/UVLO Logic High Output Current	I^{UVLO_H}		0.01	2	uA	V_{UVLO} = 5 V		
Gate Driver								
High Level Output Current	I_{OH}		-1.7	-0.5	A	$V_O = V_{CC2}$ – 3 V	13	
Low Level Output Current	I_{OL}	0.5	2.4		A	$V_O = V_{EE2}$ + 2.5 V	14	
High Level Peak Output Current	I_{OH_PEAK}			-2	A	$V_O = V_{CC2}$ – 14 V		c
Low Level Peak Output Current	I_{OL_PEAK}	2			A	$V_O = V_{EE2}$ + 14V		c
High Level Output Voltage	V_{OH}	V_{CC2}–0.5	V_{CC2}–0.2		V	I_O = –100 mA		d, e
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA		
IF to High Level Output Propagation Delay Time	t_{PLH}	50	115	250	ns	Rg = 10 Ω Cg = 10 nF f = 10 kHz Duty Cycle = 50%	15, 20	f
IF to Low Level Output Propagation Delay Time	t_{PHL}	50	150	300	ns		15, 20	g
Pulse Width Distortion	PWD	-175	35	230	ns			h, i
Dead Time Distortion	DTD	-230	-35	175	ns			i, j
VO 10% to 90% Rise Time	t_R	10	76	280	ns			
VO 90% to 10% Fall Time	t_F	10	41	280	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	30	>50		kV/s	T_A=25 °C, I_F =10 mA, V_{CM} = 1500V	22	k
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	30	>50		kV/s	T_A = 25 °C, I_F = 0 mA, V_{CM} = 1500V	23	l
Active Miller Clamp and Soft Shutdown								
Low Level SSD Current During Fault Condition	I_{SSDLF}	90	150	210	mA	V_{SSD} = 14V	16	
Clamp Threshold Voltage	V_{TH_CLAMP}	1	2.1	3	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.5	2		A	V_{CLAMP} = V_{EE2}+2.5V		
V_{CC2} UVLO Protection								
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	12	13.4	14.5	V	V_O > 5 V		e, m
V_{CC2} UVLO Threshold High to Low	V_{UVLO-}	10	11.3	12.5	V	V_O < 5 V		e, n

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}	1.6	2.1	2.4	V			
V_{CC2} to UVLO High Delay	t_{PLH_UVLO}		9	20	µs		29	o
V_{CC2} to UVLO Low Delay	t_{PHL_UVLO}		7	20	µs		29	p
V_{CC2} UVLO to VOUT High Delay	t_{UVLO_ON}		5	6.5	µs		29	q
V_{CC2} UVLO to VOUT Low Delay	t_{UVLO_OFF}		1.1	2	µs		29	r
Desaturation Protection								
Desat Sensing Threshold	V_{DESAT}	6.65	7.0	7.35	V		17	
Desat Charging Current	I_{CHG}	0.8	1.0	1.2	mA	V_{DESAT} = 0 V, V_{DESAT} =6 V	18	
Desat Discharging Current	I_{DSCHG}	19	60	106	mA	V_{DESAT} = 7.5 V	19	
Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.3	0.6	0.9	µs	RSSD = 0 Ω Cg= 10nF	29	s
Desat Sense to 90% VGATE Delay	$t_{DESAT(90\%)}$	0.05	0.2	0.5	µs		21, 29	t
Desat Sense to 10% VGATE Delay	$t_{DESAT(10\%)}$	0.5	1.2	2	µs		21, 29	u
Desat to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$		4.4	8	µs			v
Output Mute Time due to Desaturation	$t_{DESAT(MUTE)}$	3	7.5	12	ms		29	w
Time Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	3	7.5	12	ms		29	x

a. PWM switching frequency of primary gate drive (PGD) is dithered in a range of ±6% typically over 3.3 ms.

b. C_{IN} is measured between pin 7 and pin 8 of the IC.

c. Maximum pulse width=1 µs, maximum duty cycle=1%.

d. Maximum pulse width = 1.0 ms, maximum duty cycle = 1%.

e. Once V_{OH} of ACPL-33JT is allowed to go high ($V_{CC2} - V_{EE2} > V_{UVLO}$), the DESAT detection features of the ACPL-33JT will be the primary source of IGBT protection. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-33JT work in conjunction to ensure constant IGBT protection.

f. t_{PLH} is defined as propagation delay from 50% of LED input IF to 50% of High level output.

g. t_{PHL} is defined as propagation delay from 50% of LED input IF to 50% of Low level output.

h. Pulse Width Distortion (PWD) is defined as ($t_{PHL} - t_{PLH}$) of any given unit.

i. As measured from I_F to V_O.

j. Dead Time Distortion (DTD) is defined as ($t_{PLH} - t_{PHL}$) between any two ACPL-33JT under the same test conditions.

k. Common mode transient immunity in the output high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the high state (i.e., $V_O > 14V$). CM_H specification is guaranteed by design and not subjected to production test.

l. Common mode transient immunity in the output low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the low state (i.e., $V_O < 2.0V$). CM_L specification is guaranteed by design and not subjected to production test.

m. This is the “increasing” (i.e. turn-on or “positive going” direction) of $V_{CC2} - V_{EE2}$.

n. This is the “decreasing” (i.e. turn-off or “negative going” direction) of $V_{CC2} - V_{EE2}$.

o. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of /UVLO positive going edge.

p. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of /UVLO negative going edge.

q. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of High level output.

r. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of Low level output.

s. The delay time for ACPL-33JT to respond to a DESAT fault condition without any external DESAT capacitor.

t. The amount of time from when DESAT threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.

u. The amount of time from when DESAT threshold is exceeded to 10% of V_{GATE} at mentioned test conditions.

v. The amount of time from when DESAT threshold is exceeded to /Fault output Low – 50% of V_{CC1} voltage.

w. The amount of time when DESAT threshold is exceeded, Output is mute to LED input.

x. The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.

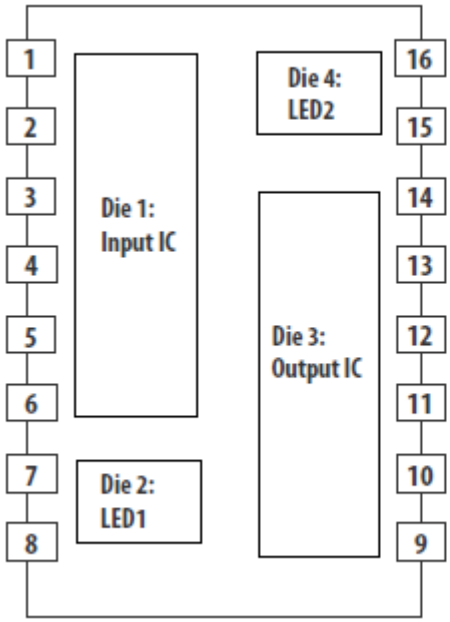
Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min. T_A = 25 °C
Resistance (Input-Output)	R_{I-O}	10^9	10^{14}		Ω	V_{I-O} = 500 Vdc
Capacitance (Input-Output)	C_{I-O}		0.8		pF	f = 1 MHz

Thermal Resistance Model for ACPL-33JT

The diagram for measurement is shown in Figure 3. This is a multi chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded and so on until the 4th die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of four heat sources.

Figure 3 Diagram of ACPL-33JT for Measurement



$$\begin{vmatrix} R11 & R12 & R13 & R14 \\ R21 & R22 & R23 & R24 \\ R31 & R32 & R33 & R34 \\ R41 & R42 & R43 & R44 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \\ P3 \\ P4 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \\ \Delta T3 \\ \Delta T4 \end{vmatrix}$$

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (C/W)
R_{12}: Thermal Resistance of Die1 due to heating of Die2 (C/W))
R_{13}: Thermal Resistance of Die1 due to heating of Die3 (C/W))
R_{14}: Thermal Resistance of Die1 due to heating of Die4 (C/W))
R_{21}: Thermal Resistance of Die2 due to heating of Die1 (C/W)
R_{22}: Thermal Resistance of Die2 due to heating of Die2 (C/W)
R_{23}: Thermal Resistance of Die2 due to heating of Die3 (C/W)
R_{24}: Thermal Resistance of Die2 due to heating of Die4 (C/W)
R_{31}: Thermal Resistance of Die3 due to heating of Die1 (C/W)
R_{32}: Thermal Resistance of Die3 due to heating of Die2 (C/W)
R_{33}: Thermal Resistance of Die3 due to heating of Die3 (C/W)
R_{34}: Thermal Resistance of Die3 due to heating of Die4 (C/W)
R_{41}: Thermal Resistance of Die4 due to heating of Die1 (C/W)
R_{42}: Thermal Resistance of Die4 due to heating of Die2 (C/W)
R_{43}: Thermal Resistance of Die4 due to heating of Die3 (C/W)
R_{44}: Thermal Resistance of Die4 due to heating of Die4 (C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

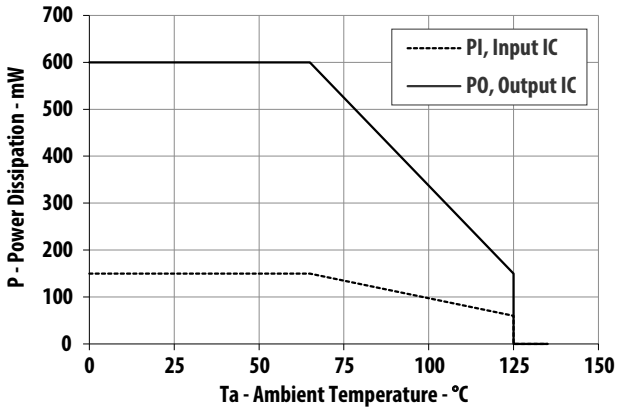
T_1: Junction temperature of Die1 due to heat from all dice (0 °C)
T_2: Junction temperature of Die2 due to heat from all dice (0 °C)
T_3: Junction temperature of Die3 due to heat from all dice (0 °C)
T_4: Junction temperature of Die4 due to heat from all dice (0 °C)

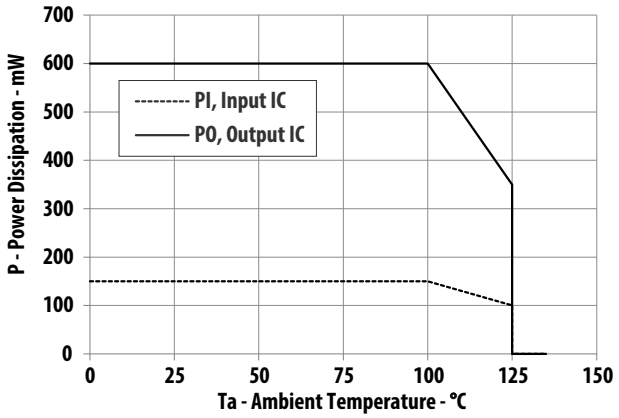
Ta: Ambient temperature (°C)

ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature deference between Die2 junction and ambient (°C)
ΔT_3: Temperature difference between Die3 junction and ambient (°C)
ΔT_4: Temperature deference between Die4 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + Ta \quad \text{---------- (1)}$$
$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + Ta \quad \text{---------- (2)}$$
$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + Ta \quad \text{---------- (3)}$$
$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + Ta \quad \text{---------- (4)}$$

Measurement is done on low effective thermal conductivity board according to JEDEC Standard 51-3 and on high effective thermal conductivity board according to JEDEC Standard 51-7.

<table>
<tr><th>Test Board</th><th>Test Board Conditions</th><th>Thermal Resistance</th><th>Power Dissipation Derating Chart</th></tr>
<tr>
<td>Low effective thermal conductivity board
 
76 mm × 76 mm</td>
<td>Single layer board for signal
Outer layer: 2 oz. copper thickness</td>
<td>R11 = 138 °C/W
R12 = 87 °C/W
R13 = 67 °C/W
R14 = 87 °C/W
R21 = 89 °C/W
R22 = 241 °C/W
R23 = 81 °C/W
R24 = 95 °C/W
R31 = 73 °C/W
R32 = 92 °C/W
R33 = 117 °C/W
R34 = 118 °C/W
R41 = 86 °C/W
R42 = 96 °C/W
R43 = 111 °C/W
R44 = 225 °C/W</td>
<td>Figure 4 PowerDerating Chart Using Low Effective Thermal Conductivity Board
 

NOTE
■ Input IC power dissipation is derated linearly above 65 °C from 150 mW to 60 mW at 125 °C.
■ Output IC power dissipation is derated linearly above 65°C from 600mW to 150mW at 125°C.</td>
</tr>
<tr>
<td>High effective thermal conductivity board
 
76 mm × 76 mm</td>
<td>4-layer board that embodies two signal layers, a power plane and a ground plane
Outer layers: 2 oz. copper thickness
Inner layers: 1 oz. copper thickness</td>
<td>R11 = 78 °C/W
R12 = 34 °C/W
R13 = 23 °C/W
R14 = 29 °C/W
R21 = 37 °C/W
R22 = 165 °C/W
R23 = 32 °C/W
R24 = 31 °C/W
R31 = 24 °C/W
R32 = 33 °C/W
R33 = 59 °C/W
R34 = 48 °C/W
R41 = 32 °C/W
R42 = 34 °C/W
R43 = 51 °C/WR
44 = 136 °C/W</td>
<td>Figure 5 Power Derating Chart Using High Effective Thermal Conductivity Board
 

NOTE
■ Input IC power dissipation is derated linearly above 100°C from 150mW to 100mW at 125°C.
■ Output IC power dissipation is derated linearly above 100°C from 600mW to 350mW at 125°C.</td>
</tr>
</table>

Notes on Thermal Calculation

Application and environmental design for ACPL-33JT needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150 °C. The following equations calculate the maximum power dissipation and corresponding effect on junction temperatures and can only be used as a reference for thermal performance comparison under specified PCB layout as shown above. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment.

Calculation of Input IC Power Dissipation, P_1

Input IC Power Dissipation (P_1) = $P_{I(Static)} + P_{I(PGD)}$

where

$P_{I(Static)}$ – Static power dissipated by the input IC = $I_{CC1} \times V_{CC1}$
$P_{I(PGD)}$ – Switching power dissipated in the PGD pin = $(V_{CC1} \times Q_{G\_ExtMOS} \times f_{PWM\_DCDC}) \times R_{O(MAX)} / (R_{O(MAX)} + R_{G\_PGD})$
Q_{G_ExtMOS} – Gate charge of external MOSFET connected to PGD pin at supply voltage
f_{PWM_DCDC} – DC-DC switching frequency
$R_{O(MAX)}$ – Maximum PGD pin output impedance = 0.3 V / 50 mA = 6
R_{G_PGD} – Gate resistance connected to PGD pin

Example:

$P_{I(Static)}$ = 6 mA × 5. 5V = 33 mW
$PI_{(PGD)}$ = (5.5 V × 5 nC ×190 kHz) × 6 Ω/(6 Ω + 10 Ω) = 1.96 mW
P_1 = 33 mW + 1.96 mW = 34.96 mW

Calculation of Input LED Power Dissipation, P_2

Input LED Power Dissipation (P_2) = IF(LED) (Recommended Max.) × $V_{F(LED)}$ (at 125 °C) × Duty Cycle

Example:

P_2 = 16 mA × 1.25 V × 50% duty cycle = 10 mW

Calculation of Output IC Power Dissipation, P_3

Output IC Power Dissipation (P_3) = $P_{O(Static)} + P_{HS} + P_{LS}$

where

$P_{O(Static)}$ – Static power dissipated by the output IC = $I_{CC2} \times V_{CC2}$
P_{HS} – High side switching power dissipation at V_O pin = $(V_{CC2} \times Q_G \times f_{PWM}) \times R_{OH(MAX)} / (R_{OH(MAX)} + R_{GH}) / 2$
P_{LS} – Low side switching power dissipation at V_O pin = $(V_{CC2} \times Q_G \times f_{PWM}) \times R_{OL(MAX)} / (R_{OL(MAX)} + R_{GL}) / 2$
Q_G – IGBT gate charge at supply voltage
f_{PWM} – Input LED switching frequency
$R_{OH(MAX)}$ – Maximum high side output impedance – $(V_{CC2} - V_{OH(MIN)}) / I_{OH(MIN)}$
R_{GH} – Gate charging resistance
$R_{OL(MAX)}$ – Maximum low side output impedance – $V_{OL(MAX)} / I_{OL(MIN)}$
R_{GL} – Gate discharging resistance

Example:

$R_{OH(MAX)} = (V_{CC2} - V_{OH(MIN))} / I_{OH(MIN)} = 3.0\ V / 0.5\ A = 6.0\ \Omega$
$R_{OL(MAX)} = V_{OL(MAX)} / I_{OH(MIN)} = 2.5\ V / 0.5\ A = 5.0\ \Omega$
$P_{HS} = (16\ V \times 1\mu C * 10\ kHz) \times 6.0\ \Omega / (6.0\ \Omega + 10\ \Omega\ ) / 2 = 30\ mW$
$P_{LS} = (16\ V \times 1\ \mu C \times 10\ kHz) \times 5.0\ \Omega / (5.0\ \Omega + 10\ \Omega) / 2 = 26.7\ mW$
$P_3 = 14.2\ mA \times 16\ V + 30\ mW + 26.7\ mW = 283.9\ mW$

Calculation of LED2 Power Dissipation, P_4

LED2 Power Dissipation (P_4) = $I_{F(LED2)}$ (Design Max.) × $V_{F(LED2)}$ (at 12 5°C) × Duty Cycle

Example:

$P_4 = 16\ mA \times 1.25\ V \times 50\%$ duty cycle = 10 mW

Calculation of Junction Temperature for High Effective Thermal Conductivity Board:

Input IC Junction Temperature = (78 °C/W × P_1 + 34 °C/W × P_2 + 23 °C/W × P_3 + 29 °C/W × P_4) + Ta
Input LED Junction Temperature = (37 °C/W × P_1 + 165 °C/W × P_2 + 32 °C/W × P_3 + 31 °C/W × P_4) + Ta
Output IC Junction Temperature = (24 ° C/W × P_1 + 33 °C/W × P_2 + 59 °C/W × P_3 + 48 °C/W × P_4) + Ta
LED2 Junction Temperature = (32 °C/W × P_1 + 34 °C/W × P_2 + 51 °C/W × P_3 + 136 °C/W × P_4) + Ta

Printed Circuit Board Layout Considerations

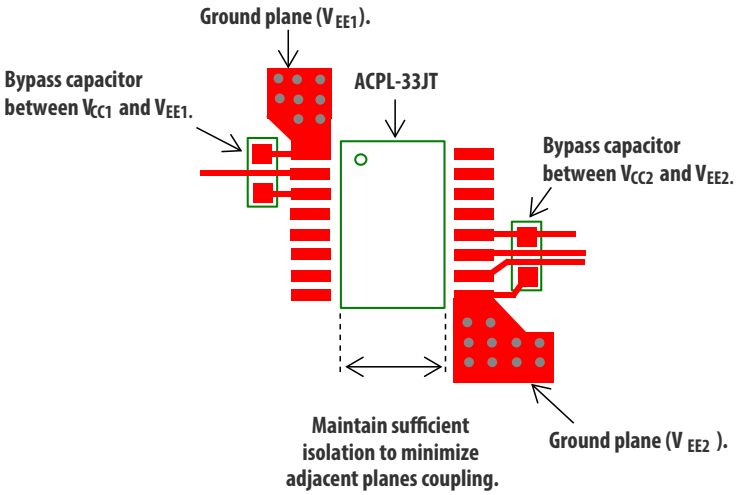
Care must be taken while designing the layout of printed circuit board (PCB) for optimum performance.

Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. The same minimum spacing between two adjacent high-side isolated regions of the printed circuit board must be maintained as well. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade CMR performance.

The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of the gate charge is supplied by the bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms.

Bypass capacitors should be placed closely in between these pins: V_{CC1} (pin 3) to V_{EE1} (pin 1) and V_{CC2} (pin 12) to V_{EE2} (pin 9). Ground plane connections are necessary for V_{EE1} and V_{EE2} in order to achieve maximum power as the ACPL-33JT is designed to dissipate the majority of heat generated through these pins. Actual power dissipation will depend on the application environment (PCB layout, airflow, part placement, etc.).

Figure 6 PCB Layout Considerations



Typical Performance Plots

Figure 7 PWM Duty Cycle vs. V_{COMP}

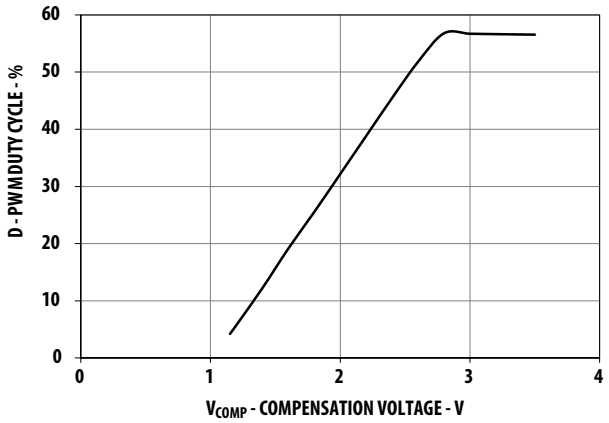


Figure 8 I_{COMP} vs. Supply Voltage

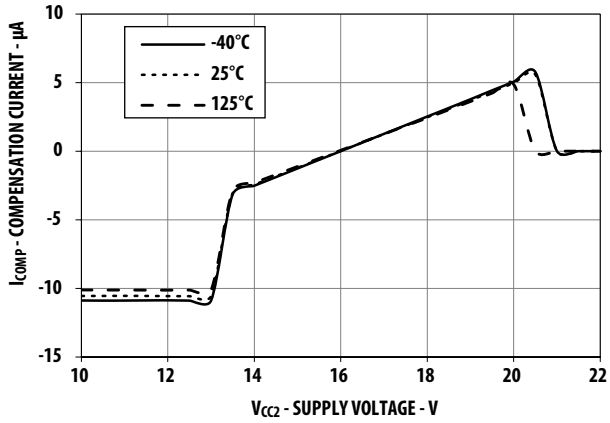


Figure 9 I_{CC1} vs. Temperature

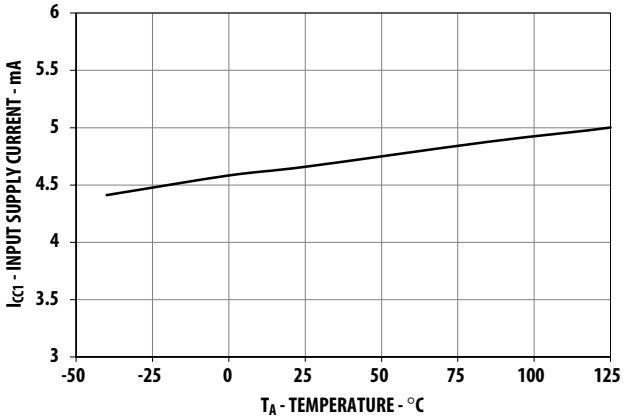


Figure 10 I_{CC2} vs. Temperature

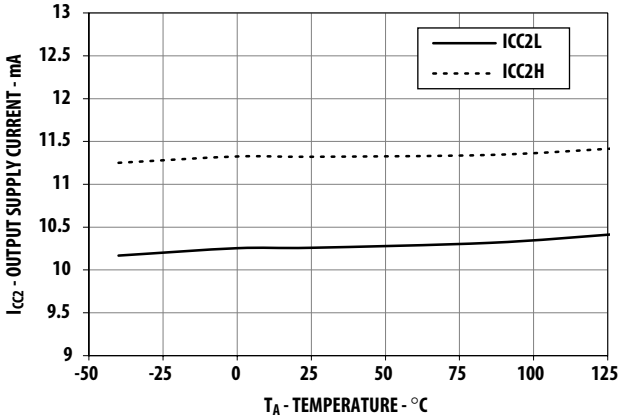


Figure 11 I_F vs. V_F

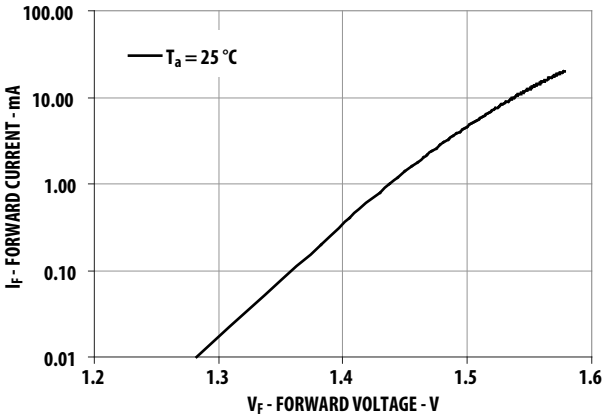


Figure 12 I_{TH} vs. Temperature

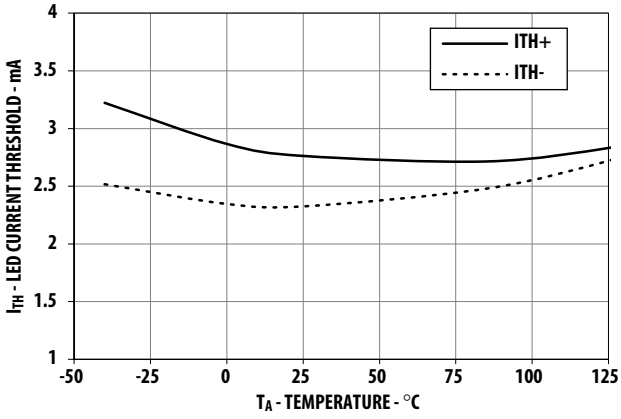


Figure 13 V_{OH} vs. I_{OH}

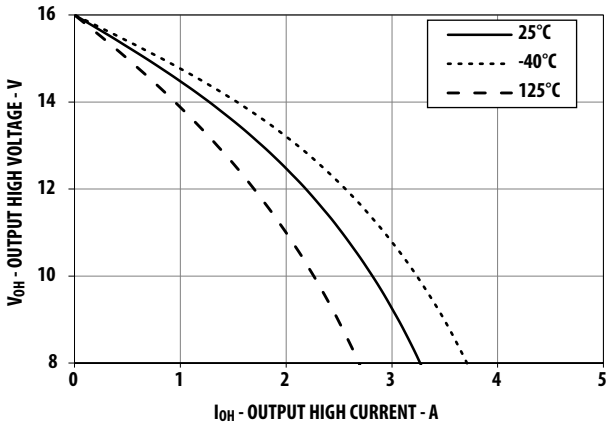


Figure 14 V_{OL} vs. I_{OL}

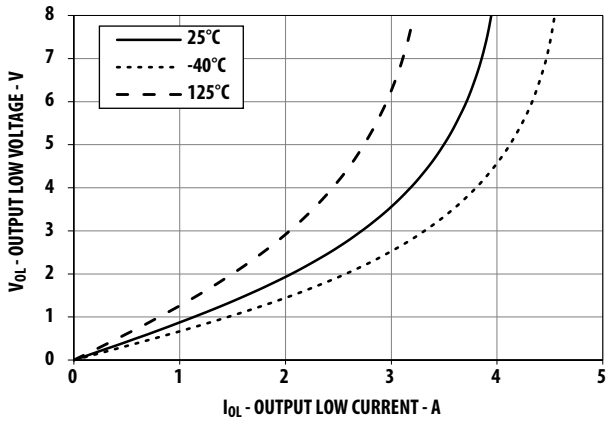


Figure 15 T_P vs. Temperature

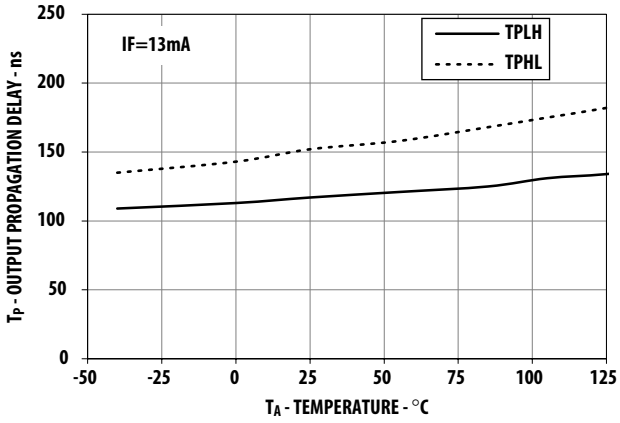


Figure 16 I_{SSD} vs. V_{SSD}

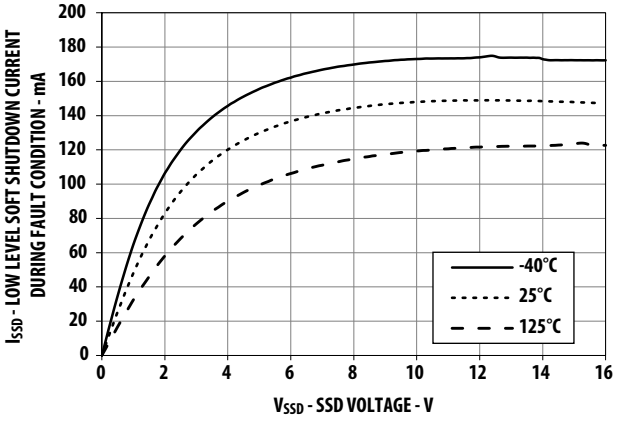


Figure 17 V_{DESAT} Threshold vs. Temperature

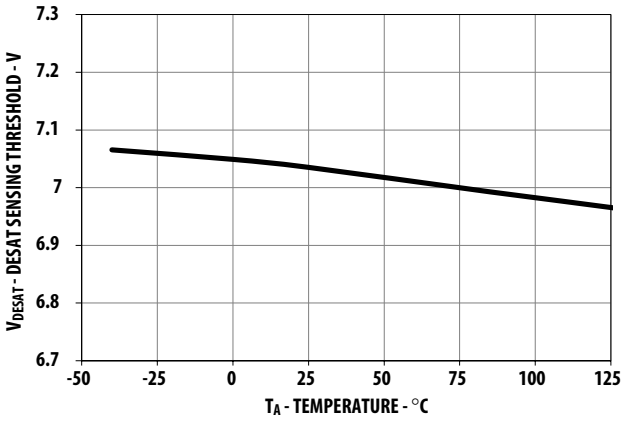


Figure 18 I_{CHG} vs. Temperature

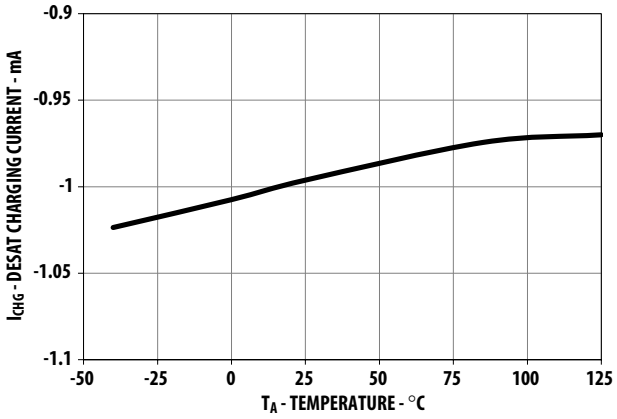


Figure 19 I_{DSCHG} vs. Temperature

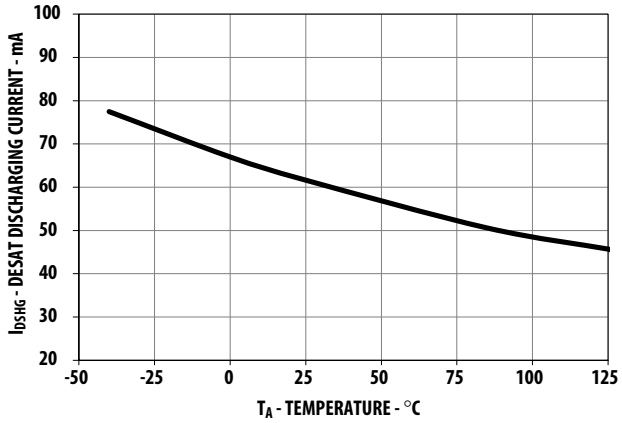


Figure 20 Propagation Delay Test Circuit

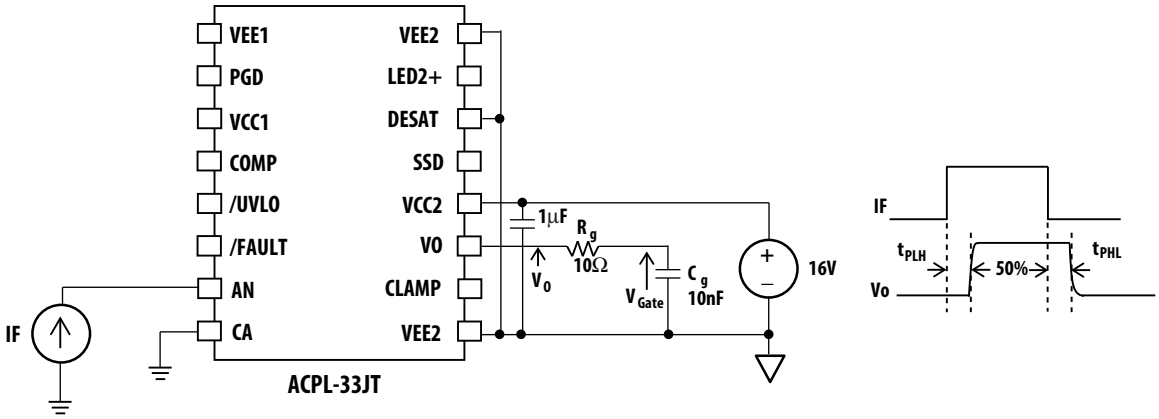


Figure 21 t_{DESAT}(90%) and t_{DESAT}(10%) Test Circuit

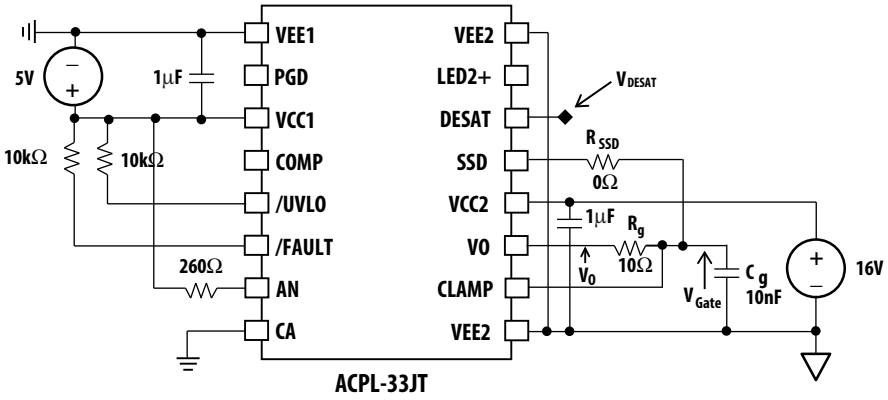


Figure 22 CMR V_O High Test Circuit

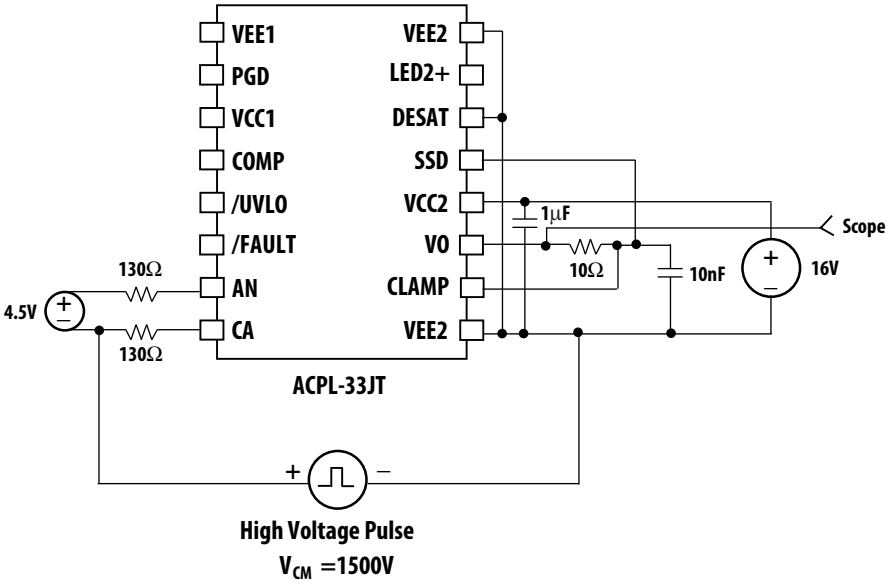
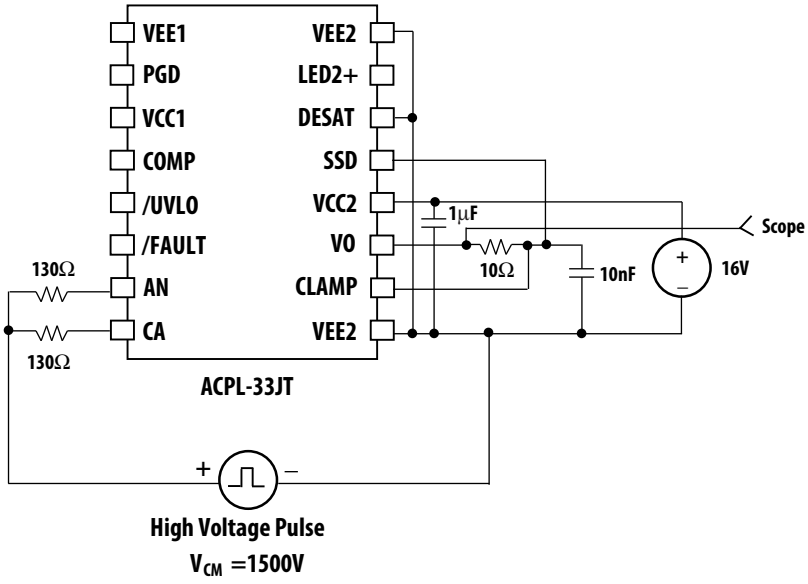
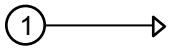
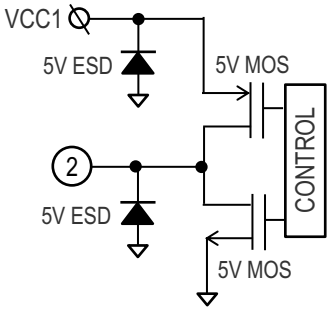
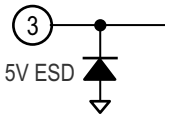
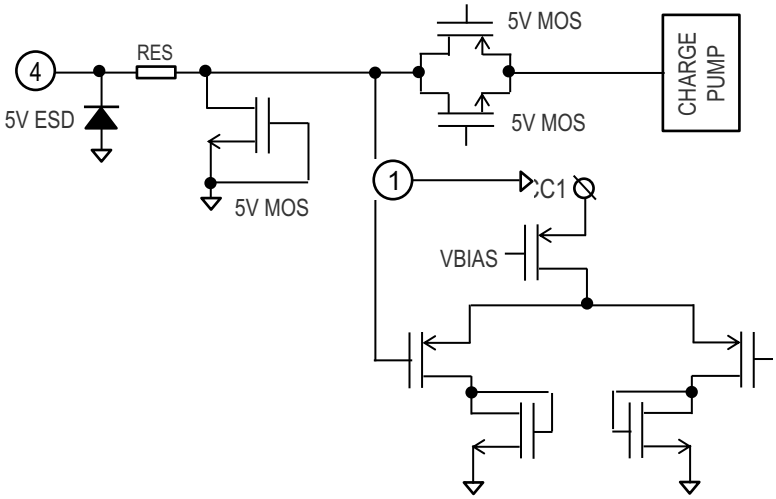
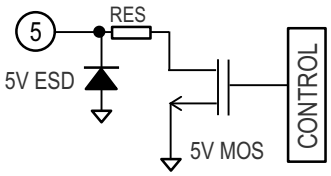
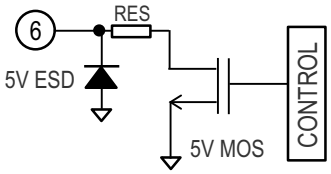
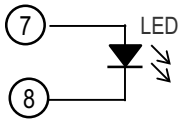
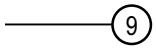
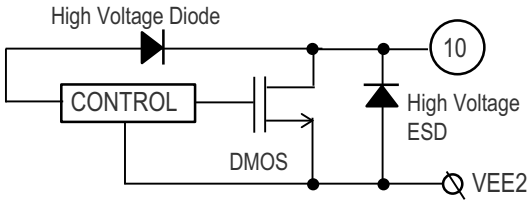
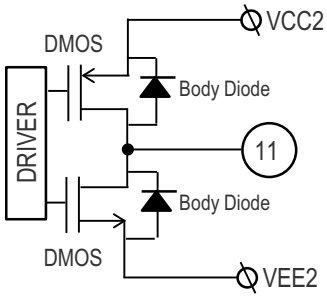
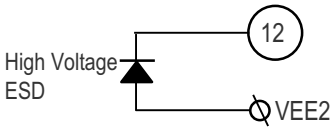
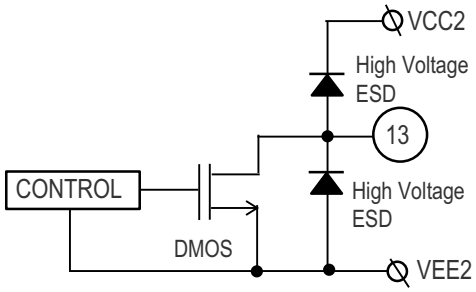
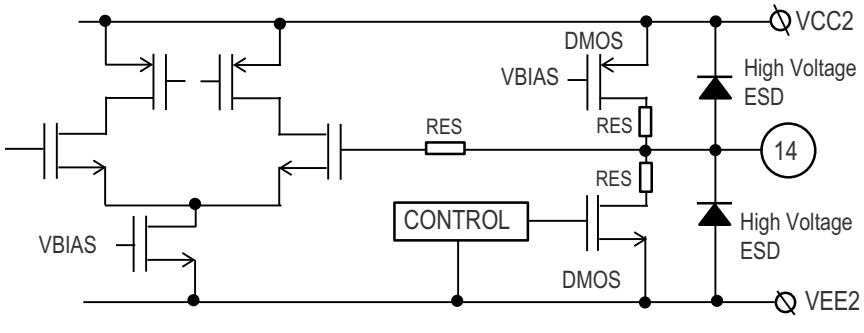


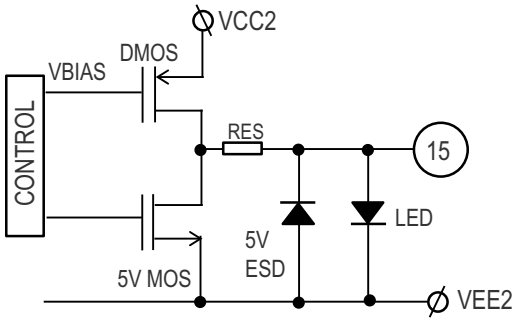
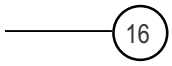
Figure 23 CMR V_O Low Test Circuit



Internal Connection Equivalent Circuits

Pin No.	Pin Nmae	Equivalent Circuits	Note
1	V_{EE1}		Input Common/GND
2	PGD		
3	V_{CC1}		
4	COMP		5
5	/UVLO		
6	/FAULT		
7, 8	Input LED 7 – Anode 8 – Cathode		

Pin No.	Pin Nmae	Equivalent Circuits	Note
9	V_{EE2}		Output Common
10	CLAMP		
11	V_O		
12	V_{CC2}		
13	SSD		
14	DESAT		

Pin No.	Pin Nmae	Equivalent Circuits	Note
15	LED2+		
16	V_{EE2}		Output Common

Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three-phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase or rail supply short circuits due to user misconnect or bad wiring; control signal failures due to noise or computational errors; overload conditions induced by the load; and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector-to-emitter voltage rises from saturation region to desaturation (active) region. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn off the over current during a fault condition.

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features that this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

The ACPL-33JT satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and optically isolated fault and UVLO status feedback signal into a single 16-pin surface mount package.

The fault detection method, which the ACPL-33JT has adopted, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off-state of the IGBT, the fault detect circuitry is simply disabled to prevent false ‘fault’ signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-33JT limits the power dissipation in the IGBT, even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

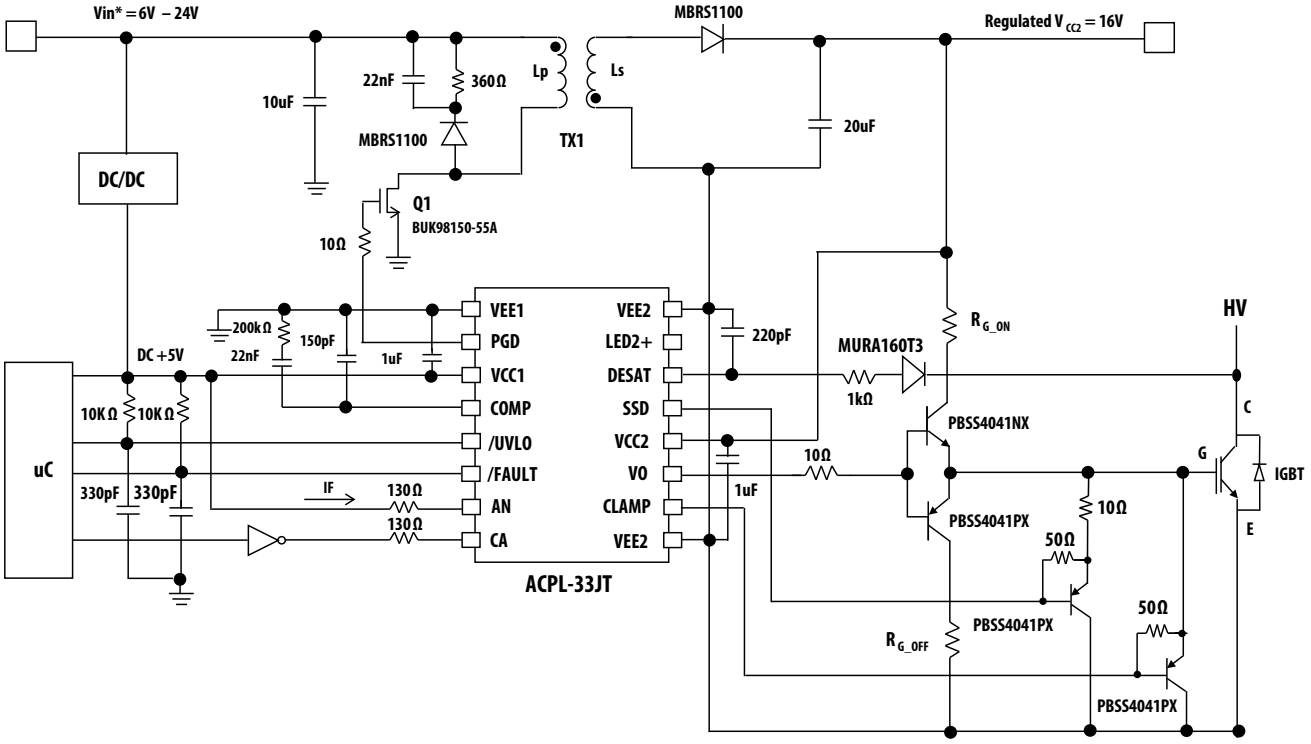
Typical Application Circuit

The ACPL-33JT has non-inverting gate control inputs, an open collector fault, and UVLO outputs suitable for wired 'OR' applications.

The application circuit shown in Figure 24 illustrates a typical gate drive implementation using the ACPL-33JT.

The two supply bypass capacitors (1 µF) provide filtering and the large transient currents necessary during a switching transition. The Desat diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open collector fault and UVLO outputs have a passive 10 kΩ pull-up resistor and a 330 pF filtering capacitor.

Figure 24 Typical Application Circuit with External Components



NOTE Component value subject to change with varying application requirements. *Vin range is dependent on transformer design.

Operation of Integrated Flyback Controller

The primary control block implements direct duty cycle control logics for line and load regulation. The primary gate drive (PGD) pin is connected to external MOSFET to switch the primary winding current. Secondary output voltage V_{CC2} is sensed and fed back to the primary control circuits. V_{CC2} over voltage can be detected and the primary gate is turned off to protect secondary overvoltage failure. The maximum PWM duty cycle is designed to be around 55% to ensure discontinuous operation mode under a high load condition. For a complete isolated DC-DC converter, connect a discrete transformer to ACPL-33JT, as in Figure 24. Keep the LED off when you are powering up V_{CC1}. To ensure proper operation of the DC-DC converter, a fast V_{CC1} rise time (≤ 5 ms) is preferred for a soft start function to control the inrush current.

The average PWM switching frequency of the primary gate drive (PGD) is dithered typically in a range of ±6%, typically over 3.3 ms. This frequency dithering feature helps to achieve better EMI performance by spreading the switching and its harmonics over a wider band.

Reference DC-DC Circuit

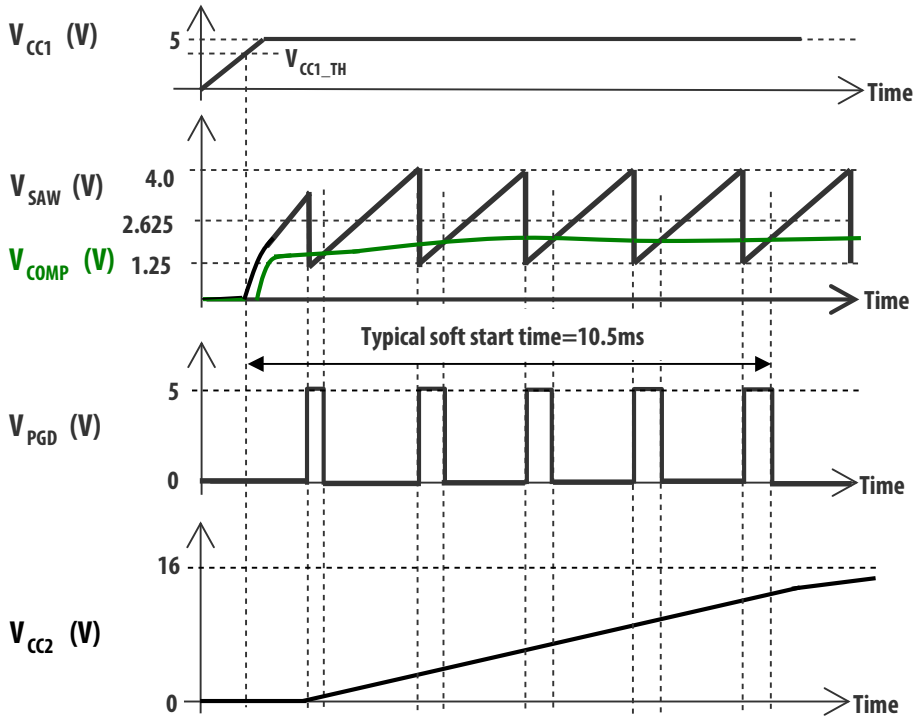
Figure 24 shows a reference circuit for DC-DC flyback conversion including the compensation network at pin 4, COMP. This compensation network is referenced to a nominal transformer of Lp = 7 µH, Ls=86 µH. For Vin = 6 V to 24 V, this circuit will nominally support a secondary-side load of up to 90 mA (including I_{CC2}) at the regulated V_{CC2} voltage.

Users must further characterize the DC-DC flyback conversion across their target operating conditions and chosen components to ensure that the required load can be supported.

Soft Start Operation

ACPL-33JT is designed with built-in soft start feature. Once V_{CC1} is higher than V_{CC1_TH}, the built-in soft start circuit starts to function. Typical soft start timing is 10.5 ms, where a typical 3 µA soft start current (I_{COMP}) charges up the compensation network through the V_{COMP} pin and gradually increases the V_{COMP} voltage to the correct working level. IC exits soft start after 10.5 ms and goes into the transition period, where I_{COMP} is increased to typical 6uA for 3.3ms. Following that, IC goes into normal regulation where ICOMP is increased to typical 10 µA. The soft start feature helps to reduce the inrush current. See Figure 25 for V_{CC1} and V_{CC2} start up profiles.

Figure 25 Operation of Integrated DCDC Flyback Controller



NOTE V_{SAW} is IC internal signal and cannot be measured externally.

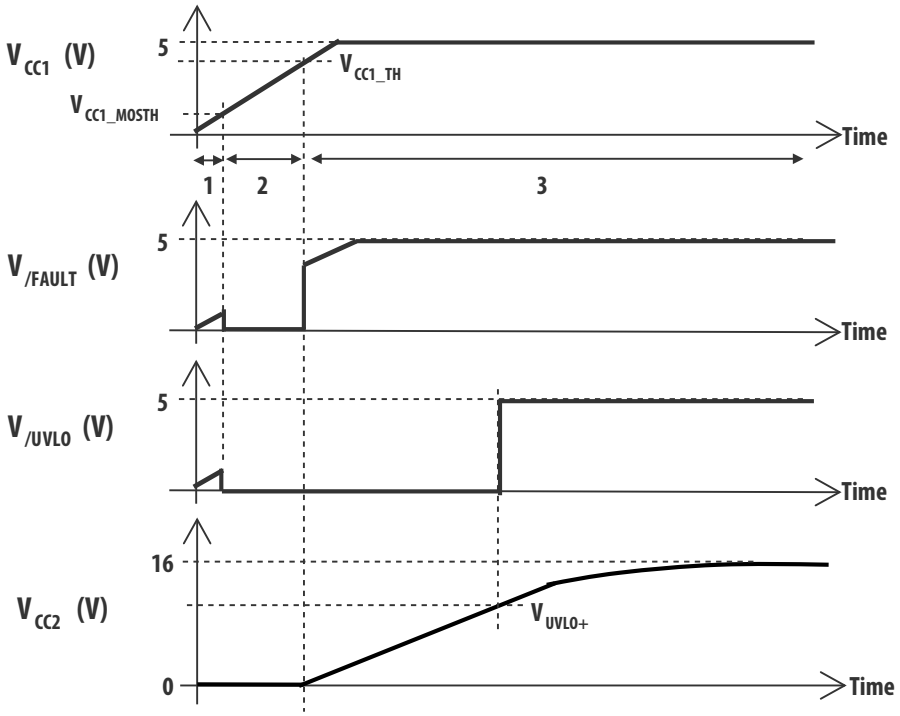
Power Up Behavior

Figure 26 describes the power up behavior of typical application circuit showed in Figure 24. The power up behavior of ACPL-33JT can be divided into three regions:

- Non operation region where V_{CC1} is less than V_{CC1_MOSTH} of 1.2 V typical.
- Initial operation region where V_{CC1} is more than typical 1.2 V and less than V_{CC1_TH} voltage. At this region, ACPL-33JT acknowledges V_{CC1} is below the V_{CC1_TH}, and pulls the UVLO and Fault pins Low.

- Active operation region where V_{CC1} exceeds V_{CC1_TH}. The primary gate drive (PGD) starts to work and regulates V_{CC2} to the typical 16V. The fault pin will be released from the initial pull down; the UVLO pin will continue to be pulled down until V_{CC2} reaches the UVLO+ threshold.

Figure 26 Power Up Behavior of Typical Circuit



Output Control and Status Flags

The outputs (V_O, SSD, /FAULT and /UVLO) of the ACPL-33JT are controlled by the combination of V_{CC1}, V_{CC2}, input LED current (IF) and IGBT desaturation condition. The following table shows the logic truth table for these outputs.

Table 1 ACPL-33JT Output Control

Conditions	Input				Output			
	V_{CC1}	V_{CC2}	I_F	Desat	V_O	SSD	/FAULT	/UVLO
VCC1 Under Voltage	Low	High	Low	Low	Low	High-Z	Low	Low
	Low	High	High	Low	High	High-Z	Low	Low
VCC2 UVLO	Low	Low	X	X	Low	High-Z	Low	Low
	High	Low	X	X	Low	High-Z	High	Low
Over Current (Desaturation)	Low	High	Low	High	Low	High-Z	Low	Low
	Low	High	High	High	High-Z	Low	Low	Low
	High	High	Low	High	Low	High-Z	High	High
	High	High	High	High	High-Z	Low	Low	High
Normal switching	High	High	Low	Low	Low	High-Z	High	High
	High	High	High	Low	High	High-Z	High	High

NOTE The logic level is defined by the respective threshold of each function pin. VCC1 logic threshold refers to VCC1_TH. /FAULT and /UVLO pins are pulled up with a 10 kΩ resistor.

DESAT Fault Detection Blanking Time

After the IGBT is turned on, the DESAT fault detection circuitry must remain disabled for a short time period to allow the collector voltage to fall below the DESAT threshold. This time period, called the total DESAT blanking time, is controlled by the both internal DESAT blanking time $t_{DESAT(BLANKING)}$) and external blanking time, determined by the internal charge current, the DESAT voltage threshold, and the external DESAT capacitor.

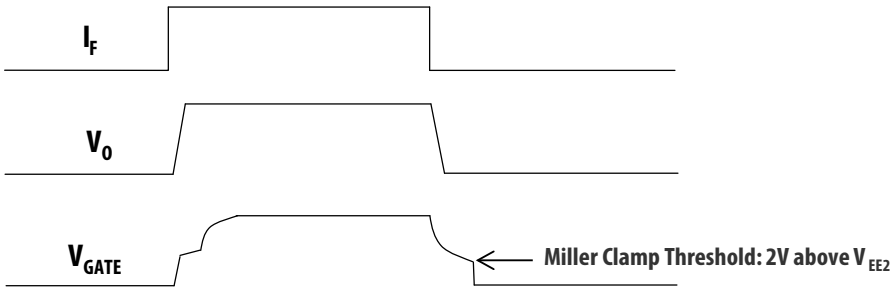
The total blanking time is calculated in terms of internal blanking time ($t_{DESAT(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as

Total DESAT blanking time, $t_{BLANK} = t_{DESAT(BLANKING)} + C_{BLANK} \times V_{DESAT} / I_{CHG}$

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-33JT is capable of delivering 2.5 A sourcing current to drive the IGBT's gate. While LED is switched off the gate driver can provide 2.5 A sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2 V with respect to V_{EE2} to provide low impedance path to miller current as shown in Figure 27.

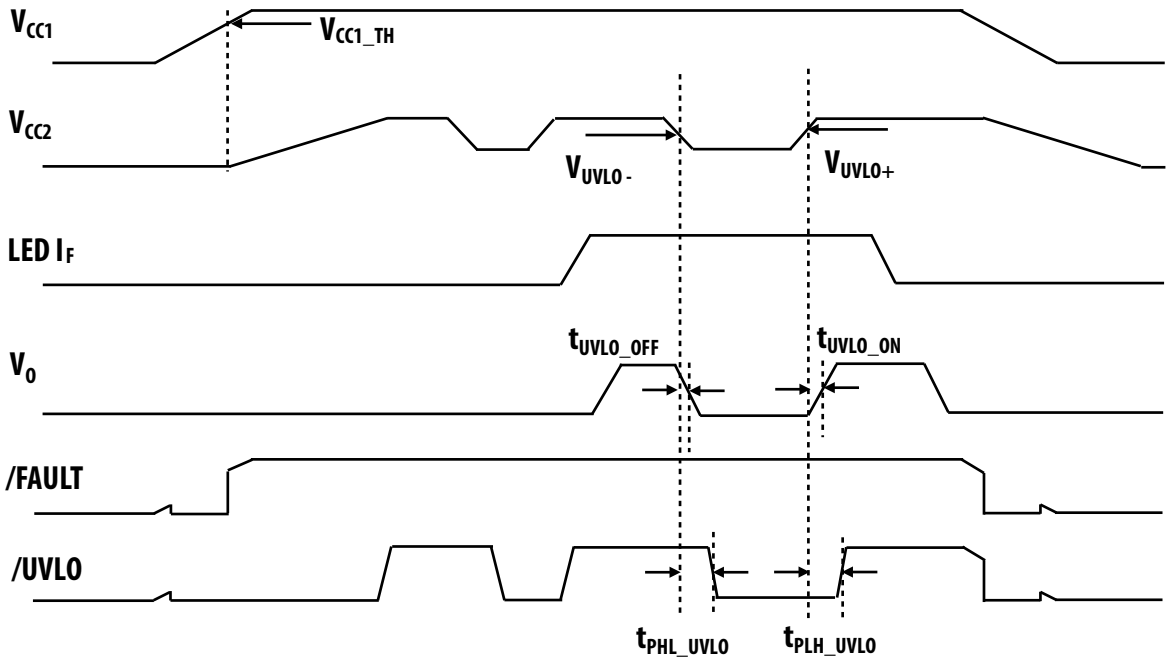
Figure 27 Gate Drive Signal Behavior



Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACPL-33JT monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT from low voltage bias. During power up, the UVLO feature forces the QCPL33JT's output low to prevent unwanted turn-on at lower voltage.

Figure 28 Circuit Behaviors at Power Up and Power Down



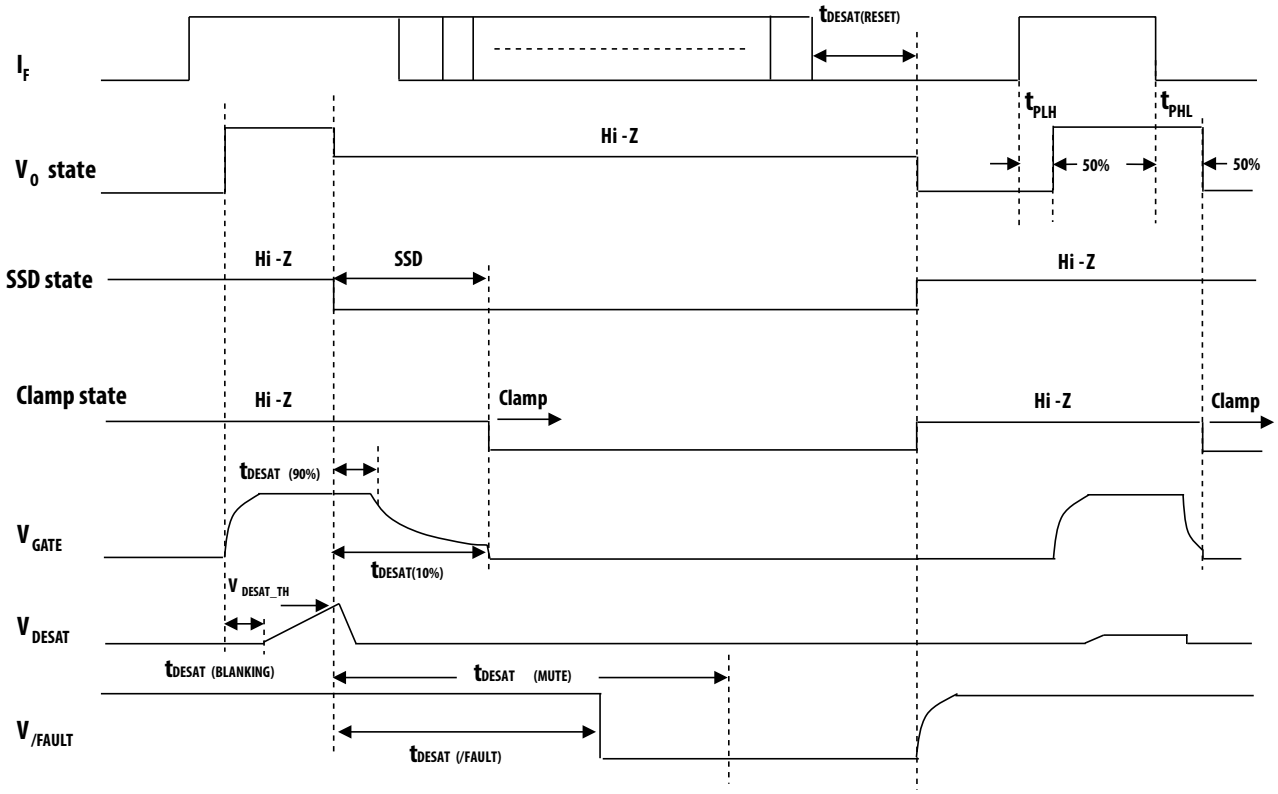
Description of Over-Voltage Protection

If VCC2 is greater than the V_{CC2} Over-Voltage Protection threshold, the primary gate drive (PGD) pin on the primary side shuts down and the DC-DC flyback conversion is stopped. Once V_{CC2} goes below the V_{CC2} Over-Voltage protection threshold, the primary gate drive (PGD) starts to regulate again. There is no feedback status for this protection feature.

During a Short Circuit

1. DESAT terminal monitors IGBT's VCE voltage.
2. When the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage (V_{GATE}) is slowly lowered by soft shutdown (SSD) pin. Output driver, V_O enters into high impedance state.
3. Output driver VO ignores all PWM commands during mute time ($t_{DESAT(MUTE)}$).
4. /FAULT output goes low, notifying the microcontroller of the fault condition.
5. Microcontroller takes appropriate action.
6. When $t_{DESAT(MUTE)}$ expires, the LED input need to be kept low for $t_{DESAT(RESET)}$ before fault condition can be cleared. /FAULT status will return to high and SSD output will return to high impedance state.
7. Output (V_O) starts to respond to LED input after fault condition is cleared.

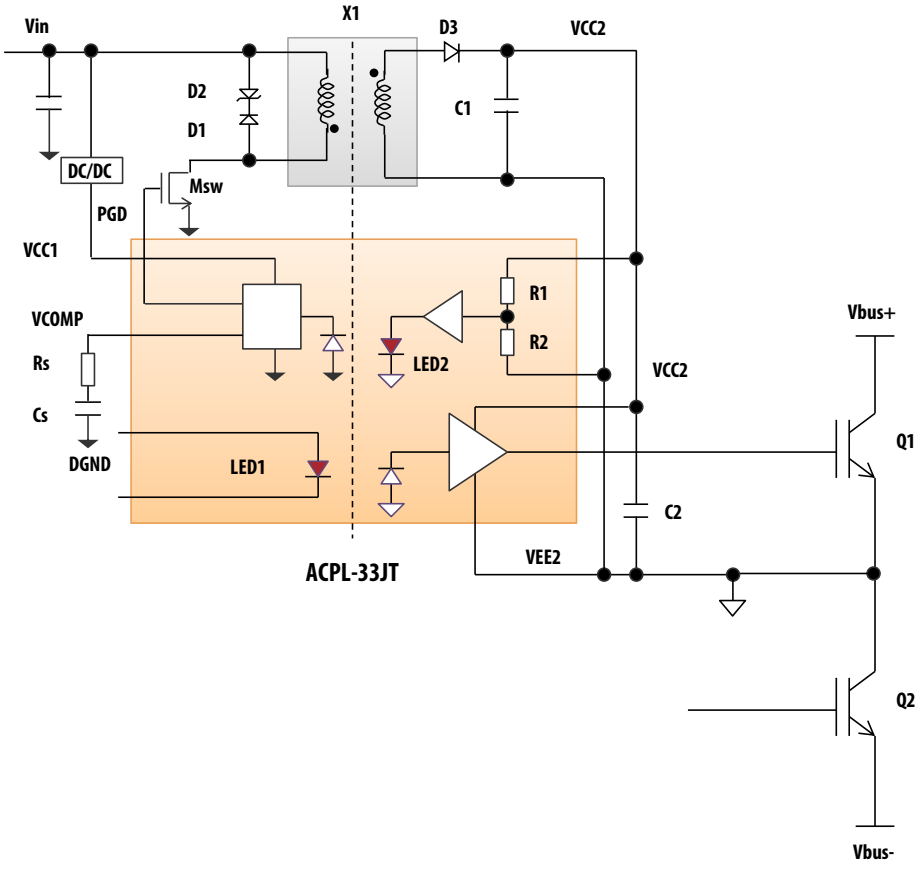
Figure 29 Circuit Behaviors During Desaturation Event



Additional Application Information on Isolated DC-DC Converter

The flyback converter uses direct duty cycle control in discontinuous mode. The output voltage is fed back through integrated optocoupler as shown in Figure 30.

Figure 30 IGBT Gate Driver with Integrated Flyback Controller



A few immediate benefits of this topology can be observed.

- Output voltage is regulated gate by gate with integrated feedback.
- Isolation boundary is well aligned with gate driver resulting concise PCB layout.
- Primary gate is used to switch the external MOS (MSW) and this provides flexibility in power design.
- Less discrete components are used and easy to design.

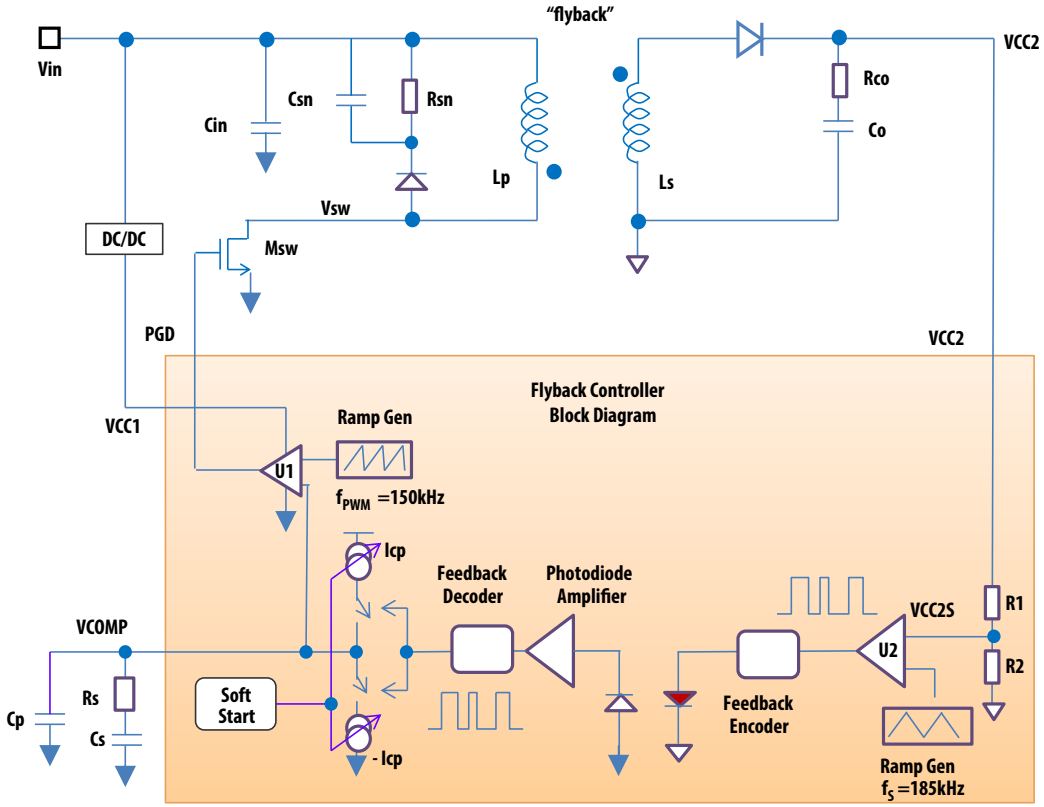
Feedback Control Loop

Isolated flyback converter is essentially a feedback control loop, whose loop dynamics must be carefully designed to ensure loop stability.

Figure 31 shows a detailed block diagram of Avago's isolated flyback converter architecture.

The feedback loop can be broken at duty cycle control voltage node V_{COMP} The forward path includes path from V_{COMP} to V_{CC2}. The feedback path includes path from V_{CC2} to V_{COMP}.

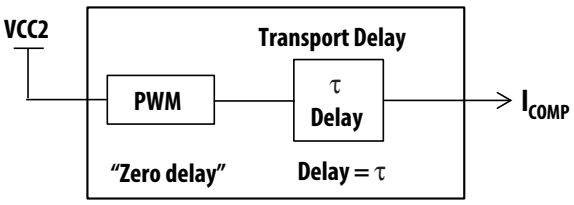
Figure 31 Block Diagram of Avago's Isolated Flyback Converter



Feedback Propagation Delay from V_{CC2} to V_{COMP}

If total propagation delay from V_{CC2} to the charge pump switches is τ, the feedback block diagram can be simplified as a zero delay PWM generator circuit whose output is the I_{COMP} current and a digital delay (transport delay) block.

Figure 32 Simplified Block of Total Feedback Delay from V_{CC2} to V_{COMP}



Equivalent small signal model of feedback GM is H_FBGM (s) = gm / ((s + 1) / τ))

Where gm is the transconductance gain from V_{CC2} to Charge Pump Output and τ is the propagation delay.

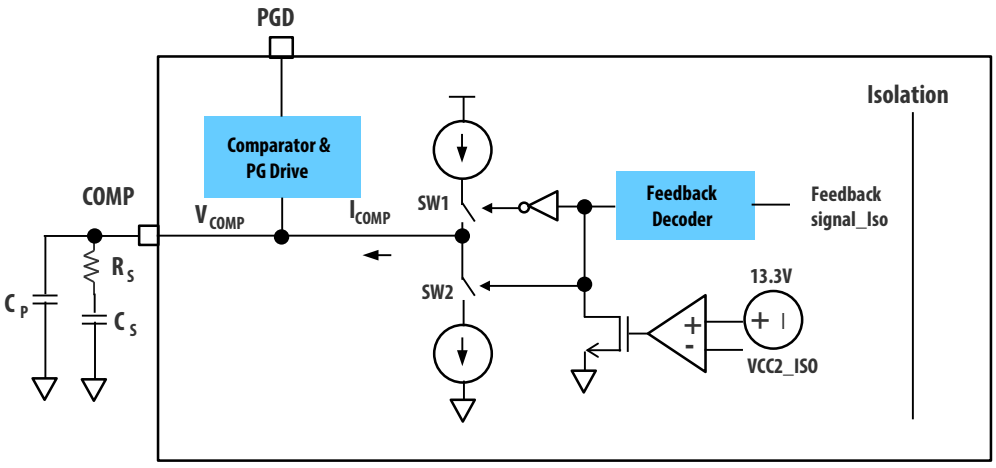
In S-domain, transport delay is transformed to the following Laplace transform, H(S) = e-st. If t is small compared to the loop bandwidth of interest, then e-st ≈ 1 / (s + 1 / τ). This is true and good approximation if the PWM frequency is also >> Loop Bandwidth.

From simulation, the propagation delay is in the 0.5 µs range and therefore the equivalent pole added to the system is the MHz region which is many orders higher than the design loop bandwidth. The effects of this high order pole for purpose of phase and gain margin can therefore be safely ignored.

Description of Charge Pump Circuit Block

Figure 33 shows the charge pump circuit block. The net output current of the COMP pin is determined by the turn-on duty difference of SW1 and SW2. If the duty of SW1 and SW2 is 50% each, there will be zero net ICOMP.

Figure 33 Charge Pump Circuit Block



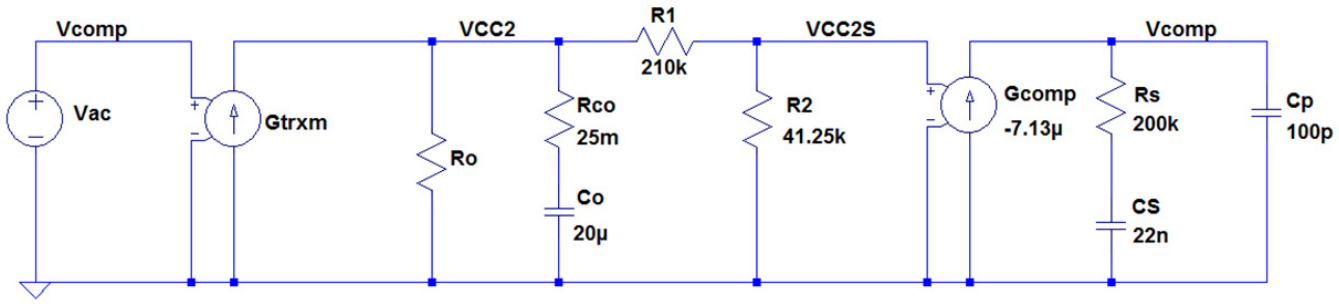
Simulation of Key Parameters in the Feedback GM Path

Parameter	Min.	Typ.	Max.	Units	Simulation Conditions
Feedback Propagation Delay	387	450	540	ns	Wafer process corner simulation for –40 °C ≤ T_J ≤ 150 °C
Feedback GM, ($\Delta I_{comp}/\Delta V_{CC2}$)	–0.772	–1.17	–1.75	uA/V	Wafer process corner simulation for –40 °C ≤ T_J ≤ 150 °C
Feedback Resistor Ratio	0.163	0.164	0.165	—	Wafer process corner simulation with ± 3sigma
Feedback Ramp Generator Saw Tooth Frequency	159	185	209	kHz	Wafer process corner simulation for –40 °C ≤ T_J ≤ 150 °C

Loop Bandwidth and Phase Margin

The close loop feedback control system can be represented in small signal model as shown in Figure 34.

Figure 34 Small Signal Model of Flyback Converter Loop



Close loop bandwidth and phase margin can be easily found out by running AC simulation on this circuit. Table 2 shows an example of AC simulation result.

Table 2 Close Loop Bandwidth and Phase Margin Simulation. Conditions Rs = 200 kOhm, Cs = 22 nF, Cp = 100 pF

Corner	GM	R_Ratio	Vin	Ro	Loop Band Width	Phase Margin	Vbg	eff	Lp	fs	Vcc2	Io	Gtrxm	Gcomp
	µA/V		Vin	kOhm	Hz	degree	V	%	uH	kHz	V	mA	A/V	µA/V
Tj =- 40 °C														
Fast	–1.75	0.164	8	1.6	123	40.7	2.75	75%	7	150	16	10	0.0435	–10.67
	–1.75	0.164	8	0.125	419	90.7	2.75	75%	7	150	16	128	0.1555	–10.67
Plot#1	–1.75	0.164	12	1.6	182	40.5	2.75	75%	7	150	16	10	0.0652	–10.67
Plot#2	–1.75	0.164	12	0.125	649	82.6	2.75	75%	7	150	16	128	0.2332	–10.67
	–1.75	0.164	18	1.6	273	40.9	2.75	75%	7	150	16	10	0.0978	–10.67
	–1.75	0.164	18	0.125	945	84.5	2.75	75%	7	150	16	128	0.3499	–10.67
Tj = 25 °C														
Typical	–1.17	0.164	8	1.6	86	40.7	2.75	75%	7	150	16	10	0.0435	–7.13
	–1.17	0.164	8	0.125	282	93.9	2.75	75%	7	150	16	128	0.1555	–7.13
Plot#3	–1.17	0.164	12	1.6	121	40.7	2.75	75%	7	150	16	10	0.0652	–7.13
Plot#4	–1.17	0.164	12	0.125	414	90.7	2.75	75%	7	150	16	128	0.2332	–7.13
	–1.17	0.164	18	1.6	182	40.6	2.75	75%	7	150	16	10	0.0978	–7.13
	–1.17	0.164	18	0.125	628	83	2.75	75%	7	150	16	128	0.3499	–7.13
Tj=150°C														
Slow	–0.772	0.164	8	1.6	60	40.7	2.75	75%	7	150	16	10	0.0435	–4.71
	–0.772	0.164	8	0.125	182	97	2.75	75%	7	150	16	128	0.1555	–4.71
Plot#5	–0.772	0.164	12	1.6	84	40.7	2.75	75%	7	150	16	10	0.0652	–4.71
Plot#6	–0.772	0.164	12	0.125	279	93.3	2.75	75%	7	150	16	128	0.2332	–4.71
	–0.772	0.164	18	1.6	120	40.6	2.75	75%	7	150	16	10	0.0978	–4.71
	–0.772	0.164	18	0.125	414	90.7	2.75	75%	7	150	16	128	0.3499	–4.71

Where

GM:	Feedback transconductance = Icomp/VCC2 (Design value)	R_Ratio	Feedback resistor ratio = R2 / (R1 + R2)
Vin:	Input voltage supply	Ro:	Load resistor
Vbg:	Vcomp (Design value)	Lp:	Primary inductance
eff:	Efficiency (Assumption)	fs:	Switching frequency
Gcomp:	GM/R_Ratio	VCC2:	Regulated output voltage
Gtrxm:	Transconductance from Vcomp to Io = Vin/Vbg*(eff/(2*Lp*fs*Ro))1/2	Io:	Output load current = VCC2 / Ro

Bode Plots of AC Simulation Result

Figure 35 Bode Plots for Fast Corner at Tj = –40 °C, GM = 1.75 µA/V, Vin = 18 V

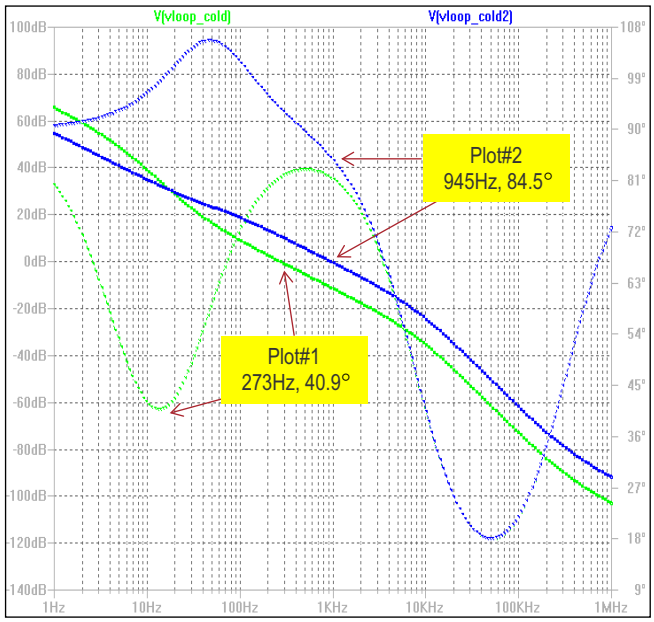


Figure 36 Bode Plots for Typical Corner at Tj = 25 °C, GM = 1.17 µA/V, Vin = 12 V

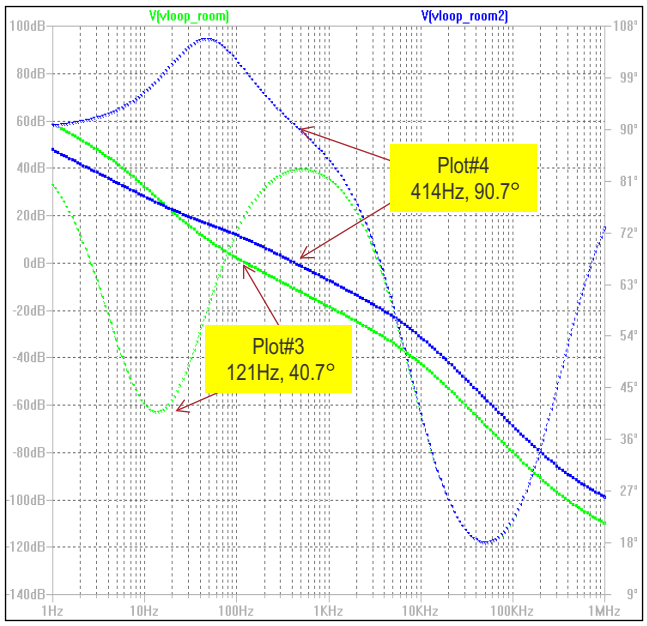
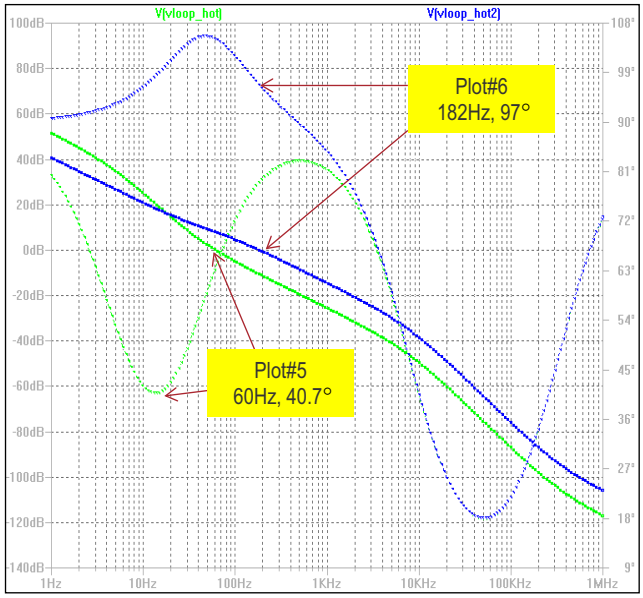


Figure 37 Bode Plots for Slow Corner at Tj = 150 °C, GM = 0.772 µA/V, Vin = 8 V



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