Middle Power Class-D Speaker Amplifier series

20W+20W
Full Digital Speaker Amplifier with built-in DSP

BM28720MUV

General Description

BM28720MUV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

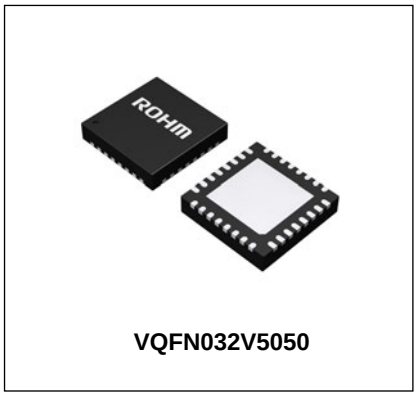
Key Specifications

- Supply voltage (VCC) 10V to 24V
- Speaker output power (VCC=18.5V, RL=8Ω) 20W+20W (Typ.)
- THD+N 0.07 [%] (Typ.)

Applications

- Flat Panel TVs (LCD, Plasma)
- Home Audio
- Desktop PC
- Amusement equipments
- Electronic Music equipments, etc.

Package W(Typ) x D(Typ) x H(Max)
VQFN032V5050 5.00mm x 5.00mm x 1.00mm



VQFN032V5050

Features

- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
  12 Band/ch P-EQ, 3 Band DRC, Pre-scaler, Channel mixer, Fine Master Volume, Hard Clipper, Level Meter etc.
- This IC has one input systems of digital audio interface. (No needs of Master Clock)
  - I^2S / LJ / RJ format
  - LRCLK: 32k/44.1k/48KHz
  - BCLK: 32fs / 48fs / 64fs
  - SDATA: 16 / 20 / 24bit
- This IC has one output systems of digital audio interface.
  - I^2S format
  - SDATA: 16 / 20 / 24bit
- With wide range of power supply voltage.
- The monaural output that can reduce the number of external parts can be used.
- With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
- Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
- This IC is built-in with various protection functions for highly reliability design.
  - High temperature protection
  - Under voltage protection
  - Output short protection
  - DC voltage protection
  - Clock stop protection
- Small package

Typical Application Circuit

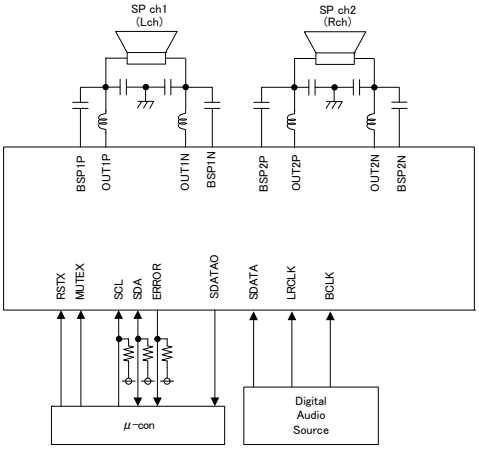


Figure 1. Typical application circuits

Pin configuration and Block diagram

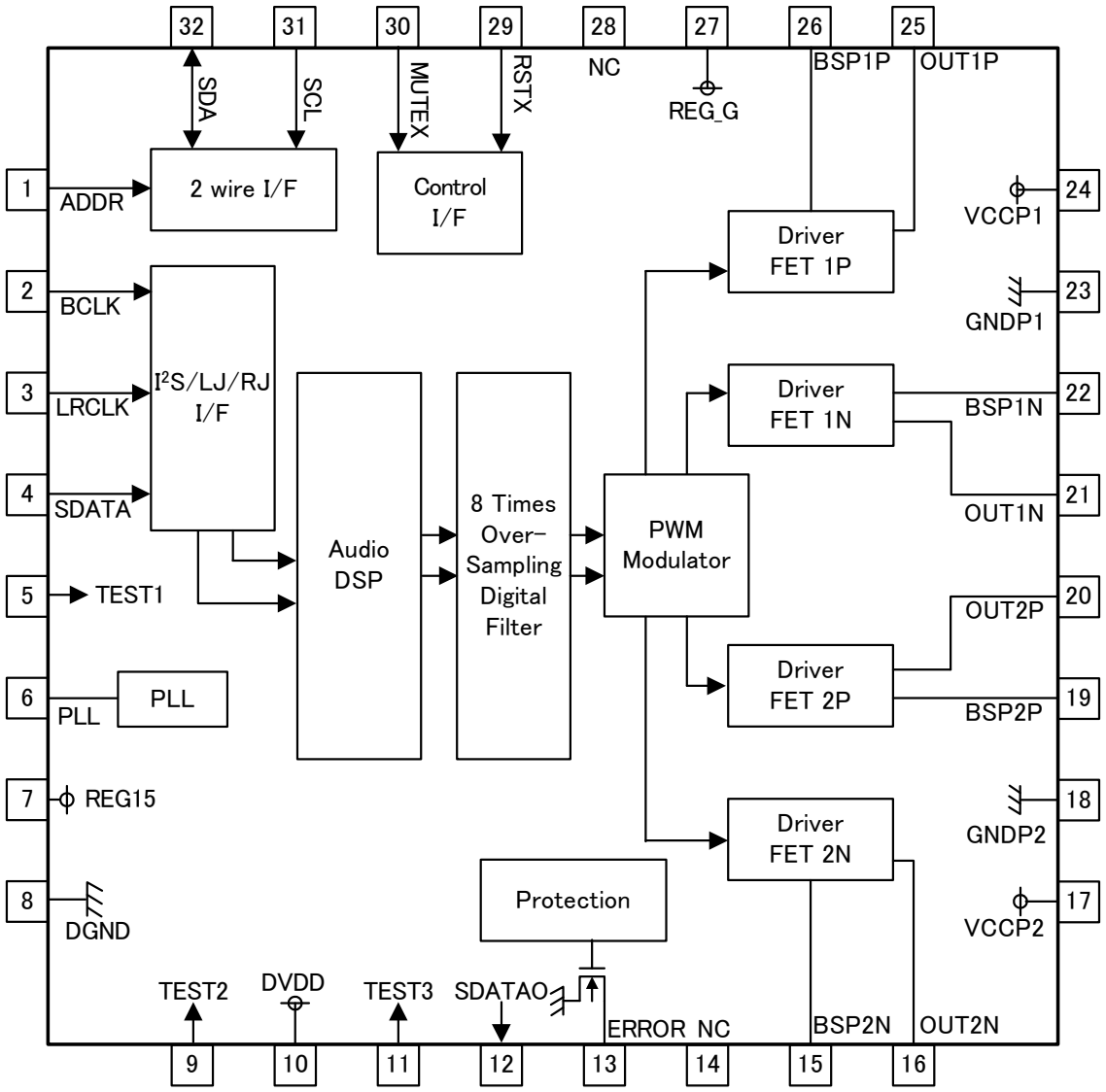


Figure 2. Pin configurations and Block diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	ADDR	I	9	TEST2	I	17	VCCP2	-	25	OUT1P	O
2	BCLK	I	10	DVDD	-	18	GNDP2	-	26	BSP1P	I
3	LRCK	I	11	TEST3	I	19	BSP2P	I	27	REG_G	O
4	SDATA	I	12	SDATAO	O	20	OUT2P	O	28	NC	-
5	TEST1	I	13	ERROR	O	21	OUT1N	O	29	RSTX	I
6	PLL	O	14	NC	-	22	BSP1N	I	30	MUTEX	I
7	REG15	O	15	BSP2N	I	23	GNDP1	-	31	SCL	I
8	DGND	-	16	OUT2N	O	24	VCCP1	O	32	SDA	I/O

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	-0.3 to 34	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	-0.3 to 4.5	V	Pin 10 (Note 1)
Power dissipation	Pd	3.26	W	(Note 3)
		4.56	W	(Note 4)
Input voltage 1	VIN1	-0.3 to DVDD+0.3	V	Pin 1 - 5, 9, 11, 12, 13, 29 -32 (Note 1)
Terminal voltage 1	VPIN1	-0.3 to 7.0	V	Pin 27 (Note 1)
Terminal voltage 2	VPIN2	-0.3 to 29	V	Pin 16, 20, 21, 25 (Note 1)(Note 5)
Terminal voltage 3	VPIN3	OUTxx+6.0	V	Pin 15, 19, 22, 26 (Note 1)
Operating temperature range	Topr	-25 to +85	℃	
Storage temperature range	Tstg	-55 to +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Pd and Tjmax=150℃.
(Note 3) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derating in done at 26.1 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
(Note 4) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area 5505mm^2)
Derating in done at 36.5 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.

(Note 5) It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10nse and ≦29V by the VCC reference. (Please refer following figure.)

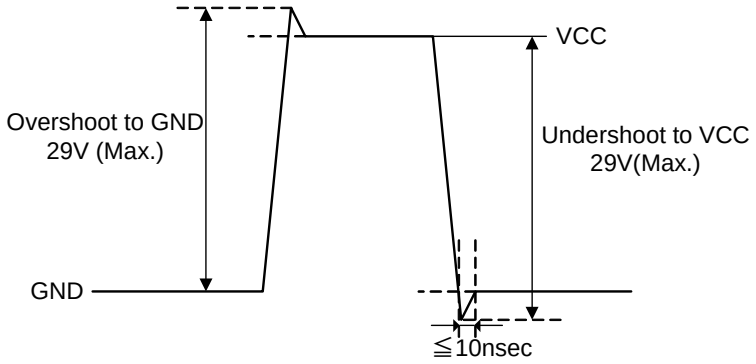


Figure 3.

Recommended Operating Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	10 to 24	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	3 to 3.6	V	Pin 10 (Note 1)
Minimum load impedance	R_L	5.4	Ω	Pin 16, 20, 21, 25 VCC = 18V to 24V (Note 6)
		3.6	Ω	Pin 16, 20, 21, 25 VCC < 18V (Note 6)

(Note 6) Do not exceed Pd.

Electrical Characteristics

(Unless otherwise specified Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz, R_L=8Ω,
DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=680pF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 17, 24, No load
	I_{DD1}	-	9	19	mA	Pin 10, -infinity dBFS input, No load
Circuit current 2 (Reset mode)	I_{CC2}	-	10	40	μA	Pin 17, 24, No load RSTX=0V, MUTEX=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 10, --infinity dBFS input, No load RSTX=0V, MUTEX=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 23, I_O=0.5mA
Regulator output voltage 1	V_{REG_G}	4.9	5.7	6.5	V	Pin 27
Regulator output voltage 2	V_{REG15}	1.3	1.5	1.7	V	Pin 7
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 1 - 5, 9, 11, 12, 29 -32
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 1 - 5, 9, 11, 12, 29 -32
Input current (Input pull-up terminal)	I_{UP}	-150	-100	-50	μA	Pin 2 – 4 VIN = 0V
Input current (Input pull-down terminal)	I_{DN}	35	70	105	μA	Pin 1, 29, 30, VIN = 3.3V
Input current (SCL, SDA terminal)	I_{IL}	-1	0	-	μA	Pin 31, 32, V IN = 0V
Input current (SCL, SDA terminal)	I_{IH}	-	0	1	μA	Pin 31, 32, VIN = 3.3V
Speaker amplifier output						
Maximum output power 1	P_{O1}	-	10	-	W	VCC=13V,THD+n=10% *8
Maximum output power 2	P_{O2}	-	20	-	W	VCC=18.5V,THD+n=10% (Note 7)
Total harmonic distortion 1	THD1	-	0.07	-	%	P_O=1W, BW=20 to 20kHz(AES17) (Note 7)
Crosstalk 1	CT1	60	80	-	dB	VCC=13V, P_O=1W, BW=IHF-A (Note 7)
Output noise voltage 1	V_{NO1}	-	80	-	μVrms	-∞dBFS Input, BW=IHF-A (Note 7)
PWM sampling frequency	f_{PWM1}	-	256	-	kHz	fs=32 kHz
	f_{PWM2}	-	352.8	-	kHz	fs=44.1 kHz
	f_{PWM3}	-	384	-	kHz	fs=48 kHz

(Note 7) These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=0V/3.3V, MUTEX=0V/3.3V, f=1kHz,
DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

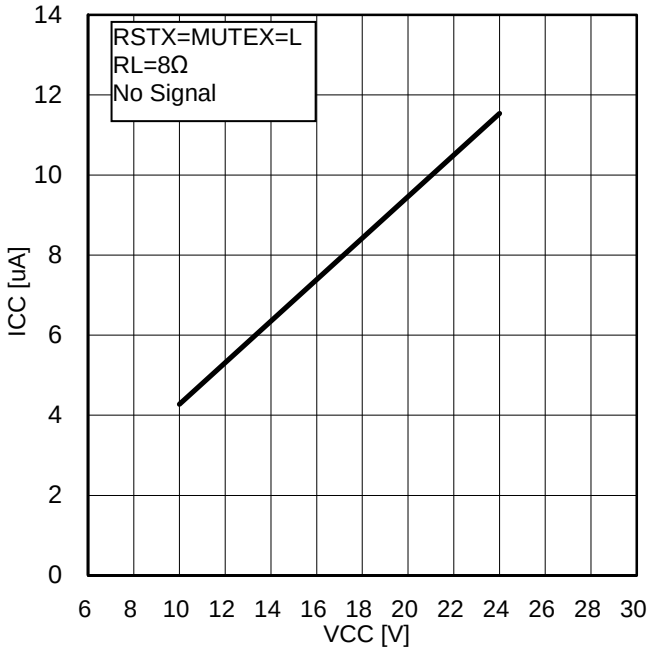


Figure 4.

Power supply voltage- Current consumption

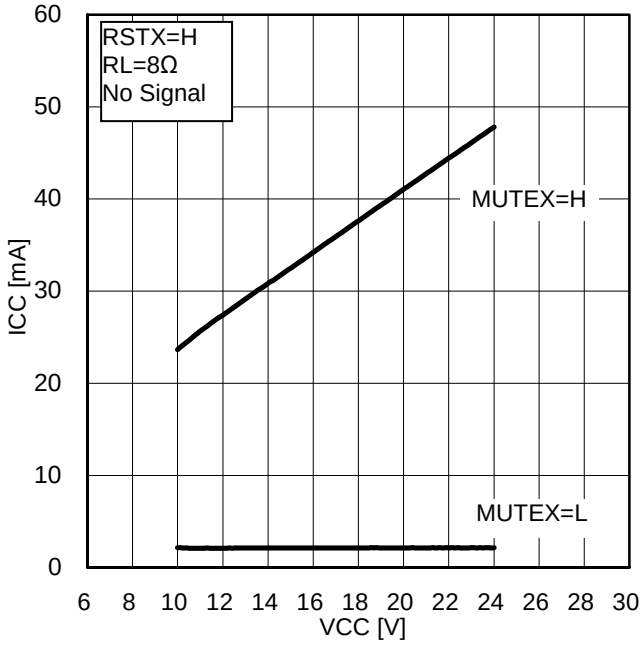


Figure 5.

Power supply voltage- Current consumption

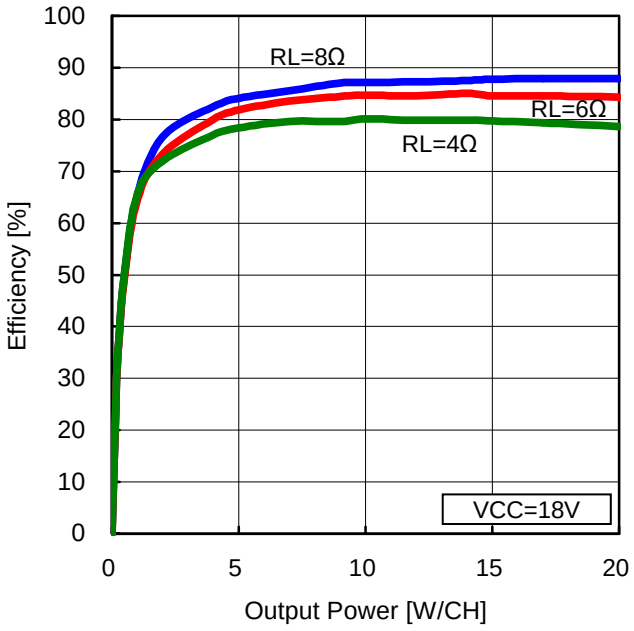


Figure 6.

Output power - Efficiency

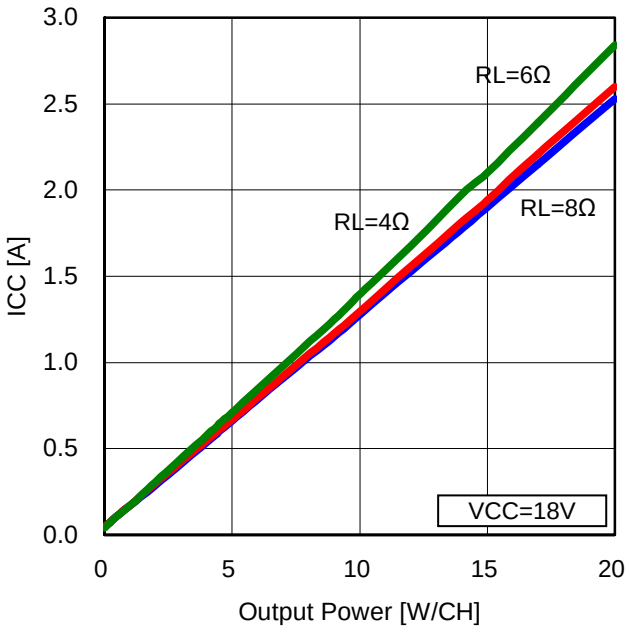


Figure 7.

Output power - Current consumption

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

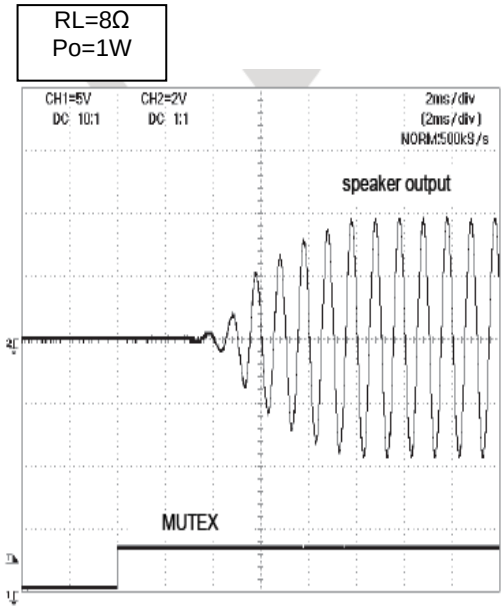


Figure 8.
Waveform at soft start

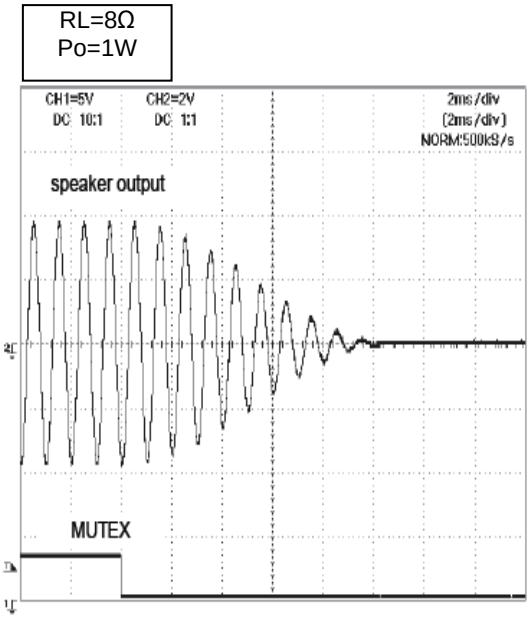


Figure 9.
Waveform at soft mute

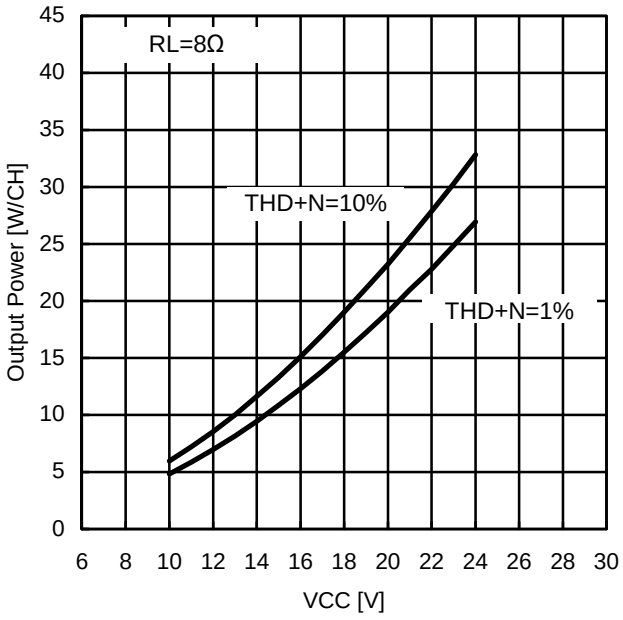


Figure 10.
Output voltage - Power voltage (R_L=8Ω)

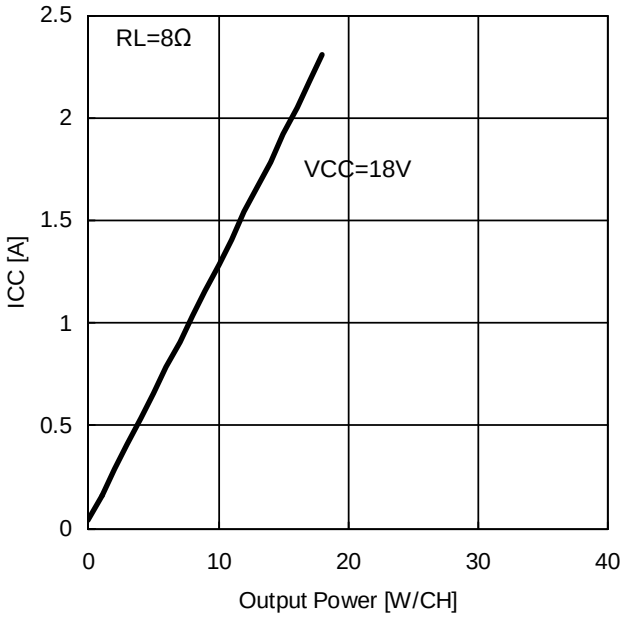


Figure 11.
Output power - Current consumption (R_L=8Ω)

※Dotted line means internal dissipation is over package power.

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

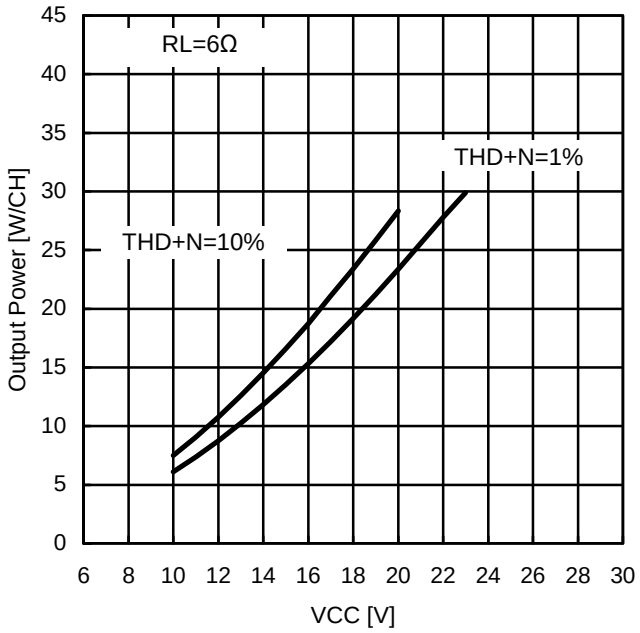


Figure 12.

Output voltage - Power voltage (R_L=6Ω)

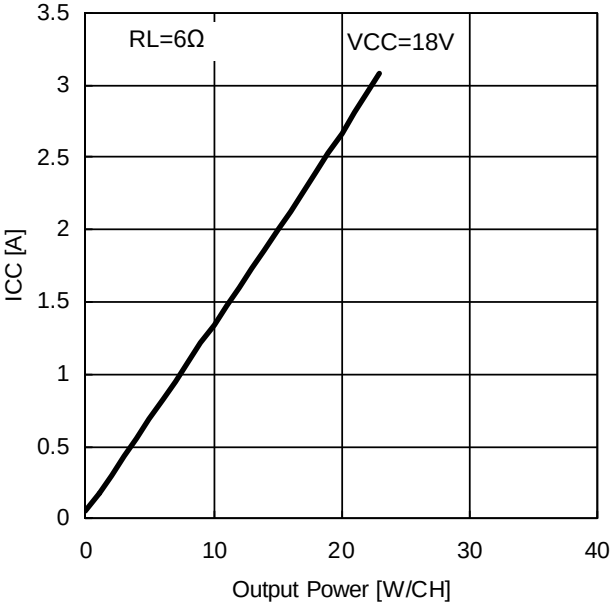


Figure 13.

Output power - Current consumption (R_L=6Ω)

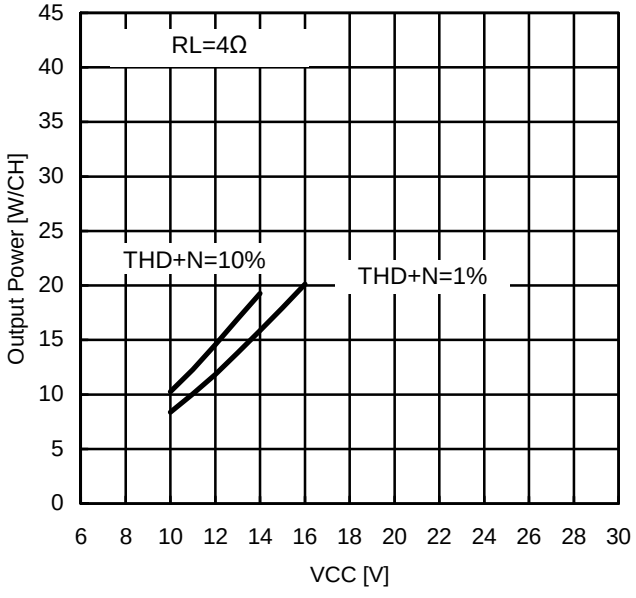


Figure 14.

Output Voltage – Power Voltage (R_L=4Ω)

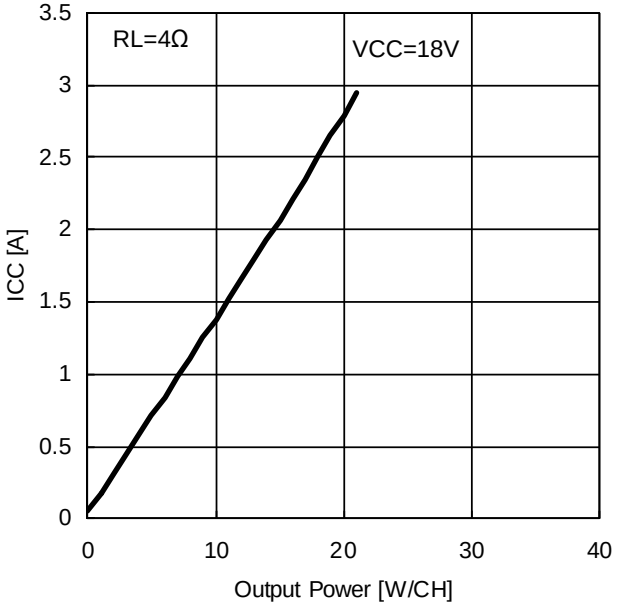


Figure 15.

Output power - Current consumption (R_L=4Ω)

※Dotted line means internal dissipation is over package power.

Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

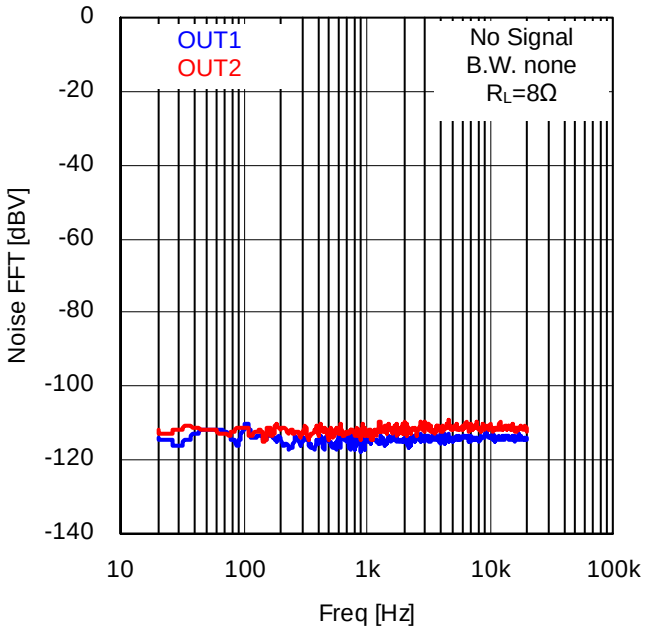


Figure 16.
FFT of output noise voltage

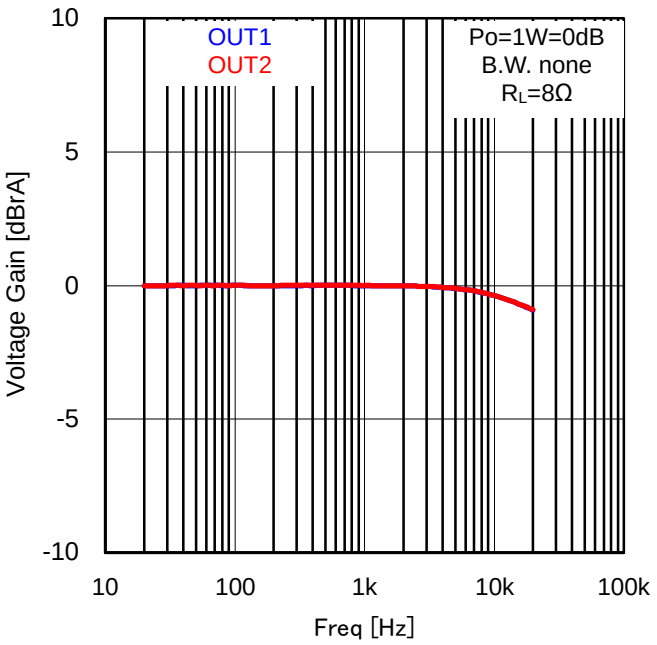


Figure 17.
Frequency – Output power

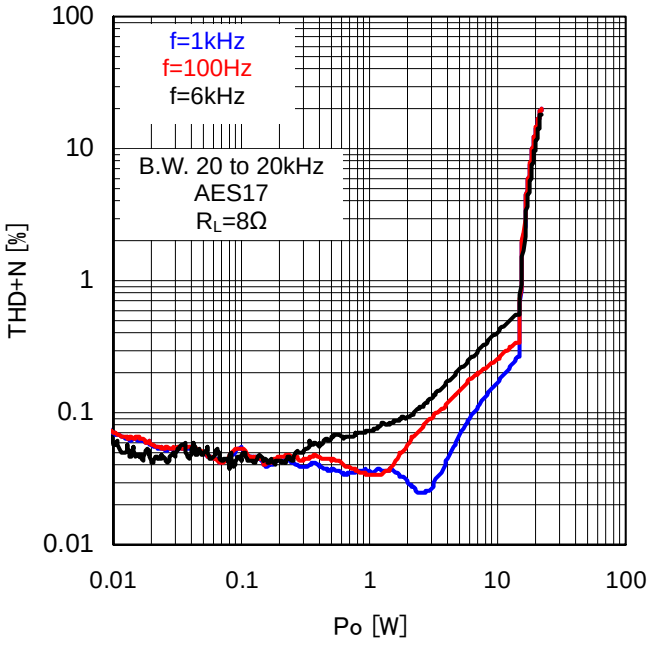


Figure 18.
Output Power - THD+N

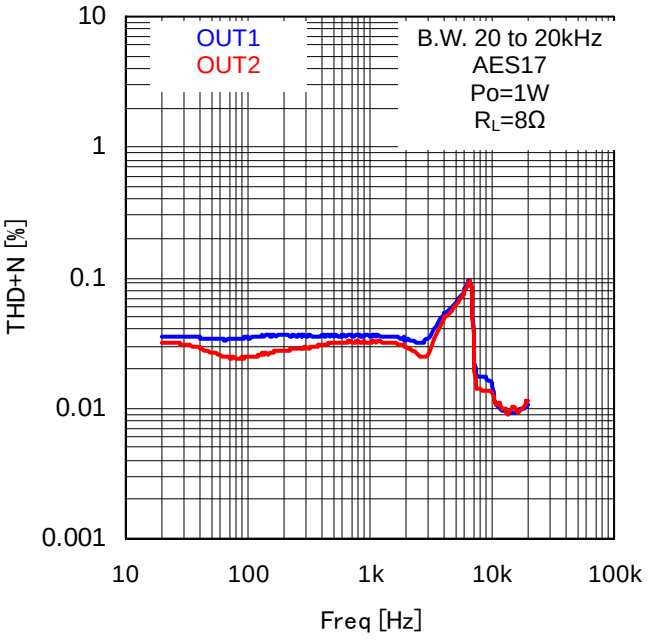


Figure 19.
Frequency - THD+N

Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

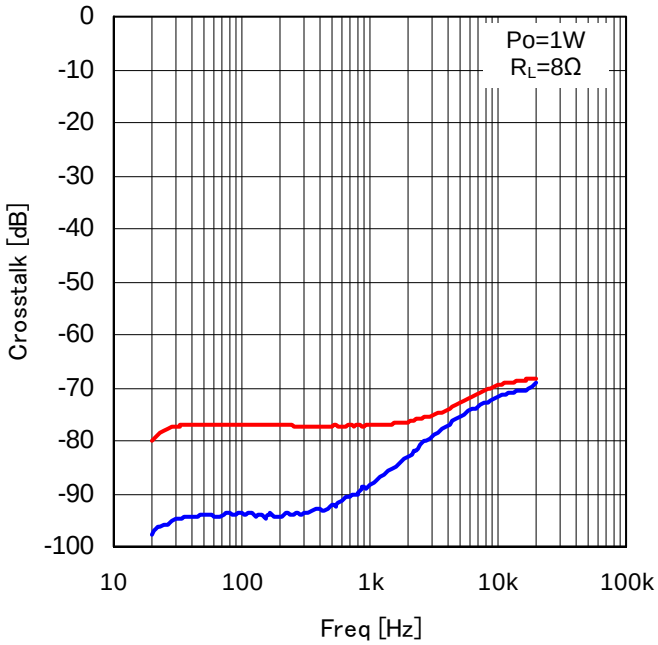


Figure 20.
Frequency - Crosstalk

Typical Performance Curves

Speaker output(R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

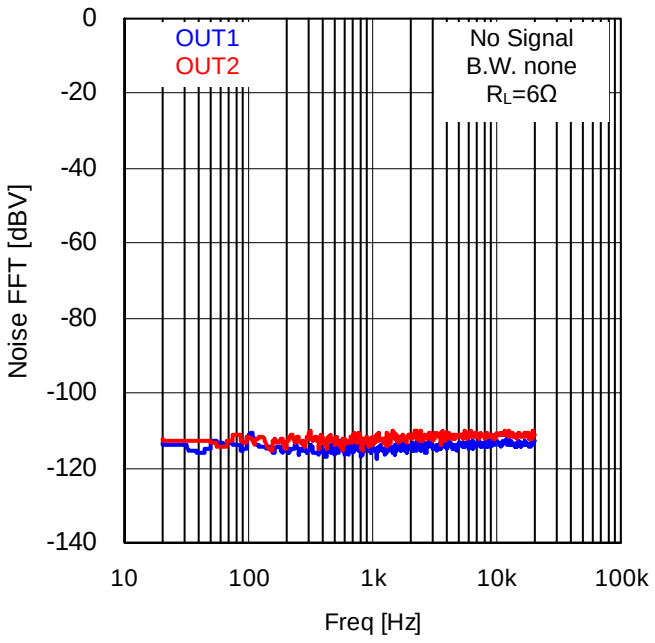


Figure 21.
FFT of output noise voltage

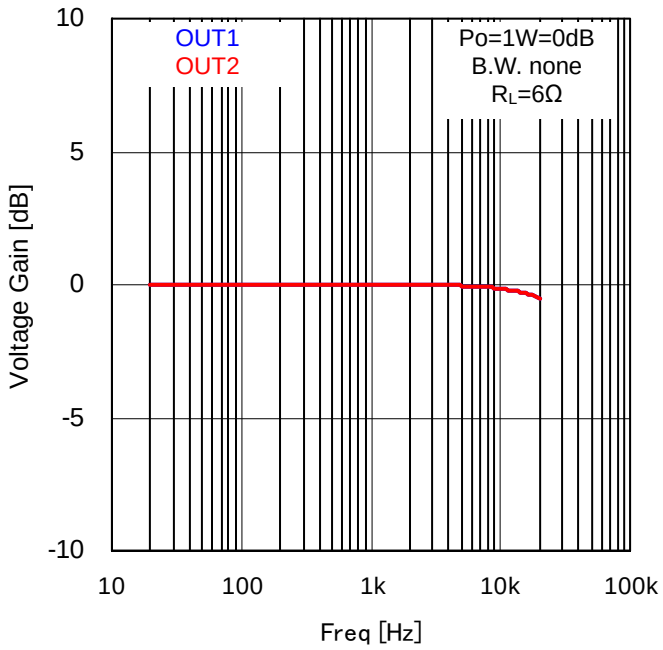


Figure 22.
Frequency – Output power

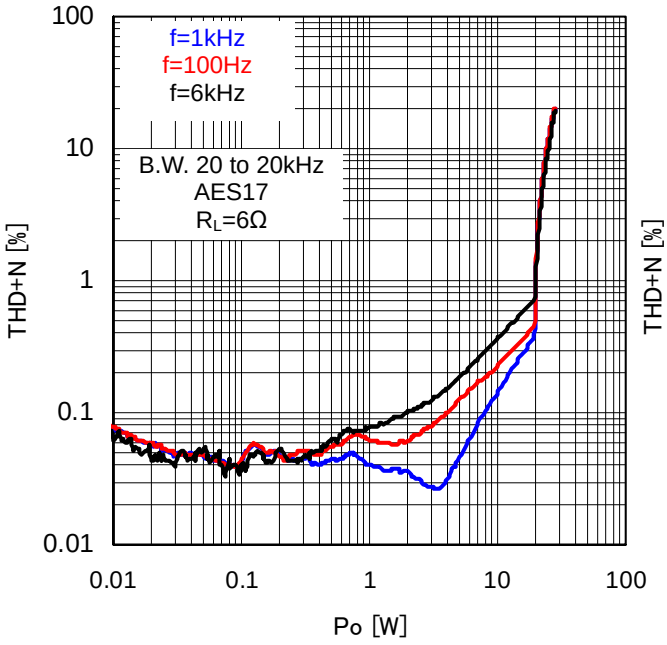


Figure 23.
Output Power - THD+N

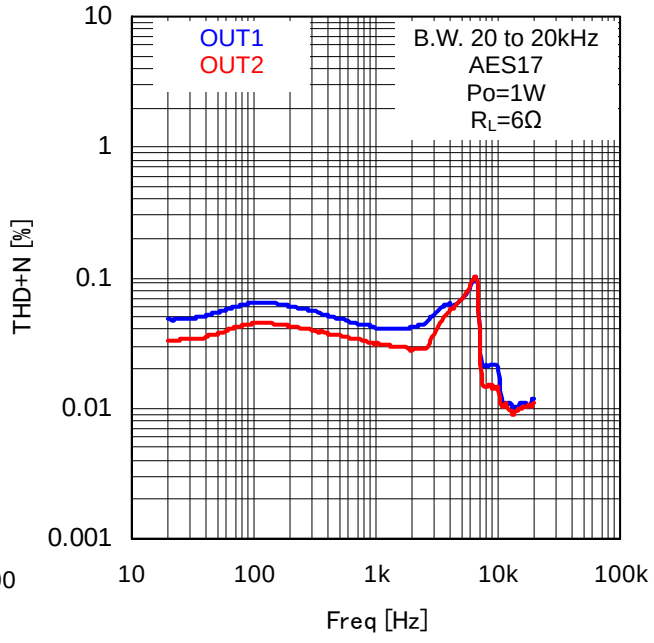


Figure 24.
Frequency - THD+N

Typical Performance Curves

Speaker output R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)
Measured by ROHM designed 4 layer board.

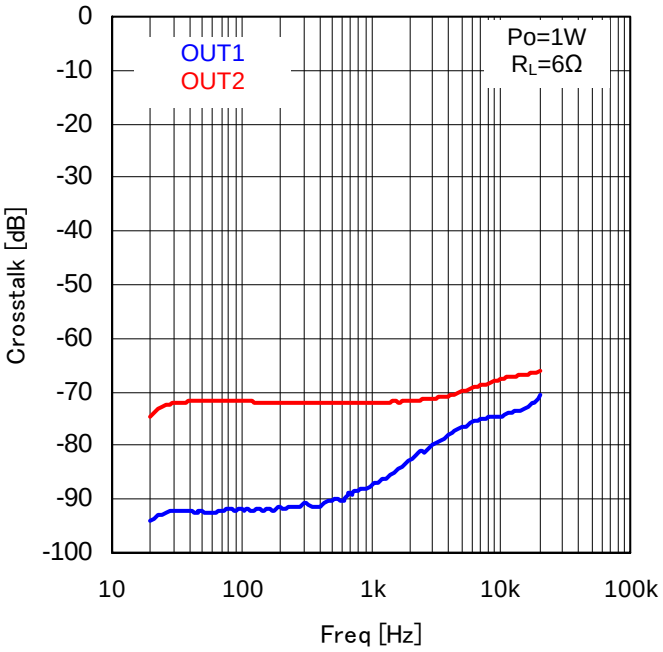


Figure 25.
Frequency - Crosstalk

Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)
Measured by ROHM designed 4 layer board.

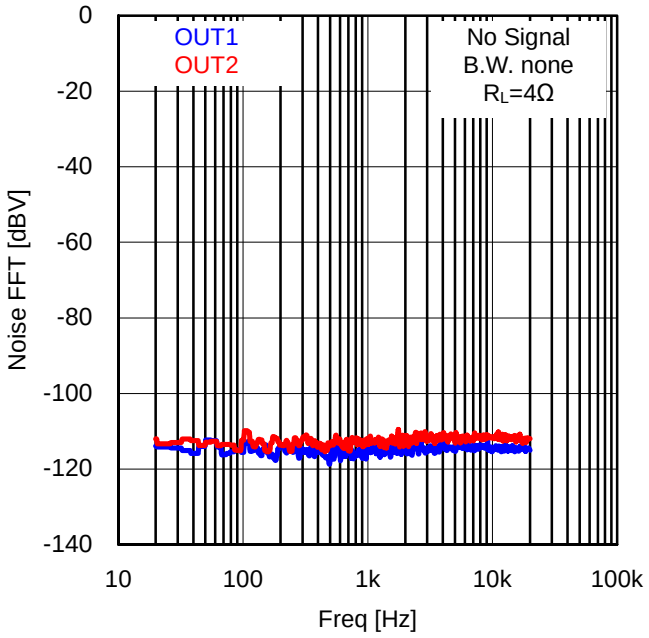


Figure 26.
FFT of output noise voltage

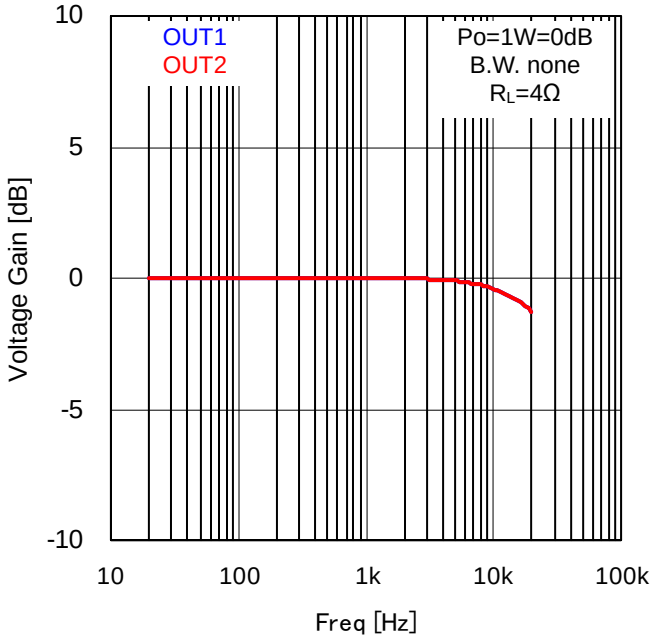


Figure 27.
Frequency – Output power

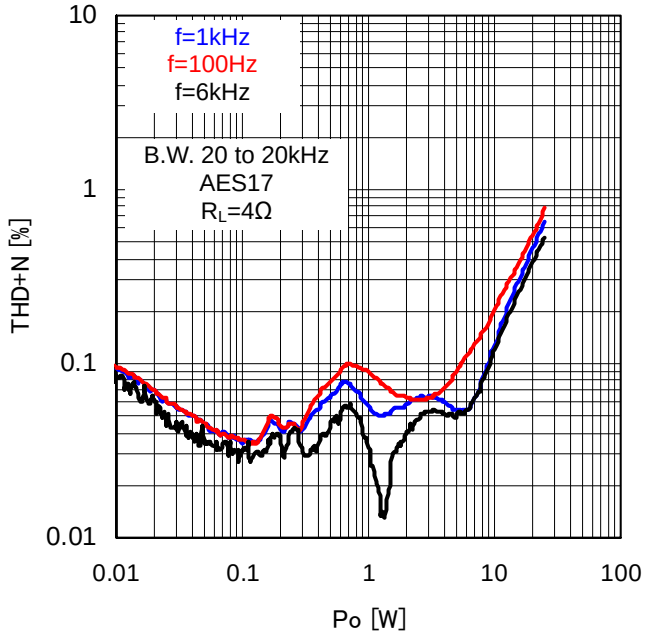


Figure 28.
Output Power - THD+N

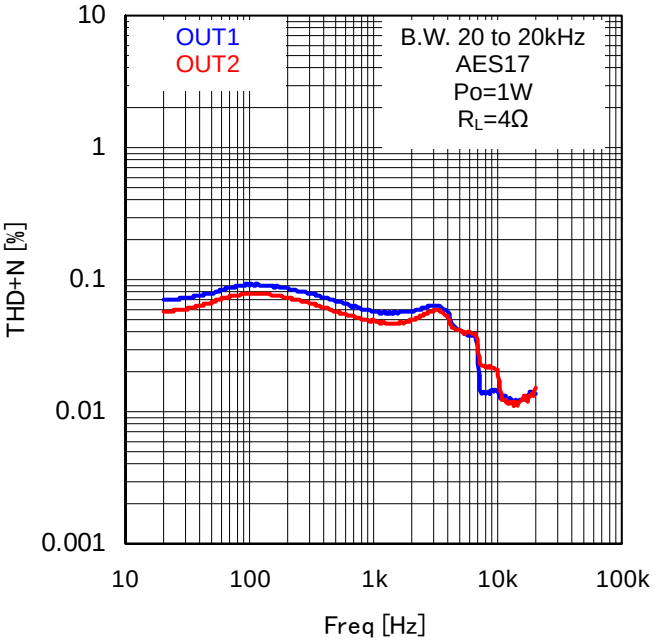


Figure 29.
Frequency - THD+N

Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V,
f=1kHz, DSP : Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal : R=5.6Ω, C=680pF)

Measured by ROHM designed 4 layer board.

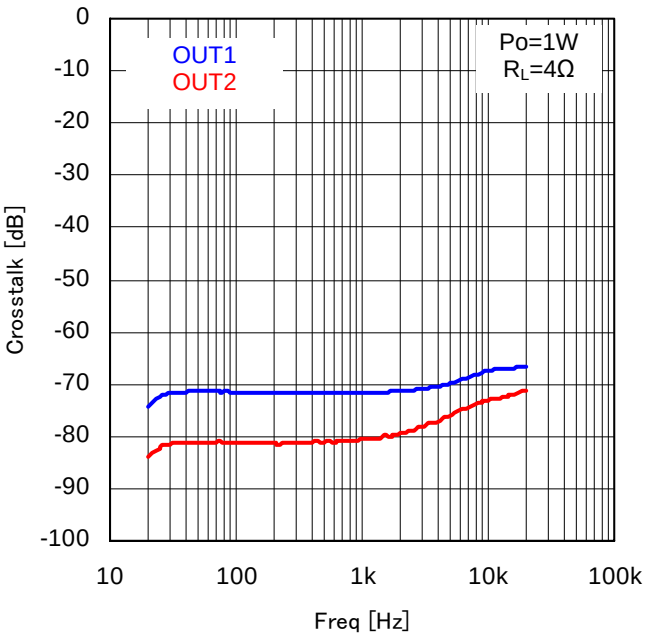


Figure 30.
Frequency - Crosstalk

Digital Block Functional Overview

No.	Function	Specification
1	Pre-scaler	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step),-∞dB ・default 0dB
2	Channel Mixer	・Lch <= Mute, Lch(default), Rch, (L+R)/2, L-R ・Rch <= Mute, Lch, Rch(default), (L+R)/2, L-R ・Lch/Rch are independent phase reversal control available.
3	12-Band Parametric Equalizer	・12-Band Bi-quad type Parametric Equalizer . ・Only 5 coefficient is required.(b0,b1,b2,a1,a2) ・The Filter types which can be realized is Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass/Notch. ・Lch/Rch become same set point or independent set. There is soft transition function.
4	Fine Master Volume	・Lch / Rch become same set point or independent set. ・+24dB to -103dB (0.125dB step),-∞dB ・There is soft transition function.
5	3 Band DRC	・Non clip output is achieved. ・Lch/Rch becomes the same control. ・Low-pass and a high region become an independent control. ・Threshold level : +12dB to -32dB (0.5dB step) ・The set point of Cross-over frequency : Divide between into 61 from 20 Hz to 20 kHz. ・The voice below the set-up detect level is decreased gently.
6	Post-scaler	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step),-∞dB ・default 0dB
7	Fine Post-Scaler	・Lch / Rch become independent set point. ・+0.7dB to -0.8dB (0.1dB step)
8	DC cut HPF	・1st order HPF ・Fc : 1Hz
9	Clipper	・Lch / Rch become same set point. ・Clip level : +3dB to -22.5dB (-0.1dB step)

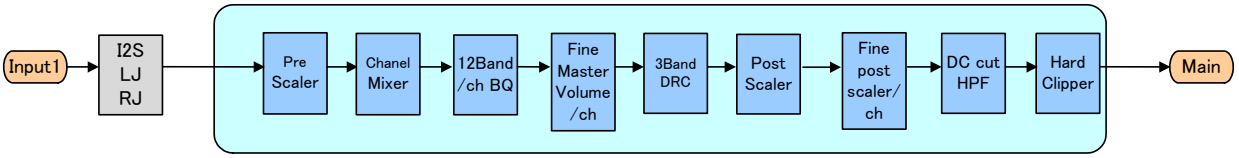


Figure 31. DSP Block diagram

RSTX pin, MUTEX pin function

RSTX (29pin)	MUTEX (30pin)	DSP block condition	Speaker output condition
L	L	Reset ON	HiZ_Low (Low consumption)
H	L	Normal operation (Mute ON)	HiZ_Low (Mute ON)
H	H	Normal operation (Mute OFF)	Normal operation (Mute OFF)
L	H	Don't use.	

(Note 1) RSTX is set Low, internal registers are initialized.
(Note 2) VCCP1, VCCP2< 2.5V, IC latched by protection circuit and ERROR terminal condition are initialized.
(Note 3) If DVDD is under 3V, RSTX is set Low once for 10ms(min), and set High again. Then DSP is needed to set parameter again.

Input Digital sound sampling frequency (fs) explanation

PWM sampling frequency of Speaker output and Soft-mute transition time depends on sampling frequency (fs) of the digital sound input. These transition times are changed by sending select address &h15[1:0].

Sampling frequency of the Digital sound input (fs)	Speaker output PWM sampling frequency	Soft-mute Transition time	
		Mute ON	Mute OFF
48kHz	384kHz	85.4msec	10.7msec
		42.7msec	10.7msec
		21.4msec	10.7msec
		10.7msec	10.7msec
44.1kHz	352.8kHz	92.9msec	11.7msec
		46.5msec	11.7msec
		23.3msec	11.7msec
		11.7msec	11.7msec
32 kHz	256kHz	128.1msec	16.1msec
		64.1msec	16.1msec
		32.1msec	16.1msec
		16.1msec	16.1msec

2 wire Bus control signal specification

1) Electrical characteristics and Timing of Bus line and I/O stage

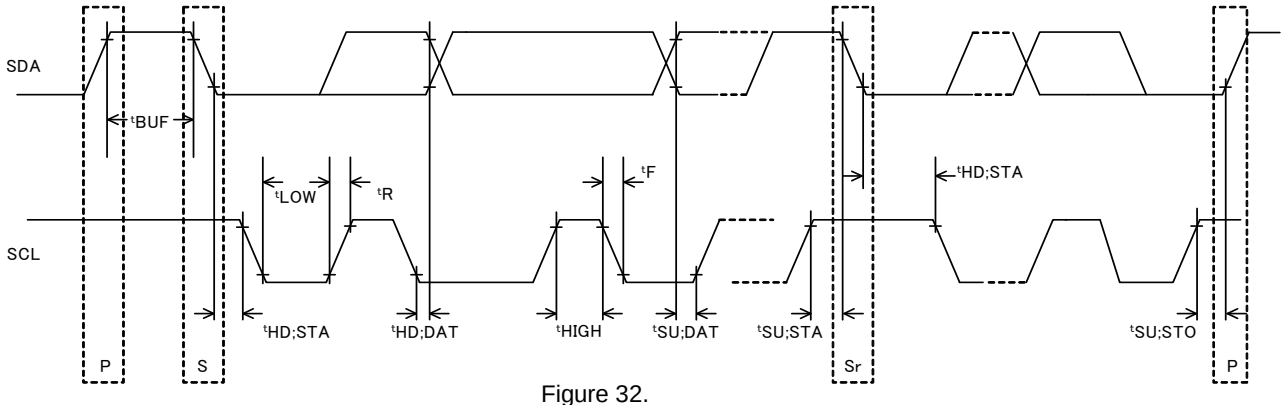


Figure 32.

SDA and SCL bus line characteristics(Unless otherwise specified Ta=25℃, VDD=3.3V)

	Parameter	Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between「Stop」condition and「Start」condition	tBUF	1.3	−	μS
3	Hold-time of (sending again)「Start」condition. After this period the first clock pulse is generated.	tHD;STA	0.6	−	μS
4	SCL clock's LOW state Hold-time	tLOW	1.3	−	μS
5	SCL clock's HIGH state Hold-time	tHIGH	0.6	−	μS
6	Set-up time of sending again「Start」condition	tSU;STA	0.6	−	μS
7	Data hold time	tHD;DAT	0 (Note 1)	−	μS
8	Data set-up time (Note 2)	tSU;DAT	500/250/150	−	ns
9	Rise-time of SDA and SCL signal	tR	20+0.1Cb	300	ns
10	Fall-time of SDA and SCL signal	tF	20+0.1Cb	300	ns
11	Set-up time of 「Stop」condition	tSU;STO	0.6	−	μS
12	Capacitive load of each bus line	Cb	−	400	pF

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.

(Note 1) To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.

(Note 2)The data set-up time is different according to the setting of SYS_CLK.
When SYS_CLK=128fs it is 500ns, for SYS_CLK=256fs it is 250ns, for SYS_CLK=512fs it will be 150ns.
Initial setting is SYS_CLK=256fs.

(Note 3) SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Please use it within 4.5V of the absolute maximum rating.

2)Command interface

2 wire Bus control is used for command interface between host CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to "Slave Address " , set and write 1 byte of "Select Address " to read out the data. 2 wire bus Slave mode format is illustrated below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

Figure 33.

S : Start Condition

Slave Address : The data of eight bits in total is sent putting up bit of Read mode (H) or Write mode (L) after slave address (7bit) set with the terminal ADDR. (MSB first)

A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.
When data is correctly sent and received,"L"is sent and received.
There was no acknowledgement for "H".

Select Address : The select address in one byte is used.(MSB first)

Data : Data byte is sent and received data(MSB first)

P : Stop Condition

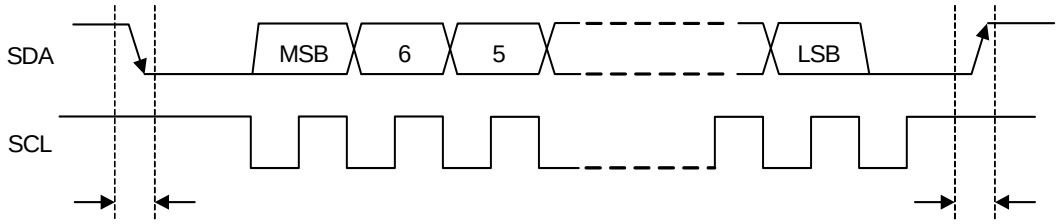


Figure 34.

3)Slave Address

・While ADDR pin is"L"

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

・While ADDR pin is"H"

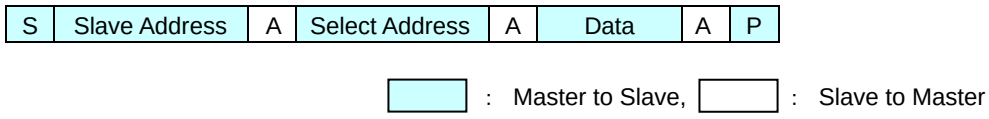
MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

Figure 35.

4) Writing of data

・Basic format



・Auto-increment format

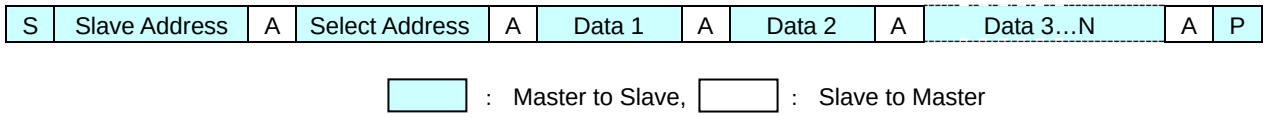


Figure 36.

5)Reading of data

First of all, the address (20h in the example) for reading is written in the register of the D0h address at the time of reading. In the following stream, data is read after the slave address. Please do not return the acknowledge when you end the reception.

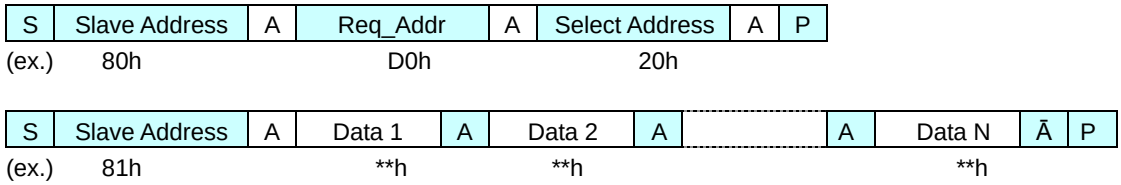


Figure 37.

Format of digital audio input

- LRCLK: It is L/R clock input signal.
  It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs) .
  The audio data of a left channel and a right channel for one sample is input to this section.

- BCLK: It is Bit Clock input signal.
  It is used for the latch of data in every one bit by sampling frequency's 48 times frequency (48fs) or 64 times sampling frequency (64fs). However if the 48fs being selected, the input will be Right-justified data format and held static.

- SDATA: It is Data input signal.
  It is amplitude data. The data length is different according to the resolution of the input digital data.
  It corresponds to 16/ 20/ 24 bit.

  The digital input has I2S, Left-justified and Right-justified formats.
  The figure below shows the timing chart of each transmission mode.

- SDATAO: Audio data after DSP processing.
  Output audio data after DSP processing.
  This output synchronous to inputted LRCK and BCLK.

Bit clock 64fs

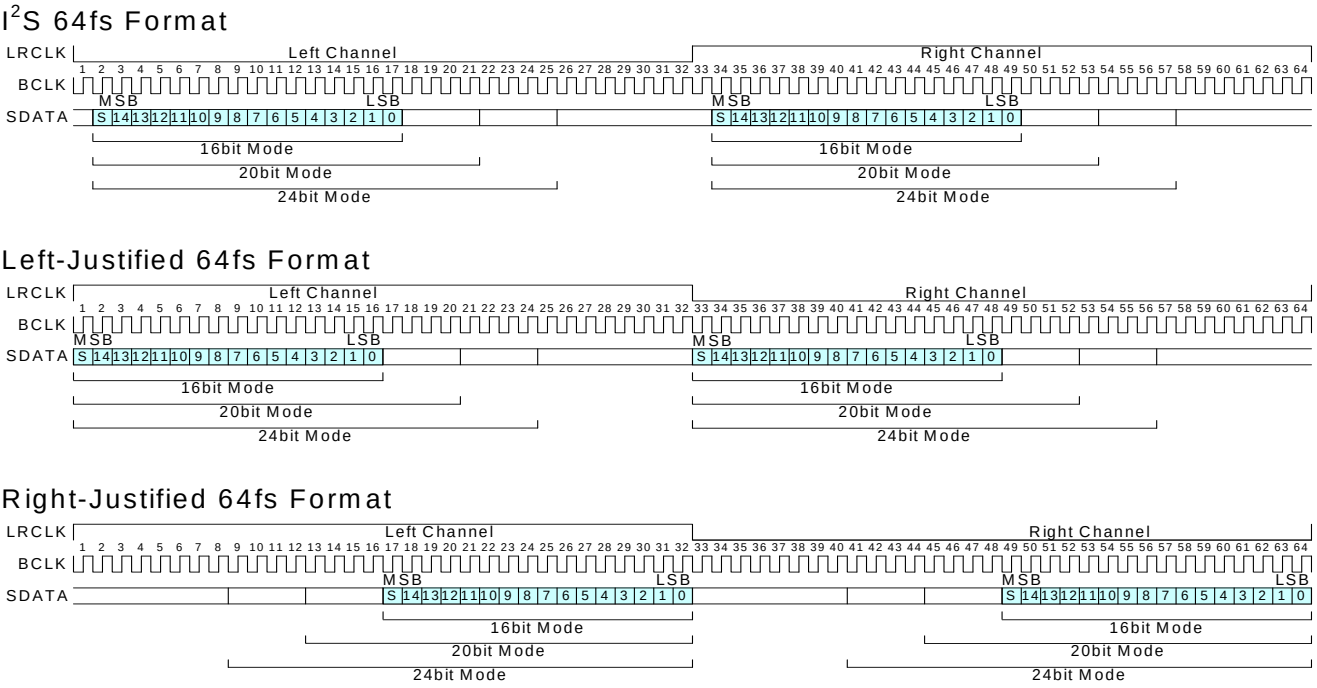
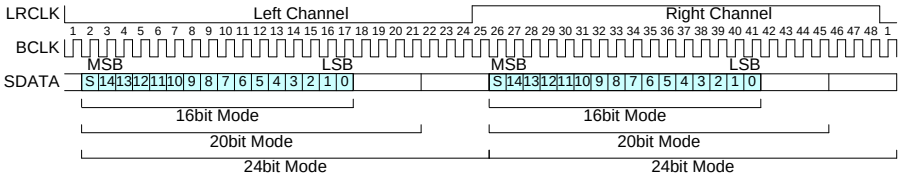


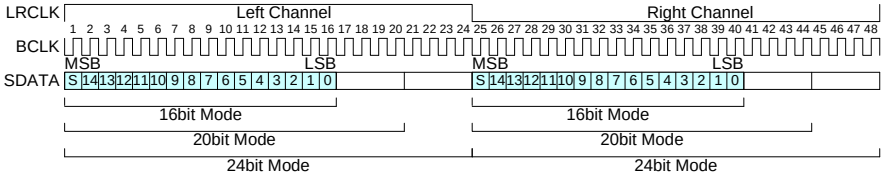
Figure 38.

Bit clock 48fs

I²S 48fs Format



Left-Justified 48fs Format



Right-Justified 48fs Format

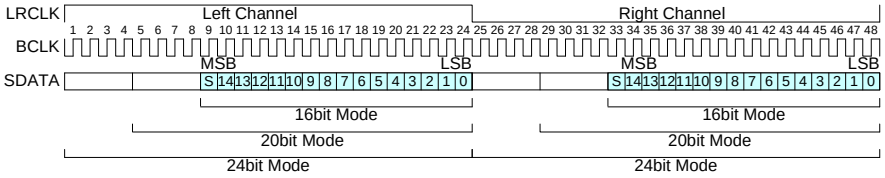
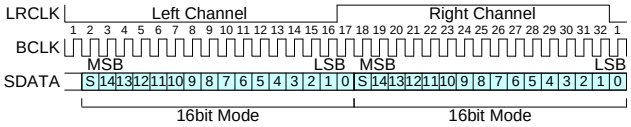


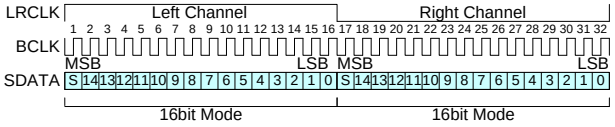
Figure 39.

Bit clock 32fs

I²S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format

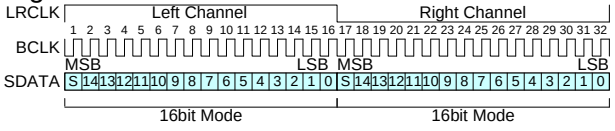


Figure 40.

Format setting for Digital Audio Interface

Please set Bit clock fs , Data strength and Format by transmitting command according to inputted Digital Serial Audio signal.

SDATAO output data bit width is able to be set independently.

Bit clock

Default = 0

Select Address	Value	Explanation of operation
&h03[5:4]	0	64fs
	1	48fs
	2	32fs

Data Format

Default = 0

Select Address	Value	Explanation of operation
&h03[3:2]	0	IIS format
	1	Left-justified format
	2	Right-justified format

Data width

Default = 2

Select Address	Value	Explanation of operation
&h03[1:0]	0	16 bit
	1	20 bit
	2	24 bit

SDATAO output Data strength

Default = 2

Select Address	Value	Explanation of operation
&h78[1:0]	0	16 bit
	1	20 bit
	2	24 bit

Audio Interface format and timing

Recommended timing and operating conditions (BCLK, LRCLK, SDATA)

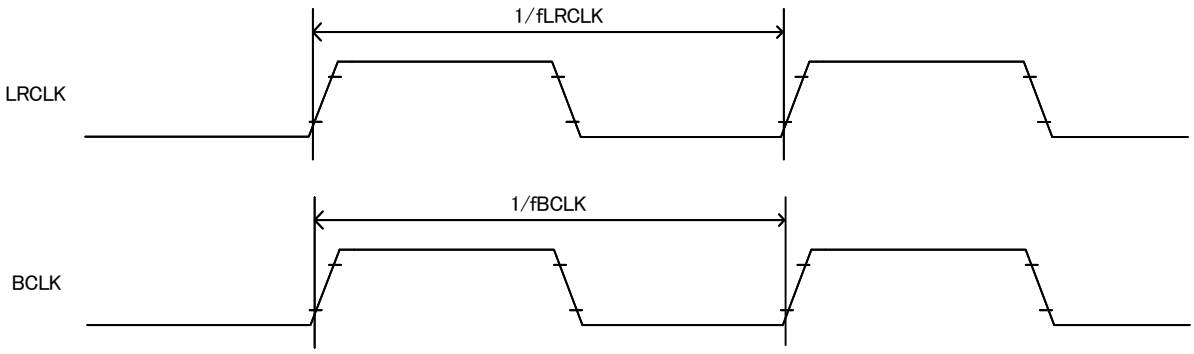


Figure 41. Clock timing

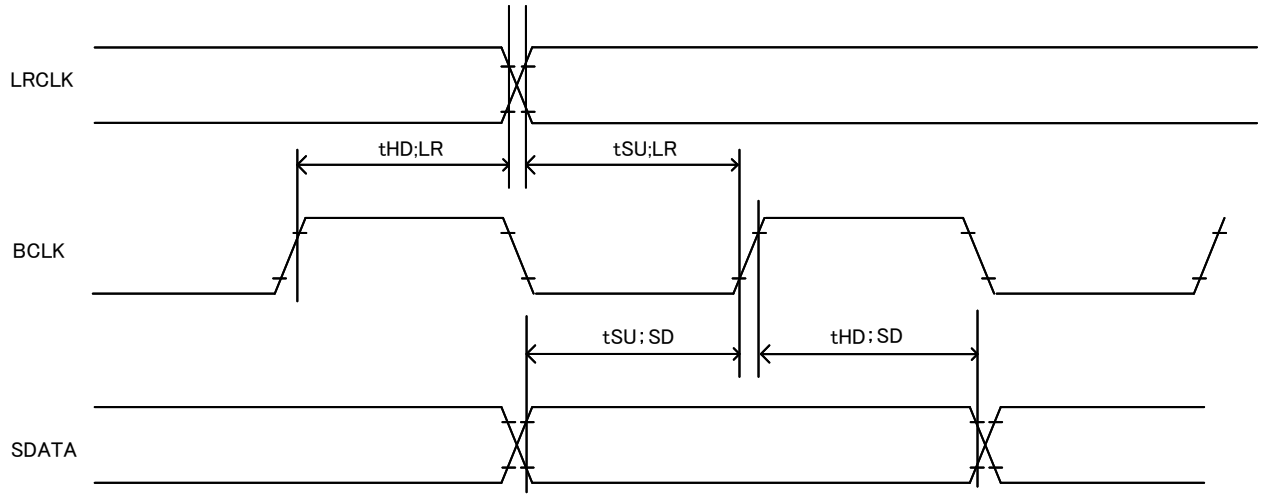
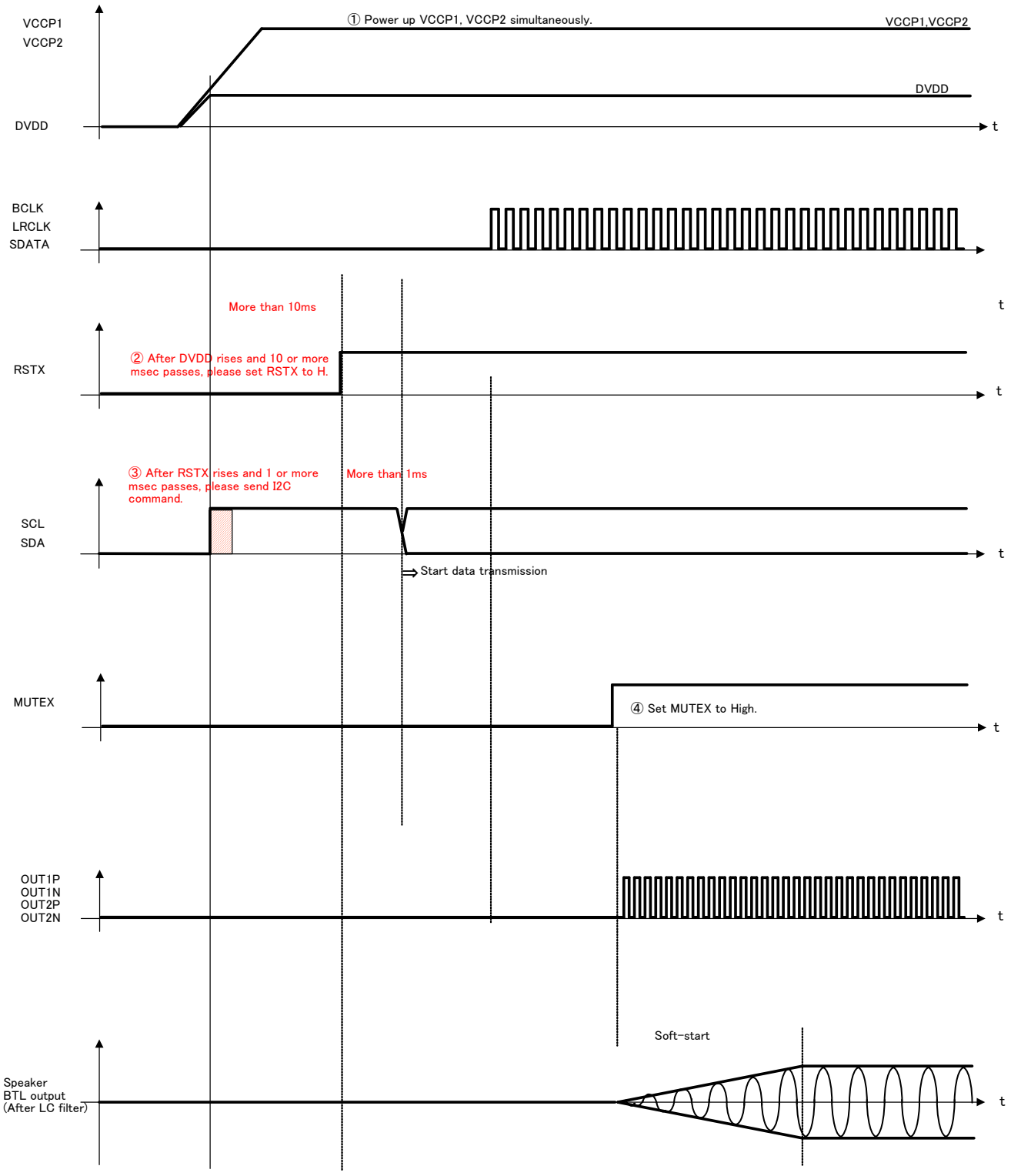


Figure 42. Audio Interface timing

No.	Parameter	Symbol	Limit		Unit
			Min.	Max.	
1	LRCLK frequency	fLRCLK	32	48	kHz
2	BCLK frequency	fBCLK	2.048	3.072	MHz
3	Setup time, LRCLK(Note 1)	tSU;LR	20	—	ns
4	Hold time, LRCLK(Note 1)	tHD;LR	20	—	ns
5	Setup time, SDATA	tSU;SD	20	—	ns
6	Hold time, SDATA	tHD;SD	20	—	ns
7	LRCLK, DUTY	dLRCLK	40	60	%
8	BCLK, DUTY	dBCLK	40	60	%

(Note 1) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

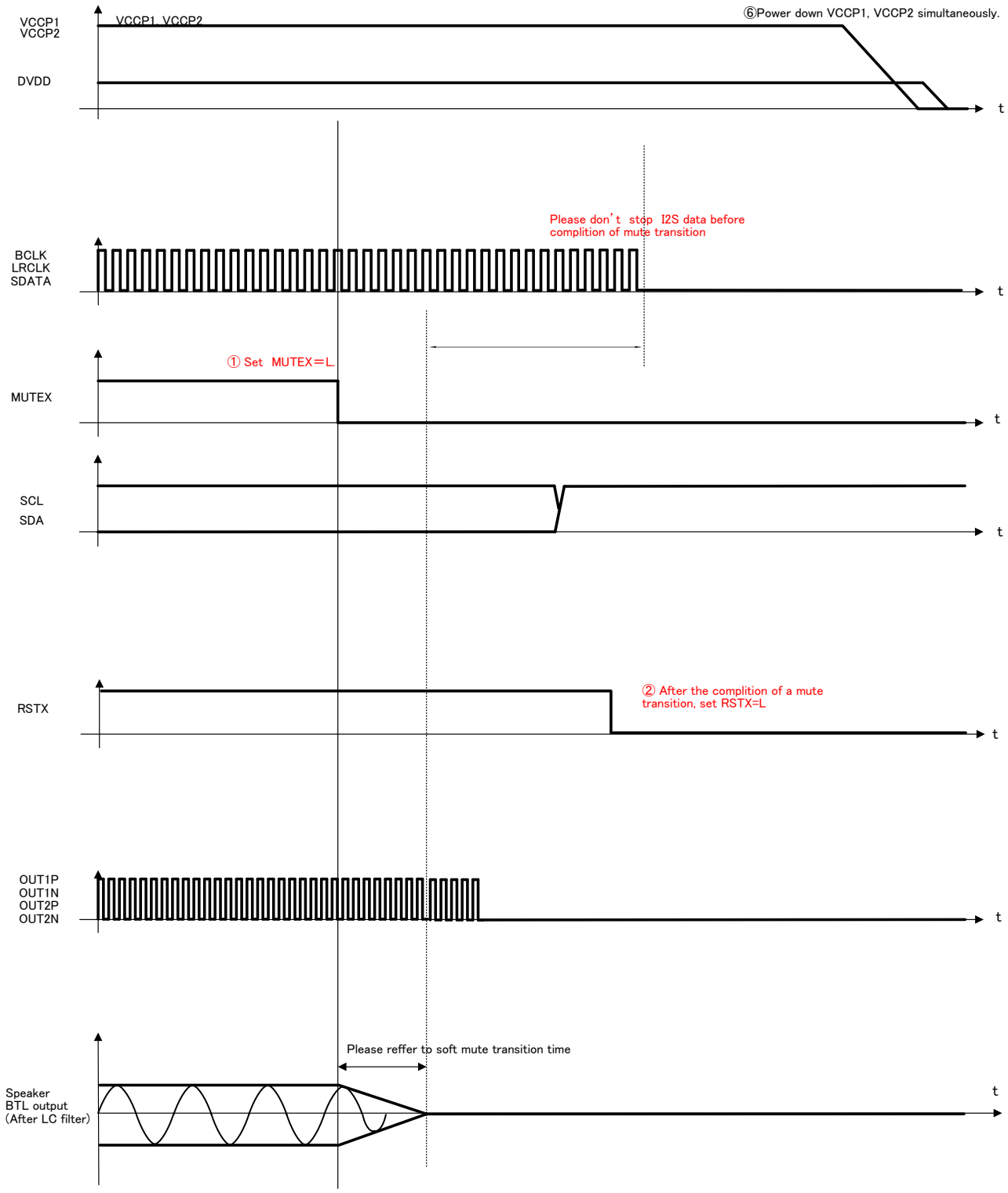
Power supply start-up sequence



※To avoid POP noise or canceling error protection of IC, please set RSTX is L⇒H before MUTEX is L⇒H regularly.

Figure 43.

Power supply shut-down sequence



※To avoid POP noise or canceling error protection of IC, please set MUTEX is H⇒L and keep mute transition time before RSTX is H⇒L regularly.

Figure 44.

About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR output
Output short protection	Detecting condition	Detecting current = 7.2A (TYP.)	HiZ_Low (Latch) (Note 2)	L (Latch)
DC voltage protection	Detecting condition	PWM output Duty=0% or 100% for 12μsec(TYP)and over	HiZ_Low (Latch) (Note 2)	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	HiZ_Low	L
	Releasing condition	Chip temperature to be below 120℃ (TYP.)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 7.0V (TYP.)	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 7.5V (TYP.)	Normal operation	
Clock stop protection	Detecting condition	BCLK signal have stopped among constant period. LRCLK signal have stopped among constant period. BCLK frequency is under constant value. BCLK frequency is over constant value. Please refer to chapter 6 about constant value.(Note 1)	HiZ_Low	H
	Releasing condition	LRCLK signal haven't stopped among constant period and BCLK continues 30 or more msec of condition within constant frequency.	Normal operation	

(Note 1) The ERROR pin is Nch open-drain output.
(Note 2) Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.
The following procedures ① or ② is available for recovery.
①After MUTEX pin is made Low once over the soft mute transition time, MUTEX pin is returned to High again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

1) Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set Low once over the soft mute transition time(see page 15/80), MUTEX pin is returned to High again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

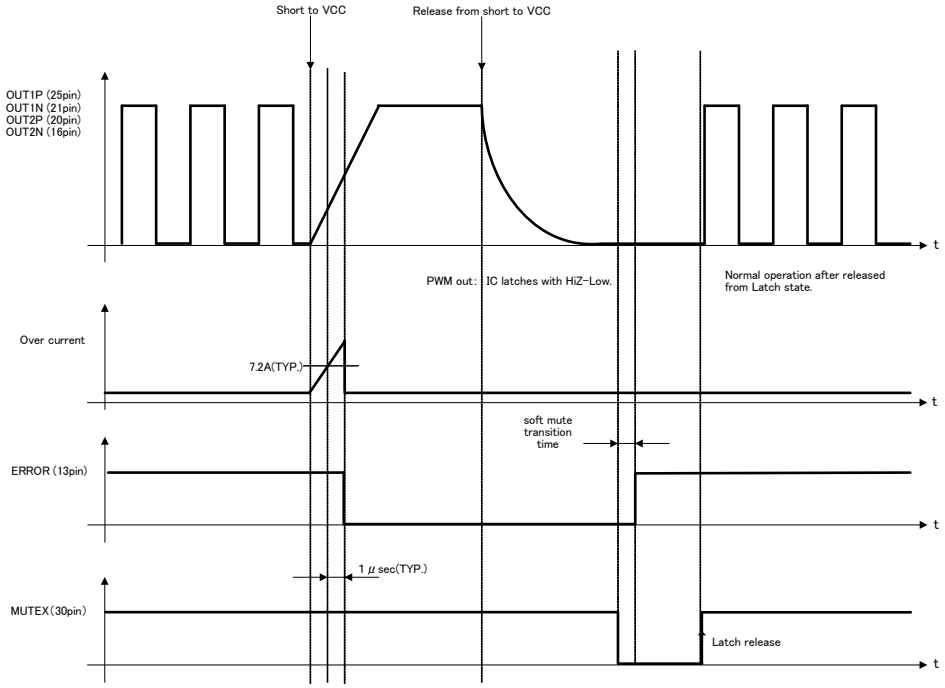


Figure 45.

2) Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(see page 15/76), MUTEX pin is returned to High again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

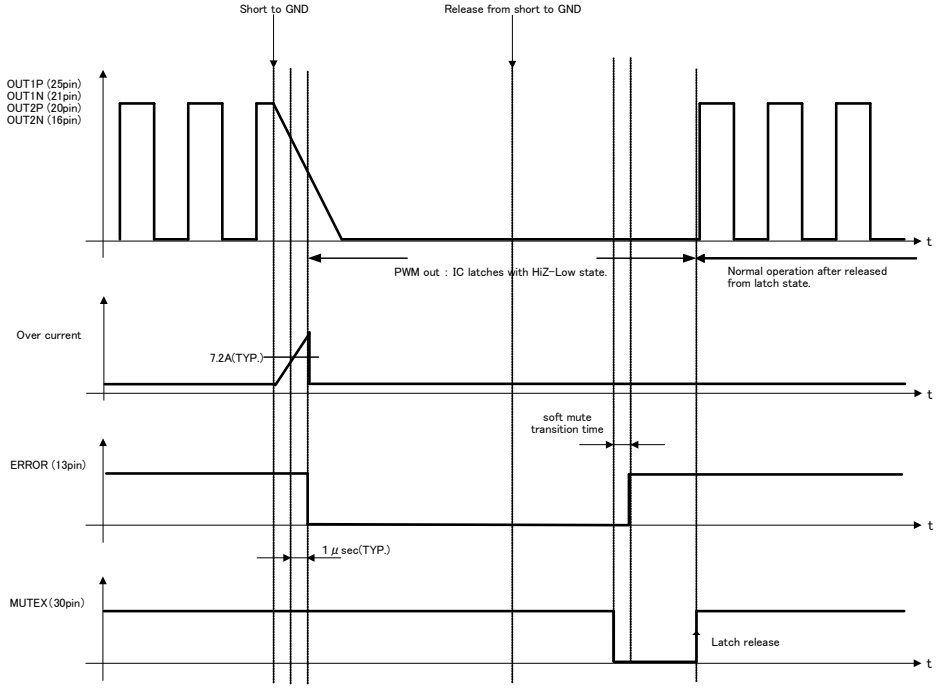


Figure 46.

3) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High and PWM output Duty=0% or 100% over 12μsec.(fs=48kHz) Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(see page 15/76), MUTEX pin is returned to High again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

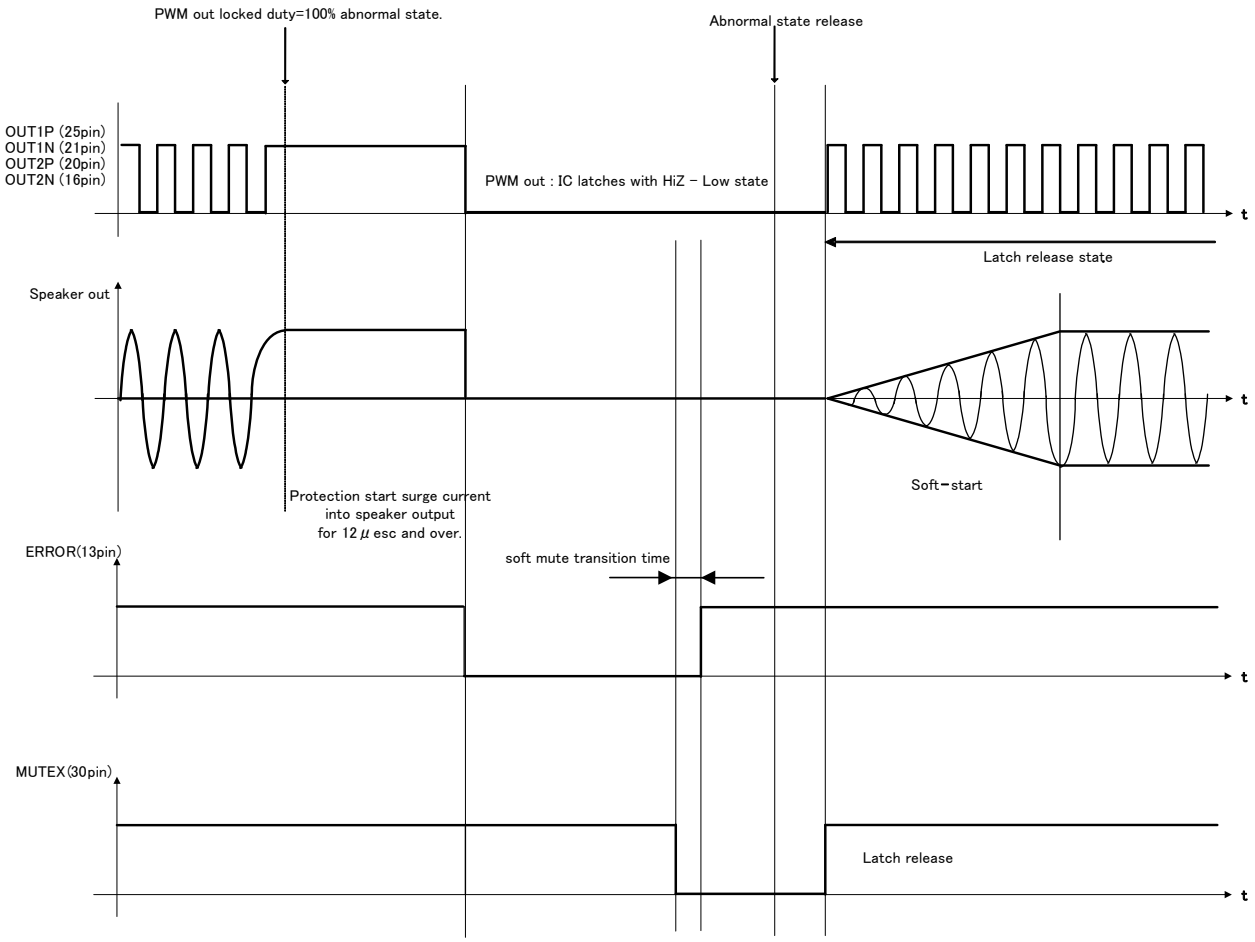


Figure 47.

4) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150℃(TYP.) or more. The speaker output is muted when detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120℃ (TYP.) or less. The speaker output is outputted when released.

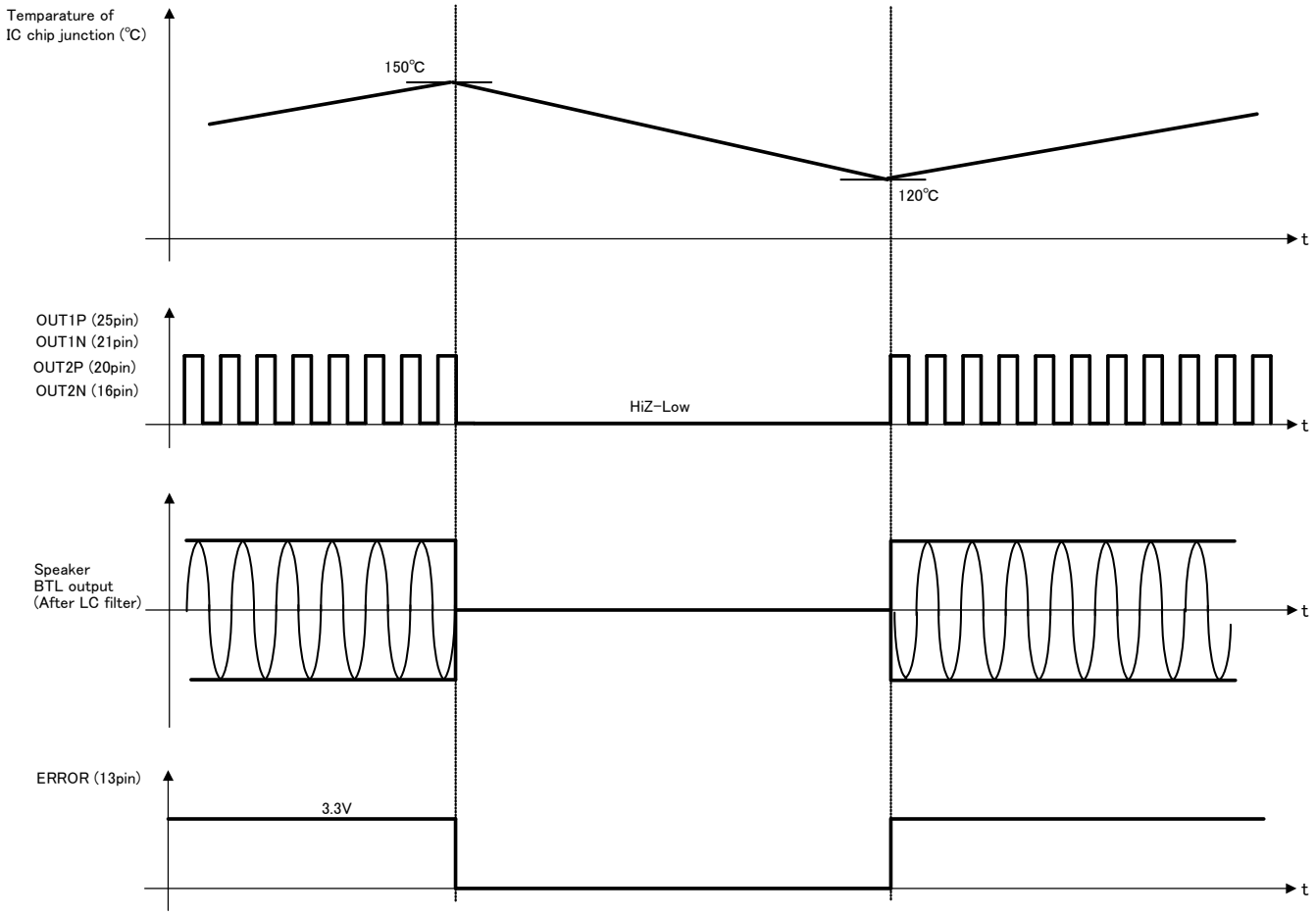


Figure 48.

5) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 7.0V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes more than 7.5V. The speaker output is outputted when released.

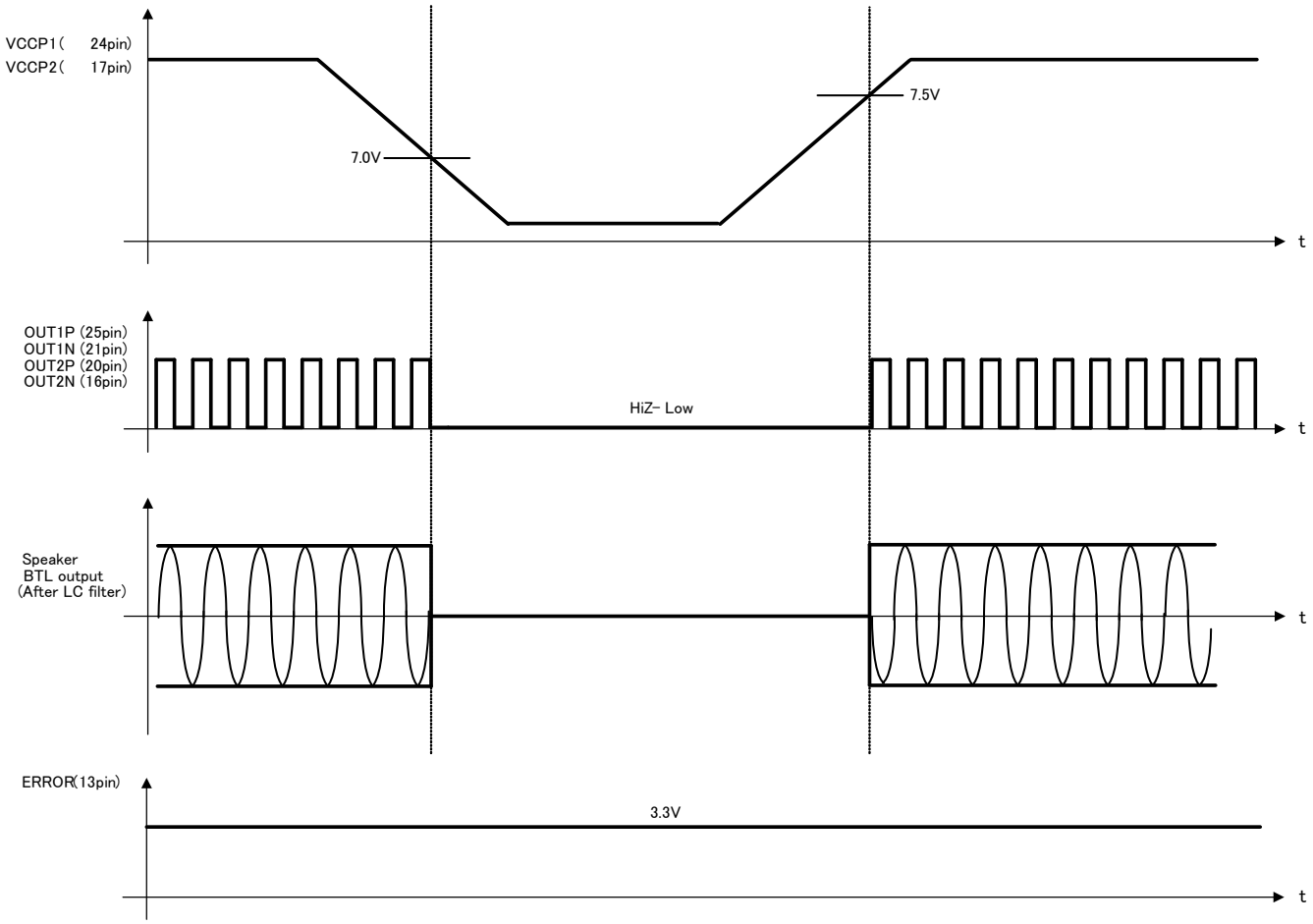


Figure 49.

6) Clock stop protection

This IC has the clock stop protection circuits that make the speaker output mute when the BCLK and LRCLK frequency of the digital sound input are decreased or low frequency.

Detecting condition - BCLK frequency is low or stop, LRCLK frequency is stop. The speaker output is muted.

Releasing condition - BCLK and LRCK are OK over 60msec (max).

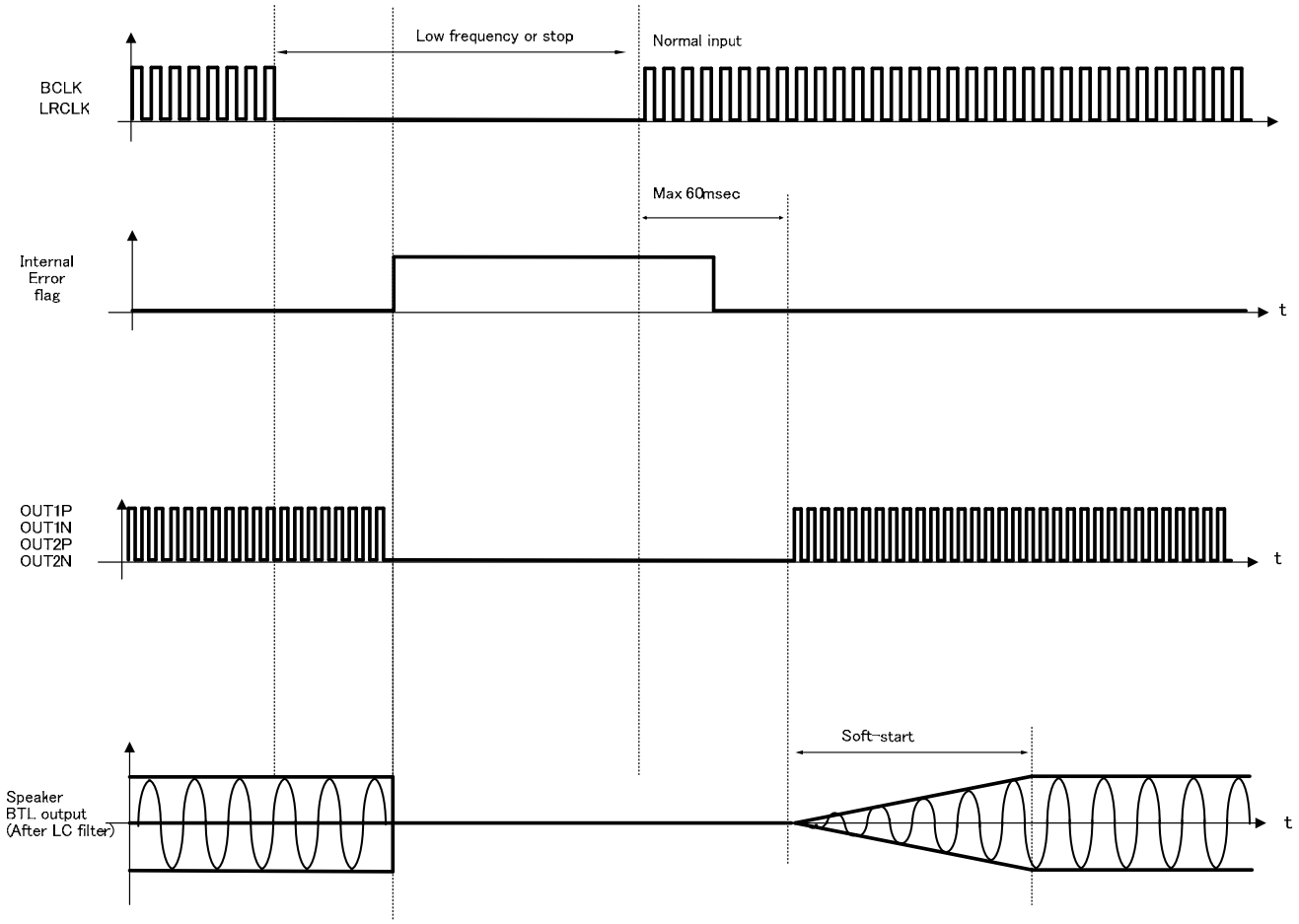


Figure 50.

Functional descriptions of DSP Block

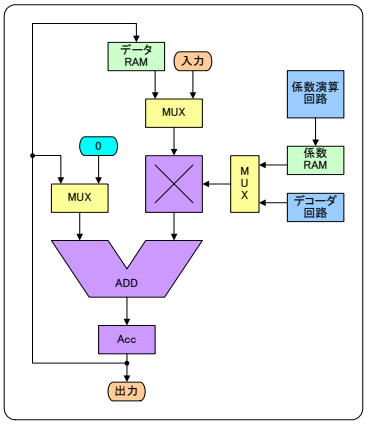
1. Digital Sound Processing(DSP)

The digital sound processing (DSP) part of BM28720 is composed of the special hard ware which is the optimal for FPD-TV, the Mini/Micro Compo. BM28720MUV does the following processing using this special DSP.

Pre-scaler, Channel mixer, 12 Band P-EQ, Fine Master Volume, 3 Band DRC, Fine Post-scaler, DC cutHPF, Hard Clipper

The outline and signal flow of the DSP part

Data width:	32 bit (DATA RAM)
Machine cycle:	20.3ns (1024fs, fs=48kHz)
Multiplier:	32×24 → 56 bit
Adder:	56+56 → 56 bit
Data RAM:	512×32 bit
Coefficient RAM:	512×24 bit
Sampling frequency :	fs=32k,44.1k,48kHz



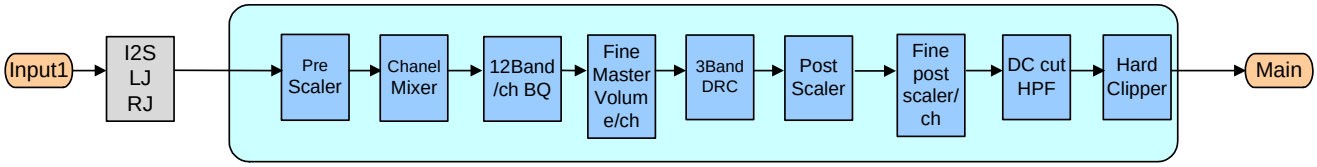


Figure 51.

The digital signal from 16 bits to 24 bits is inputted to the DSP but extends 8bit(+48dB) as the overflow margin to the upper side. When doing the processing which exceeds this range, it processes a clip in the DSP. Incidentally, in case of the 2nd IIR-type (BQ) filter which is often used generally as the digital filter, because it consumes a lot of overflow margins, the output of the multiplier and the adder inside needs note.

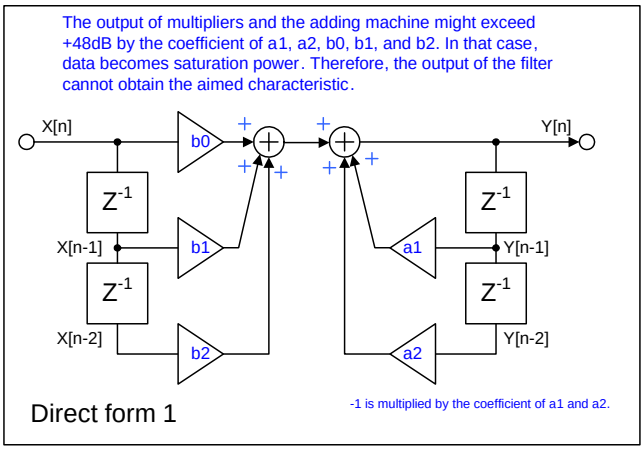


Figure 52.

The management of audio data is as follows by each block.

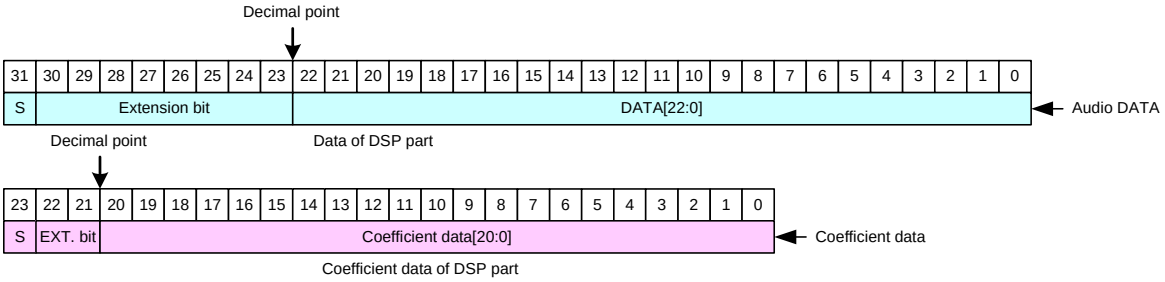


Figure 53.

1-1. Bypass

It passes in the each function of the DSP by the command. Because it left the set value of the each function can be passed in, it is possible to do the confirmation of ON/OFF of the sound effect easily.
The effect which is possible about the bypass, 1) 10Band BQ, 2) 10Band DRC and the whole DSP can be passed.

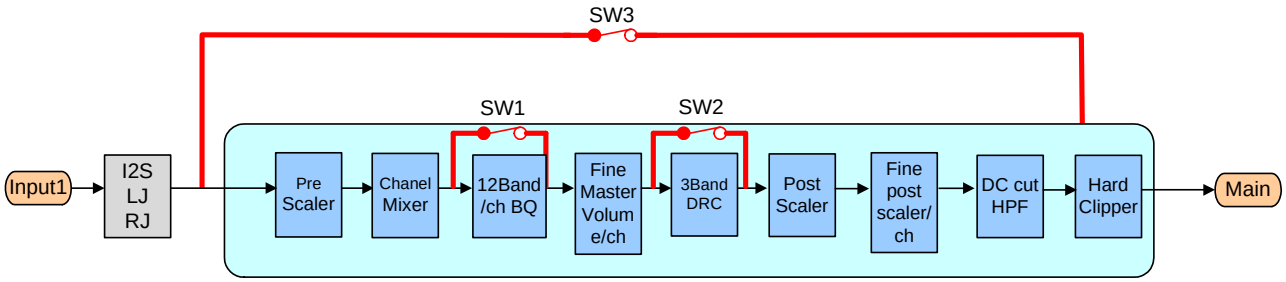


Figure 54.

Default = 00h

Select Address	bit	Explanation of operation (*) '1' bypasses each function.
&h02 [2:0]	2	Bypass of 12Band BQ (SW1) 0:Normal 1:Bypass
	1	Bypass of 3band DRC (SW2) 0:Normal 1:Bypass
	0	Bypass of DSP (SW3) 0:Normal 1:Bypass

1-2. Pre-scaler

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-scaler. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch concurrency control)
Pre-scaler doesn't have a soft transfer feature.

Default = 60h

Select Address	Explanation of operation
&h16 [7:0]	

Command Value	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

1-3. Channel setup with a phase inversion function (Channel Mixer 1)

It sets a mixing in the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. It makes a stereo signal a monaural here. Also, the phase-inversion, the mute on each channel can be set.

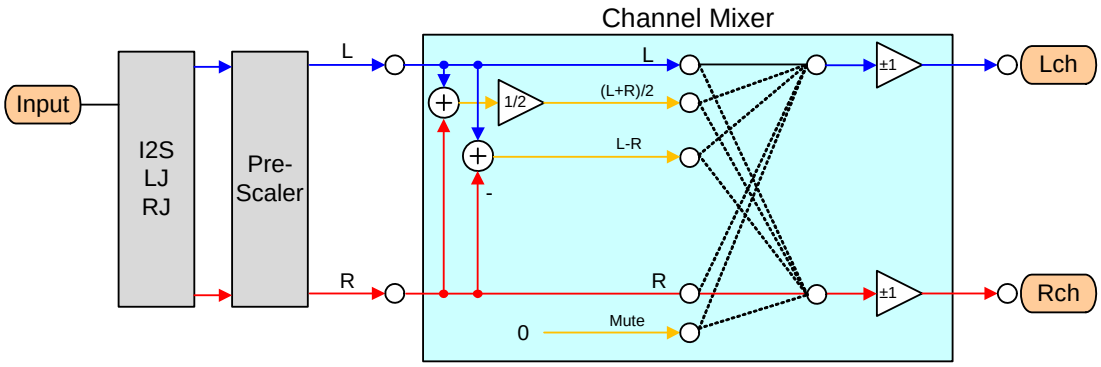


Figure 55.

DSP Input : The data inputted into Lch of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h17[7]	0	Normal
	1	Invert

DSP Input : The data inputted into Lch of DSP is mixed.

Default = 1

Select Address	Value	Explanation of operation
&h17 [6:4]	0	Mute
	1	Lch data input
	2	Rch data input
	3	(Lch + Rch) / 2
	4	Lch-Rch

DSP input: The data inputted into Rch of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h17 [3]	0	Normal
	1	Invert

DSP Input: The data inputted into Rch of DSP is mixed.

Default = 2

Select Address	Value	Explanation of operation
&h17 [2:0]	0	Mute
	1	Lch data input
	2	Rch data input
	3	(Lch + Rch) / 2
	4	Lch-Rch

1-4. Parametric Equalizer

In this IC, the following block has the feature of the parametric equalizer.
12Band BQ, Crossover filter of 3Band DRC block and BQ of the smooth transition.
The shape is used peaking filter, low shelf filter, high shelf filter, lowpass filter, highpass filter, notch filter and all path filters.
Setting the coefficient of the digital filter in the IC by transmit to the coefficient RAM via command. 12Band BQ have the soft transfer feature. Incidentally, the detailed order of the parameter setting refers to the following PEQ setting method.

Select of PEQ independence or synchronous setting

Default = 0h

Select Address	Value	Explanation of operation
&h60 [4]*	0	L/R common setting
	1	L/R independence setting

*&h60[4] setting note.
Please re-set all the parametric equalizers when you change the setting of &h60[4].
The parametric equalizers for which the re-setting is necessary are 18 (BQ1-12, DRC1,DRC2,and DRC3).

Select of smooth transition

Default = 0h

Select Address	Value	Explanation of operation
&h53 [6]	0	Use smooth transition
	1	Not use smooth transition

Select of PEQ soft transition independent setting(This needs to set if &h60[4] is set to 1.)

Default = 0h

Select Address	Value	Explanation of operation
&h51 [7]*	0	Transmit to Lch
	1	Transmit to Rch

Select of PEQ soft transition Band

Default = 0h

Select Address	Explanation of operation
&h51 [4:0]*	

Command	PEQ	Command	PEQ
00	12BAND(1)	0A	12BAND(11)
01	12BAND(2)	0B	12BAND(12)
02	12BAND(3)		
03	12BAND(4)		
04	12BAND(5)		
05	12BAND(6)		
06	12BAND(7)		
07	12BAND(8)		
08	12BAND(9)		
09	12BAND(10)		

Setting of smooth transition time

Default = 3h

Select Address	Value	Explanation of operation
&h53 [3:2]	0	2.7ms
	1	5.3ms
	2	10.7ms
	3	21.3ms

Setting of smooth transition wait time

Default = 0h

Select Address	Value	Explanation of operation
&h53 [1:0]	0	2.7ms
	1	5.3ms
	2	10.7ms
	3	21.3ms

Transfer start setting to coefficient RAM

Default = 0

Select Address	Value	Explanation of operation
&h57 [0]	0	Transfer stop
	1	Transfer start (After transferring is completed, it becomes 0 by the automatic operation.)

Setting of smooth transition start

Default = 0

Select Address	Value	Explanation of operation
&h58 [0]	0	Stop the smooth transition operation
	1	Start the smooth transition operation (After the transition is completed, it becomes 0 by the automatic operation)

* This register cannot read-out.

Read-out smooth transition status

Select Address	Explanation of operation
&h59 [0]	"1" is read while software is changing. "0" is read usually.

[Attention] The data of coefficient RAM can be read. Set values such as F, Q, and Gain cannot be read.

1-5. Volume

Volume is from+24dB to -103dB, and can be selected by the step of 0.125dB. And it is possible to be setting of -∞dB, too. At the time of switching of Volume, smooth transition is performed. Soft transition duration is optional with the command. L/R synchronous or L/R independent can be selected by &h10[7].

It becomes the following formula at the transition from AdB to BdB. C is smooth transition duration selected by &h15[7:6] command.

$$\text{Transition time} = \left| \left(10^{\frac{A}{20}} - 10^{\frac{B}{20}}\right) * C \right| \text{ ms}$$

Setting of soft transition time

Default = 0

Select Address	Value	Explanation of operation
&h15 [7:6]	0	21.3ms
	1	42.7ms
	2	85.3ms

Lch/common volume setting

Default = FFh

Select Address	Explanation of operation
&h11 [7:0]	

Command	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	-0.5dB
32	-1dB
⋮	⋮
FE	-103dB
FF	-∞

Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125dB carving.
When L/R synchronous volume setting, &11[7:0] is enable.
When L/R independent volume setting, &11[7:0] is the volume setting of Lch.

Lch/common fine volume setting

Default = 0h

Select Address	Value	Explanation of operation
&h10 [1:0]	0	0dB
	1	-0.125dB
	2	-0.25dB
	3	-0.375dB

【Note1】
It is possible to use with the 0.5-dB step in changing only &h11[7:0] when &h10[1:0]=0.

The Lch/Rch independent volume setting and the synchronous volume setting can be selected by &h10[7] command.
When Lch/Rch independent volume set, the volume setting of Lch is the setting of &h10[1:0] and &h11, and the volume setting of Rch is the settings of &h10[5:4] and &h13.

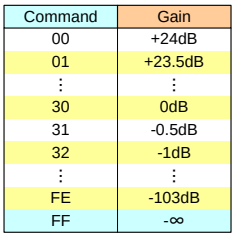
Setting of Lch/Rch independent volume

Default = 0

Select Address	Value	Explanation of operation
&h10[7]	0	Lch/Rch common volume setting
	1	Lch/Rch independent volume setting

Setting of volume (Setting of Rch volume, It is enable only to set an independent volume.)

Default = FFh

Select Address	Explanation of operation
&h12 [7:0]	

Command	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	-0.5dB
32	-1dB
⋮	⋮
FE	-103dB
FF	-∞

Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125dB carving.

Setting of fine volume (Setting of Rch fine volume, It is enable only to set an independent volume.)

Default = 0h

Select Address	Value	Explanation of operation
&h10 [5:4]	0	0dB
	1	-0.125dB
	2	-0.25dB
	3	-0.375dB

【Note2】
It is possible to use with the 0.5-dB step in changing only &h13[7:0] when &h10[5:4]=0.

【Note3】
It is possible to use with the 0.125-dB step in setting both &h10[1:0] and &h11[7:0].
In case of &h10[1:0]=0, it becomes the set value of &h11[7:0].
In case of &h10[1:0]=1, it becomes the -0.125dB set value of &h11[7:0].
In case of &h10[1:0]=2, it becomes the -0.25dB set value of &h11[7:0].
In case of &h10[1:0]=3, it becomes the -0.375dB set value of &h11[7:0].
Because it is fixed by the transfer of &h11 in any case, the soft transfer can be beforehand begun in the set value for the direct following of the purpose in setting &h11 after setting in &h10.
&h10[5:4] is the same function as &h10[1:0], &h13 is the same function as &h11 when Lch/Rch independently set for Rch.

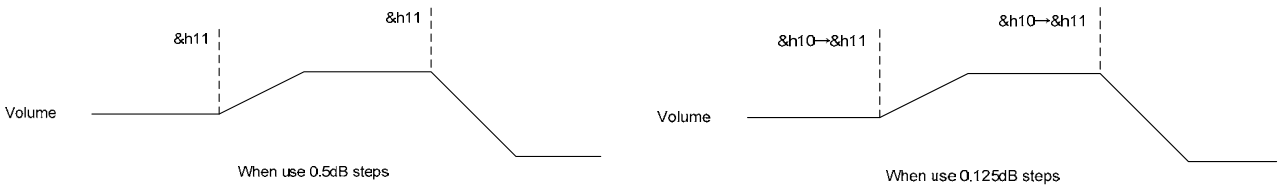


Figure 56.

1-6. 3 band DRC

This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.
There are three kinds of DRC (DRC1, DRC2, and DRC3), and no clip can be output to each three BAND.
DRC1, DRC2 and DRC3 can set up two threshold value levels. Moreover, it is possible to also change slope.

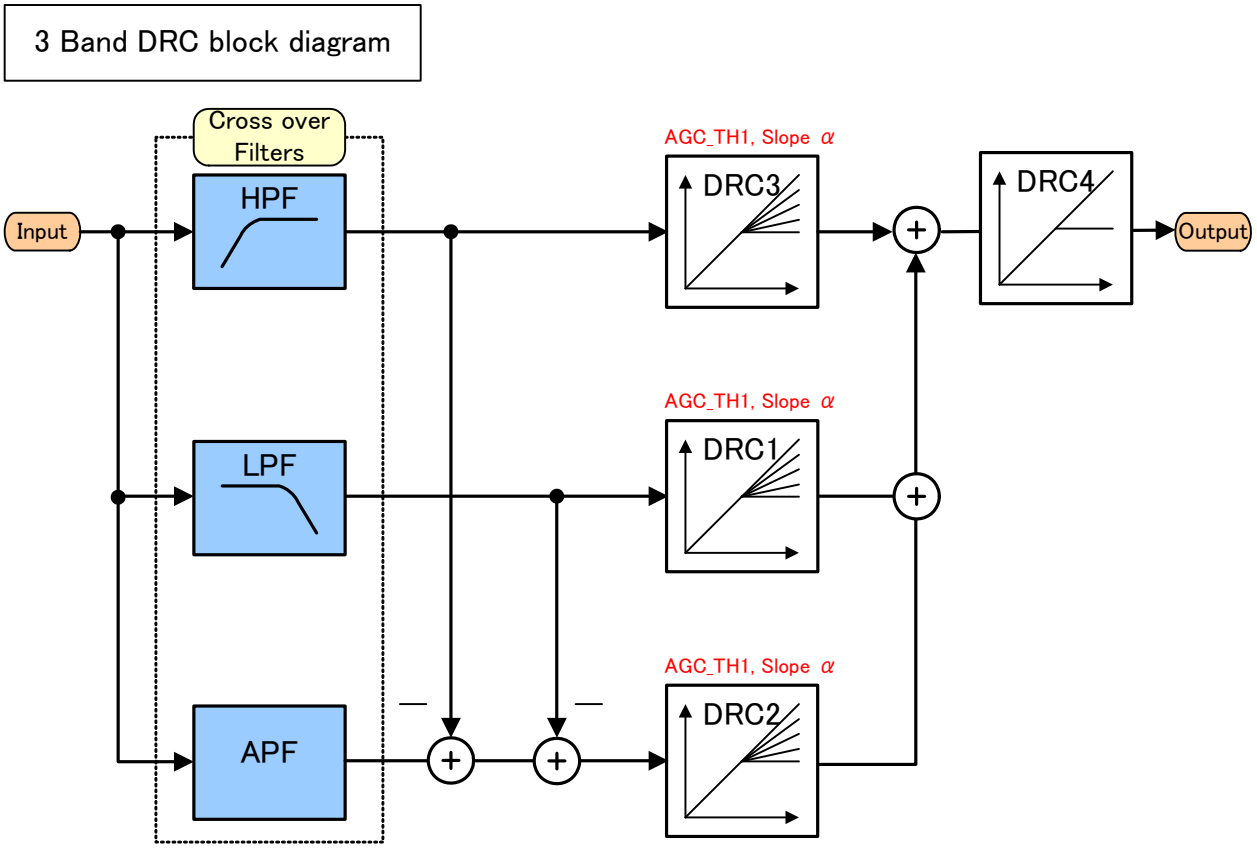


Figure 57.

DRC transition figure

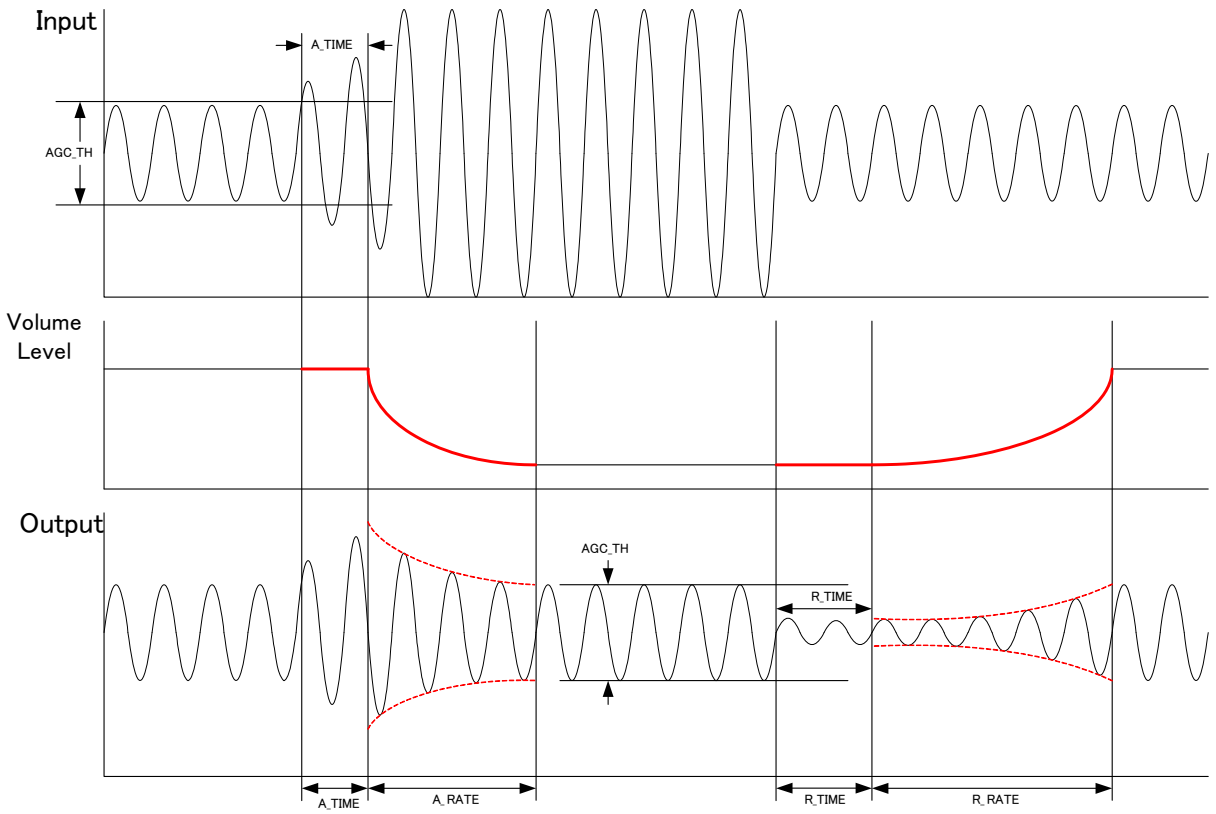


Figure 58.

DRC input-and-output gain characteristics

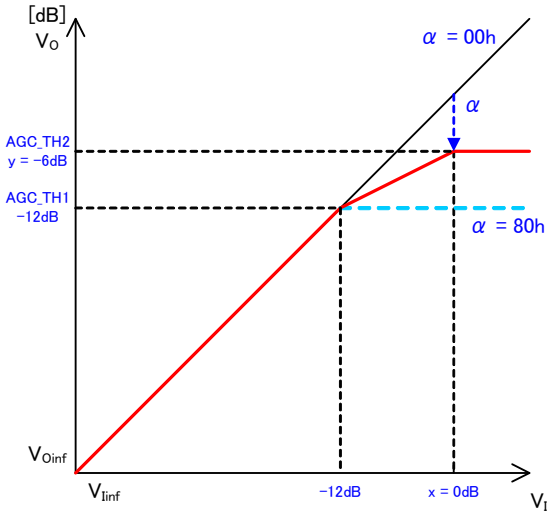


Figure 59.

The formula which asks for Slope alpha is described below.

Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

α = 85.266 → 55_H

55_H calculated is set as &h25 or &h2A

Volume Curve

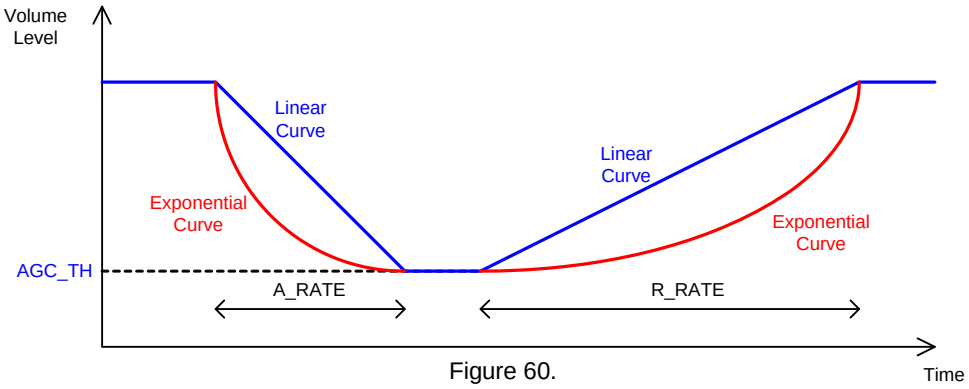


Figure 60.

DRC1 ON/OFF setting of slope variable function.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [7]	0	Not use
	1	Use

DRC1 ON/OFF setting of compressor

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [6]	0	Not use
	1	Use

DRC2 ON/OFF setting of slope variable function.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [5]	0	Not use
	1	Use

DRC2 ON/OFF setting of compressor

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [4]	0	Not use
	1	Use

DRC3 ON/OFF setting of slope variable function.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [3]	0	Not use
	1	Use

DRC3 ON/OFF setting of compressor

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [2]	0	Not use
	1	Use

DRC4 ON/OFF setting of compressor

OFF is through output.

Default = 0

Select Address	Value	Explanation of operation
&h3F [4]	0	Not use
	1	Use

The volume curve at the time of an attack (A_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h21[7]	0	Linear curve
	1	Exponential curve

The volume curve at the time of a release (R_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h21 [6]	0	Linear curve
	1	Exponential curve

The choice of the DRC composition

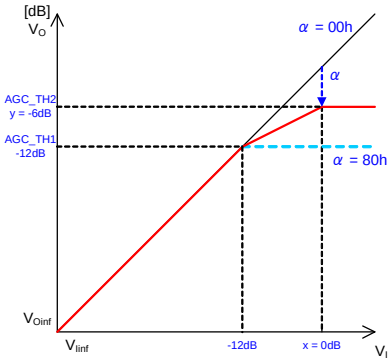
It uses a standard in 3Band DRC but it is possible to use as 1Band DRC, too.
To make the composition of 1Band DRC, it chooses through setting in HPF, LPF and APF.

To set the crossover filter (HPF, LPF and APF) which divides the frequency band of 3Band DRC, therefore, it is referred to the chapter 1-4.

Slope (α) setting of DRC1, DRC2, and DRC3

DRC1, DRC2 and DRC3 are individually setting.

Default = 80h

Select Address	Explanation of operation
DRC1 &h29 [7:0] DRC2 &h31 [7:0] DRC3 &h39 [7:0]	 The formula which asks for Slope alpha is described below. alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$ TH is AGC_TH1. x is input level. y is output level. Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$ $\alpha = 85.266 \rightarrow 55_H$ 55H calculated is set as &h29 or &h31

AGC_TH1 setting of DRC1, DRC2, and DRC3

DRC1, DRC2 and DRC3 are individually setting.

Please set below to the setting value of AGC_TH2.

Default = 40h

Select Address	Explanation of operation
DRC1 &h28 [6:0] DRC2 &h30 [6:0] DRC3 &h38 [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

AGC_TH2 setting of DRC1, DRC2, DRC3, and DRC4

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = 40h

Select Address	Explanation of operation
DRC1 &h2C [6:0] DRC2 &h34 [6:0] DRC3 &h3C [6:0] DRC4 &h40 [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

A_RATE setting of DRC1, DRC2, DRC3, and DRC4

(It is the transition time of a compression curve at the time of an attack.)

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = 3h

Select Address	Explanation of operation
Slope function of DRC1 &h2A [6:4] Slope function of DRC2 &h32 [6:4] Slope function of DRC3 &h3A [6:4] Compressor of DRC1 &h2E [6:4] Compressor of DRC2 &h36 [6:4] Compressor of DRC3 &h3D [6:4] Compressor of DRC4 &h41 [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

R_RATE setting of DRC1, DRC2, DRC3, and DRC4 (It is the transition time of an extension curve at the time of release.)

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = Bh

Select Address	Explanation of operation
Slope function of DRC1 &h2A [3:0] Slope function of DRC2 &h32 [3:0] Slope function of DRC3 &h3A [3:0] Compressor of DRC1 &h2E [3:0] Compressor of DRC2 &h36 [3:0] Compressor of DRC3 &h3D [3:0] Compressor of DRC4 &h41 [3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME1 setting of DRC1, DRC2, DRC3, and DRC4 (Detection time setting of attack operation)

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = 1h

Select Address	Explanation of operation
Slope function of DRC1 &h2B [7:4] Slope function of DRC2 &h33 [7:4] Slope function of DRC3 &h3B [7:4] Compressor of DRC1 &h2F [7:4] Compressor of DRC2 &h37 [7:4] Compressor of DRC3 &h3E [7:4] Compressor of DRC4 &h42 [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC1, DRC2, DRC3, and DRC4 (Detection time setting of release operation)

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = 3h

Select Address	Explanation of operation
Slope function of DRC1 &h2B [2:0] Slope function of DRC2 &h33 [2:0] Slope function of DRC3 &h3B [2:0] Compressor of DRC1 &h2F [2:0] Compressor of DRC2 &h37 [2:0] Compressor of DRC3 &h3E [2:0] Compressor of DRC4 &h42 [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

【Question】
Recommendation value setting of 3 bands DRC？

【Answer】
The recommendation value of 3 band DRC was examined to speaker protection using FPD TV.
・A_RATE : 4ms
・R_RATE : 2s or more
・A_TIME : 0.5ms
・R_TIME : 50ms or more
It is not uncomfortable to a music source to arrange all DRC (DRC1, DRC2 and DRC3) with the same value.

【Question]
When master volume is increased, why is it that only the sound of a high region becomes large?
【Answer】
It investigated about the cross over frequency and the relation of AGC_TH2 of DRC for high frequency band.
Its sound energy decreases, so that music data becomes high frequency. When a cross over frequency is set up highly, unless it lowers AGC_TH2 of DRC for high frequency band, when master volume is increased, the effect by limit cannot be heard.

The red line shows the Peak level.

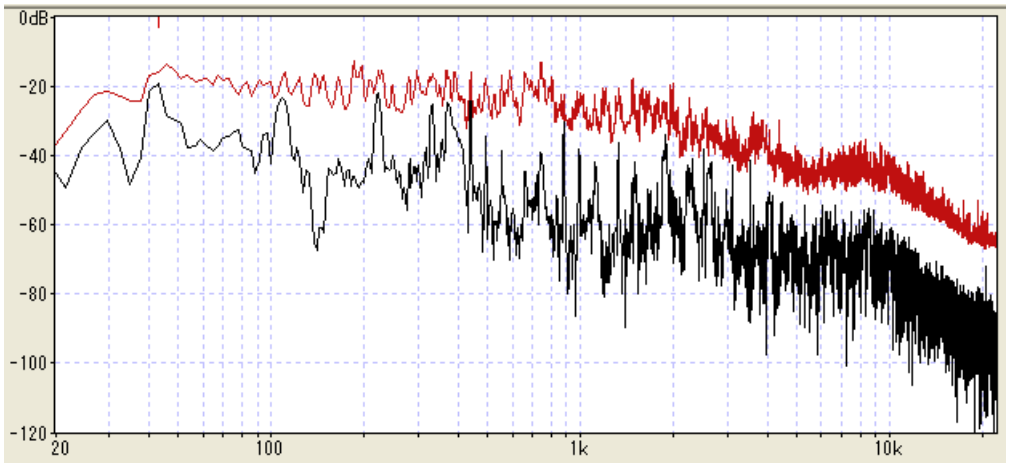
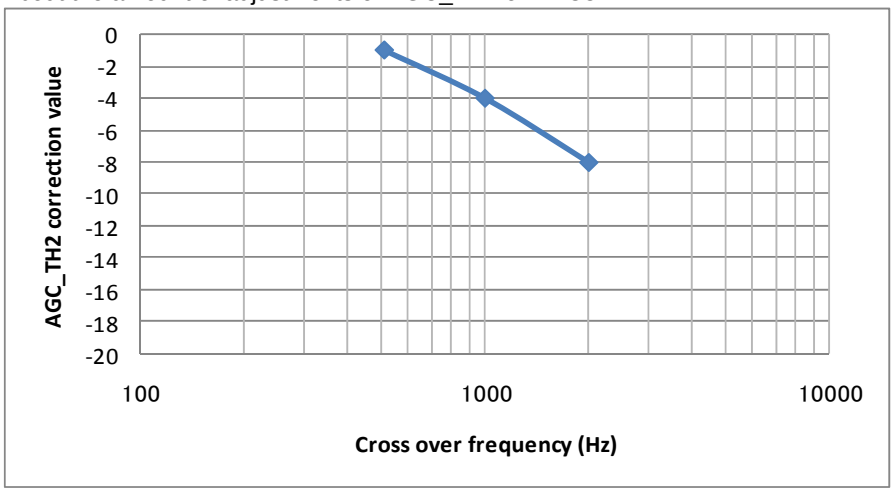


Figure 61.

About the amount of adjustments of AGC_TH2 of DRC3.



Please use as a standard of the adjustment value from AGC_TH2 value of DRC for low frequency band.
Moreover, the amount of adjustments decreases by setting up a cross over frequency lowness.

Figure 62.

1-7. Post-scaler

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-scaler. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch concurrency control)
Pre-scaler doesn't have a soft transfer feature.

Default = 60h

Select Address	Explanation of operation
&h13 [7:0]	

Command Value	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

1-8. Fine Post-scaler

An adjustable range can be set up at a 0.1dB step from +0.7dB to –0.8dB. Fine Post-scaler does not have a smooth transition function.
(Independent control of Lch/Rch.)

Default=8h

Select Address	Explanation of operation
Lch &h14 [7:4] Rch &h14 [3:0]	

Command	Gain	Command	Gain
0	-0.8dB	8	0dB
1	-0.7dB	9	+0.1dB
2	-0.6dB	A	+0.2dB
3	-0.5dB	B	+0.3dB
4	-0.4dB	C	+0.4dB
5	-0.3dB	D	+0.5dB
6	-0.2dB	E	+0.6dB
7	-0.1dB	F	+0.7dB

1-9. Hard Clipper

When measuring the rated output of the television, THD+N measures in 10%. It can be made to clip with any output amplitude by using a clipper function. For example, the rated output of 10W or 5W can be gained using the amplifier of 15W output.

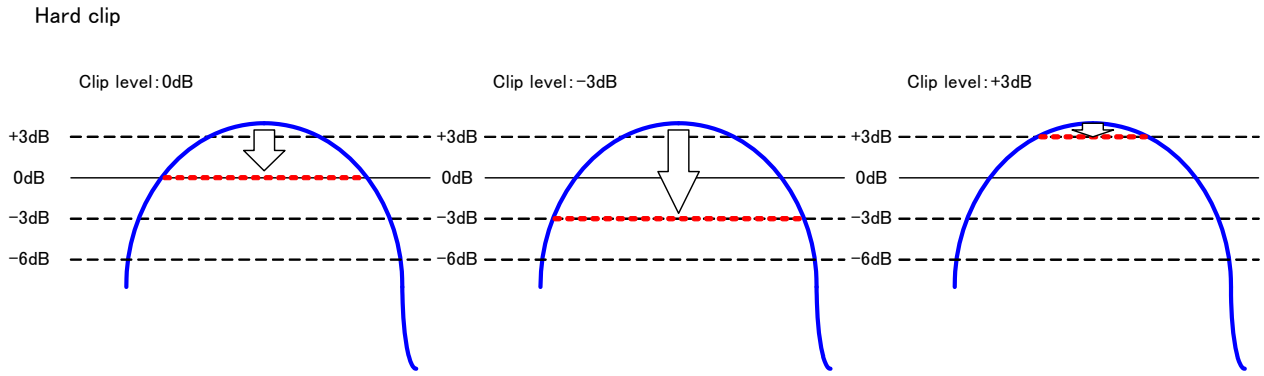


Figure 63.

Clipper setting
Default = 1

Select Address	Value	Explanation of operation
&h1A [0]	0	Clipper function is not used.
	1	Hard clipper function is used.

Clip level selection

Default = E1h

Select Address	Explanation of operation
&h1B [7:0]	Command / Gain

Command	Gain
00	-22.5dB
⋮	⋮
E0	-0.1dB
E1	0dB
E2	+0.1dB
⋮	⋮
FF	+3dB

1-10. DC cut HPF (Back)

DC offset element of the digital signal outputted from audio DSP is cut by this HPF.
The cutoff frequency fc of HPF uses the 1Hz filter, and the degree uses the first-order filter.

Default = 1

Select Address	Value	Explanation of operation
&h18 [0]	0	Not use
	1	Use

1-11. RAM clear

The data RAM of DSP and coefficient RAM are cleared.
40us or more is required until all the data is cleared.

Clear of the data RAM

Default = 1

Select Address	Value	Explanation of operation
&h01 [7]	0	Normal
	1	Clear operation

Clear of coefficient RAM

Default = 1

Select Address	Value	Explanation of operation
&h01 [6]	0	Normal
	1	Clear operation

1-12. Audio Output Level Meter

It is possible to output the peak level of the PCM data inputted into a PWM processor.
A peak value can be read using the 2-wire command interface as 16 bit data of an absolute value.
The interval holding a peak value can be selected from six steps (50ms step) from 50ms to 300ms.
A peak hold result can be selected from L channel, R channel, and a monophonic channel {(Lch+Rch) /2}.

Audio Output Level Meter block diagram

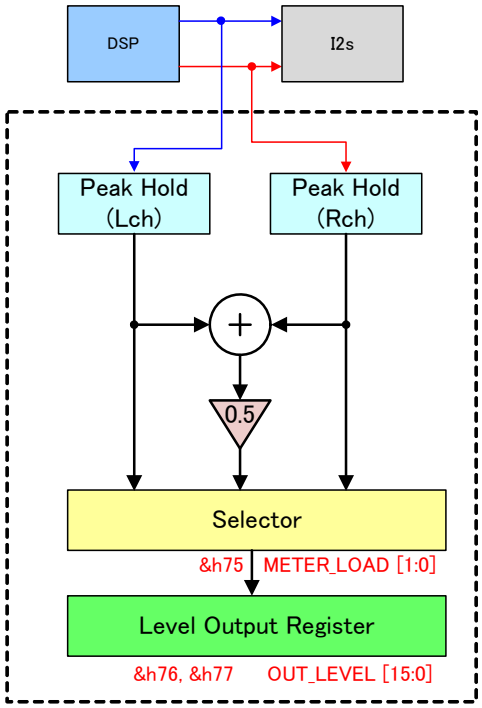


Figure 64.

Setting of the peak level hold time interval of Audio Output Level Meter

Default = 00h

Select Address	Explanation of operation
&h74 [2:0]	

Command	Hold time
0	50ms
1	100ms
2	150ms
3	200ms
4	250ms
5	300ms

The signal of Audio Level Meter read-back is selected.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.

Default = 0

Select Address	Value	Explanation of operation
&h75 [1:0]	0	The peak level of L channel
	1	The peak level of R channel
	2	The peak level of monophonic channel {(Lch+Rch) /2}

Read-back of Audio Output Level
&h76 (upper 8 bits) and a &h77 (lower 8 bits) commands are read for the maximum within the period appointed by the command &h74 using the 2-wire interface.

(Example)
When FFFFh is read, mean 1.0 (0dBFs).
When 8000h is read, mean 0.5 (-6dBFs).

2. Setting and reading method of parametric equalizer

It explains a detailed sequence of the setting method and the reading method of the parametric equalizer separately for usage.

2-1 PEQ coefficient setting

The parametric equalizer consists of Bi-quad filter as follows. Each coeffiect of Bi-quad filter can be written directly. It is S2.21 format, and setting range is -4≦x＜+4.
Moreover, the coefficient address is shown in Table 1.

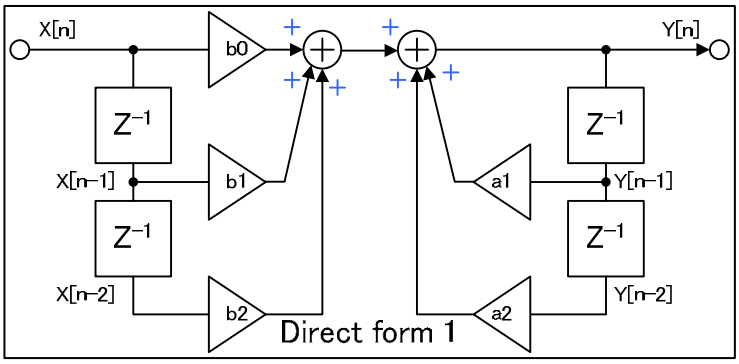


Figure 65.

2-1-1 Writing sequence (It sets up in number order)

1. Address setting (&h61) (*1)Table 1 is referred to.
2. 24bit coefficient Upper[23:16]bit setting (&h62[7:0])
3. 24bit coefficient Middle[15:8]bit setting (&h63[7:0])
4. 24bit coefficient Lower [7:0]bit setting (&h64[7:0])
5. The writing of coefficients is performed. (&h65[0] = 1) (*2)

(*2) After writing complete of coefficients is cleared automatically. It is not necessary to transmit h65[0] =L. Coefficient writing takes about 100µsec.100µsec should not change an address setup and several 24-bit setup after coefficient write-in execution.

(ex) When 0x3DEDE7 is written, same L/Rch, 16band BQ1 b0
1. &h61 = 00h (16band BQ1 b0 is appointed)
2. &h62 = 3Dh (Upper[23:16] is setting)
3. &h63 = EDh (Middle[15:8] is setting)
4. &h64 = E7h (Lower[7:0] is setting)
5. &h65 = 01h (Coefficient transfer) (*3)

(*3) After writing complete of coefficients is cleared automatically.
6. 100µsec or more µsec wait

The writing of other coefficients is performed.

2-1-2 Read-back sequence (It sets up in number order)

1. Address setting (&h61) (*4)Table 1 is referred to.
2. Setting of a read-back register address (&hD0)
3. Read-back of the 24bit coefficient Upper[23:16]bit (&h66[7:0])
4. Read-back of the 24bit coefficient Middle[15:8]bit (&h67[7:0])
5. Read-back of the 24bit coefficient Lower[7:0]bit (&h68[7:0])

2-1-3 When the coefficient of PEQ is set up directly and a soft transition is performed

1. Set PEQ coefficient to soft transition address whose address is 50-54.Please refer to Table1.
   Since in the case of &h60[4]=1(Enable L/R independent setting) and &h53 [5:4] =0 a soft transition is carried out and it is set to LR simultaneous , please write a coefficient in both LR address.
   In the case of &h53[5:4]=1, coefficient is set to only Lch address.
   In the case of &h53[5:4]=2, coefficient is set to only Rch address.
2. Select PEQ Band that is performed soft transition by setting &h51[4:0] address.(Refer to chapter 1-4)
3. &h58[0]=1h：Start soft transition (After the completion of soft transition this register is automatically cleared by 0 h)
4. Wait soft transition completion(about 24msec), or read command &h59 [0], and stand by until it is cleared by 0 h.

Table1. Specified coefficient

&h61[6:0] Value	Select coefficient	&h61[6:0] Value	Select coefficient	&h61[6:0] Value	Select coefficient
00	12BandBQ1 b0	23	12BandBQ8 b0	46	DRC2_1 b0
01	12BandBQ1 b1	24	12BandBQ8 b1	47	DRC2_1 b1
02	12BandBQ1 b2	25	12BandBQ8 b2	48	DRC2_1 b2
03	12BandBQ1 a1	26	12BandBQ8 a1	49	DRC2_1 a1
04	12BandBQ1 a2	27	12BandBQ8 a2	4A	DRC2_1 a2
05	12BandBQ2 b0	28	12BandBQ9 b0	4B	DRC2_2 b0
06	12BandBQ2 b1	29	12BandBQ9 b1	4C	DRC2_2 b1
07	12BandBQ2 b2	2A	12BandBQ9 b2	4D	DRC2_2 b2
08	12BandBQ2 a1	2B	12BandBQ9 a1	4E	DRC2_2 a1
09	12BandBQ2 a2	2C	12BandBQ9 a2	4F	DRC2_2 a2
0A	12BandBQ3 b0	2D	12BandBQ10 b0	50	Smooth BQ b0
0B	12BandBQ3 b1	2E	12BandBQ10 b1	51	Smooth BQ b1
0C	12BandBQ3 b2	2F	12BandBQ10 b2	52	Smooth BQ b2
0D	12BandBQ3 a1	30	12BandBQ10 a1	53	Smooth BQ a1
0E	12BandBQ3 a2	31	12BandBQ10 a2	54	Smooth BQ a2
0F	12BandBQ4 b0	32	12BandBQ11 b0	55	DRC3_1 b0
10	12BandBQ4 b1	33	12BandBQ11 b1	56	DRC3_1 b1
11	12BandBQ4 b2	34	12BandBQ11 b2	57	DRC3_1 b2
12	12BandBQ4 a1	35	12BandBQ11 a1	58	DRC3_1 a1
13	12BandBQ4 a2	36	12BandBQ11 a2	59	DRC3_1 a2
14	12BandBQ5 b0	37	12BandBQ12 b0	5A	DRC3_2 b0
15	12BandBQ5 b1	38	12BandBQ12 b1	5B	DRC3_2 b1
16	12BandBQ5 b2	39	12BandBQ12 b2	5C	DRC3_2 b2
17	12BandBQ5 a1	3A	12BandBQ12 a1	5D	DRC3_2 a1
18	12BandBQ5 a2	3B	12BandBQ12 a2	5E	DRC3_2 a2
19	12BandBQ6 b0	3C	DRC1_1 b0		
1A	12BandBQ6 b1	3D	DRC1_1 b1		
1B	12BandBQ6 b2	3E	DRC1_1 b2		
1C	12BandBQ6 a1	3F	DRC1_1 a1		
1D	12BandBQ6 a2	40	DRC1_1 a2		
1E	12BandBQ7 b0	41	DRC1_2 b0		
1F	12BandBQ7 b1	42	DRC1_2 b1		
20	12BandBQ7 b2	43	DRC1_2 b2		
21	12BandBQ7 a1	44	DRC1_2 a1		
22	12BandBQ7 a2	45	DRC1_2 a2		

When L/R independent, Lch:&h61[7]=0, Rch: &h61[7]=1
When L/R same, &h61[7] is not reflected.

3. The mute function by a terminal

BM28720MUV has a mute function of audio DSP by a terminal.
It is possible to perform mute of the output from Audio DSP by setting a MUTEX terminal to "L."

Transition time setting at the time of mute is as follows.
Smooth transition mute time setting
The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7ms fixed.

Default = 3

Select Address	Value	Explanation of operation
&h15 [1:0]	0	10.7ms
	1	21.4ms
	2	42.7ms
	3	85.4ms

&h15[1:0] Mute time setting

It is only operated by mute terminal.

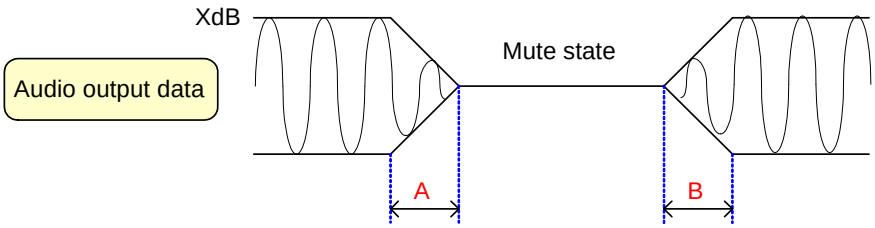


Figure 66.

&h15[1:0] setting

Command	A	B
0	10.7ms	10.7ms
1	21.4ms	10.7ms
2	42.7ms	10.7ms
3	85.4ms	10.7ms

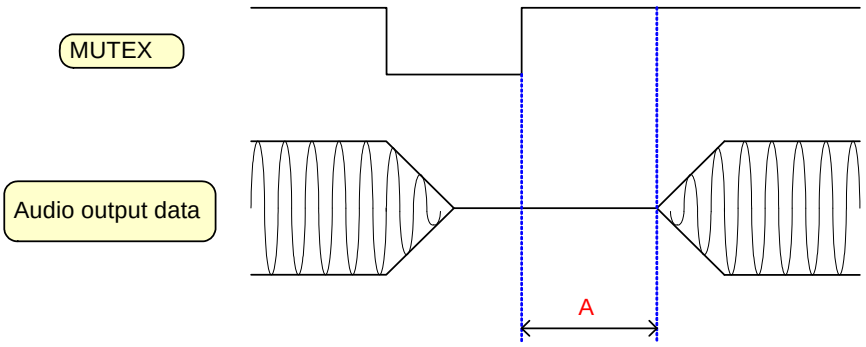
Smooth transition mute release time setting

Time after detecting mute release until it actually begins mute release operation is set up.

Default = 0

Select Address	Value	Explanation of operation
&h15 [5:4]	0	0ms
	1	100ms
	2	200ms
	3	300ms

Operation of mute delay &h15[5:4]



Command	A
0	0ms
1	100ms
2	200ms
3	300ms

Figure 67.

【Question】

When mute release is performed, what happens during mute operation?
Moreover, when there is release delay time, what happens?

【Answer】

When mute release is performed during mute operation, mute release operation is started in an instant.
(When delay setting is 0) Return time at this time becomes shorter than mute release time (for example, 10ms).
Next, when there is setting of release delay time, a delay timer starts a count from the time of performing mute release, and mute release operation is started after delay time completing.
When mute release time setting is set to 10ms, it is designing so that a mute release curve may draw f curve.

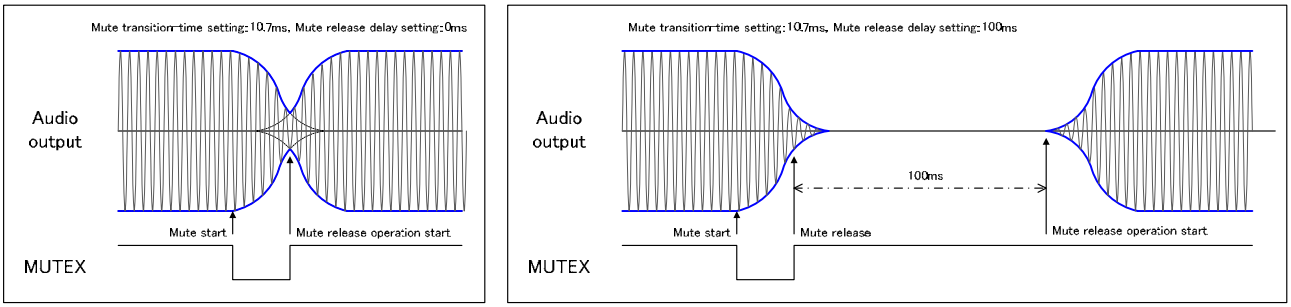


Figure 68.

4. Small signal input detection function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set. Setting of a detection level and detection time can be performed.
If the signal below a setting detection level continues in both L channel and R channel, a small signal detection flag will become "H". A detection result can be read from command &h72 [2:0].
The point which acts as a monitor of the small signal becomes input data of audio DSP block.

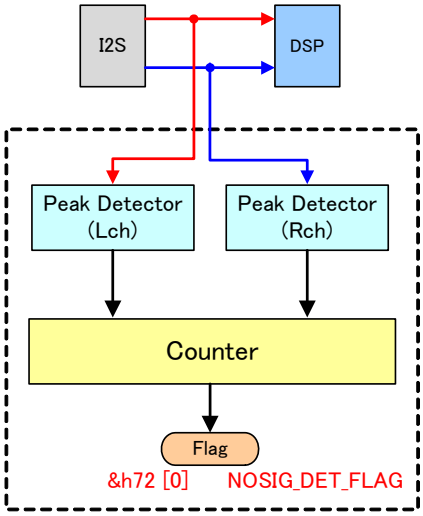


Figure 69.

Detection level setting

Default = 00h

Select Address	Explanation of operation

Command	Level	Command	Level	Command	Level
00	-∞	08	-77dB	10	-69dB
01	-96dB	09	-76dB	11	-68dB
02	-92dB	0A	-75dB	12	-67dB
03	-88dB	0B	-74dB	13	-66dB
04	-84dB	0C	-73dB	14	-65dB
05	-80dB	0D	-72dB	15	-64dB
06	-79dB	0E	-71dB	16	-62dB
07	-78dB	0F	-70dB	17	-60dB

Detection time setting

Default = 0

Select Address	Value	Explanation of operation
&h71 [1:0]	0	42.7ms
	1	85.4ms
	2	170.7ms
	3	341.4ms

* Sampling frequency is value of Fs = 48kHz. In the case of Fs = 44.1kHz, it will be about 1.09 times the setting value.

Detection flag read-back (Read Only)

Select Address	Value	Explanation of operation
&h72 [0]	0	Un-detecting.
	1	Detecting

5. Clock stop detection and detection of BCLK frequency begin too low or too high or asynchronous state detection

5-1. Clock stops detection

BM28720MUV needs some clock source for generating proper clock to process Audio data.
By stopping these cock sources, these clocks to process Audio data also stop.
To prevent noise sounds, we need to detect BCLK or LRCLK stop condition.
As we detect stop flag that is to be valid, output is gone to mute state (mute instantly).

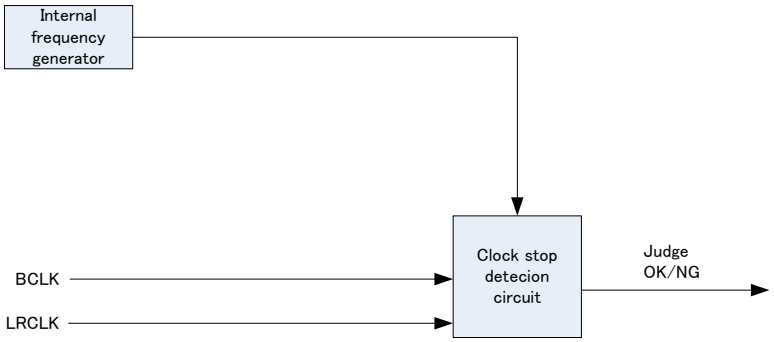


Figure 70.

Each detect condition is set by below command. We can check detected result by reading back flag register.
These flags are cleared only by sending specified commands.

LRCLK stop detection time
Default = 2h(LRCK)

Select Address	Value	Operation
LRCLK &h07 [2:0]	0	10μs to 20μs
	1	20μs to 40μs
	2	50μs to 100μs
	3	100μs to 200μs
	4	200μs to 400μs
	5	300μs to 600μs
	6	400μs to 800μs
	7	500μs to 1000μs

※Detection time has the above-mentioned variation within the limits.

BCLK stop detection time
Default = 0h(BCK)

Select Address	Value	Operation
BCLK &h08 [6:4]	0	10μs to 20μs
	1	20μs to 40μs
	2	50μs to 100μs
	3	100μs to 200μs
	4	200μs to 400μs
	5	300μs to 600μs
	6	400μs to 800μs
	7	500μs to 1000μs

※Detection time has the above-mentioned variation within the limits.

Stop detection flag read back register (Read Only)

Select Address	Value	Operation
&h09 [5]	0	Normal
	1	Detection of LRCLK stop flag
&h09 [4]	0	Normal
	1	Detection of BCLK stop flag

Stop detection flag clear register (Write Only)

Select Address	Operation
&h09 [1]	LRCLK stop detection flag is cleared by writing 1.
&h09 [0]	BCLK stop detection flag is cleared by writing 1.

※When using a clock shutdown auto return facility (Chapter 17), the above-mentioned flag is cleared automatically.

LRCLK stop flag valid or invalid selection
Default = 0h

Select Address	Value	Operation
&h07 [3]	0	Valid
	1	Invalid

BCLK stop flag valid or invalid selection
Default = 0h

Select Address	Value	Operation
&h08 [7]	0	Valid
	1	Invalid

5-2. Synchronous blank detection

As for synchronous blank detecting function, it detects as synchronous blank error when it counts between the rising edges of LRCK with internal clock (49.152MHz), and it shifts more than the definite value, and whether PLL is normally locked is judged.

Input sampling frequency	32kHz,44.1kHz,48kHz
Count value (Start of counting from 0)	1023

As for the detection result, reading from the register is possible. As a result of the judgment as synchronous blank once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, the setting of the detection approval frequency is also possible, and if the error more than the predetermined number is detected, the flag (&h06[1]) becomes "1" by the command.

Synchronous blank flag reading register (Read Only)

Select Address	Value	Explanation of operation
&h06 [1]	0	Normal
	1	Synchronous blank detect

Synchronous blank flag clear register(Write Only)

Select Address	Explanation of operation
&h06 [0]	When "1" is written, the synchronous blank flag is cleared.

*When the clock stop automatic return function (Chapter 7) is used, these flags are cleared by the automatic operation.

Synchronous blank count setting
Default = 2h

Select Address	Explanation of operation
&h06 [6:4]	Please set 2.

5-3. BCLK high or low speed detection

BCLK high or low speed detection function is that judge BCLK speed being too high or low by measuring by using internal clock(12MHz to 25MHz).
When using a BCLK speed detection, speed failure detection can be more correctly performed by making a command set reflect about an input sample rate.
When you validate sample rate setting, please be sure to set up the sample ring rate inputted with &h0c [1:0] command. A high speed and the low-speed detection flag can set up validity and the disabled, respectively, and if the validated flag is materialized, mute (mute instantly) will be carried out.

Valid or invalid frequency value setting up by &h0C[1:0] command.
Default = 0h

Select Address	Value	Operation
&h0A [3]	0	Valid
	1	Invalid

Setting of sampling rate
Default = 0h

Select Address	Value	Operation
&h0C [1:0]	0	48kHz
	1	44.1kHz
	2	32kHz

The constraints of a high speed or a low-speed condition
Default = 0h

Select Address	Value	Operation
&h0A [2]	0	±10%

We can check detection result by reading back.
The result judged that is once unusual is not cleared until it transmits a clear command, even if the condition of a clock returns to normal. We can set up
We can set up the constraints of the count of formation, and it does not set a flag until it detects it by count continuation.

BCLK high speed flag(Read Only)

Select Address	Value	Operation
&h0A [1]	0	Normal
	1	High speed detection flag

BCLK low speed flag(Read Only)

Select Address	Value	Operation
&h0B [1]	0	Normal
	1	Low speed detection flag

High speed detection clears register(Write Only)

Select Address	Operation
&h0A [0]	If “1” writes in, a high speed detection flag will be cleared.

※When using a clock shutdown auto return facility (Chapter 7), the above-mentioned flag is cleared automatically.

Low speed detection clear register(Write Only)

Select Address	Operation
&h0B [0]	If “1” writes in, a high speed detection flag will be cleared.

※When using a clock shutdown auto return facility (Chapter 7), the above-mentioned flag is cleared automatically.

A constraint of the count of judging with high speed flag detection
Default = 2h

Select Address	Operation
&h0A [6:4]	Please set up one or more. (1-7 are set up) A will become "&h0A[1]=1" if the BCLK high speed condition more than the count of setting up is detected continuously.

A constraint of the count of judging with low speed flag detection
Default = 2h

Select Address	Operation
&h0B [6:4]	Please set 2.

High speed detection flag valid or invalid
Default = 0h

Select Address	Value	Operation
&h0A [7]	0	Valid
	1	Invalid

Low speed detection flag valid or invalid
Default = 0h

Select Address	Value	Operation
&h0B [7]	0	Valid
	1	Invalid

The frequency range of BCLK by which high speed detection or low speed detection is carried out becomes below.

Setting1	Setting2	Low speed	High speed
10%(&h0A[2]=0)	48kHz(&h0C[1:0]=0)	Under 20.0k to 41.3kHz	Over 55.6k to 111.4kHz
	44.1kHz(&h0C[1:0]=1)	Under 18.9k to 38.0kHz	Over 51.1k to 102.4kHz
	32kHz(&h0C[1:0]=2)	Under 13.7k to 27.6kHz	Over 37.1k to 74.3kHz
20%(&h0A[2]=1)	48kHz(&h0C[1:0]=0)	Under 19.2k to 38.4kHz	Over 62.4k to 128.4kHz
	44.1kHz(&h0C[1:0]=1)	Under 17,6k to 35.3kHz	Over 57.3k to 114.7kHz
	32kHz(&h0C[1:0]=2)	Under 12.8k to 25.6kHz	Over 41.6k to 83.2kHz

6. Auto recovery from clock error function

Detection flag and a BCLK high speed, and low speed detection flag formation, it will be in a mute condition (mute instantly) about an output.
In that case, if the clock error auto return facility is enabled, when it returns to a normal input, a mute condition will be canceled automatically.
When the clock error auto return facility is repealed, it is necessary to control a series of operations called a mute-on and flag clear command transmission, an internal-RAM-data clear, and mute release from an external microcomputer.
Since it is invalid immediately after a wake-up, &h0D[6] =1 is set up before mute release, and it recommends validating.

Valid or invalid auto recover from clock error
Default = 0h

Select Address	Value	Operation
&h0D [6]	0	Invalid
	1	Valid

Each error flag can be read from the following addresses. When 1 is read from a read address, the error flag stands. Moreover, a flag is not cleared until it writes 0 in the target address, even if error status will be canceled, once a flag leaves.

Error flag read register

Select Address	Operation
&h0E [6]	Asynchronous flag
&h0E [4]	LRCLK stop flag
&h0E [3]	BCLK stop flag
&h0E [2]	BCLK high speed detection flag
&h0E [1]	BCLK low speed detection flag

7. The wake-up Procedure of power-up

It recommends starting power-up in the following Procedures.

1. Power up
○ Wait over 10msec
2. Release reset(RSTX=H)
3. &h0C[1:0]=*h : Sampling rate(Please set up 0h in the case of 48kHz, set up 1h in the case of 44.1kHz and 2h in 32kHz.)
○ Please input BCLK and LRCLK
4. &hE9=10h : changing clock to normal state
○ Wait over 5msec
5. &h0x01=00h : Set RAM clear OFF
6. &h0D[6]=1h : Valid auto recover from clock error
7. &h0E[7:1]=0h : Clear error flag
8. &h92[4:0]=11h : PWM setting1
9. &h93[4:0]=1Ch : PWM setting2
10. &h94[4:0]=15h : PWM setting3
11. &h95[4:0]=04h : PWM setting4
12. Please set up DSP function such as volume, PEQ, DRC, and Scaler etc.
13. MUTEX=H : Release mute

8. The operating procedure in a status with an unstable clock

In the segment where the input of I2S signal of BCLK, LRCLK, and SDATA may become unstable, please set to MUTEX=L and carry out mute.

1.MUTEX=L

○ After stabilizing I2S input, it is 20 ms or more WAIT.

2.MUTEX=H

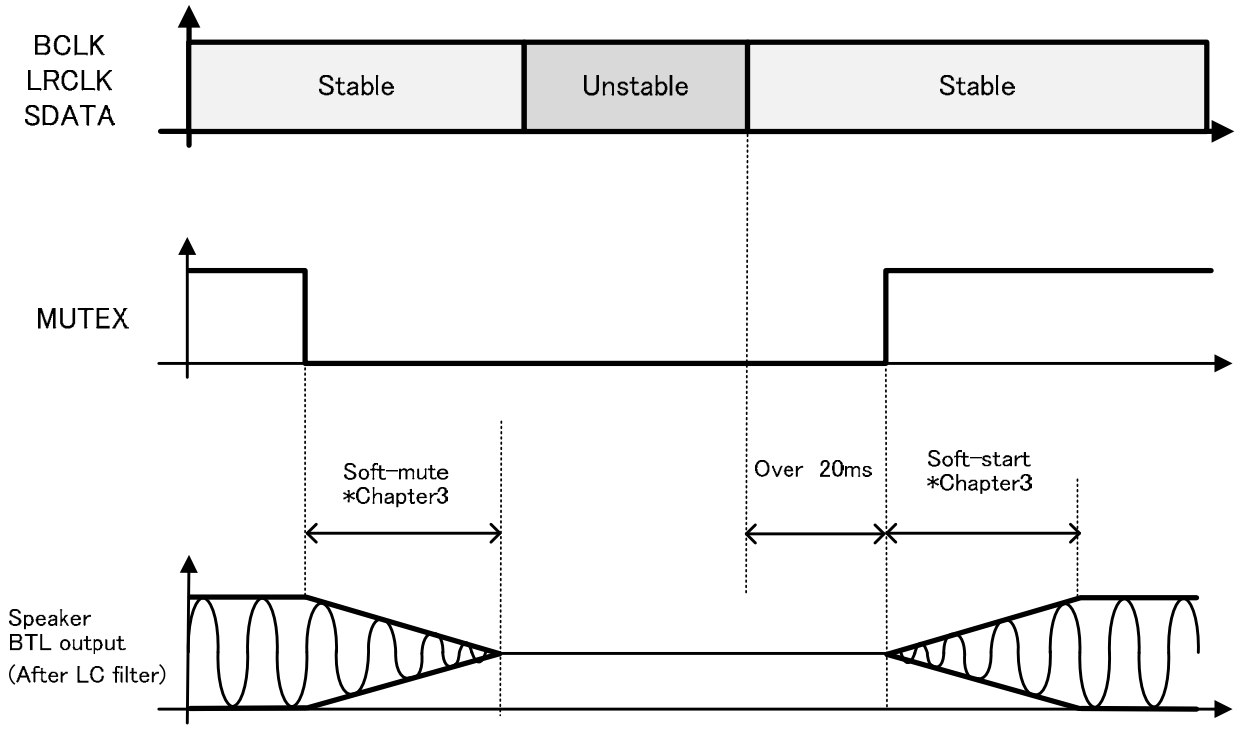


Figure 71.

9. I2S Data output select

Output I2S data signal From SDATAO (pin12). That SDATAO synchronize to inputted LRCK and BCK signal.
This function is valid for I2S or Left-justified format.
And enable to select output SDATA signal as shown below.

SDATAO output select
Default = 0h

Select Address	Value	Explanation of operation
&h78 [6:4]	0	DSP output (point1)
	1	DSP input (pont2)
	2	Pre scaler output (point3)
	3	Mixer output (point4)
	4	12Band PEQ output (point5)
	5	Fine master volume output (point6)
	6	No use
	7	Scaler output (point7)

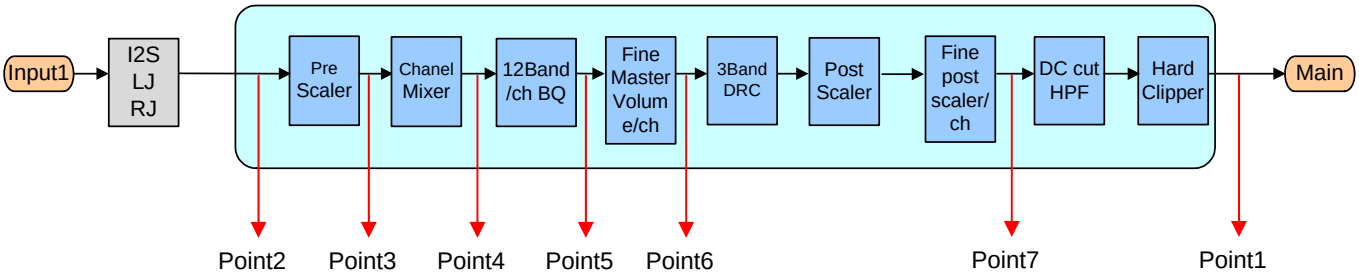


Figure 72.

Application Circuit Example1 (Stereo BTL output, R_L=8Ω, Vcc=10V to 18V)

・When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz and decrease the influence of LCR resonance using application circuit. Please refer 5) Output LC Filter Circuit (Vcc=18V to 24V)

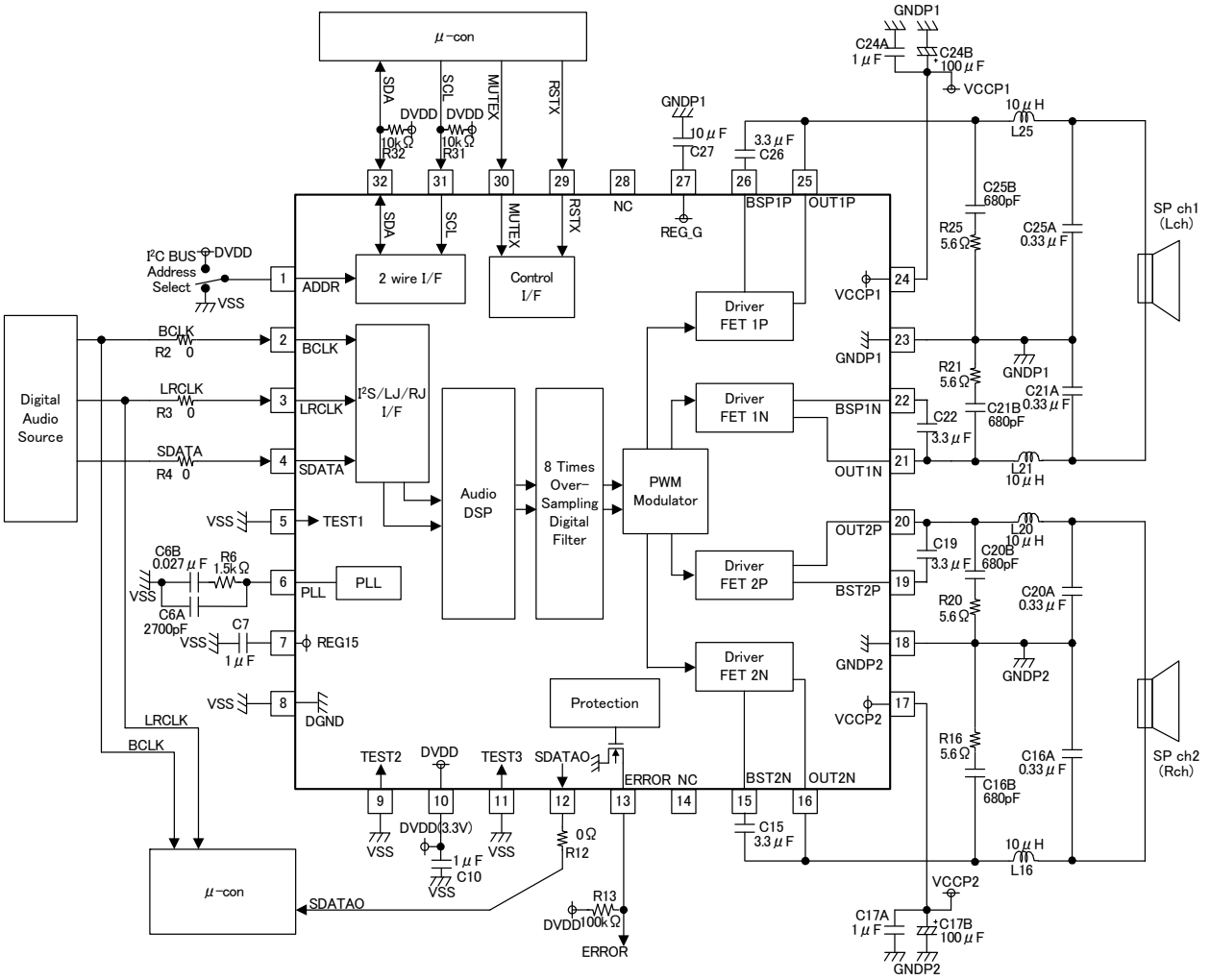


Figure 73.

BOM list1(Stereo BTL output, R_L=8Ω, Vcc=10V to 18V)

Parts	Qty	Parts No.	Description	Company	Product No.
Inductor	4	L16, L20, L21, L25	10uH / (±20%) / 7.6mm×7.6mm	TOKO	B1047AS-100M
Resister	4	R16, R20 R21, R25	5.6Ω / 1/10W / J(±5%) / 1.6mm×0.8mm	ROHM	MCR03EZPJ5R6
	1	R6	1.5kΩ / 1/16W / F(±1%) / 1.0mm×0.5mm		MCR01MZPF1501
	2	R31, R32	10kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ103
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%) / 1.6mm×0.8mm		MCR03EZPJ000
	1	R13	100kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ104
Capacitor	4	C16B, C20B C21B, C25B	680pF / 50V / B(±10%) / 1.6mm×0.8mm	MURATA	GRM188B11H681KA01
	1	C6A	2700pF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J272KA01
	1	C6B	0.027uF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J273KE01
	4	C16A, C20A, C21A, C25A,	0.33uF / 50V / B(±10%) / 2.0mm×1.25mm		GRM219B31H34KA87
	2	C17A, C24A (Note 1)	1uF / 50V / B(±10%) / 2.0mm×1.25mm		GRM21BB31H105KA12
	4	C15, C19, C22, C26	3.3uF / 16V / B(±10%) / 1.6mm×0.8mm		GRM188B31C335KA12
	2	C7, C10	1uF / 10V / B(±10%) / 1.6mm×0.8mm		GRM185B31A105KE43
	1	C27	10uF / 10V / B(±10%) / 1.6mm×0.8mm		GRM188B31A106KE15
	2	C17B, C24B	100uF / 35V / (±20%) / φ8mm×11.5mm	PANASONIC	ECA1VMH101

(Note 1) Please put the C17A and C24A near the VCCP1 and VCCP2 pins on the board.

Application Circuit Example2 (Monaural BTL output, R_L=8Ω, Vcc=10V to 18V)

・When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz and decrease the influence of LCR resonance using application circuit. Please refer 5) Output LC Filter Circuit (Vcc=18V to 24V)

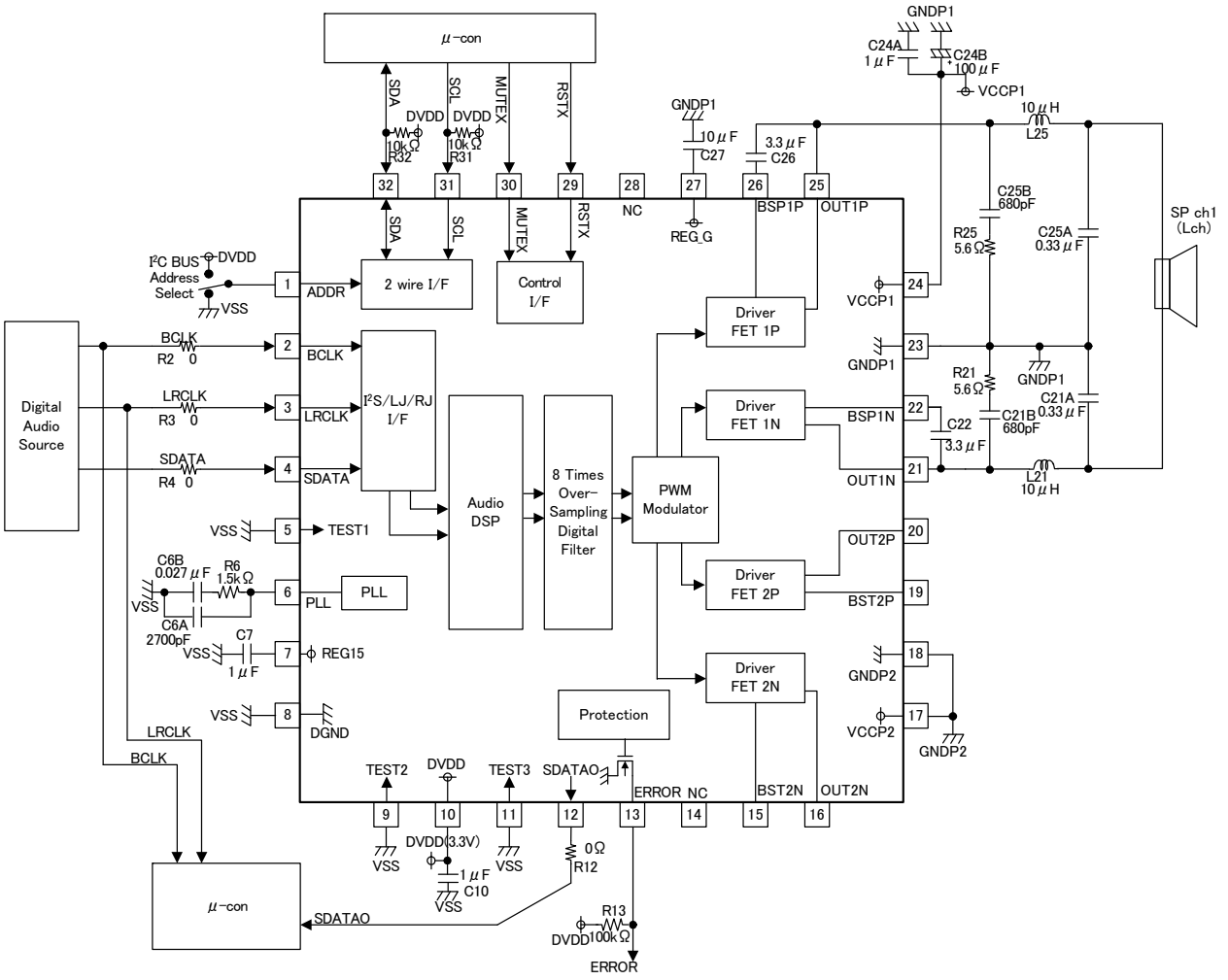


Figure 74.

BOM list2(Monaural BTL output, R_L=8Ω, Vcc=10V to 18V)

Parts	Qty	Parts No.	Description	Company	Product No.
Inductor	2	L21, L25	10uH / (±20%) / 7.6mm×7.6mm	TOKO	B1047AS-100M
Resister	2	R21, R25	5.6Ω / 1/10W / J(±5%) / 1.6mm×0.8mm	ROHM	MCR03EZPJ5R6
	1	R6	1.5kΩ / 1/16W / F(±1%) / 1.0mm×0.5mm		MCR01MZPF1501
	2	R31, R32	10kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ103
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%) / 1.6mm×0.8mm		MCR03EZPJ000
	1	R13	100kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ104
Capacitor	2	C21B, C25B	680pF / 50V / B(±10%) / 1.6mm×0.8mm	MURATA	GRM188B11H681KA01
	1	C6A	2700pF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J272KA01
	1	C6B	0.027uF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J273KE01
	2	C21A, C25A	0.33uF / 50V / B(±10%) / 2.0mm×1.25mm		GRM219B31H334KA87
	1	C24A (Note 1)	1uF / 50V / B(±10%) / 2.0mm×1.25mm		GRM21BB31H105KA12
	2	C22, C26	3.3uF / 16V / B(±10%) / 1.6mm×0.8mm		GRM188B31C335KA12
	2	C7, C10	1uF / 10V / B(±10%) / 1.6mm×0.8mm		GRM185B31A105KE43
	1	C27	10uF / 10V / B(±10%) / 1.6mm×0.8mm		GRM188B31A106KE15
	1	C24B	100uF / 35V / ±20% / φ8mm×11.5mm	PANASONIC	ECA1VMH101

(Note 1) Please put the C24A near the VCCP1 pins on the board.

Selection of Components Externally Connected (Vcc=10V to 18V)

1) Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequency 384kHz(fs=48kHz) in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_{L1}. This filter reduces unwanted emission this way. In addition, coil L and capacitor Cg composes a filter against in-phase components, reducing unwanted emission further.

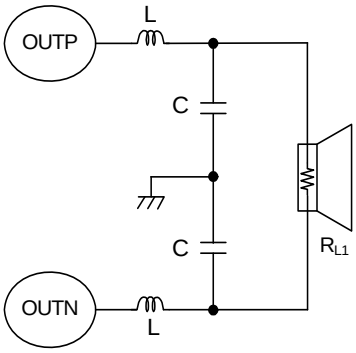


Figure 75.

Following presents output LC filter constants with typical load impedances.

R_{L1}	L	C
4Ω	10μH	1μF
6Ω	10μH	0.47μF
8Ω	10μH	0.33μF

Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

2) The value of the LC filter circuit computed equation

The output LC filter circuit of BM28720MUV is as it is shown in Figure 76. The LC filter circuit of Figure 76 is thought to substitute it like Figure 77 on the occasion of the computation of the value of the LC filter circuit.

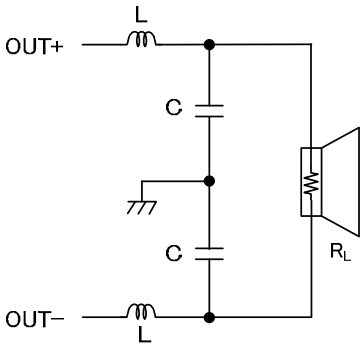


Figure 76. Output LC filter 1

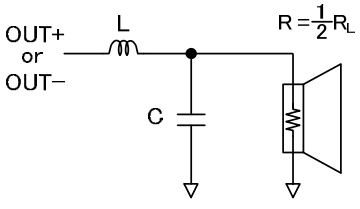


Figure 77. Output LC filter 2

The transfer function H(s) of the LC filter circuit of Figure 77 becomes the following.

$$H(s) = \frac{\frac{1}{LC}}{s^2 + \frac{1}{CR}s + \frac{1}{LC}} = \frac{\omega^2}{s^2 + \frac{\omega}{Q}s + \omega^2}$$

The ω and Q become the followings here.

$$\omega^2 = \frac{1}{LC} \qquad \omega = 2\pi f_{CL} \qquad f_{CL} = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = R\sqrt{\frac{C}{L}} = \frac{1}{2}R_L\sqrt{\frac{C}{L}}$$

Therefore, L and C become the followings.

$$L = \frac{1}{\omega^2 C} = \frac{R_L}{4\pi f_{CL} Q} \qquad C = \frac{Q}{\omega R} = \frac{Q}{\pi f_{CL} R_L}$$

The R_L and L should be made known, and fCL is set up, and C is decided.

3) The settlement of the L value of the coil

A standard for selection of the L value of a coil to use is to take the following back anti-matter into consideration except for the factor such as a low cost-ization, miniaturization, pale pattern.

①When L value was made small.
(1) Circuit electric currents increase without a signal. And, efficiency in the low output gets bad.
(2) Direct current resistance value is restrained small when the coil of other L value and size are made the same. Therefore, maximum output is easy to take out. And, it can be used in the low power supply voltage because DC electric current (allowable electric current) value can be taken greatly.

②When L value was made large.
(1) Circuit electric current is restrained low without a signal. Efficiency in the low output improves.
(2) Direct current resistance value grows big when the coil of other L value and size are made the same. Therefore, maximum output is hard to take out. And, because it becomes small, use becomes difficult 【 the DC electric current (allowable electric current) value 】 in the low power supply voltage, too.

4) The settlement of the fCL

As for the settlement of the fixed number of the LC filter circuit, it is taken into consideration about two points of the following, and set up.

①The PWM sampling frequency fPWM (=8fS) of BM28720MUV is set up in 384kHz (@fS=48kHz).
It is set up with fC < fPWM to restrain career frequency omission after the LC filter circuit.
②When fc is lowered too much, the voltage profit of the voice obi stage (especially, the neighborhood of 20kHz) declines in the speaker output frequency character of the difference movement mode.
And, the speaker output frequency character of the difference movement mode becomes the following.

RL=8Ω				RL=6Ω				RL=4Ω			
L[uH]	C[uF]	fc[kHz]	Q	L[uH]	C[uF]	fc[kHz]	Q	L[uH]	C[uF]	fc[kHz]	Q
10	0.1	75.32	0.40	10	0.1	51.01	0.30	10	0.1	32.19	0.20
	0.15	80.85	0.49		0.15	54.76	0.37		0.15	33.35	0.24
	0.22	86.79	0.59		0.22	56.73	0.44		0.22	34.55	0.30
	0.33	89.92	0.73		0.33	63.1	0.54		0.33	35.8	0.36
	0.47	86.79	0.87		0.47	66.68	0.65		0.47	38.37	0.43
	1.0	69.01	1.26		1.0	62.29	0.95		1.0	44.1	0.63
15	0.1	46.99	0.33	15	0.1	33.11	0.24	15	0.1	21.68	0.16
	0.15	49.66	0.40		0.15	34.36	0.30		0.15	22.08	0.20
	0.22	53.46	0.48		0.22	35.65	0.36		0.22	22.49	0.24
	0.33	57.54	0.59		0.33	38.37	0.44		0.33	22.91	0.30
	0.47	59.7	0.71		0.47	41.3	0.53		0.47	23.77	0.35
	1.0	52.75	1.03		1.0	44.67	0.77		1.0	27.47	0.52
22	0.1	30.76	0.27	22	0.1	22.49	0.20	22	0.1	14.72	0.13
	0.15	31.92	0.33		0.15	22.91	0.25		0.15	14.72	0.17
	0.22	33.73	0.40		0.22	23.77	0.30		0.22	15	0.20
	0.33	36.31	0.49		0.33	24.66	0.37		0.33	15.28	0.24
	0.47	39.08	0.58		0.47	26.06	0.44		0.47	15.56	0.29
	1.0	39.30	0.85		1.0	30.05	0.64		1.0	17.33	0.43

5) Output LC Filter Circuit (Vcc=18V to 24V)

When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz or less and decrease the influence of LCR resonance using application circuit.

R_{L1}	L	C
4Ω	10μH	1μF
6Ω	15μH	0.47μF
8Ω	15μH	0.33μF
	22μH	0.47μF

Use coils with a low direct current resistance and with a sufficient margin of allowable currents. A high direct current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.
Use capacitors with a low equivalent series resistance and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient voltage rating because massive amount of high frequency currents flow is expected.

In addition, please do not place the C_{BTL} shown in Figure 78.
When considering only common mode signals, OUTP and OUTN are equal to each other and this circuit is equivalent to the circuit shown in Figure 79.
Therefore, LC resonance may occur depending on the constant of a LC filter.

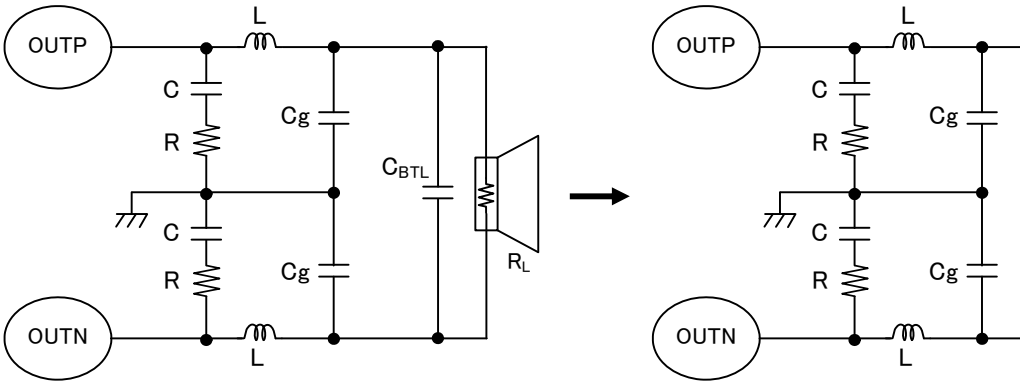


Figure 78. Figure 79.

6) The settlement of the snubber

The Snubber circuit must be optimized for application circuit to reduce the overshoot and undershoot of output PWM.

① Measure the spike resonance frequency f1 of the PWM output wave shape (When it stands up.) by using FET probe in the OUT terminal. (Figure 81) The FET probe is to monitor very near pin and shorten ground lead at the time of that.
② Measure resonance frequency f2 of the spike as a snubber circuit fixed number R=0Ω (Only with the condenser C, to connect GND) At this time, the value of the condenser C is adjusted until it becomes half of the frequency (2f2=f1) of the resonance frequency f1 of ①. The value of C which it could get here is three times of the parasitic capacity Cp that a spike is formed. (C=3Cp)
③ Parasitic inductance Lp is looked for at the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

④ The character impedance Z of resonance is looked for from the parasitic capacity Cp and the parasitism inductance Lp at the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

⑤ A snubber circuit fixed number R is set up in the value which is the same as the character impedance Z. A snubber circuit fixed number C is set up in the value of 4-10 times of the parasitic capacity Cp. (C=4Cp to 10Cp) Decide it with trade-off with the character because switching electric currents increase when the value of C is enlarged too much.

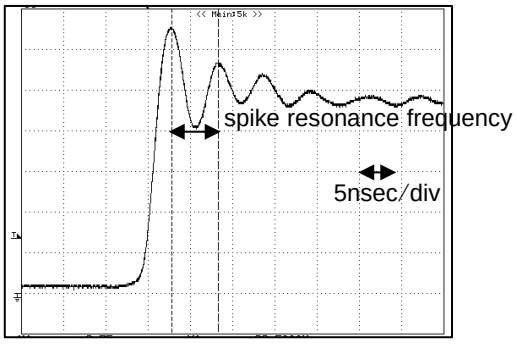


Figure 80. PWM Output waveform
（measure of spike resonance frequency

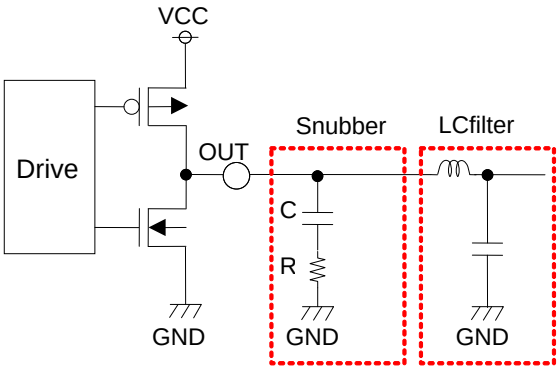


Figure 81. snubber schematic

Following presents Snubber filter constants with the recommendation value at ROHM 4 layer board.

R_L	C	R
4Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω ,1/10W J(±5%)
6Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω ,1/10W J(±5%)
8Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω ,1/10W J(±5%)

Level Diagram of Audio Signal

Level diagram of audio signal is shown the below figure. Speaker output level is depended on I2S digital audio input level, DSP gain, PWM gain, BTL gain and Loss of power stage and low pass filter.
I2S input level is full-scale signal, the supply voltage of the block is DVDD, and therefore, 0dBFS is equal to DVDD voltage [Vpp]. DSP gain is set by 2 wire control variably, and -0.5dB is set at PWM Modulator block usually. At the Power stage, the PWM Modulator output is shifted PWM signal level from DVDD to VCC, and added loss of the output transistor resistance rDS and DC resistance of coil rDC.

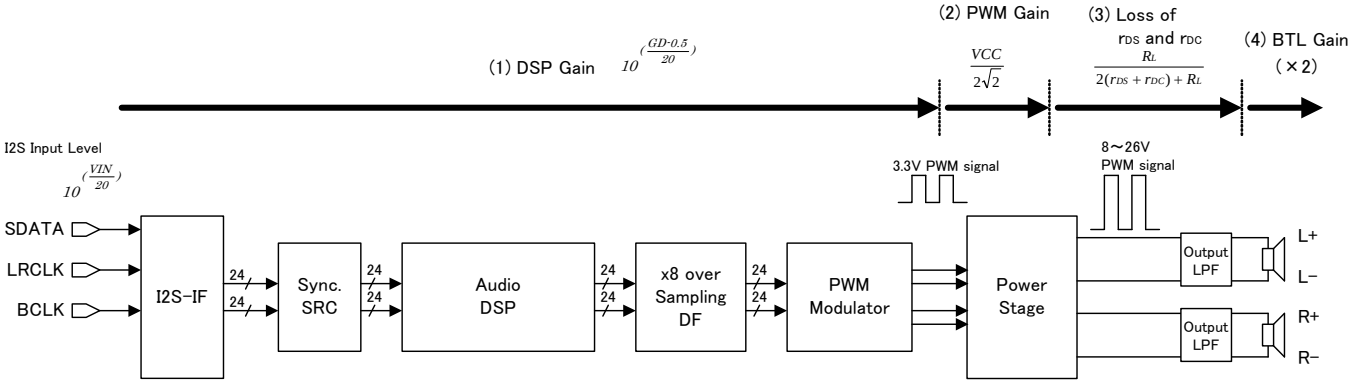


Figure 82. Level Diagram of Audio Signal

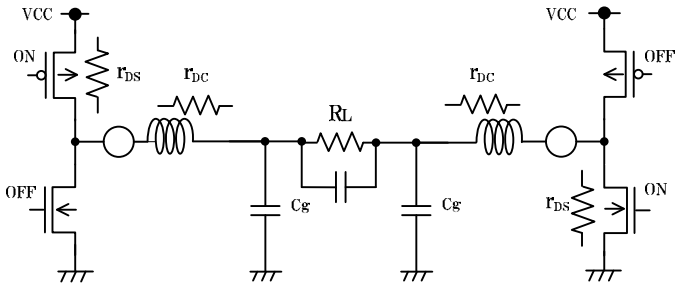


Figure 83. Output LPF circuit

In Bridge-Tied-Load (BTL) connection, the following formula gives an approximate value of output power *Po at non*-clipping output waveform:

$$P_O = \frac{\left(10^{VIN/20} \times 10^{(GD-0.5)/20} \times \frac{VCC}{2\sqrt{2}} \times 2 \times \frac{R_L}{2 \times (r_{DS} + r_{DC}) + R_L}\right)^2}{R_L}$$

I2S Input Level / DSP Gain / PWM Gain / BTL Gain / Loss of rDS and rDC

VIN : I2S Input level [dBFS]
GD : DSP gain [dB]
VCC : Power supply voltage of Power stage [V]
DVDD : Power supply voltage of DSP block [V]
RL : Load impedance [Ω]
rDS : Turn-on resistance of output MOS Tr. [Ω]
(typ.=160m Ω)
rDC : DC resistance of output LPF coil [Ω]

If the circuit is driven further until an output waveform is clipped, an output power higher than that without distortion is obtained. In general a clipped output is quantified where “THD+N = 1% and 10%,” and a maximum output power under that status is calculated by the following formula:

$$P_{O(1\%)} = \frac{\left(10^{(-0.5/20)} \times \frac{\mathrm{VCC}}{\sqrt{2}} \times \frac{R_L}{2(r_{DS} + r_{DC}) + R_L}\right)^2}{R_L} [W]$$

$$P_{O(10\%)} = P_{O(1\%)} \times 1.25 [W]$$

Power Dissipation

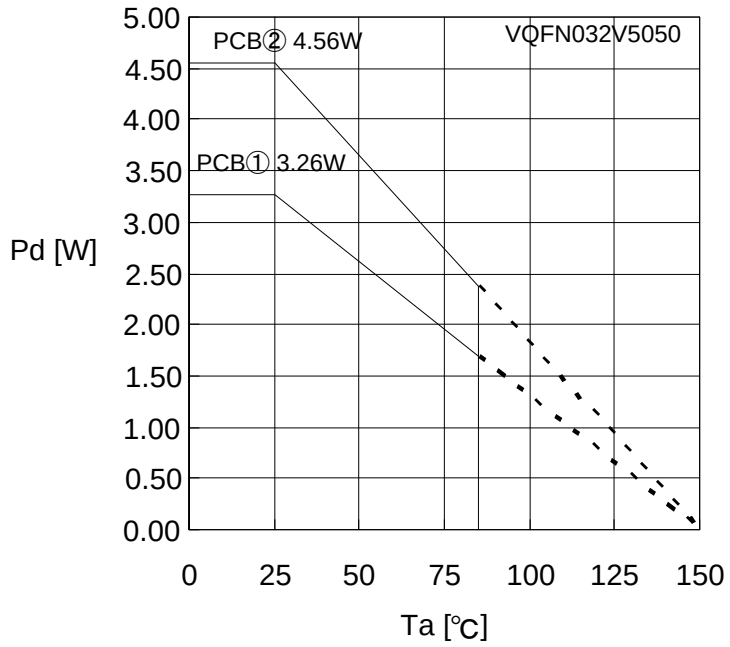


Figure 84. Allowable Power Dissipation

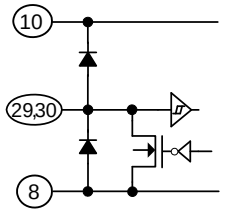
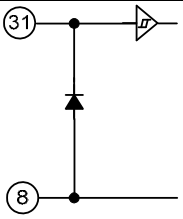
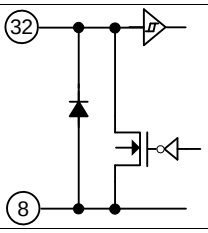
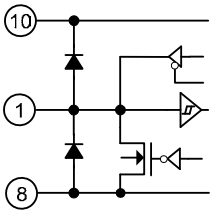
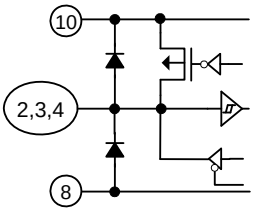
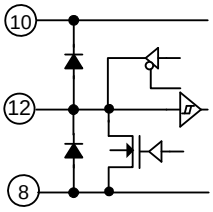
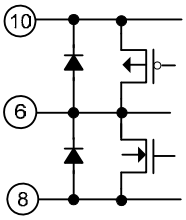
Measuring instrument：TH-156(Shibukawa Kuwano Electrical Instruments Co, Ltd.)
Measuring conditions：Installation on ROHM’s board
Board size：74.2mm×74.2mm×1.6mm(with thermal via on board)
Material：FR4
・The board on exposed heat sink on the back of package are connected by soldering.

PCB①：4- layer board (Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2) , θja = 36.48℃/W
PCB②：4-layer board(back copper foil size: 5505mm^2), θja = 26.08℃/W

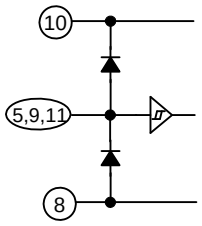
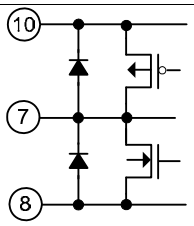
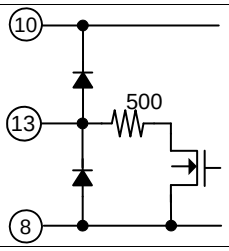
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.
Class D speaker amplifier is high efficiency and low heat generation by comparison with conventional Analog power amplifier. However, In case it is operated continuously by maximum output power, Power dissipation (Pdiss) may exceed package dissipation. Please consider about heat design that Power dissipation (Pdiss) does not exceed Package dissipation (Pd) in average power (Poav). (Tjmax ：Maximum junction temperature=150℃, Ta ：Peripheral temperature[℃], θja ：Thermal resistance of package[℃/W], Poav：Average power[W], η：Efficiency)

Package dissipation : Pd(W)=(Tjmax - Ta)／θja
Power dissipation : Pdiss(W)= Poav ×(1／η- 1)

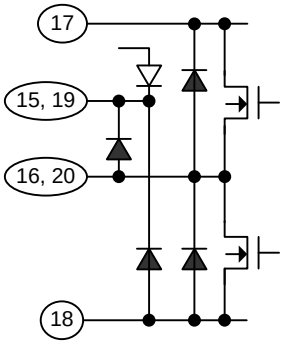
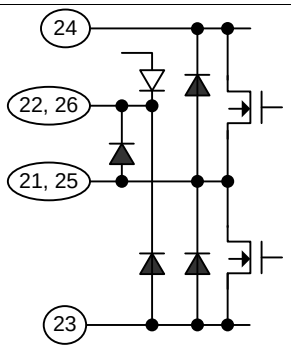
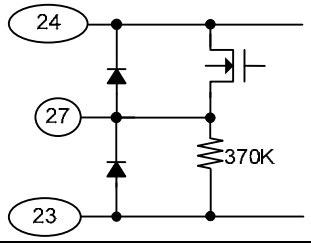
I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
29	RSTX	0V	Reset pin for Digital circuit H:Reset OFF L:Reset ON	
30	MUTEX	0V	Speaker output mute control pin H:Mute OFF L:Mute ON	
8	DGND	0V	GND pin for Digital I/O	—
31	SCL	—	2 wire transmit clock input pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
32	SDA	—	2 wire data input/output pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
1	ADDR	0V	2 wire Slave address select pin	
4 3 2	SDATA LRCLK BCLK	3.3V	Digital sound signal input pin	
12	SDATAO	0V	Digital sound signal output pin	
6	PLL	1V	PLL's filter pin	

I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
10	DVDD	3.3V	Power supply pin for Digital I/O.	—
5 9 11	TEST1 TEST2 TEST3	— — —	Test pin Please connect to VSS.	
7	REG15	1.5V	Internal power supply pin for Digital circuit	
13	ERROR	3.3V	Error flag pin H: Normal operation L: Error	
14 28	NC	—	Non Connection Pin	—

I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
17	VCCP2	VCC	Power supply pin for ch2 PWM signal	
20	OUT2P	VCC to 0V	Output pin of ch2 positive PWM Please connect to Output LPF.	
19	BSP2P	–	Boot-strap pin of ch2 positive Please connect the capacitor.	
18	GNDP2	0V	GND pin for ch2 PWM signal	
16	OUT2N	VCC to 0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
15	BSP2N	–	Boot-strap pin of ch2 negative Please connect the capacitor.	
22	BSP1N	–	Boot-strap pin of ch1 negative Please connect the capacitor.	
21	OUT1N	VCC to 0V	Output pin of ch1 negative PWM Please connect to Output LPF.	
23	GNDP1	0V	GND pin for ch1 PWM signal	
26	BSP1P	–	Boot-strap pin of ch1 positive Please connect the capacitor.	
25	OUT1P	VCC to 0V	Output pin of ch1 positive PWM Please connect to Output LPF.	
24	VCCP1	VCC	Power supply pin for ch1 PWM signal	
27	REG_G	5.2V	Internal power supply pin for gate driver Please connect the capacitor.	

Operational Notes

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) Power supply lines
As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

3) GND potential (Pin 8, 18, 23)
Any state must become the lowest voltage about DGND, GNDP1 and GNDP2 terminal.

4) Input terminal
The parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than DGND and VSS. Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit
This product is provided with a built-in thermal shutdown circuit. When the thermal shutdown circuit operates, the output transistors are placed under open status. The thermal shutdown circuit is primarily intended to shut down the IC avoiding thermal runaway under abnormal conditions with a chip temperature exceeding Tjmax = 150℃.

7) Shorts between pins and miss-installation
When mounting the IC on a board, pay adequate attention to orientation and placement discrepancies of the IC. If it is miss-installed and the power is turned on, the IC may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the IC or between a pin and a power supply or a pin and a GND.

8) Power supply on/off (Pin 10, 17, 24)
In case power supply is started up, RSTX(Pin 29) and MUTEX(Pin 30) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.

9) ERROR terminal (Pin 13)
An error flag is outputted when Output short protection or DC voltage protection. This flag is the function which the condition of this product is shown in.

10) N.C. terminal (Pin 14, 28)
N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.

11) TEST terminal (Pin 5, 9, 11)
TEST terminal connects with ground to prevent the malfunction by external noise.

12) Precautions for Speaker-setting
If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

13) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

14) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

Ordering Information

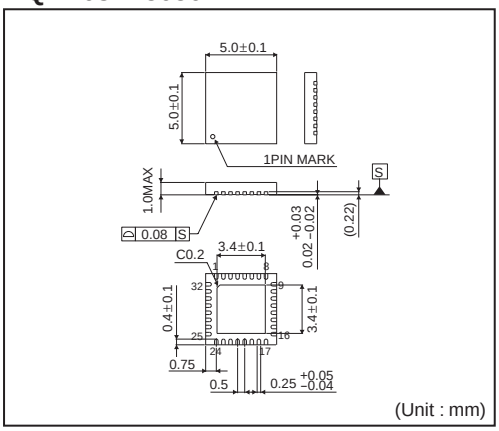
B	M	2	8	7	2	0	M	U	V	-	E2

Package
MUV:
VQFN032V5050

Packaging and forming specification
E2: Embossed tape and reel

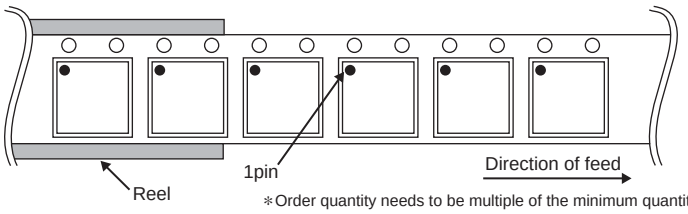
Physical Dimensions Tape and Reel Information

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagram

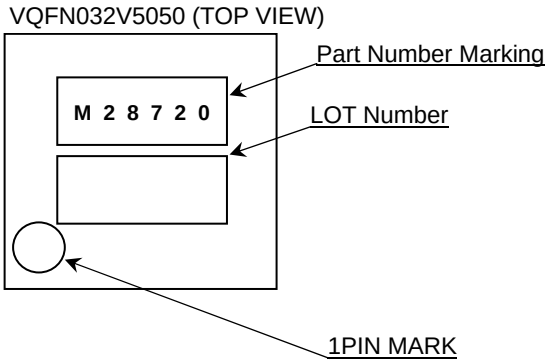


Figure 85.

Revision History

Date	Revision	Changes
2013/10/21	001	First version
2013/12/10	002	Corrected (P2) Corrected performance curves (P5-7) Modified recommend constant (P63-64, 67, 68) Deleted application circuit (P63-64)

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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