

# PCA9701; PCA9702

18 V tolerant SPI 16-bit/8-bit GPI with  $\overline{\text{INT}}$

Rev. 7 — 26 September 2014

Product data sheet

## 1. General description

The PCA9701/PCA9702 are low power 18 V tolerant SPI General Purpose Input (GPI) shift register designed to monitor the status of switch inputs. It generates an interrupt when one or more of the switch inputs change state. The input level is recognized as a HIGH when it is greater than  $0.7 \times V_{DD}$  and as a LOW when it is less than  $0.4 \times V_{DD}$  (minimum threshold of 2 V at 5 V node). The PCA9701 can monitor up to 16 switch inputs and the PCA9702 can monitor up to 8 switch inputs.

The falling edge of the  $\overline{\text{CS}}$  pin samples the input port status and clears the interrupt. When  $\overline{\text{CS}}$  is LOW, the rising edge of the SCLK loads the shift register and shifts the value out of the shift register. The serial input is sampled on the falling edge of SCLK.

Each of the input ports has a 18 V breakdown ESD protection circuit. When used with a series resistor (minimum 100 k $\Omega$ ), the input can connect to a 12 V battery and support double battery, reverse battery, 27 V jump start and 40 V load dump conditions in automotive applications. Higher voltages can be tolerated on the inputs depending on the series resistor used to limit the input current.

With both the high breakdown voltage and high ESD, these devices are useful for both automotive and mobile applications.

The PCA9703/PCA9704 are new pin compatible devices for the PCA9701/PCA9702 which have an interrupt masking feature allowing selected inputs to not generate interrupts and provides higher ground offset of  $0.55 \times V_{DD}$  (minimum of 2.5 V at 5 V node) with minimum hysteresis of  $0.05 \times V_{DD}$  (minimum of 225 mV at 5 V node).

## 2. Features and benefits

- 16 general purpose input ports (PCA9701) or 8 general purpose input ports (PCA9702)
- 18 V tolerant input ports with 100 k $\Omega$  external series resistor
- Input LOW threshold  $0.4 \times V_{DD}$  with minimum of 2 V at  $V_{DD} = 4.5$  V
- Open-drain interrupt output
- Interrupt enable pin (INT\_EN) disables interrupt output
- $V_{DD}$  range: 2.5 V to 5.5 V
- $I_{DD}$  is very low 2.5  $\mu\text{A}$  maximum
- SPI serial interface with speeds up to 5 MHz
- ESD protection exceeds 8 kV HBM per JESD22-A114, 350 V MM, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range:  $-40$  °C to  $+125$  °C



- PCA9701 offered in SO24, TSSOP24 and HWQFN24 packages
- PCA9702 offered in TSSOP16 package

### 3. Applications

- Body control modules
- Switch monitoring
- Industrial equipment
- Cellular telephones
- Emergency lighting
- SBC wake pin extension

### 4. Ordering information

Table 1. Ordering information

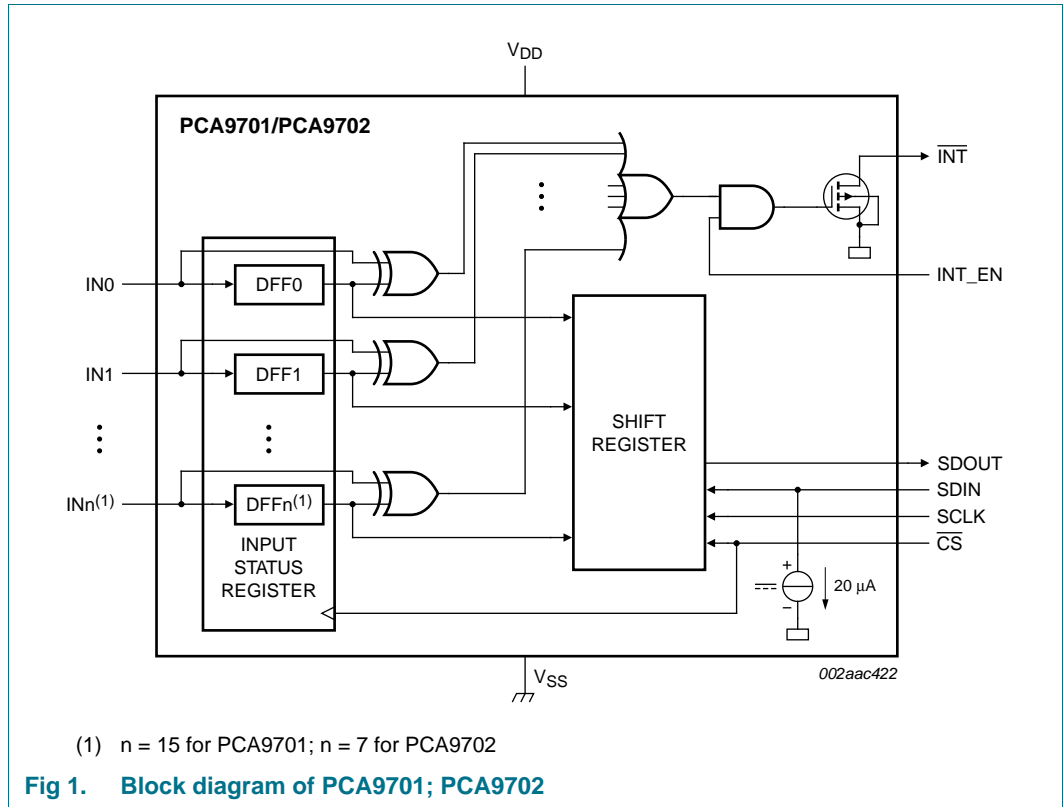
| Type number | Topside marking | Package |   |          |
|-------------|-----------------|---------|---|----------|
|             |                 | Name    | Description   | Version  |
| PCA9701D    | PCA9701D        | SO24    | plastic small outline package; 24 leads; body width 7.5 mm  | SOT137-1 |
| PCA9701HF   | 9701            | HWQFN24 | plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm | SOT994-1 |
| PCA9701PW   | PCA9701PW       | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm                                  | SOT355-1 |
| PCA9702PW   | PCA9702         | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm                                  | SOT403-1 |

#### 4.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method                       | Minimum order quantity | Temperature range                    |
|-------------|-----------------------|---------|--------------------------------------|------------------------|--------------------------------------|
| PCA9701D    | PCA9701D,118          | SO24    | Reel 13" Q1/T1<br>*standard mark SMD | 1000                   | T <sub>amb</sub> = -40 °C to +125 °C |
| PCA9701HF   | PCA9701HF,118         | HWQFN24 | Reel 13" Q1/T1<br>*standard mark SMD | 6000                   | T <sub>amb</sub> = -40 °C to +125 °C |
| PCA9701PW   | PCA9701PW,118         | TSSOP24 | Reel 13" Q1/T1<br>*standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +125 °C |
| PCA9702PW   | PCA9702PW,118         | TSSOP16 | Reel 13" Q1/T1<br>*standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +125 °C |

5. Block diagram



## 6. Pinning information

### 6.1 Pinning

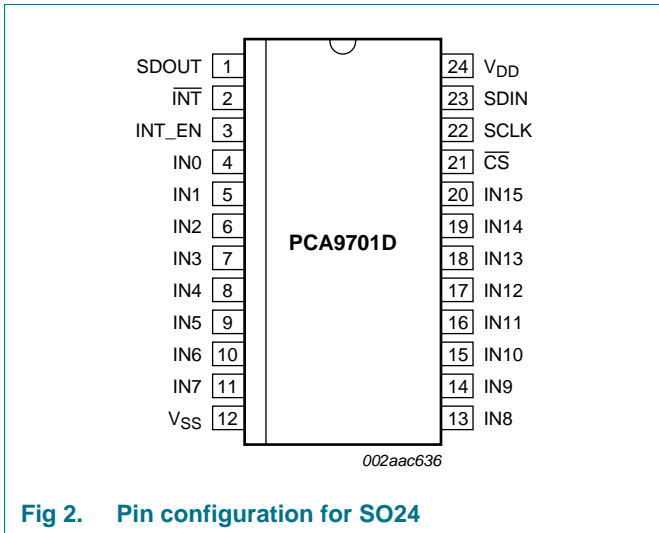


Fig 2. Pin configuration for SO24

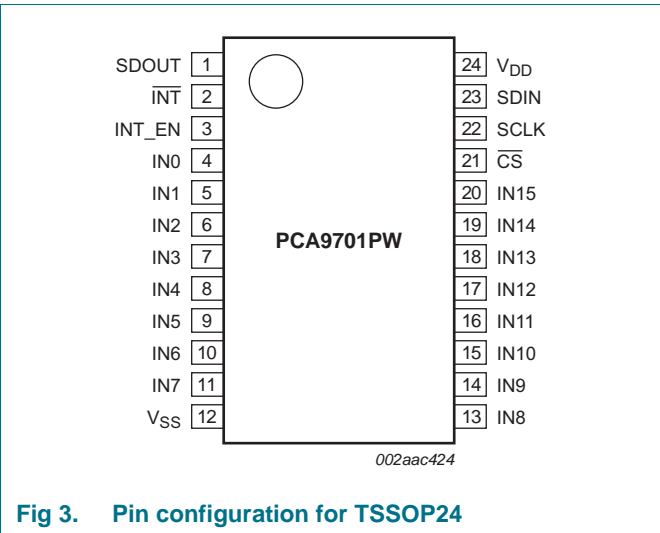


Fig 3. Pin configuration for TSSOP24

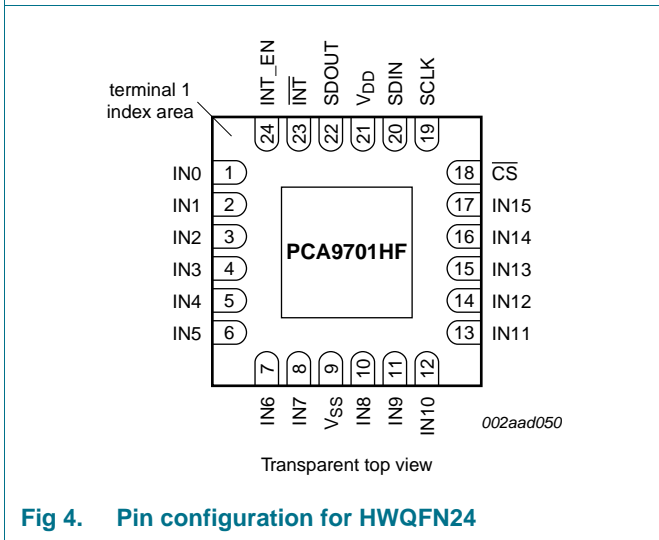


Fig 4. Pin configuration for HWQFN24

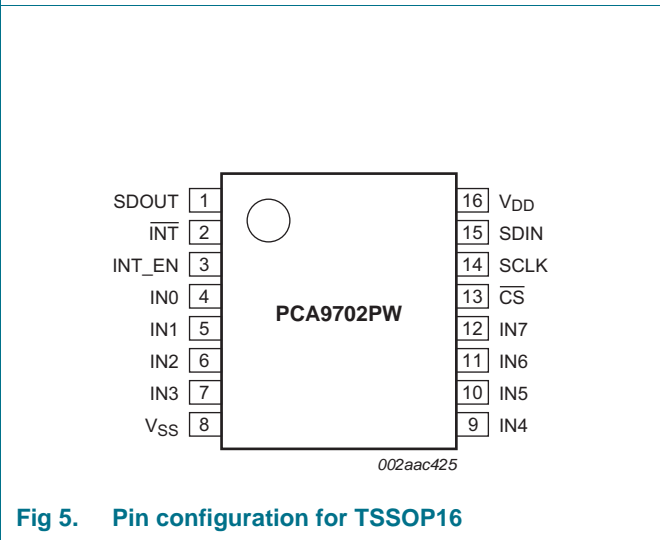


Fig 5. Pin configuration for TSSOP16

## 6.2 Pin description

Table 3. Pin description

| Symbol                  | Pin           |                  |         | Type   | Description   |
|-------------------------|---------------|------------------|---------|--------|---|
|                         | SO24, TSSOP24 | HWQFN24          | TSSOP16 |        |   |
| SDOUT                   | 1             | 22               | 1       | output | 3-state serial data output; normally high-impedance   |
| $\overline{\text{INT}}$ | 2             | 23               | 2       | output | open-drain interrupt output (active LOW)  |
| INT_EN                  | 3             | 24               | 3       | input  | interrupt output enable<br>1 = interrupt is enabled<br>0 = interrupt is disabled and high-impedance |
| IN0                     | 4             | 1                | 4       | input  | input port 0  |
| IN1                     | 5             | 2                | 5       | input  | input port 1  |
| IN2                     | 6             | 3                | 6       | input  | input port 2  |
| IN3                     | 7             | 4                | 7       | input  | input port 3  |
| IN4                     | 8             | 5                | 9       | input  | input port 4  |
| IN5                     | 9             | 6                | 10      | input  | input port 5  |
| IN6                     | 10            | 7                | 11      | input  | input port 6  |
| IN7                     | 11            | 8                | 12      | input  | input port 7  |
| V <sub>SS</sub>         | 12            | 9 <sup>[1]</sup> | 8       | ground | ground supply   |
| IN8                     | 13            | 10               | -       | input  | input port 8  |
| IN9                     | 14            | 11               | -       | input  | input port 9  |
| IN10                    | 15            | 12               | -       | input  | input port 10   |
| IN11                    | 16            | 13               | -       | input  | input port 11   |
| IN12                    | 17            | 14               | -       | input  | input port 12   |
| IN13                    | 18            | 15               | -       | input  | input port 13   |
| IN14                    | 19            | 16               | -       | input  | input port 14   |
| IN15                    | 20            | 17               | -       | input  | input port 15   |
| $\overline{\text{CS}}$  | 21            | 18               | 13      | input  | chip select (active LOW)  |
| SCLK                    | 22            | 19               | 14      | input  | serial input clock  |
| SDIN                    | 23            | 20               | 15      | input  | serial data input (20 $\mu$ A pull-down)  |
| V <sub>DD</sub>         | 24            | 21               | 16      | supply | supply voltage  |

[1] HWQFN24 package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

## 7. Functional description

PCA9701 is a 16-bit General Purpose Input (GPI) with an open-drain interrupt output designed to monitor switch status. By putting an external 100 k $\Omega$  series resistor at the input port, the device allows the input to tolerate momentary double 12 V battery, reverse battery, 27 V jump start or 40 V load dump conditions. The interrupt output is asserted when an input port status changes. The open-drain interrupt output is enabled when  $\overline{\text{INT\_EN}}$  is HIGH and disabled when  $\overline{\text{INT\_EN}}$  is LOW. The input port status is accessed via the 4-wire SPI interface. The PCA9702 is the 8-bit version of the PCA9701.

Multiple PCA9701 or PCA9702 devices can be serially connected for monitoring a large number of switches by connecting the  $\overline{\text{SDOUT}}$  of one device to the  $\overline{\text{SDIN}}$  of the next device.  $\overline{\text{SCLK}}$  and  $\overline{\text{CS}}$  must be common among all devices and interrupt outputs may be tied together. No external logic is necessary because all the devices' interrupt outputs are open-drain that function as 'wired-AND' and can simply be connected together to a single pull-up resistor.

### 7.1 SPI bus operation

The PCA9701 or PCA9702 interfaces with the controller via the 4-wire SPI bus that is comprised of the following signals: chip select ( $\overline{\text{CS}}$ ), serial clock (SCLK), serial data in ( $\overline{\text{SDIN}}$ ), and serial data out ( $\overline{\text{SDOUT}}$ ). To access the device, the controller asserts  $\overline{\text{CS}}$  LOW, then sends SCLK and  $\overline{\text{SDIN}}$ . When reading/writing is complete, the controller de-asserts  $\overline{\text{CS}}$ . See [Figure 6](#) for register access timing.

#### 7.1.1 $\overline{\text{CS}}$ - chip select

The  $\overline{\text{CS}}$  pin is the device chip select and is an active LOW input. The falling edge of  $\overline{\text{CS}}$  captures the input port status in the input status register. If the interrupt output is asserted, the falling edge of  $\overline{\text{CS}}$  will clear the interrupt. When  $\overline{\text{CS}}$  is LOW, the SPI interface is active. When  $\overline{\text{CS}}$  is HIGH, the SPI interface is disabled.

#### 7.1.2 SCLK - serial clock input

SCLK is the serial clock input to the device. It should be LOW and remain LOW during the falling and rising edge of  $\overline{\text{CS}}$ . When  $\overline{\text{CS}}$  is LOW, the first rising edge of SCLK parallel loads the shift register from the input. The subsequent rising edges on SCLK serially shifts data out from the shift register. The falling edge of SCLK samples the data on  $\overline{\text{SDIN}}$ .

#### 7.1.3 $\overline{\text{SDIN}}$ - serial data input

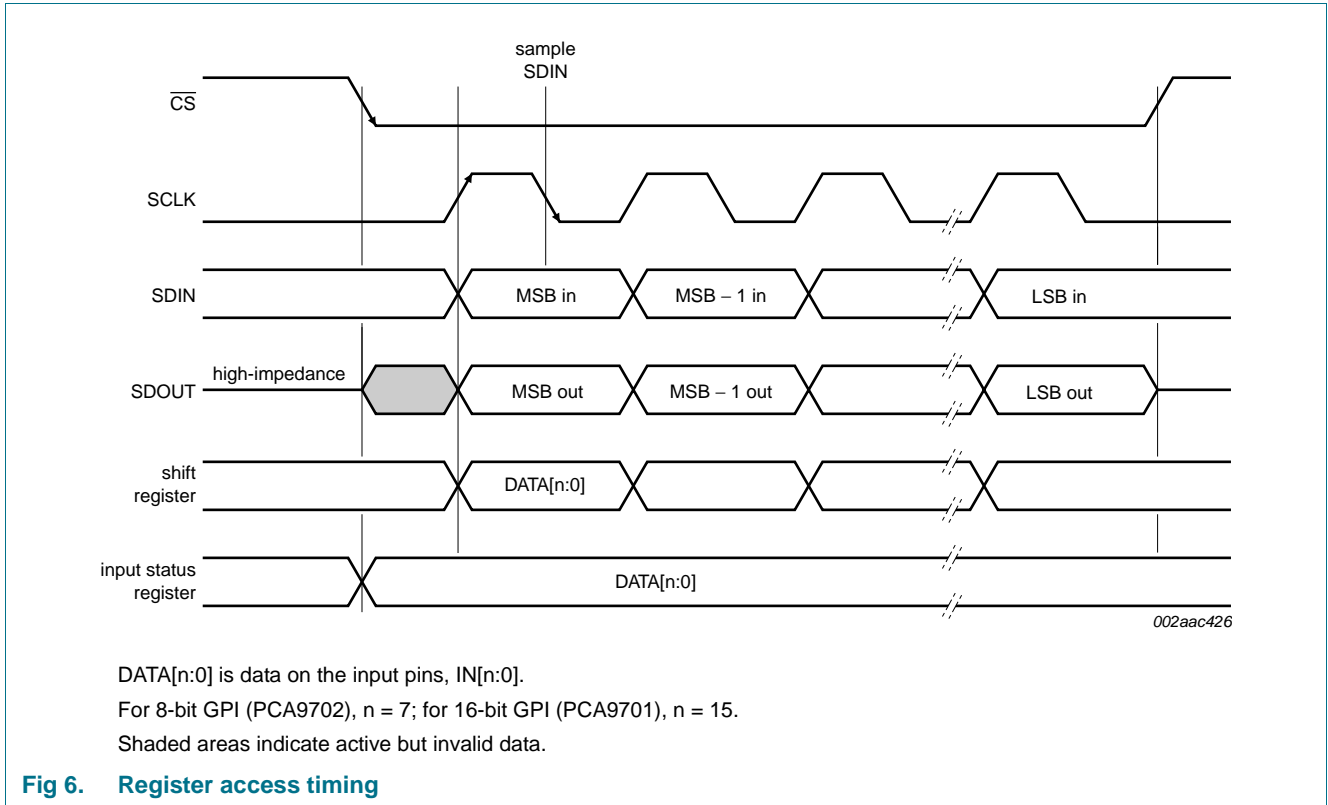
$\overline{\text{SDIN}}$  is the serial data input port. The data is sampled into the shift register on the falling edge of SCLK.  $\overline{\text{SDIN}}$  is only active when  $\overline{\text{CS}}$  is LOW. This input has a 20  $\mu\text{A}$  pull-down current source.

#### 7.1.4 $\overline{\text{SDOUT}}$ - serial data output

$\overline{\text{SDOUT}}$  is the serial data output signal.  $\overline{\text{SDOUT}}$  is high-impedance when  $\overline{\text{CS}}$  is HIGH and switches to low-impedance after  $\overline{\text{CS}}$  goes LOW. When  $\overline{\text{CS}}$  is LOW, after the first rising edge of SCLK the most significant bit in the shift register is presented on  $\overline{\text{SDOUT}}$ . Subsequent rising edges of SCLK shift the remaining data from the shift register onto  $\overline{\text{SDOUT}}$ .

7.1.5 Register access timing

Figure 6 shows the waveforms of the device operation. Initially  $\overline{CS}$  is HIGH and SCLK is LOW. On the falling edge of  $\overline{CS}$ , input port status, DATA[n:0] is captured into the input status register, and subsequently the first rising edge of SCLK parallel loads the shift register. The falling edge of SCLK samples the data on the SDIN. The MSB from the shift register is valid and available on the SDOUT after the first rising edge of SCLK.



7.2 Interrupt output

$\overline{INT}$  is the open-drain interrupt output and is active LOW. A pull-up resistor of approximately 10 kΩ is recommended. The interrupt output is asserted when the input status is changed, and is cleared on the falling edge of  $\overline{CS}$  or when the input port status matches the input status register. When there are multiple devices, the  $\overline{INT}$  outputs may be tied together to a single pull-up.

Table 4 illustrates the state of the interrupt output versus the state of the input port and input status register. The interrupt output is asserted when the input port and input status register differ.

**Table 4. Interrupt output function truth table**

H = HIGH; L = LOW; X = don't care

| INT_EN | Input port status | Input status register <sup>[1]</sup> | $\overline{\text{INT}}$ output <sup>[2]</sup> |
|--------|-------------------|--------------------------------------|---|
| H      | L                 | L                                    | H   |
| H      | L                 | H                                    | L   |
| H      | H                 | L                                    | L   |
| H      | H                 | H                                    | H   |
| L      | X                 | X                                    | H   |

[1] Input status register is the value or content of the D flip-flops.

[2] Logic states shown for  $\overline{\text{INT}}$  pin assumes 10 kΩ pull-up resistor.

### 7.3 General Purpose Inputs

The General Purpose Inputs (GPI) are designed to behave like a typical input in the 0 V to 5.5 V range, but are also designed to have low leakage currents at elevated voltages. The input structure allows for elevated voltages to be applied through a series resistor. The series resistor is required when the input voltage is above 5.5 V. The series resistor is required for two reasons: first, to prevent damage to the input avalanche diode, and second, to prevent the ESD protection circuitry from creating an excessive current flow. The ESD protection circuitry includes a latch-back style device, which provides excellent ESD protection during assembly or typical 5.5 V applications. The series resistor limits the current flowing into the part and provides additional ESD protection. The limited current prevents the ESD latch-back device from latching back to a low voltage, which would cause excessive current flow and damage the part.

The minimum required series resistance for applications with input voltages above 5.5 V is 100 kΩ. For applications requiring an applied voltage above 27 V, [Equation 1](#) is recommended to determine the series resistor. Failure to include the appropriate input series resistor may result in product failure and will void the warranty.

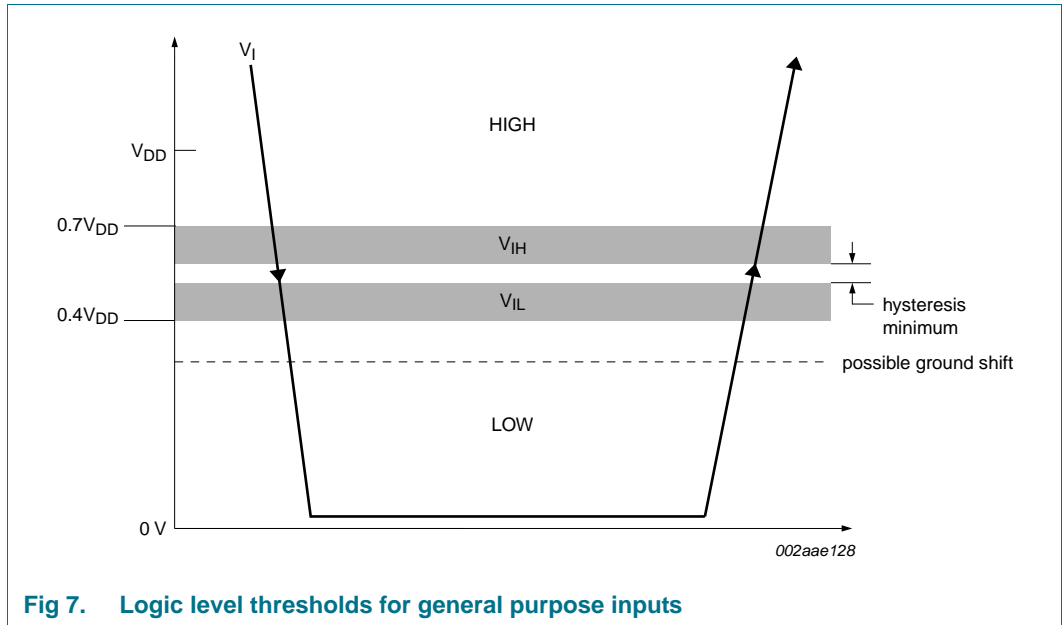
$$R_s = \frac{\text{voltage applied} - 17 \text{ V}}{I_I} \tag{1}$$

The series resistor should be placed physically as close as possible to the connected input to reduce the effective node capacitance. The input response time is effected by the RC time constant of the series resistor and the input node capacitance.



7.3.1  $V_{IL}$ ,  $V_{IH}$  and switching points

A minimum LOW threshold of 2.0 V is guaranteed for the logical switching points for the inputs. See [Figure 7](#) for details.

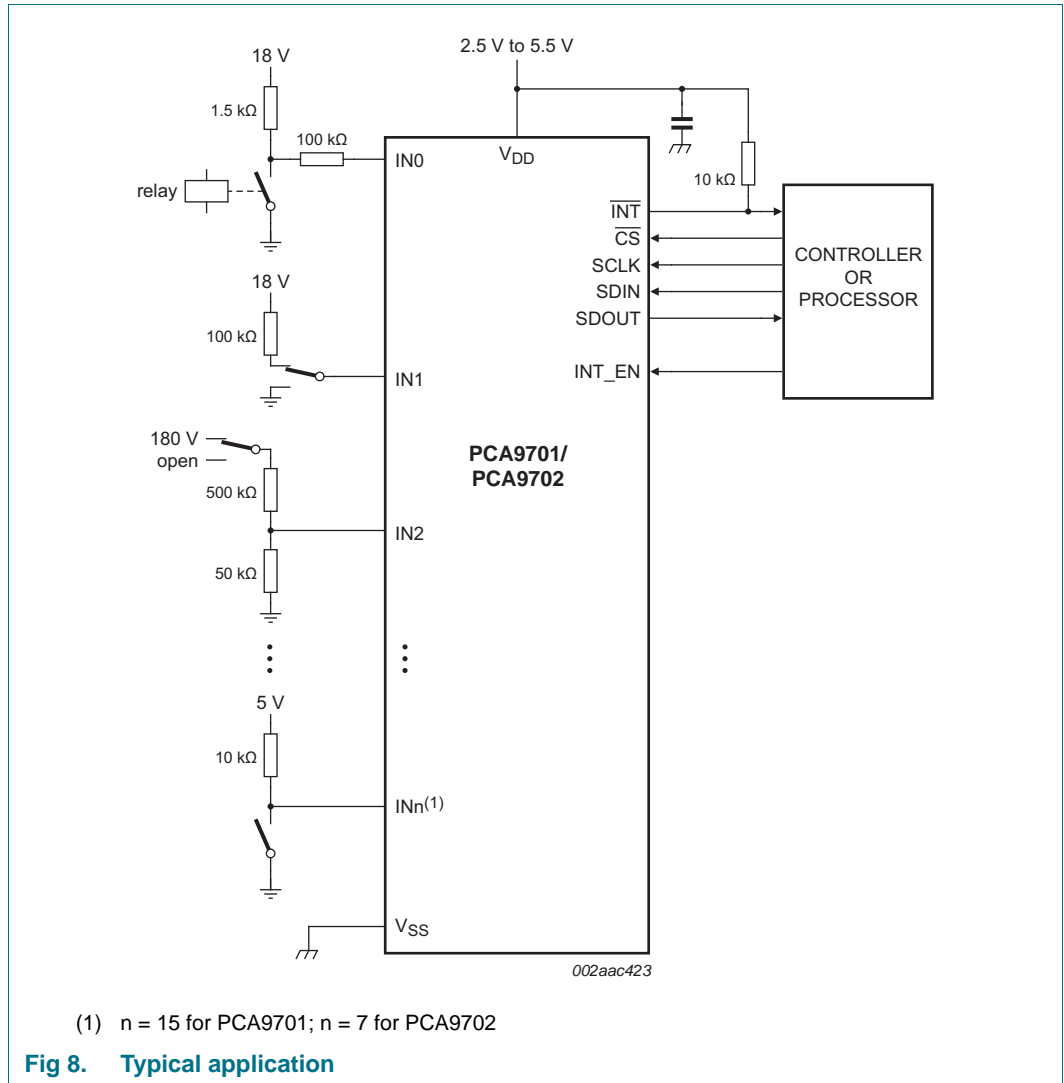


The  $V_{IL}$  is specified as a maximum of  $0.40 \times V_{DD}$  and is 2.0 V at 4.5 V  $V_{DD}$ . This means that if the user applies 2.0 V or less to the input (with  $V_{DD} = 4.5$  V), or as the voltage passes this threshold, they will always see a LOW.

The  $V_{IH}$  is specified as a minimum of  $0.7 \times V_{DD}$ . This means that if the user applies 3.15 V or more to the input (with  $V_{DD} = 4.5$  V), or as the voltage passes this threshold, they will always see a HIGH.

## 8. Application design-in information

### 8.1 General application



### 8.2 Automotive application

Supports:

- 12 V battery (8 V to 16 V)
- Double battery (16 V to 32 V)
- Reverse battery (−8 V to −16 V)
- Jump start (27 V for 60 seconds)
- Load dump (40 V)

8.2.1 SBC wake port extension with cyclic biasing

System Basis Chips (SBC) offer many functions needed for in-vehicle networking solutions. Some of the features built into SBC are:

- Transceivers (HS-CAN, LIN 2.0)
- Scalable voltage regulators
- Watchdog timers; wake-up function
- Fail-safe function

For more information on SBC, refer to

[http://www.nxp.com/index.html#/pip/pip=\[pfp=53482\]|pp=\[t=pfp,i=53482\]](http://www.nxp.com/index.html#/pip/pip=[pfp=53482]|pp=[t=pfp,i=53482]).

8.2.1.1 UJA106x with PCA9701, standby

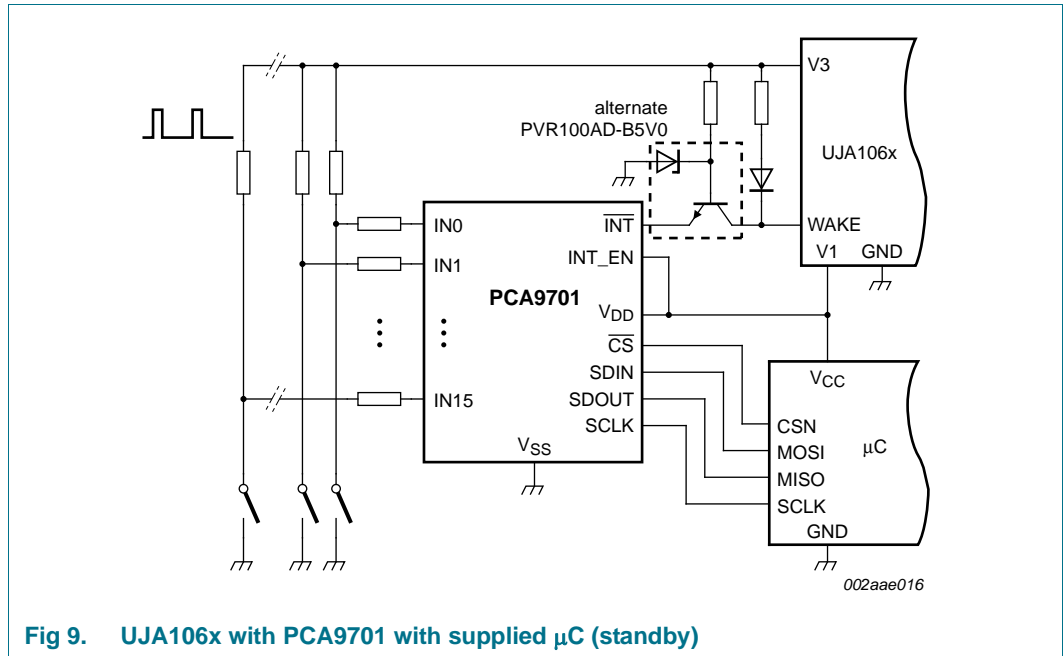


Fig 9. UJA106x with PCA9701 with supplied μC (standby)

- PCA970x fits to SBC UJA106x and UJA107xA family
- PCA970x can be powered by V1 of SBC
- Extends the SBC with 8/16 additional wake inputs
- μC can be set to stop-mode during standby to save ECU standby current. SBC with GPI periodically monitors the wake inputs
  - Cyclic bias via V3
  - Very low system current consumption even with clamped switches



8.2.1.3 UJA107xA with PCA9701, standby

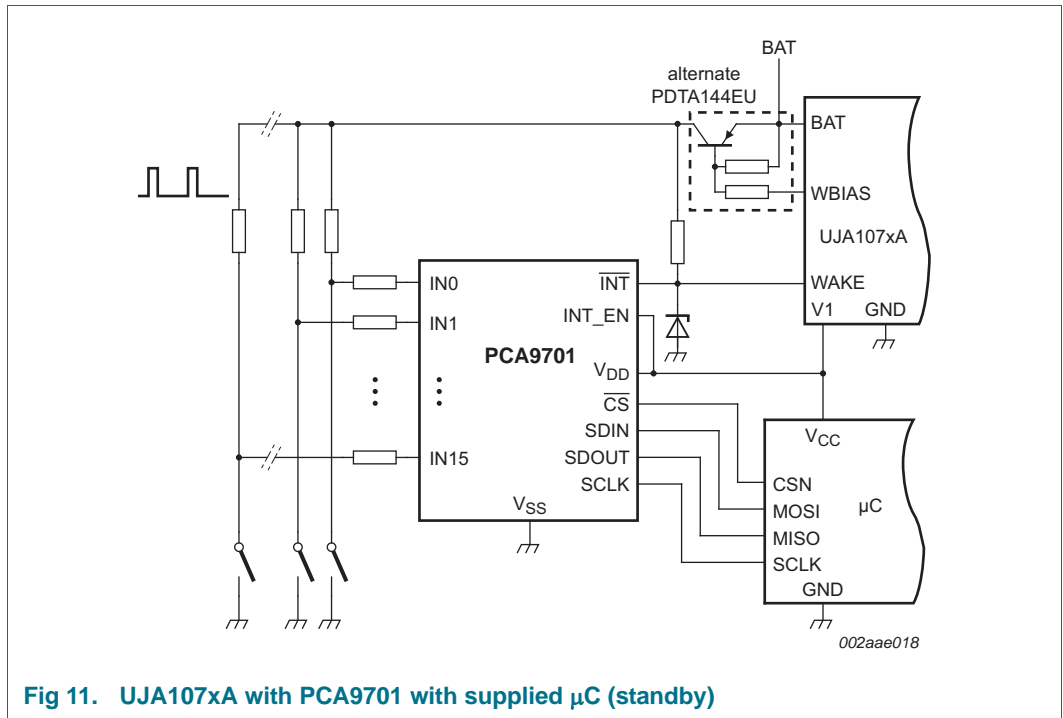


Fig 11. UJA107xA with PCA9701 with supplied  $\mu$ C (standby)

- UJA107xA SBC provides WBIAS pin for cyclic biasing of the inputs
- Compatible with UJA107xA based ASSPs

8.2.2 Application examples including switches to battery

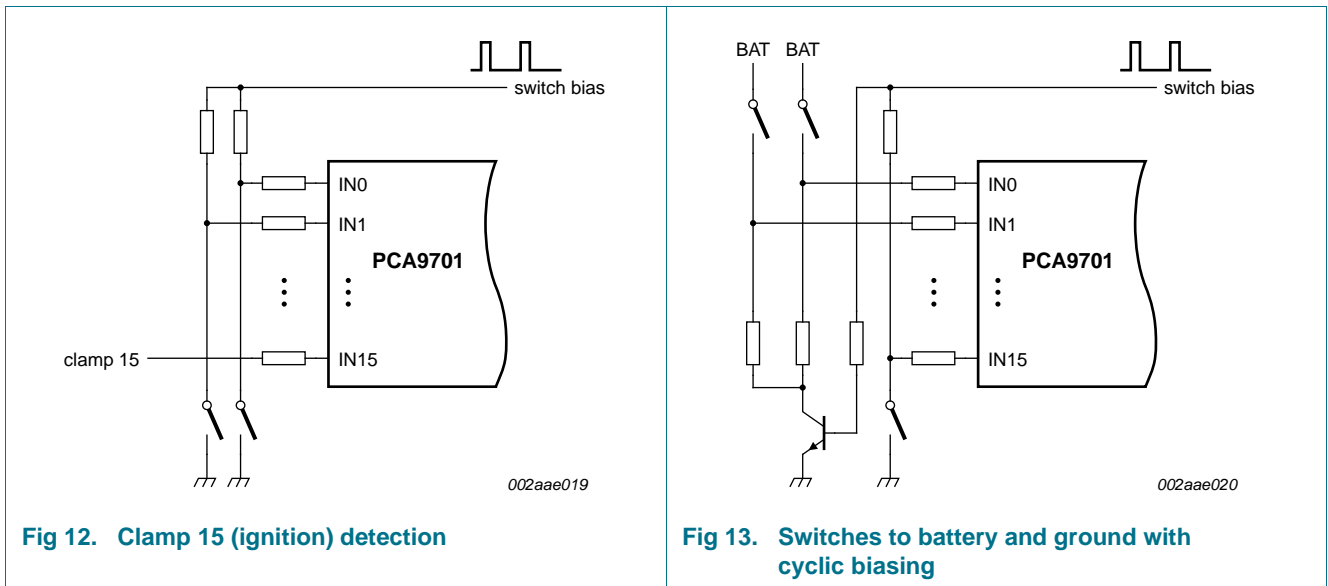


Fig 12. Clamp 15 (ignition) detection

Fig 13. Switches to battery and ground with cyclic biasing

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

$T_{amb} = -40\text{ °C}$  to  $+125\text{ °C}$ , unless otherwise specified.

| Symbol       | Parameter                    | Conditions   |        | Min  | Max  | Unit               |
|--------------|------------------------------|--|--------|------|------|--------------------|
| $V_{DD}$     | supply voltage               |  |        | -0.5 | +6.0 | V                  |
| $I_I$        | input current                | IN[n:0] pins with series resistor and $V_I > 5.5\text{ V}$ , | [1][2] | -    | 350  | $\mu\text{A}$      |
| $V_I$        | input voltage                | GPI pins IN[n:0]; no series resistor                         | [1][2] | -0.5 | +6   | V                  |
|              |                              | SPI pins   |        | -0.5 | +6   | V                  |
| $T_{stg}$    | storage temperature          |  |        | -65  | +150 | $^{\circ}\text{C}$ |
| $T_{j(max)}$ | maximum junction temperature | operating  |        | -    | 125  | $^{\circ}\text{C}$ |

[1] With GPI external series resistors, the inputs support double battery, reverse battery and load dump conditions. During double battery or load dump the input pin will drain slightly higher leakage current until the input drops to 18 V. For more detail of leakage current specification, please refer to [Table 6 "Static characteristics"](#). See [Section 7.3](#) for series resistor requirements.

[2]  $n = 15$  for PCA9701;  $n = 7$  for PCA9702.

## 10. Static characteristics

**Table 6. Static characteristics**
 $V_{DD} = 2.5\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                        | Parameter                             | Conditions   | Min              | Typ | Max         | Unit          |
|-------------------------------|---------------------------------------|--|------------------|-----|-------------|---------------|
| <b>Supply</b>                 |                                       |  |                  |     |             |               |
| $V_{DD}$                      | supply voltage                        |  | 2.5              | 3.3 | 5.5         | V             |
| $I_{DD}$                      | supply current                        | $V_{DD} = 5.5\text{ V}$ ; input = 5 V or 18 V; INT_EN = $V_{DD}$                   | -                | 1.0 | 2.5         | $\mu\text{A}$ |
| $V_{POR}$                     | power-on reset voltage <sup>[1]</sup> |  | -                | 1.8 | 2.2         | V             |
| <b>General Purpose Inputs</b> |                                       |  |                  |     |             |               |
| $V_{IL}$                      | LOW-level input voltage               |  | <sup>[2]</sup> - | -   | $0.4V_{DD}$ | V             |
| $V_{IH}$                      | HIGH-level input voltage              |  | $0.7V_{DD}$      | -   | -           | V             |
| $I_I$                         | input current                         | GPI recommended maximum current; $V_I > 5.5\text{ V}$ ; with series resistor $R_s$ | <sup>[3]</sup> - | -   | 100         | $\mu\text{A}$ |
| $I_{IH}$                      | HIGH-level input current              | each input; $V_I = V_{DD}$   | -1               | -   | +1          | $\mu\text{A}$ |
| $I_{LI}$                      | input leakage current                 | $V_I = 17\text{ V}$ ; 100 k $\Omega$ series resistor                               | -1               | -   | +1          | $\mu\text{A}$ |
| $C_i$                         | input capacitance                     | $V_I = V_{SS}$ or $V_{DD}$   | -                | 2.0 | 5.0         | pF            |
| <b>Interrupt output</b>       |                                       |  |                  |     |             |               |
| $I_{OL}$                      | LOW-level output current              | $V_{DD} = 4.5\text{ V}$ ; $V_{OL} = 0.4\text{ V}$                                  | 6                | -   | -           | mA            |
|                               |                                       | $V_{DD} = 2.5\text{ V}$ ; $V_{OL} = 0.4\text{ V}$                                  | 3                | -   | -           | mA            |
| $I_{OH}$                      | HIGH-level output current             | $V_{OH} = V_{DD}$  | -1               | -   | +1          | $\mu\text{A}$ |
| $C_o$                         | output capacitance                    |  | -                | 2   | 5           | pF            |
| <b>SPI and control</b>        |                                       |  |                  |     |             |               |
| $V_{IL}$                      | LOW-level input voltage               |  | -                | -   | $0.3V_{DD}$ | V             |
| $V_{IH}$                      | HIGH-level input voltage              |  | $0.7V_{DD}$      | -   | 5.5         | V             |
| $I_{IH}$                      | HIGH-level input current              | SDIN; $V_I = V_{DD} = 5.5\text{ V}$  | -                | 20  | 40          | $\mu\text{A}$ |
| $I_{OL}$                      | LOW-level output current              | SDOUT; $V_{OL} = 0.4\text{ V}$   |                  |     |             |               |
|                               |                                       | $V_{DD} = 4.5\text{ V}$  | 5                | -   | -           | mA            |
|                               |                                       | $V_{DD} = 2.5\text{ V}$  | 3                | -   | -           | mA            |
| $I_{OH}$                      | HIGH-level output current             | SDOUT; $V_{OH} = V_{DD} - 0.5\text{ V}$  |                  |     |             |               |
|                               |                                       | $V_{DD} = 4.5\text{ V}$  | -5               | -11 | -           | mA            |
|                               |                                       | $V_{DD} = 2.5\text{ V}$  | -3               | -7  | -           | mA            |
| $C_i$                         | input capacitance                     | $V_I = V_{SS}$ or $V_{DD}$   | -                | 2   | 5           | pF            |
| $C_o$                         | output capacitance                    | SDOUT; $\overline{CS} = V_{DD}$  | -                | 4   | 6           | pF            |

[1]  $V_{DD}$  must be lowered to 0.2 V for at least 5  $\mu\text{s}$  in order to reset device.

[2] Minimum  $V_{IL}$  is 2.0 V at  $V_{DD} = 4.5\text{ V}$ .

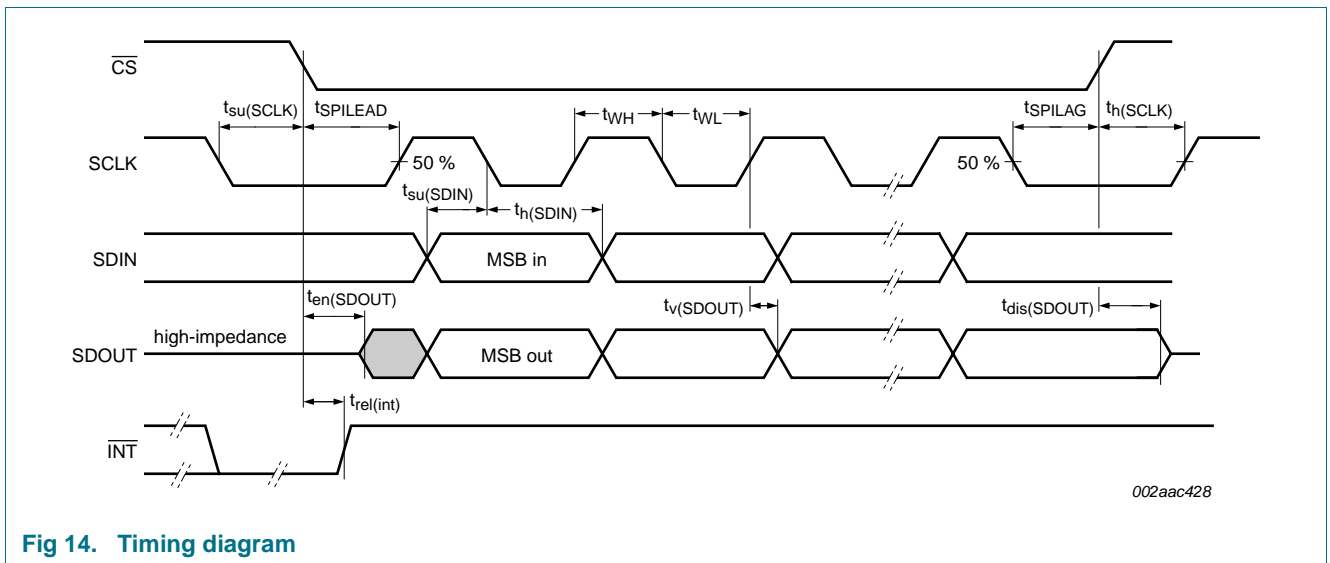
[3] For GPI pin voltages  $> 5.5\text{ V}$ , see [Section 7.3](#).

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol           | Parameter                          | Conditions   | Min | Typ | Max | Unit |
|------------------|------------------------------------|--|-----|-----|-----|------|
| $f_{max}$        | maximum input clock frequency      |  | -   | -   | 5   | MHz  |
| $t_r$            | rise time                          | SDOUT; 10 % to 90 % at 5 V   | -   | 35  | 60  | ns   |
| $t_f$            | fall time                          | SDOUT; 90 % to 10 % at 5 V   | -   | 25  | 50  | ns   |
| $t_{WH}$         | pulse width HIGH                   | SCLK   | 50  | -   | -   | ns   |
| $t_{WL}$         | pulse width LOW                    | SCLK   | 50  | -   | -   | ns   |
| $t_{SPILEAD}$    | SPI enable lead time               | $\overline{CS}$ falling edge to SCLK rising edge                                       | 50  | -   | -   | ns   |
| $t_{SPILAG}$     | SPI enable lag time                | SCLK falling edge to $\overline{CS}$ rising edge                                       | 50  | -   | -   | ns   |
| $t_{su(SDIN)}$   | SDIN set-up time                   | SDIN to SCLK falling edge  | 20  | -   | -   | ns   |
| $t_h(SDIN)$      | SDIN hold time                     | from SCLK falling edge   | 30  | -   | -   | ns   |
| $t_{en(SDOUT)}$  | SDOUT enable time                  | from $\overline{CS}$ LOW to SDOUT low-impedance; <a href="#">Figure 17</a>             | -   | -   | 55  | ns   |
| $t_{dis(SDOUT)}$ | SDOUT disable time                 | from rising edge of $\overline{CS}$ to SDOUT high-impedance; <a href="#">Figure 17</a> | -   | -   | 85  | ns   |
| $t_v(SDOUT)$     | SDOUT valid time                   | from rising edge of SCLK; <a href="#">Figure 18</a>                                    | -   | -   | 55  | ns   |
| $t_{su(SCLK)}$   | SCLK set-up time                   | SCLK falling to $\overline{CS}$ falling  | 50  | -   | -   | ns   |
| $t_h(SCLK)$      | SCLK hold time                     | SCLK rising after $\overline{CS}$ rising   | 50  | -   | -   | ns   |
| $t_{POR}$        | power-on reset pulse time          | time before $\overline{CS}$ is active after $V_{DD} > V_{POR}$                         | -   | -   | 250 | ns   |
| $t_{rel(int)}$   | interrupt release time             | after $\overline{CS}$ going LOW; <a href="#">Figure 19</a>                             | -   | -   | 500 | ns   |
| $t_v(INT\_N)$    | valid time on pin $\overline{INT}$ | after $IN_n$ changes or $INT\_EN$ goes HIGH  | -   | -   | 100 | ns   |



**Fig 14. Timing diagram**



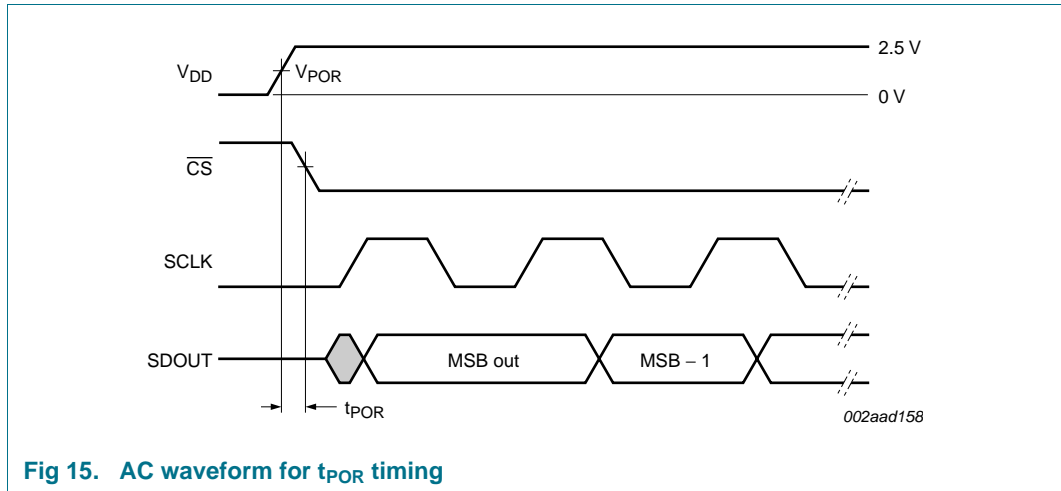


Fig 15. AC waveform for  $t_{\text{POR}}$  timing

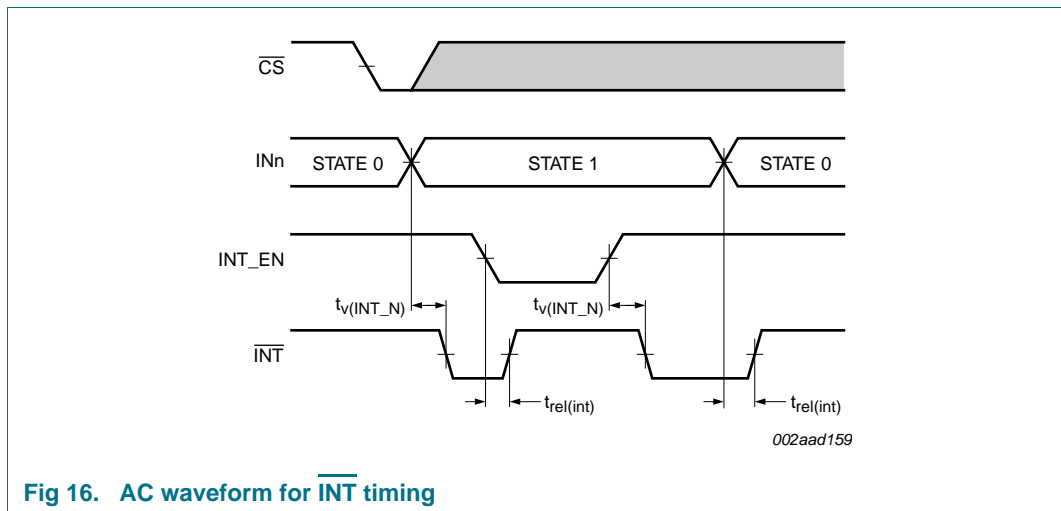


Fig 16. AC waveform for  $\overline{\text{INT}}$  timing

12. Test information

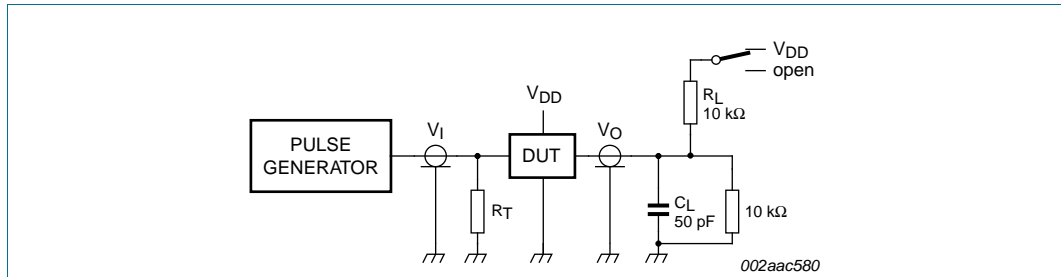


Fig 17. Test circuitry for enable/disable times, SDOUT ( $t_{en(\text{SDOUT})}$  and  $t_{dis(\text{SDOUT})}$ )

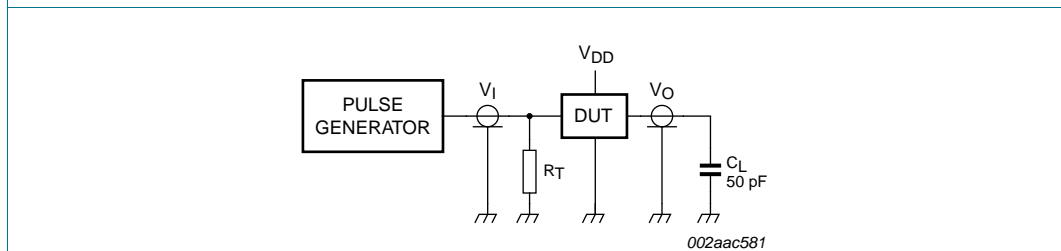


Fig 18. Test circuitry for switching times, SDOUT ( $t_{v(\text{SDOUT})}$ )

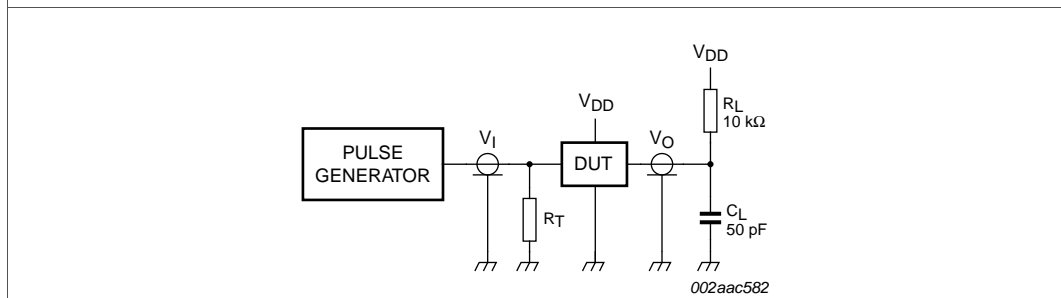


Fig 19. Test circuitry for switching times,  $\overline{\text{INT}}$

$R_L$  = load resistance.

$C_L$  = load capacitance includes jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generators.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

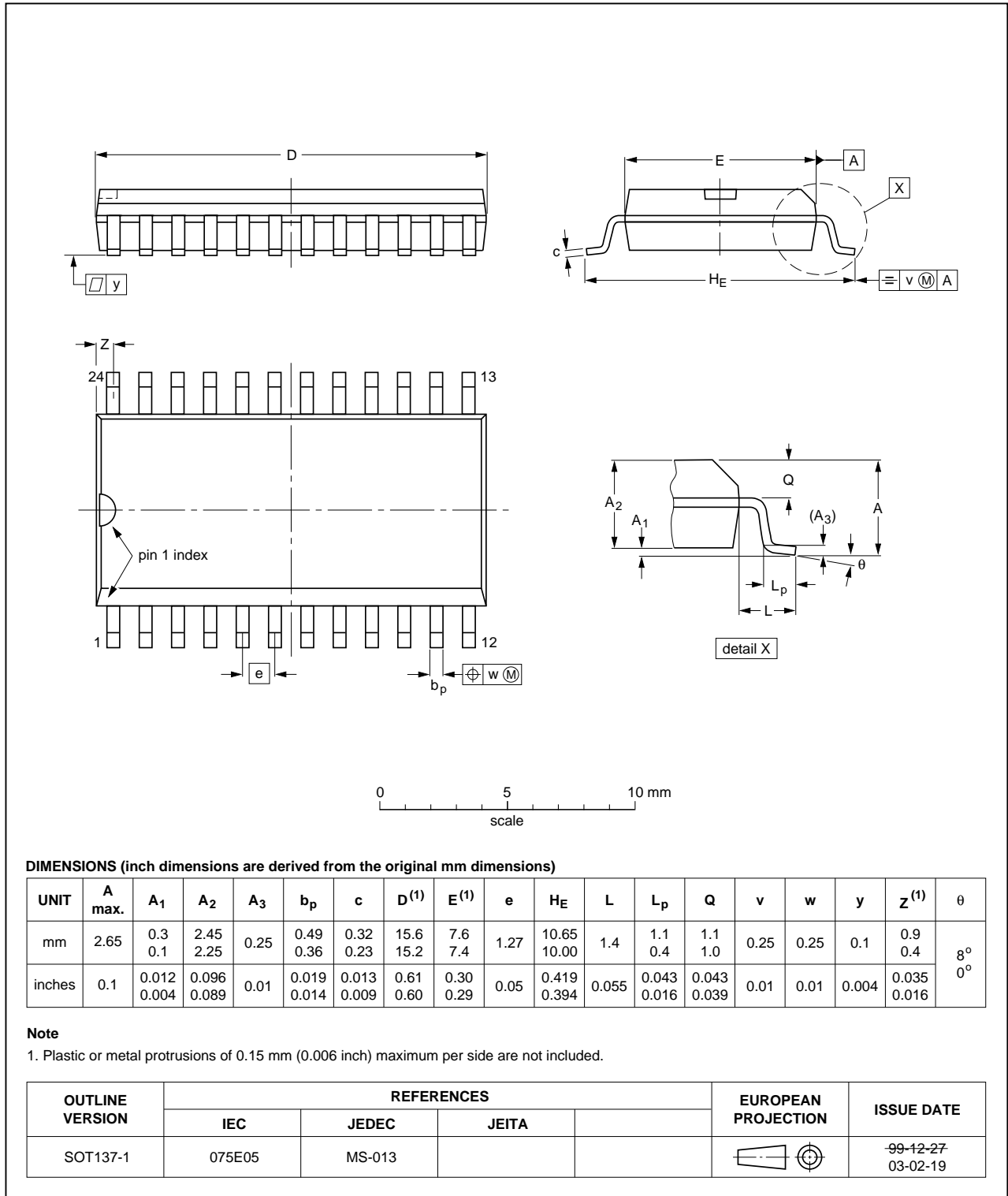


Fig 20. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

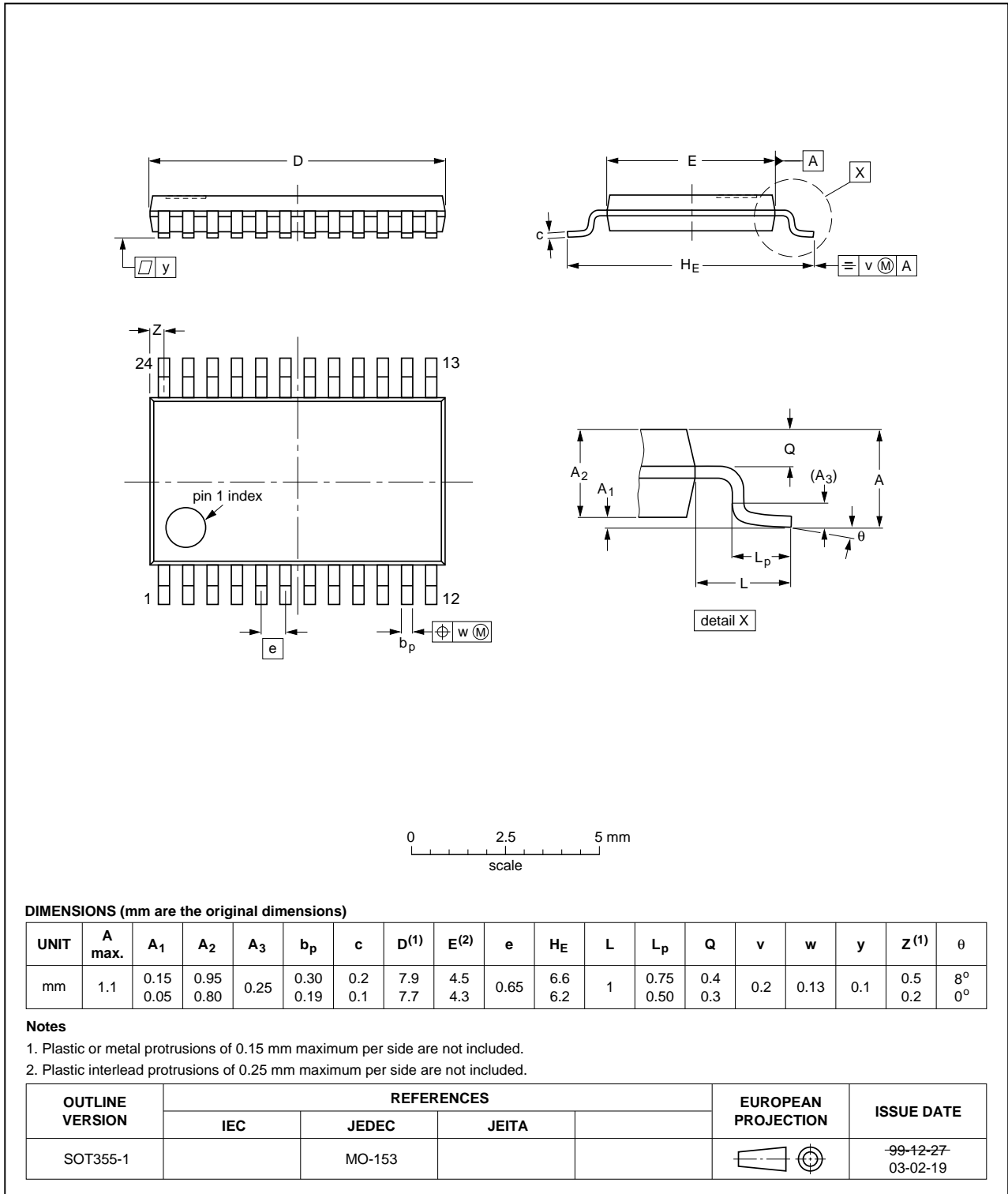


Fig 21. Package outline SOT355-1 (TSSOP24)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

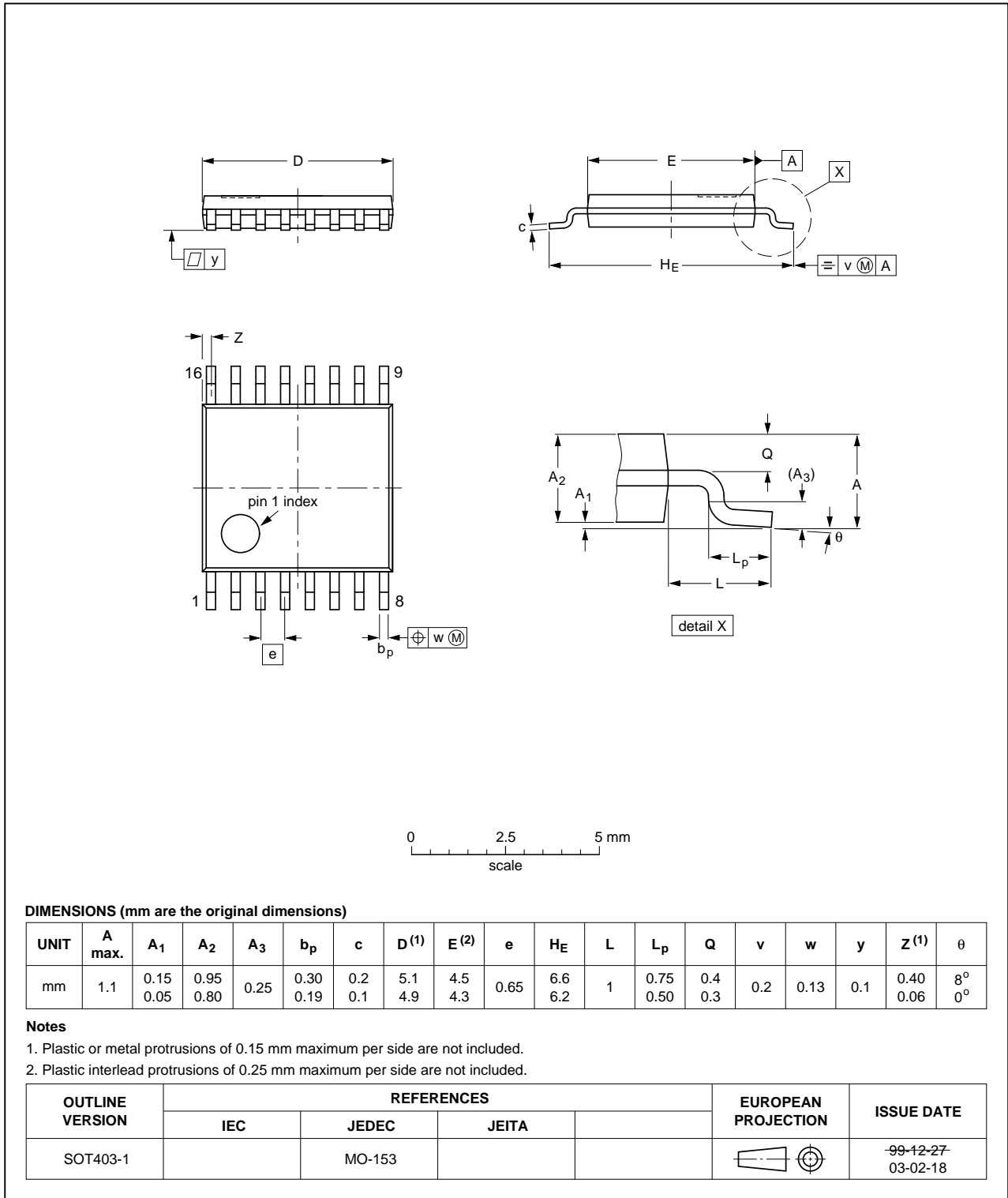
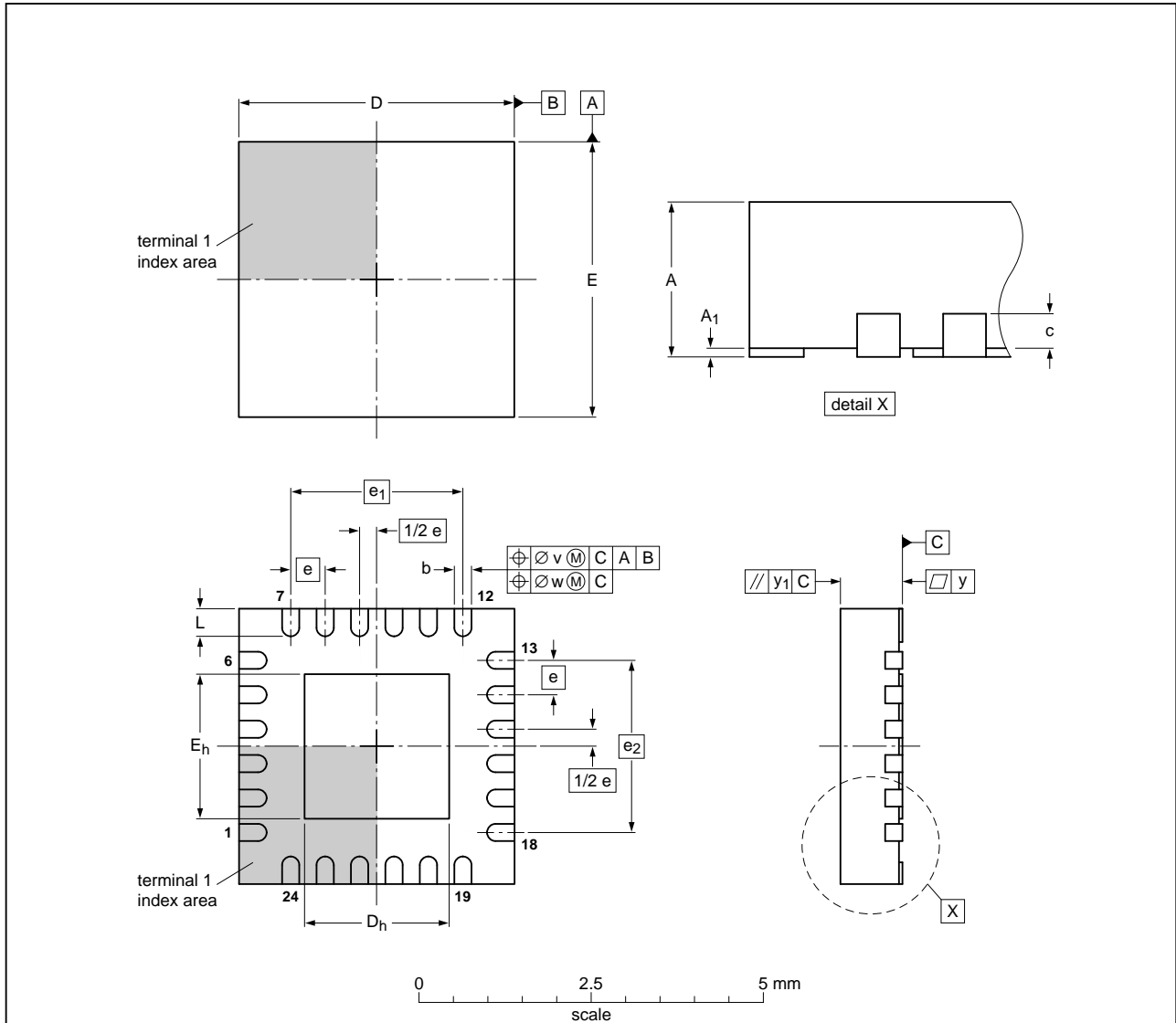


Fig 22. Package outline SOT403-1 (TSSOP16)

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads;  
24 terminals; body 4 x 4 x 0.75 mm

SOT994-1



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A <sup>(1)</sup><br>max | A <sub>1</sub> | b            | c   | D <sup>(1)</sup> | D <sub>h</sub> | E <sup>(1)</sup> | E <sub>h</sub> | e   | e <sub>1</sub> | e <sub>2</sub> | L          | v   | w    | y    | y <sub>1</sub> |
|------|-------------------------|----------------|--------------|-----|------------------|----------------|------------------|----------------|-----|----------------|----------------|------------|-----|------|------|----------------|
| mm   | 0.8                     | 0.05<br>0.00   | 0.30<br>0.18 | 0.2 | 4.1<br>3.9       | 2.25<br>1.95   | 4.1<br>3.9       | 2.25<br>1.95   | 0.5 | 2.5            | 2.5            | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1            |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |        |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|--------|-------|--|------------------------|----------------------|
|                    | IEC        | JEDEC  | JEITA |  |                        |                      |
| SOT994-1           | ---        | MO-220 | ---   |  |                        | 07-02-07<br>07-03-03 |

Fig 23. Package outline SOT994-1 (HWQFN24)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 24](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

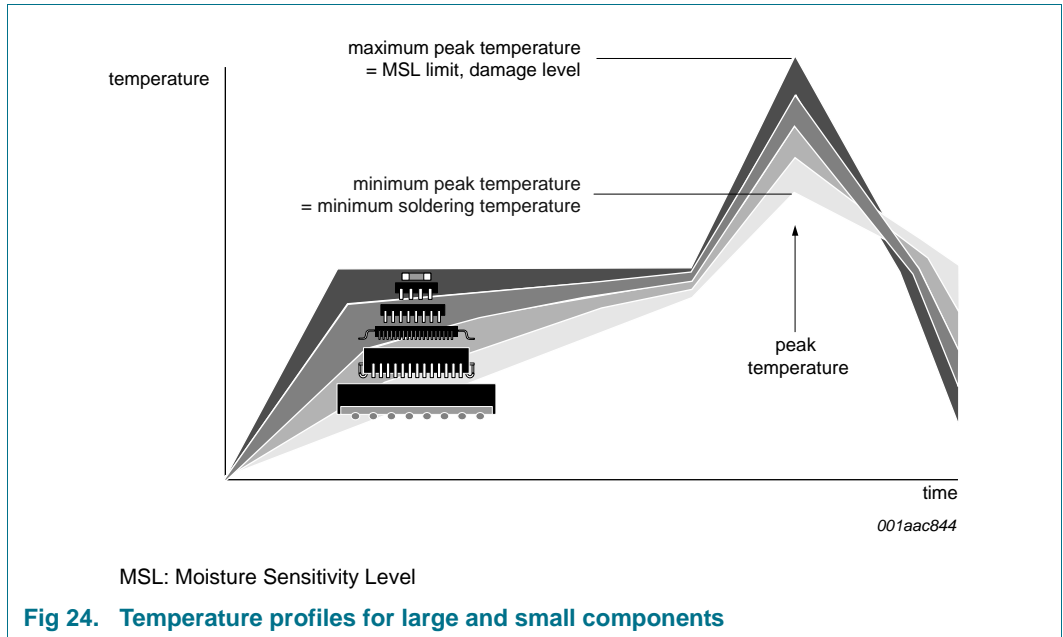
Table 9. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 24](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Abbreviations

Table 10. Abbreviations

| Acronym | Description                           |
|---------|---------------------------------------|
| ASSP    | Application Specific Standard Product |
| CAN     | Controller Area Network               |
| CDM     | Charged-Device Model                  |
| DUT     | Device Under Test                     |
| ECU     | Electronic Control Unit               |
| ESD     | ElectroStatic Discharge               |
| GPI     | General Purpose Input                 |
| HBM     | Human Body Model                      |
| HS-CAN  | High-Speed Controller Area Network    |
| LIN     | Local Interconnect Network            |
| LSB     | Least Significant Bit                 |
| MM      | Machine Model                         |
| MSB     | Most Significant Bit                  |
| PCB     | Printed-Circuit Board                 |
| PPAP    | Production Part Approval Process      |
| RC      | Resistor-Capacitor network            |
| SBC     | System Basis Chip                     |
| SPI     | Serial Peripheral Interface           |
| μC      | microcontroller                       |

## 16. Revision history

Table 11. Revision history

| Document ID         | Release date   | Data sheet status    | Change notice | Supersedes          |
|---------------------|--|----------------------|---------------|---------------------|
| PCA9701_PCA9702 v.7 | 20140926   | Product data sheet   | -             | PCA9701_PCA9702 v.6 |
| Modifications:      | <ul style="list-style-type: none"> <li>• <a href="#">Section 1 “General description”</a>, <a href="#">Section 2 “Features and benefits”</a>: deleted references to “AEC-Q100”</li> <li>• <a href="#">Table 1 “Ordering information”</a>: <ul style="list-style-type: none"> <li>– removed type number PCA9701PW/Q900 (and associated table note [1])</li> </ul> </li> <li>• <a href="#">Figure 3 “Pin configuration for TSSOP24”</a> deleted “PCA9701PW/Q900”</li> <li>• Added <a href="#">Table 2 “Ordering options”</a></li> </ul> |                      |               |                     |
| PCA9701_PCA9702 v.6 | 20111214   | Product data sheet   | -             | PCA9701_PCA9702 v.5 |
| PCA9701_PCA9702 v.5 | 20091111   | Product data sheet   | -             | PCA9701_PCA9702 v.4 |
| PCA9701_PCA9702 v.4 | 20090716   | Product data sheet   | -             | PCA9701_PCA9702 v.3 |
| PCA9701_PCA9702 v.3 | 20081203   | Product data sheet   | -             | PCA9701_PCA9702 v.2 |
| PCA9701_PCA9702 v.2 | 20070829   | Product data sheet   | -             | PCA9701_PCA9702 v.1 |
| PCA9701_PCA9702 v.1 | 20070323   | Objective data sheet | -             | -                   |

## 17. Legal information

### 17.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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