## General Description

The 843S104I-133 is a PLL-based clock synthesizer specifically designed for low phase noise applications. This device generates a 133.33MHz differential LVPECL clock from an input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference is applied to the PCLK, nPCLK pins.The device offers spread spectrum clock output for reduced EMI applications. An I$^2$C bus interface is used to enable or disable spread spectrum operation as well as to select either a down spread value of -0.35% or -0.5%.The 843S104I-133 is available in a lead-free 32-Lead VFQFN package.

## Features

- Four LVPECL output pairs
- Crystal oscillator interface: 25MHz
- Differential PCLK, nPCLK input pair
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Output frequency: 133.33MHz
- PCI Express (2.5 Gb/s) and Gen 2 (5 Gb/S) jitter compliant
- RMS phase jitter @ 133.33MHz (12kHz – 20MHz): 1.2ps (typical)
- I$^2$C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

## Block Diagram
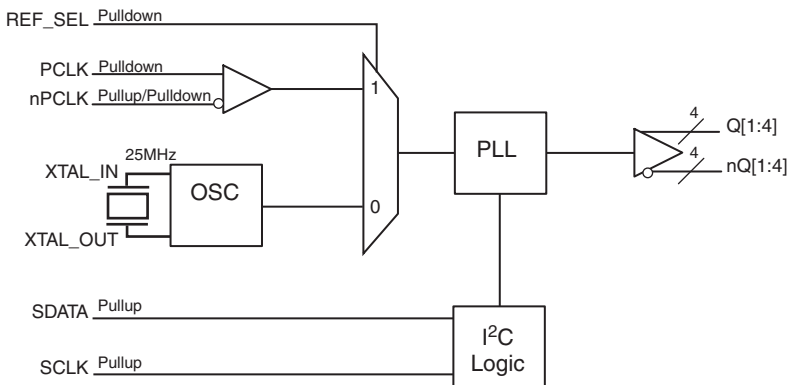


## Pin Assignment
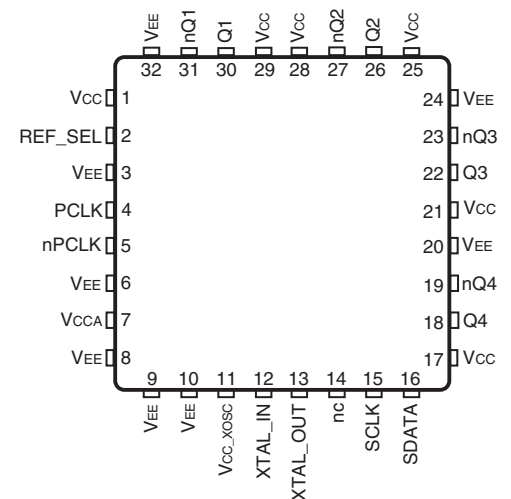


**843S104I-133**
**32-Lead VFQFN**
**5.0mm x 5.0mm package body**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 17, 21, 25, 28, 29 | $V_{CC}$ | Power | | Core supply pins. |
| 2 | REF_SEL | Input | Pulldown | Select input for XTAL (LOW) or REF_IN (HIGH). LVCMOS/LVTTL interface levels. |
| 3, 6, 8, 9, 10, 20, 24, 32 | $V_{EE}$ | Power | | Negative power supply pins. |
| 4 | PCLK | Input | Pulldown | Non-inverting external 25MHz differential reference input. LVPECL input levels. |
| 5 | nPCLK | Input | Pullup/ Pulldown | Inverting external 25MHz differential reference input. LVPECL input levels. |
| 7 | $V_{CCA}$ | Power | | Analog supply for PLL. |
| 11 | $V_{CC\_XOSC}$ | Power | | Analog supply for crystal oscillator. |
| 12, 13 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 14 | nc | Unused | | No connect. |
| 15 | SCLK | Input | Pullup | I2C compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels. |
| 16 | SDATA | I/O | Pullup | I2C compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels. |
| 18,19 | Q4, nQ4 | Output | | Differential output pair. LVPECL interface levels. |
| 22, 23 | Q3, nQ3 | Output | | Differential output pair. LVPECL interface levels. |
| 26, 27 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |
| 30, 31 | Q1, nQ1 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup and Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal I$^2$C serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the serial interface initialize to their default settings upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

# Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3A.

The block write and block read protocol is outlined in Table 3B, while Table 3C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3A.Command Code Definition**

| Bit | 7 | 6, 5 | 4:0 |
|---|---|---|---|
| **Description** | 0 = Block read or block write operation, 1 = Byte read or byte write operation. | Chip select address, set to "00" to access device. | Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be "00000". |

**Table 3B. Block Read and Block Write Protocol**

| Bit | Description = Block Write | Bit | Description = Block Read |
|---|---|---|---|
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits | 11:18 | Command Code - 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29:36 | Data byte 1 - 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 - 8 bits | 30:37 | Byte Count from slave - 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte/Slave Acknowledges | 39:46 | Data Byte 1 from slave - 8 bits |
| | Data Byte N - 8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 48:55 | Data Byte 2 from slave - 8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data Bytes from Slave/Acknowledge |
| | | | Data Byte N from slave - 8 bits |
| | | | Not Acknowledge |
| | | | Stop |

**Table 3C. Byte Read and Byte Write Protocol**

| Bit | Description = Byte Write | Bit | Description = Byte Read |
|---|---|---|---|
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits | 11:18 | Command Code - 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data from slave - 8 bits |
| | | 38 | Not Acknowledge |
| | | 39 | Stop |

# Control Registers

**Table 3D. Byte 0: Control Register 0**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 1 | Q4EN | Q4, nQ4 Output Enable<br>0 = Low<br>1 = Enable |
| 5 | 1 | Q3EN | Q3, nQ3 Output Enable<br>0 = Low1 = Enable |
| 4 | 1 | Q2EN | Q2, nQ2 Output Enable<br>0 = Low<br>1 = Enable |
| 3 | 1 | Q1EN | Q1, nQ1 Output Enable<br>0 = Low<br>1 = Enable |
| 2 | 1 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3E. Byte 1: Control Register 1**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3F. Byte 2: Control Register 2**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 1 | SS_SEL | Spread Spectrum Selection<br>0 = -0.35%, 1 = - 0.5% |
| 6 | 1 | Reserved | Reserved |
| 5 | 1 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 0 | SSM | Q Spread Spectrum Enable<br>0 = Spread Off,<br>1 = Spread On |
| 1 | 1 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3G. Byte 3:Control Register 3**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 1 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 1 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 1 | Reserved | Reserved |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Table 3H. Byte 4: Control Register 4**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Table 3I. Byte 5: Control Register 5**

| Bit | @Power-up | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3J. Byte 6: Control Register 6**

| Bit | @Power-up | Name | Description |
|-----|-----------|------|-------------|
| 7 | 0 | TEST_SEL | REF/N or Hi-Z Select<br>0 = Hi-Z, 1 = REF/N |
| 6 | 0 | TEST_MODE | TEST Clock Mode Entry Control<br>0 = Normal Operation,<br>1 = REF/N or Hi-Z Mode |
| 5 | 0 | Reserved | Reserved |
| 4 | 1 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Table 3K. Byte 7: Control Register 7**

| Bit | @Power-up | Name | Description |
|-----|-----------|------|-------------|
| 7 | 0 | | Revision Code Bit 3 |
| 6 | 0 | | Revision Code Bit 2 |
| 5 | 0 | | Revision Code Bit 1 |
| 4 | 0 | | Revision Code Bit 0 |
| 3 | 0 | | Vendor ID Bit 3 |
| 2 | 0 | | Vendor ID Bit 2 |
| 1 | 0 | | Vendor ID Bit 1 |
| 0 | 1 | | Vendor ID Bit 0 |

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|------|--------|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ (LVPECL)<br>  Continuous Current<br>  Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 39.5°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics, $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ − 0.22 | 3.3 | $V_{CC}$ | V |
| $V_{CC\_XOSC}$ | Analog Supply Voltage | | $V_{CC}$ − 0.05 | 3.3 | $V_{CC}$ | V |
| $I_{EE}$ | Power Supply Current | | | | 130 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 22 | mA |
| $I_{CC\_XOSC}$ | Crystal Oscillator Supply Current | | | | 5 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|--|-----------------|---------|---------|---------|-------|
| $V_{IH}$ | Input High Voltage | SDATA, SCLK | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | SDATA, SCLK | | 1.7 | | $V_{CC}$ + 0.3 | V |
| $I_{IH}$ | Input High Current | SDATA, SCLK | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 10 | μA |
| | | REF_SEL | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 150 | μA |
| $I_{IL}$ | Input Low Current | SDATA, SCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | μA |
| | | REF_SEL | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | μA |

**Table 4C. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C)

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|--|-----------------|---------|---------|---------|-------|
| $I_{IH}$ | Input High Current | PCLK, nPCLK | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 150 | μA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | μA |
| | | nPCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | μA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.3 | | 1.0 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage; NOTE 3 | | | $V_{CC}$ − 1.3 | | $V_{CC}$ − 0.8 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 3 | | | $V_{CC}$ − 2.0 | | $V_{CC}$ − 1.6 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | | 0.6 | | 1.0 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.
NOTE 3: Outputs terminated with 50Ω to $V_{CC}$ − 2V.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------|---------|---------|---------|-------|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

  — 

# AC Electrical Characteristics

**Table 6. AC Characteristics, $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$ | Output Frequency | | | 133.33 | | MHz |
| $f_{REF}$ | Reference Frequency | | | 25 | | MHz |
| $tjit(\varnothing)$ | RMS Phase Jitter, (Random); NOTE 1 | SSC Off, Integration Range: 12kHz – 20MHz | | 1.2 | | ps |
| $t_j$ | Phase Jitter Peak-to-Peak; NOTE 2 | Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 11 | | ps |
| $t_{REFCLK\_HF\_RMS}$ | Phase Jitter rms; NOTE 3 | 133.33MHz 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2 | | 1.3 | | ps |
| $t_{REFCLK\_LF\_RMS}$ | Phase Jitter rms; NOTE 3 | 133.33MHz 25MHz crystal input Low Band: 10kHz - 1.5MHz | | 0.21 | | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 100 | | 250 | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Please refer to Phase Noise Plot.

NOTE 2: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of $10^6$ clock periods. See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

NOTE 3: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps rms for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0 ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

## Typical Phase Noise at 133.33MHz



**Offset Frequency (Hz)**
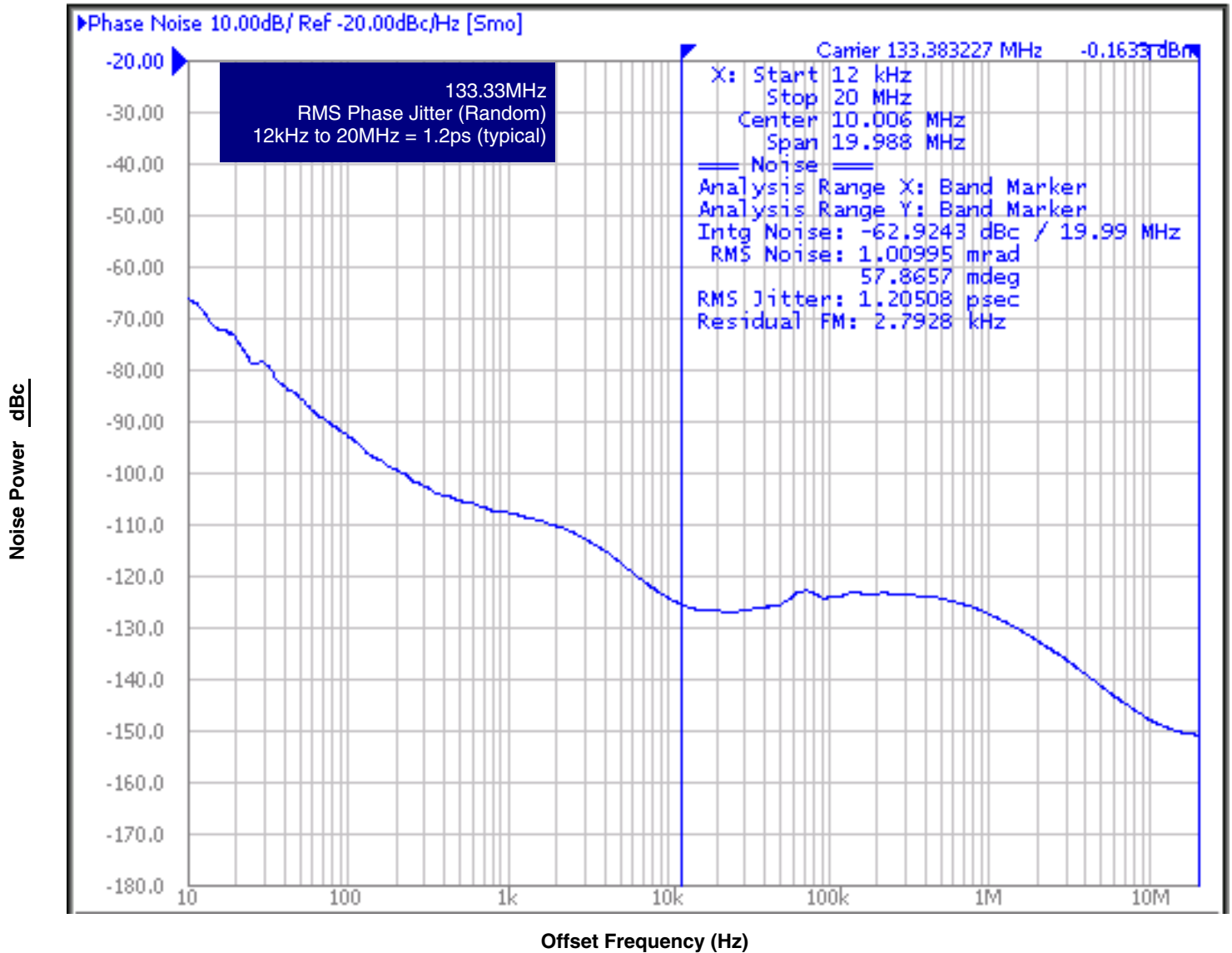
# Parameter Measurement Information
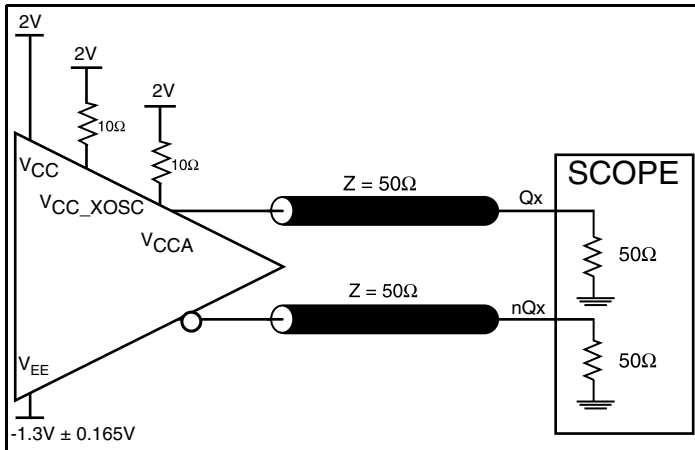
**3.3V LVPECL Output Load AC Test Circuit**
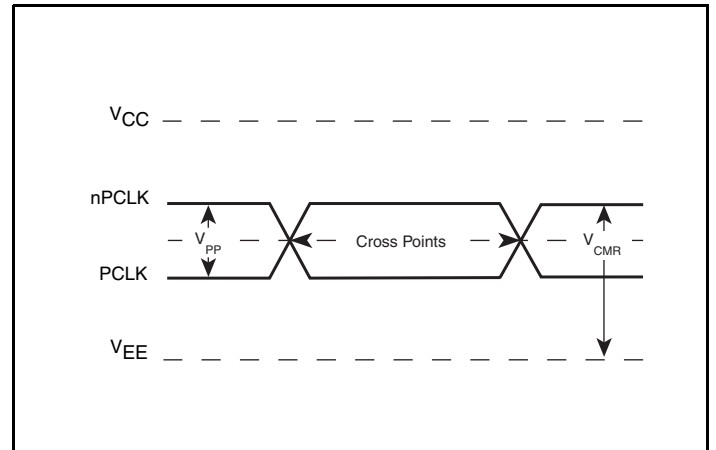
**Differential Input Level**

**RMS Phase Jitter**

$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$
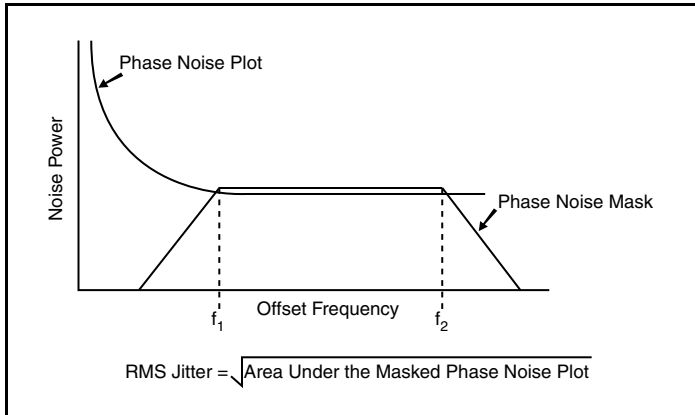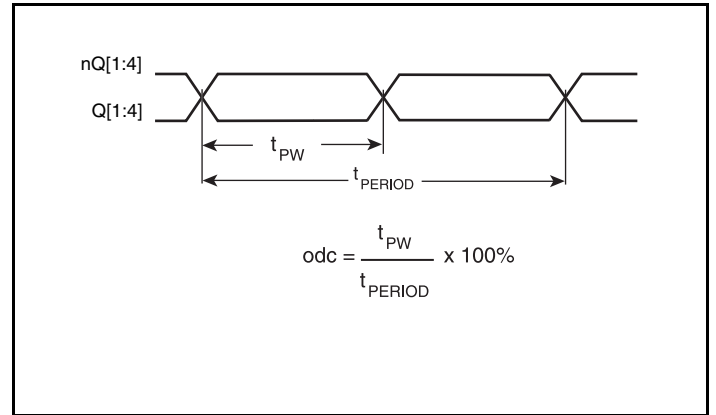
**Output Duty Cycle/Pulse Width/Period**

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
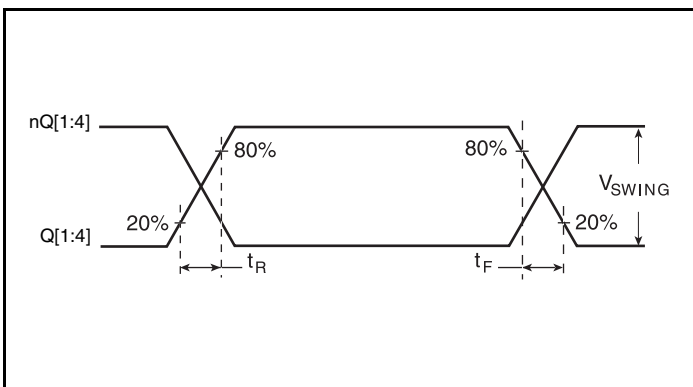
**Rise/Fall Time**

# Applications Information

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843S104I-133 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CC\_XOSC}$ and $V_{CCA}$ should be individually connected to the power supply plane through vias, and 0.01μF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{CC}$ pin and also shows that $V_{CCA}$ requires that an additional 10Ω resistor along with a 10μF bypass capacitor be connected to the $V_{CCA}$ pin.
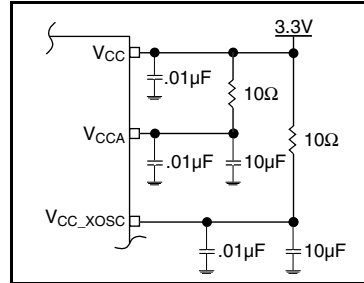


**Figure 1. Power Supply Filtering**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullup and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The 843S104I-133 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
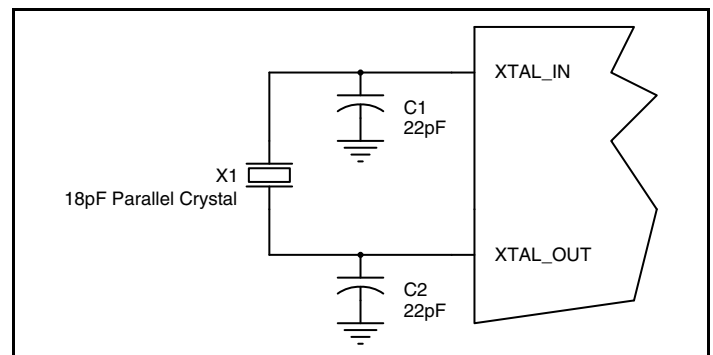


**Figure 2. Crystal Input Interface**

# Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 3B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.
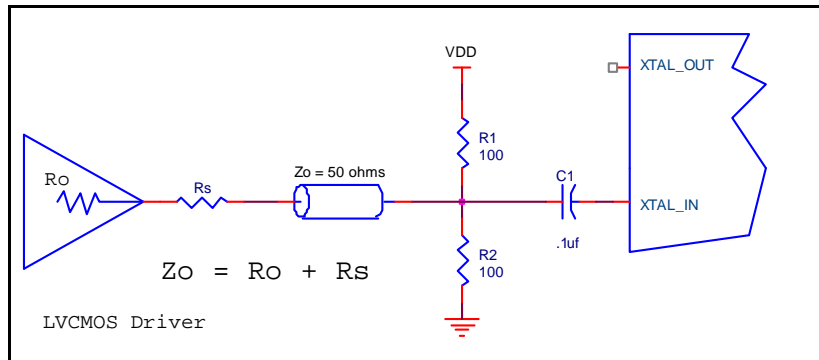
**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**
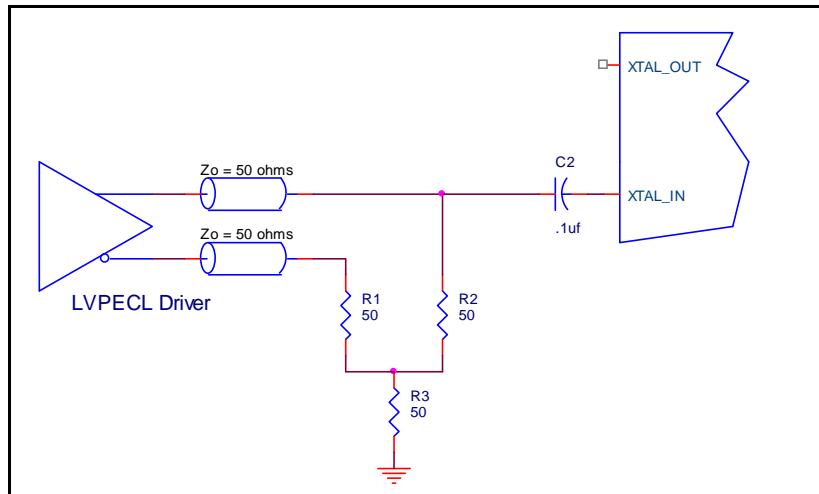
**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 4A to 4F* show interface examples for PCLK/nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.
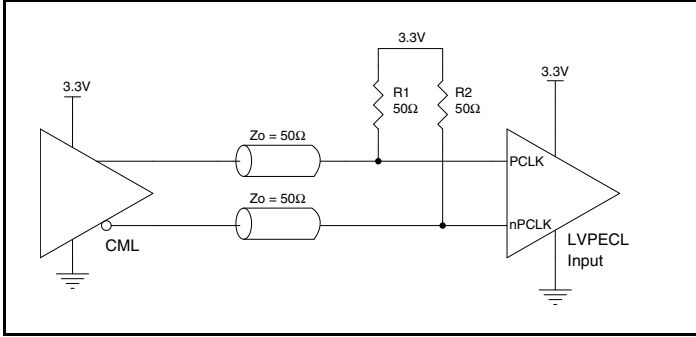


**Figure 4A.   PCLK/nPCLK Input
Driven by a CML Driver**
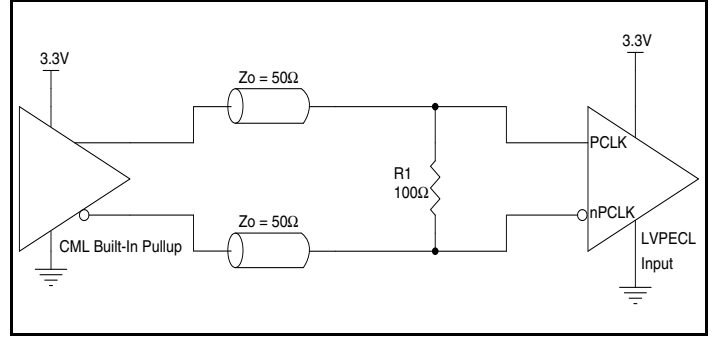


**Figure 4B.   PCLK/nPCLK Input
Driven by a Built-In Pullup CML Driver**
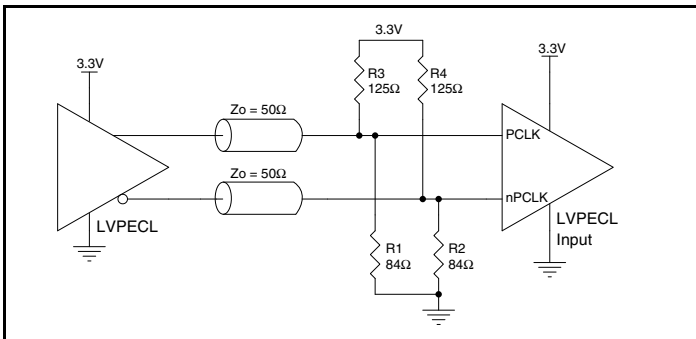


**Figure 4C.   PCLK/nPCLK Input
Driven by a 3.3V LVPECL Driver**
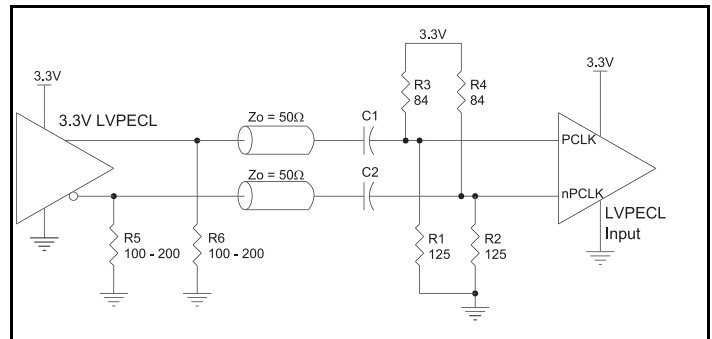


**Figure 4D.   PCLK/nPCLK Input Driven by
a 3.3V LVPECL Driver with AC Couple**
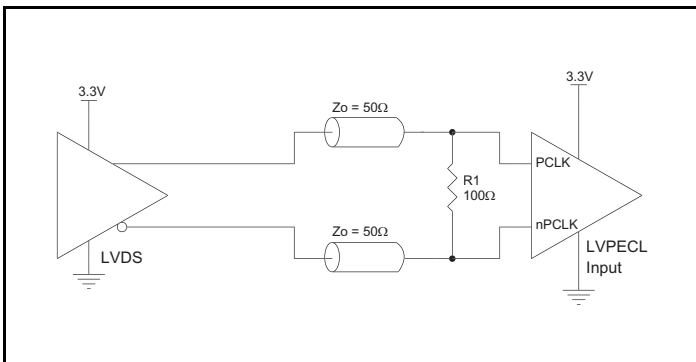


**Figure 4E.   PCLK/nPCLK Input Driven by
a 3.3V LVDS Driver**
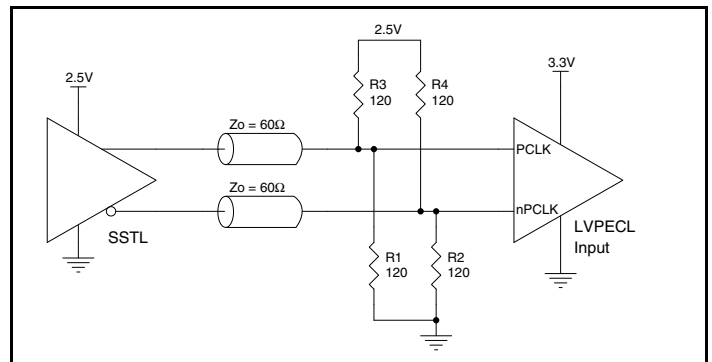


**Figure 4F.   PCLK/nPCLK Input
Driven by an SSTL Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
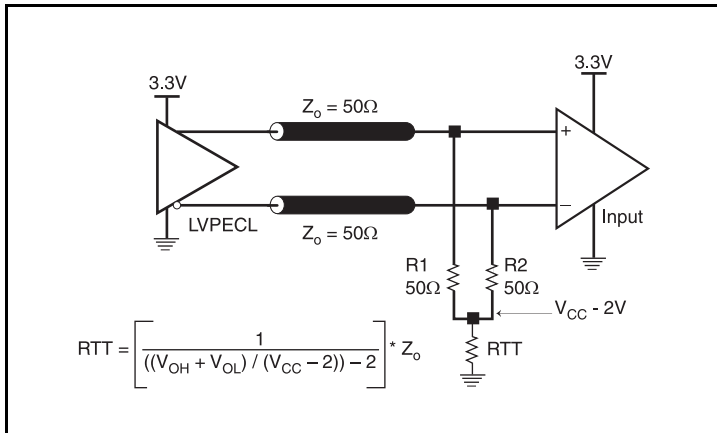
**Figure 5A. 3.3V LVPECL Output Termination**
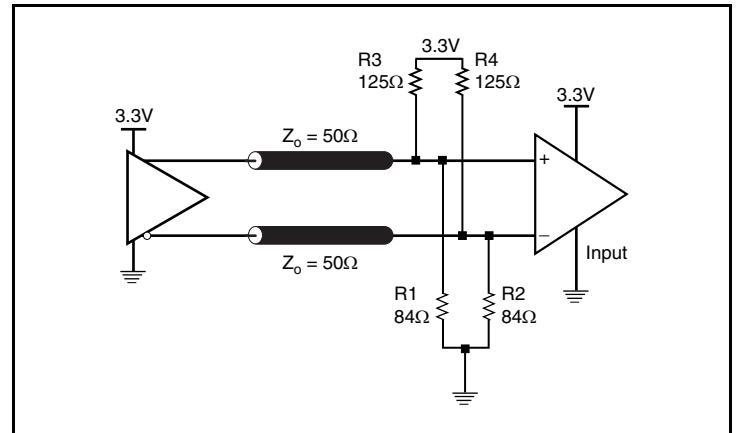
**Figure 5B. 3.3V LVPECL Output Termination**

$$RTT = \left[ \frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2} \right] * Z_o$$

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.
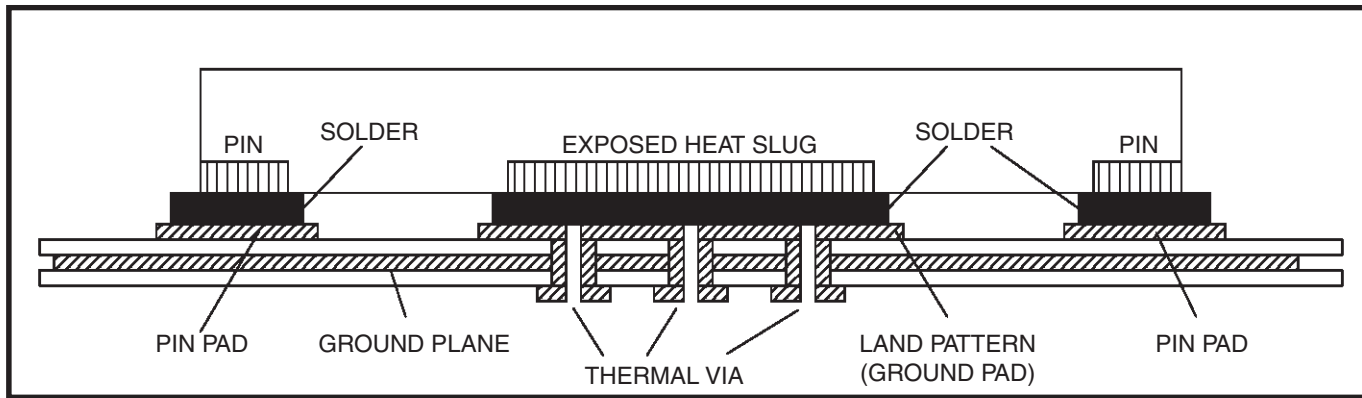


**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Schematic Example

*Figure 7* shows an example of 843S104I-133 application schematic. In this example, the device is operated at $V_{CC}$ = 3.3V.

The 18pF parallel resonant 25MHz crystal is used. The C1 and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing

frequency accuracy. for the LVPECL output drivers, only two termination examples are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.
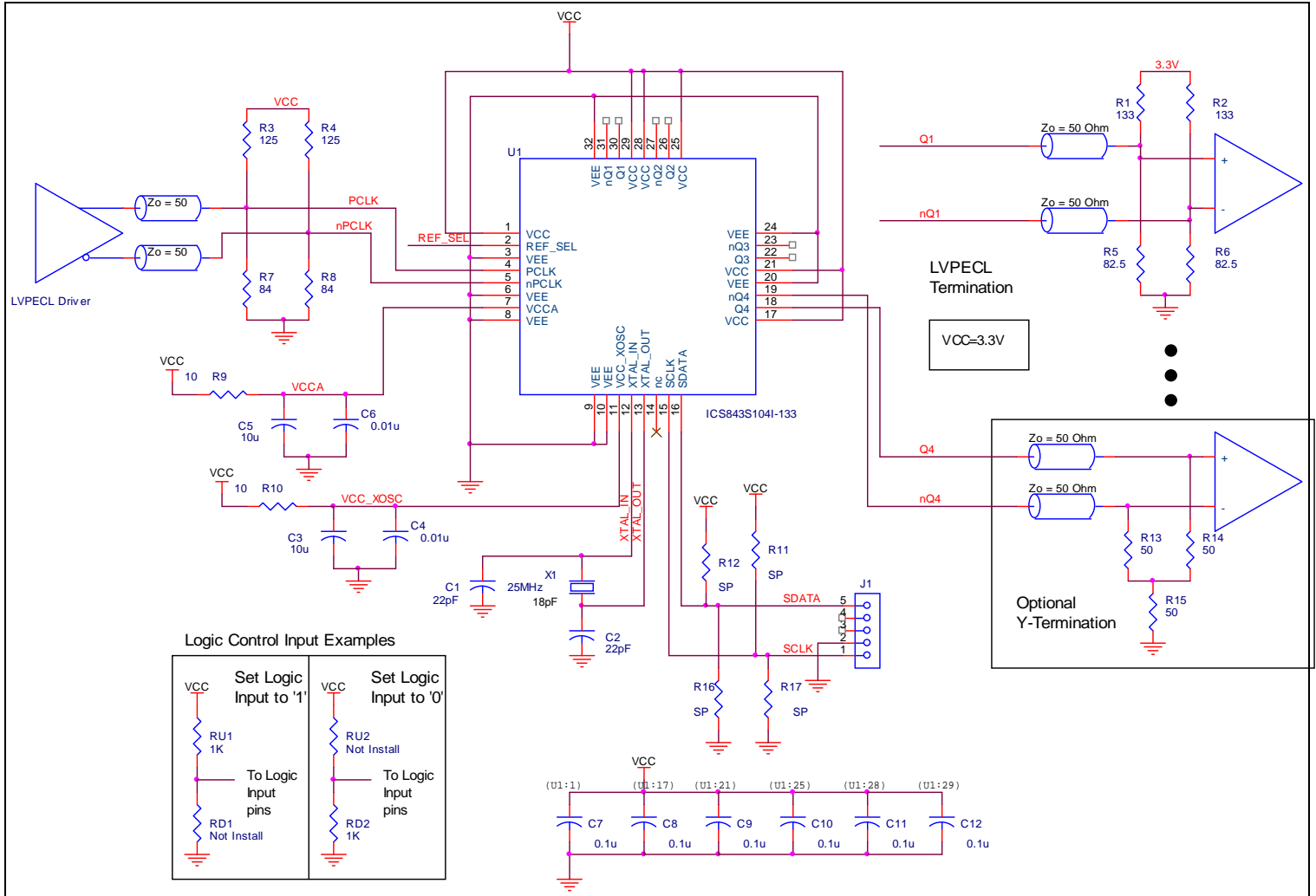


**Figure 7. 843S104I-133 Schematic Layout**

# PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].
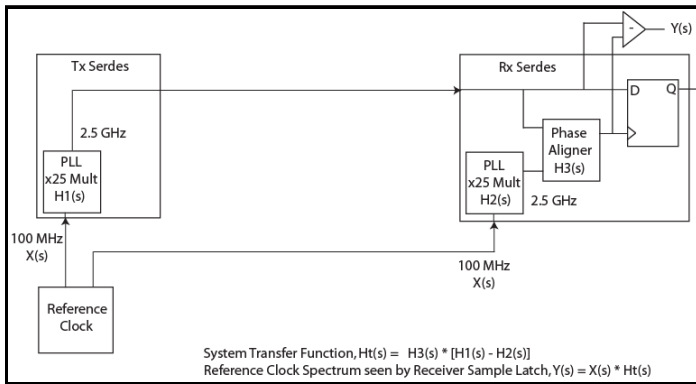


**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.
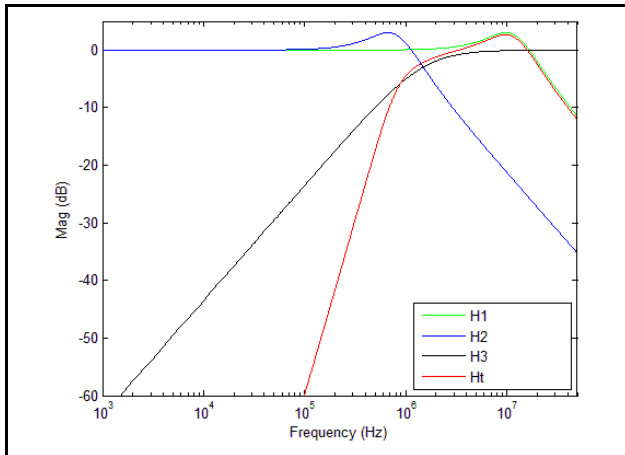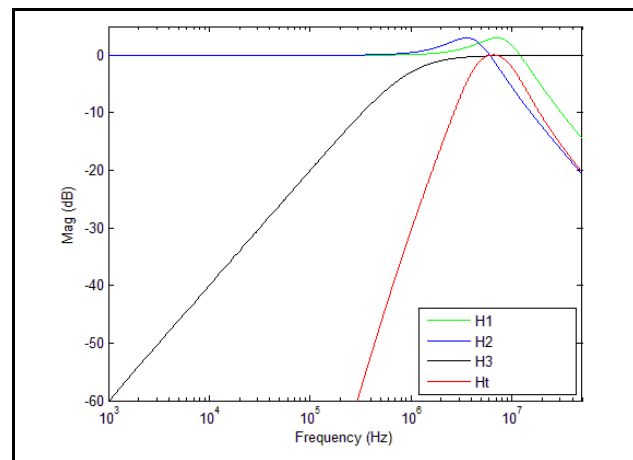


**PCIe Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.
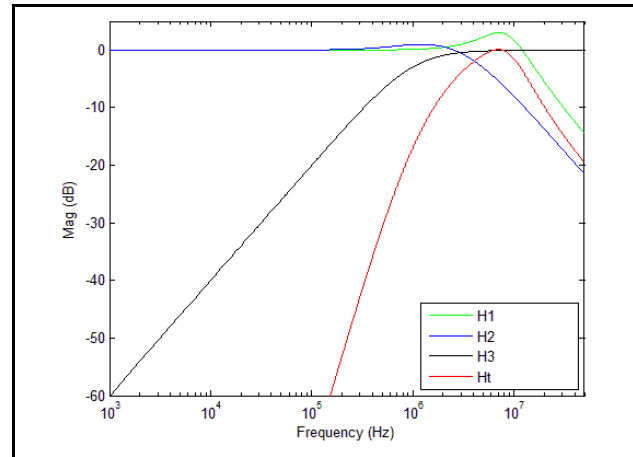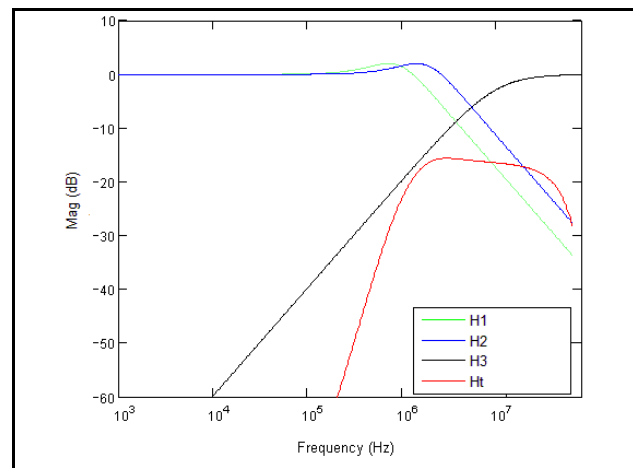


**PCIe Gen 2A Magnitude of Transfer Function**



**PCIe Gen 2B Magnitude of Transfer Function**

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

# Power Considerations

This section provides information on power dissipation and junction temperature for the 843S104I-133.
Equations and example calculations are also provided.

**1. Power Dissipation.**

The total power dissipation for the 843S104I-133 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 130mA = **450.45mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32mW = **128mW**

**Total Power**$_{\_MAX}$ (3.3V, with all outputs switching) = 450.45mW + 128mW = **578.45mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.578W * 39.5°C/W = 107.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resitance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

**3. Calculations and Equations.**

The purpose of this section is to derive the power dissipated into the load.

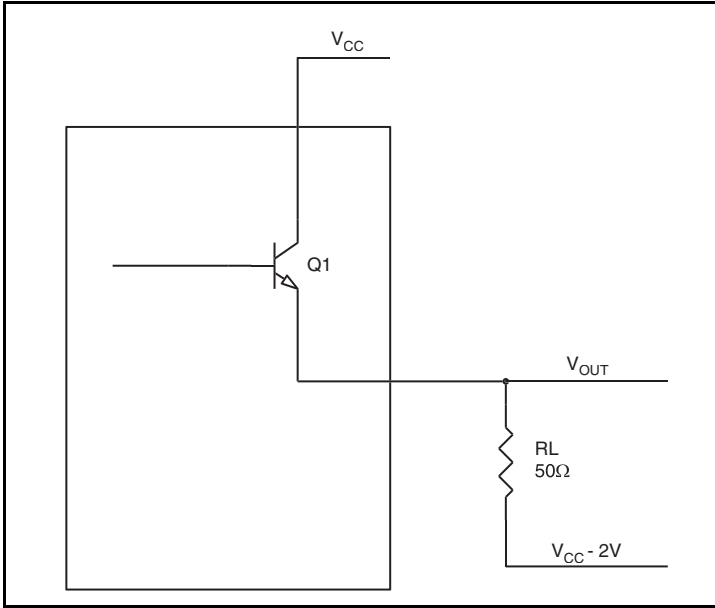LVPECL output driver circuit and termination are shown in *Figure 8.*



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \textbf{V}_{CC\_MAX} - \textbf{0.8V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \textbf{0.8V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \textbf{V}_{CC\_MAX} - \textbf{1.6V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \textbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.8V)/50\Omega] * 0.8V = \textbf{19.2mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.6V)/50\Omega] * 1.6V = \textbf{12.8mW}$

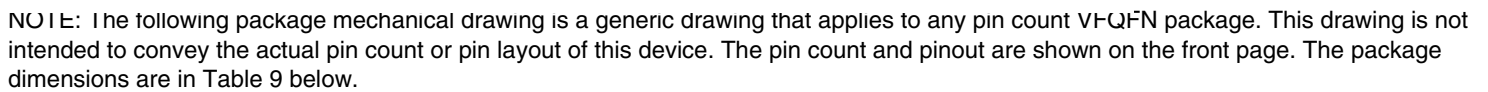Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

# Transistor Count

The transistor count for 843S104I-133 is: 11,927

# Package Outline and Package Dimensions

## Package Outline - K Suffix for 32 Lead VFQFN

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9 below.

**Table 9. Package Dimensions**

| JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters | | | |
|---|---|---|---|
| Symbol | Minimum | Nominal | Maximum |
| N | | 32 | |
| A | 0.80 | | 1.00 |
| A1 | 0 | | 0.05 |
| A3 | | 0.25 Ref. | |
| b | 0.18 | 0.25 | 0.30 |
| $N_D$ & $N_E$ | | | 8 |
| D & E | | 5.00 Basic | |
| D2 & E2 | 3.0 | | 3.3 |
| e | | 0.50 Basic | |
| L | 0.30 | 0.40 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 843S104BKI-133LF | ICS04BI133L | "Lead-Free" 32 Lead VFQFN | Tray | -40°C to 85°C |
| 843S104BKI-133LFT | ICS04BI133L | "Lead-Free" 32 Lead VFQFN | Tape & Reel | -40°C to 85°C |

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| B | | 11<br>12<br>14<br>17 | Updated header/footer throughout the datasheet.<br>Deleted *IDT* prefix from part number.<br>Application Information, updated:<br>  Updated *Overdriving the XTAL Interface*,<br>  *Termination for 3.3V LVPECL Outputs*<br>  *PCI Express Application Note* | 10/20/15 |
| | T10 | 22 | Ordering Information Table - deleted Tape & Reel Count, and table note. | |
| B | | | Updated data sheet headers and footers. | 4/28/16 |