

### FEATURES

- Very low offset voltage  
125  $\mu\text{V}$  maximum
- Supply current: 215  $\mu\text{A}/\text{amp}$  typical
- Input bias current: 200 pA maximum
- Low input offset voltage drift: 1.2  $\mu\text{V}/^\circ\text{C}$  maximum
- Very low voltage noise: 11 nV/ $\sqrt{\text{Hz}}$
- Operating temperature:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Rail-to-rail output swing
- Unity gain stable
- $\pm 2.5\text{V}$  to  $\pm 15\text{V}$  operation

### APPLICATIONS

- Portable precision instrumentation
- Laser diode control loops
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers

### GENERAL DESCRIPTION

The AD8622/AD8624 are dual and quad precision rail-to-rail output operational amplifiers with low supply currents of only 350  $\mu\text{A}/\text{amplifier}$  maximum over temperature and supply voltages. The AD8622/AD8624 also has an input bias current cancellation circuitry that provides a very low input bias current over the full operating temperature.

With a typical offset voltage of only 10  $\mu\text{V}$ , offset drift of 0.5  $\mu\text{V}/^\circ\text{C}$ , and noise of only 0.2  $\mu\text{V}$  p-p (0.1 Hz to 10 Hz), they are perfectly suited for applications where large error sources cannot be tolerated. Many systems can take advantage of the low noise, dc precision, and rail-to-rail output swing provided by the AD8622/AD8624 to maximize the signal-to-noise ratio and dynamic range for low power operation. The AD8622/AD8624 are specified for the extended industrial temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The AD8622 is available in lead-free 8-lead SOIC and MSOP packages, while the AD8624 is available in lead-free 14-lead TSSOP and 16-lead LFCSP packages.

### PIN CONFIGURATIONS

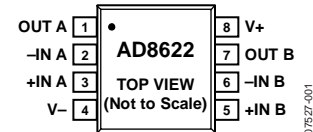


Figure 1. 8-Lead Narrow-Body SOIC



Figure 2. 8-Lead MSOP

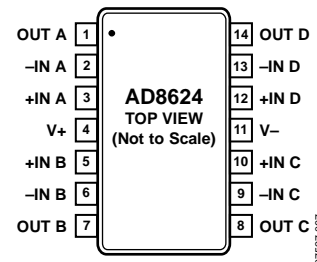
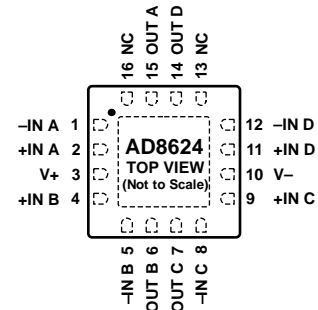


Figure 3. 14-Lead TSSOP



- NOTES  
 1. NC = NO CONNECT.  
 2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V-.

Figure 4. 16-Lead LFCSP

Table 1. Low Power Op Amps

Supply	40V	36V	12V to 18V	6V
Single	OP97	OP777 OP1177	AD8663	
Dual	OP297	OP727 OP2177	AD8667	ADA4692-2
Quad	OP497	OP747 OP4177	AD8669	ADA4692-4

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## REVISION HISTORY

### 12/13—Rev. C to Rev. D

Change to Figure 58 .....	17
Updated Outline Dimensions .....	19

### 6/11—Rev. B to Rev. C

Changes to Figure 13.....	7
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### 2/10—Rev. A to Rev. B

Changed 16-Lead to 14-Lead in Figure 62 Caption.....	19
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### 1/10—Rev. 0 to Rev. A

Added 14-Lead TSSOP .....	Universal
Added 16-Lead LFCSP.....	Universal
Added Figure 3 and Figure 4; Renumbered Sequentially .....	1
Changes to Table 5.....	5
Changes to Figure 10 to Figure 16.....	6
Changes to Figure 26.....	9
Changes to Figure 29.....	10
Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	19

### 7/09—Revision 0: Initial Version

## SPECIFICATIONS

ELECTRICAL CHARACTERISTICS— $\pm 2.5$  V OPERATION

$V_{SY} = \pm 2.5$  V,  $V_{CM} = 0$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	125	$\mu\text{V}$
					230	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	200	pA
					400	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	200	pA
					300	pA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-1.3		+1.3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -1.3$ V to $+1.3$ V $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	120		dB
			107			dB
Open-Loop Gain	$A_{VO}$	$R_L = 10$ k $\Omega$ , $V_O = -2.0$ V to $+2.0$ V $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	118	135		dB
			109			dB
Input Resistance, Differential Mode	$R_{INDM}$			1		G $\Omega$
Input Resistance, Common Mode	$R_{INCM}$			1		T $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			5.5		pF
Input Capacitance, Common Mode	$C_{INCM}$			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 100$ k $\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.45	2.49		V
			2.41			V
		$R_L = 10$ k $\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.40	2.45		V
			2.36			V
Output Voltage Low	$V_{OL}$	$R_L = 100$ k $\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-2.49	-2.45	V
					-2.41	V
		$R_L = 10$ k $\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-2.45	-2.40	V
					-2.36	V
Short-Circuit Current	$I_{SC}$			$\pm 30$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1$ kHz, $A_v = 1$		2		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.0$ V to $\pm 18.0$ V $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	125	145		dB
			120			dB
Supply Current/Amplifier	$I_{SY}$	$I_O = 0$ mA $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		175	225	$\mu\text{A}$
					310	$\mu\text{A}$
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10$ k $\Omega$ , $C_L = 100$ pF, $A_v = 1$		0.28		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 10$ k $\Omega$ , $C_L = 20$ pF, $A_v = 1$		540		kHz
Phase Margin	$\Phi_M$	$R_L = 10$ k $\Omega$ , $C_L = 20$ pF, $A_v = 1$		74		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_n$ p-p	$f = 0.1$ Hz to $10$ Hz		0.2		$\mu\text{V}$ p-p
Voltage Noise Density	$e_n$	$f = 1$ kHz		12		nV/ $\sqrt{\text{Hz}}$
Uncorrelated Current Noise Density	$i_{n\_uncorr}$	$f = 1$ kHz		0.15		pA/ $\sqrt{\text{Hz}}$
Correlated Current Noise Density	$i_{n\_corr}$	$f = 1$ kHz		0.07		pA/ $\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—±15 V OPERATION**

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	125	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	230	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		45	200	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		35	500	pA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			500	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13.8\text{ V to } +13.8\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-13.8	135	+13.8	V
Open-Loop Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = -13.5\text{ V to } +13.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	125	137		dB
Input Resistance, Differential Mode	$R_{INDM}$			1		G $\Omega$
Input Resistance, Common Mode	$R_{INCM}$			1		T $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			5.5		pF
Input Capacitance, Common Mode	$C_{INCM}$			3		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.94	14.97		V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.84	14.89		V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.86			V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.75			V
Short-Circuit Current	$I_{SC}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-14.97	-14.94	V
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = 1$			-14.92	V
					-14.89	V
					-14.80	V
				$\pm 40$		mA
				1.5		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.0\text{ V to } \pm 18.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	125	145		dB
Supply Current/Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	215	250	$\mu\text{A}$
					350	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = 1$		0.48		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = 1$		560		kHz
Phase Margin	$\Phi_M$	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = 1$		75		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		0.2		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		11		nV/ $\sqrt{\text{Hz}}$
Uncorrelated Current Noise Density	$i_{n\_uncorr}$	$f = 1\text{ kHz}$		0.15		pA/ $\sqrt{\text{Hz}}$
Correlated Current Noise Density	$i_{n\_corr}$	$f = 1\text{ kHz}$		0.06		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	$\pm 18$ V
Input Voltage	$\pm V_{SY}$
Input Current <sup>1</sup>	$\pm 10$ mA
Differential Input Voltage <sup>2</sup>	$\pm 10$ V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}\text{C}$

<sup>1</sup>The input pins have clamp diodes to the power supply pins. The input current should be limited to 10 mA or less whenever input signals exceed the power supply rail by 0.5 V.

<sup>2</sup>Differential input voltage is limited to 10 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC_N (R-8)	120	45	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP (RM-8)	142	45	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU-14)	112	35	$^{\circ}\text{C}/\text{W}$
16-Lead LFCSP (CP-16-17)	55	14	$^{\circ}\text{C}/\text{W}$

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise noted.



Figure 5. Input Offset Voltage Distribution



Figure 8. Input Offset Voltage Distribution



Figure 6. Input Offset Voltage Drift Distribution

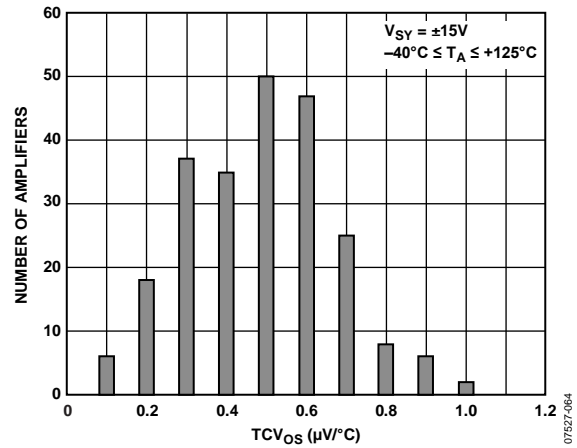


Figure 9. Input Offset Voltage Drift Distribution



Figure 7. Input Offset Voltage vs. Common-Mode Voltage

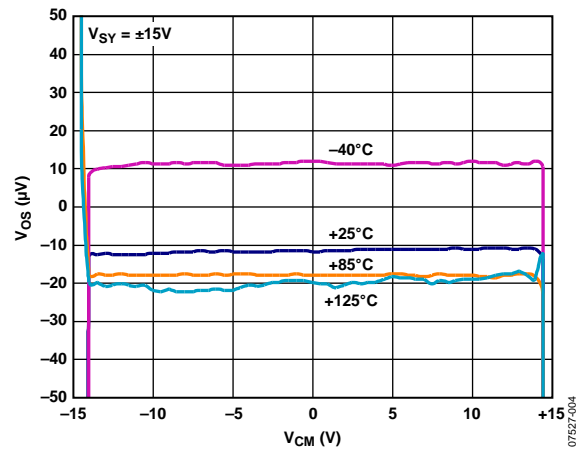


Figure 10. Input Offset Voltage vs. Common-Mode Voltage



Figure 11. Input Bias Current vs. Temperature



Figure 14. Input Bias Current vs. Temperature



Figure 12. Input Bias Current vs. Common-Mode Voltage



Figure 15. Input Bias Current vs. Common-Mode Voltage



Figure 13. Output Voltage to Supply Rail vs. Load Current



Figure 16. Output Voltage to Supply Rail vs. Load Current



Figure 17. Output Voltage to Supply Rail vs. Temperature



Figure 20. Output Voltage to Supply Rail vs. Temperature



Figure 18. Supply Current vs. Supply Voltage



Figure 21. Supply Current vs. Temperature

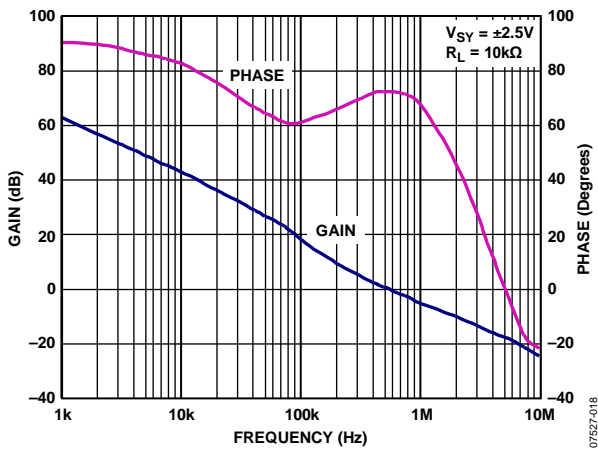


Figure 19. Open-Loop Gain and Phase vs. Frequency



Figure 22. Open-Loop Gain and Phase vs. Frequency





Figure 23. Closed-Loop Gain vs. Frequency



Figure 26. Closed-Loop Gain vs. Frequency



Figure 24. Output Impedance vs. Frequency



Figure 27. Output Impedance vs. Frequency



Figure 25. CMRR vs. Frequency



Figure 28. CMRR vs. Frequency



Figure 29. PSRR vs. Frequency



Figure 32. PSRR vs. Frequency



Figure 30. Small-Signal Overshoot vs. Load Capacitance



Figure 33. Small-Signal Overshoot vs. Load Capacitance

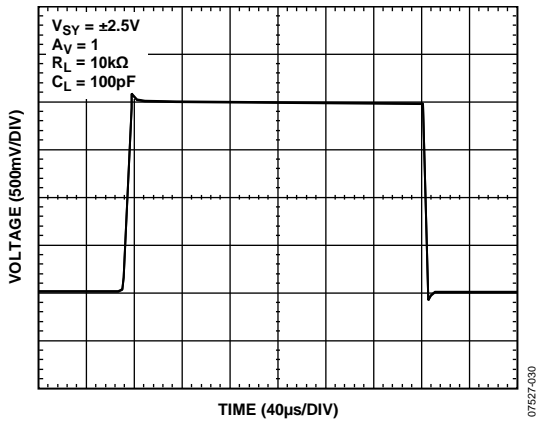


Figure 31. Large-Signal Transient Response

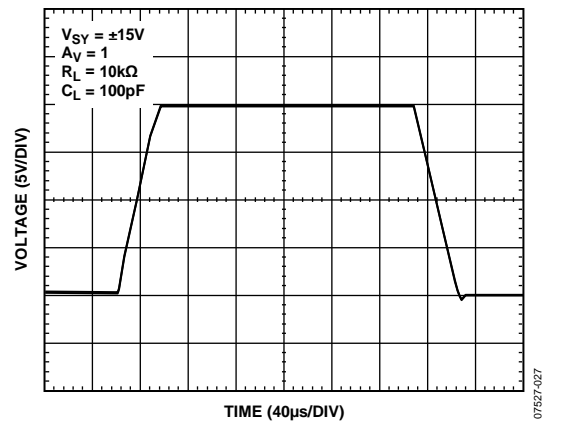


Figure 34. Large-Signal Transient Response



Figure 35. Small-Signal Transient Response



Figure 38. Small-Signal Transient Response



Figure 36. Negative Overload Recovery



Figure 39. Negative Overload Recovery



Figure 37. Positive Overload Recovery



Figure 40. Positive Overload Recovery



Figure 41. Output Step vs. Settling Time



Figure 44. Output Step vs. Settling Time



Figure 42. Voltage Noise Density vs. Frequency



Figure 45. Voltage Noise Density vs. Frequency

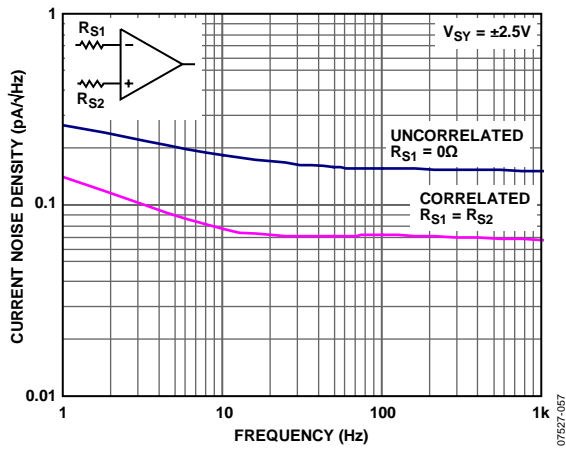


Figure 43. Current Noise Density vs. Frequency



Figure 46. Current Noise Density vs. Frequency



Figure 47. 0.1 Hz to 10 Hz Noise



Figure 49. 0.1 Hz to 10 Hz Noise



Figure 48. THD + Noise vs. Amplitude

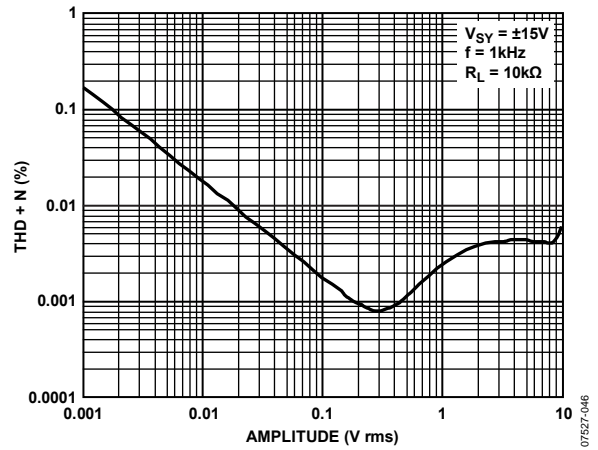


Figure 50. THD + Noise vs. Amplitude



Figure 51. THD + Noise vs. Frequency



Figure 53. THD + Noise vs. Frequency



Figure 52. Channel Separation vs. Frequency

## APPLICATIONS INFORMATION

### INPUT PROTECTION

The maximum differential input voltage that can be applied to the AD8622/AD8624 is determined by the internal diodes connected across its inputs and series resistors at each input. These internal diodes and series resistors limit the maximum differential input voltage to  $\pm 10$  V and are needed to prevent base-emitter junction breakdown from occurring in the input stage of the AD8622/AD8624 when very large differential voltages are applied. In addition, the internal resistors limit the currents that flow through the diodes. However, in applications where large differential voltages can be inadvertently applied to the device, large currents may still flow through these diodes. In such a case, external resistors must be placed at both inputs of the op amp to limit the input currents to  $\pm 10$  mA (see Figure 54).



Figure 54. Input Protection

### PHASE REVERSAL

An undesired phenomenon, phase reversal (also known as phase inversion) occurs in many op amps when one or both of the inputs are driven beyond the specified input voltage range (IVR), in effect reversing the polarity of the output. In some cases, phase reversal can induce lockups and even cause equipment damage as well as self destruction.

The AD8622/AD8624 amplifiers have been carefully designed to prevent output phase reversal when both inputs are maintained within the specified input voltage range. In addition, even if one or both inputs exceed the input voltage range but remain within the supply rails, the output still does not phase reverse. Figure 55 shows the input/output waveforms of the AD8622/AD8624 configured as a unity-gain buffer with a supply voltage of  $\pm 15$  V.



Figure 55. No Phase Reversal

### MICROPOWER INSTRUMENTATION AMPLIFIER

The AD8622 is a dual, high precision, rail-to-rail output op amp operating at just 215  $\mu$ A quiescent current per amplifier. Its ultralow offset, offset drift, and voltage noise, combined with its very low bias current and high common-mode rejection ratio (CMRR), are ideally suited for high accuracy and micropower instrumentation amplifier.

Figure 56 shows the classic 2-op-amp instrumentation amplifier with four resistors using the AD8622. The key to high CMRR for this instrumentation amplifier are resistors that are well matched from both the resistive ratio and the relative drift. For true difference amplification, matching of the resistor ratio is very important, where  $R3/R4 = R1/R2$ . Assuming perfectly matched resistors, the gain of the circuit is  $1 + R2/R1$ , which is approximately 100. Tighter matching of two op amps in one package, like the AD8622, offers a significant boost in performance over the classical 3-op-amp configuration. Overall, the circuit only requires about 430  $\mu$ A of supply current.



- NOTES
- $V_O = 100(V_2 - V_1)$
  - TYPICAL:  $0.01\text{mV} < |V_2 - V_1| < 149.7\text{mV}$
  - TYPICAL:  $-14.97\text{V} < V_O < +14.97\text{V}$
  - USE MATCHED RESISTORS.

Figure 56. Micropower Instrumentation Amplifier

**HALL SENSOR SIGNAL CONDITIONING**

The AD8622/AD8624 is also highly suitable for high accuracy, low power signal conditioning circuits. One such use is in Hall sensor signal conditioning (see Figure 57). The magnetic sensitivity of a Hall element is proportional to the bias voltage applied across it. With 1 V bias voltage, the Hall element consumes about 2.5 mA of supply current and has a sensitivity of 5.5 mV/mT typical. To reduce power consumption, bias voltage must be reduced, but at the risk of lower sensitivity. The only way to achieve higher sensitivity is by introducing a gain using a precision micropower amplifier. The AD8622/AD8624, with all its features, is well suited to amplify the sensitivity of the Hall element.

The ADR121 is a precision micropower 2.5 V voltage reference. A precision voltage reference is required to hold a constant current so that the Hall voltage only depends on the intensity of the

magnetic field. Using the 4.12k:98.8k resistive divider, the bias voltage of the Hall element is reduced to 100 mV, leading to only 250  $\mu$ A of power consumption. The 3-op-amp in-amp configuration of the AD8622/AD8624 then increases the sensitivity to 55 mV/mT. The key to high CMRR for this in-amp configuration are resistors that are well matched (where  $R1/R2 = R3/R4$ ) from both the resistive ratio and relative drift. The resistors are important in determining the performance over manufacturing tolerances, time and temperature. At least 1% or better resistors are recommended. Using the AD8622/AD8624 to amplify the sensor signal can reduce power while also achieving higher sensitivity. The total current consumed is just 1.2 mA, resulting in 21 $\times$  improvement in sensitivity/power.



- NOTES
1. USE MATCHED RESISTORS FOR IN-AMP.
  2. FOR INFORMATION ON C1, C2, AND C3, REFER TO ADR121 DATA SHEET.

Figure 57. Hall Sensor Signal Conditioning

07527-652



# SIMPLIFIED SCHEMATIC



Figure 58. Simplified Schematic

07527-982

OUTLINE DIMENSIONS

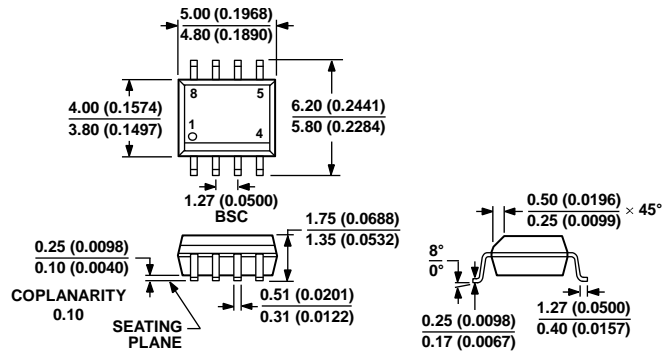


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 59. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

100709-B



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 60. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

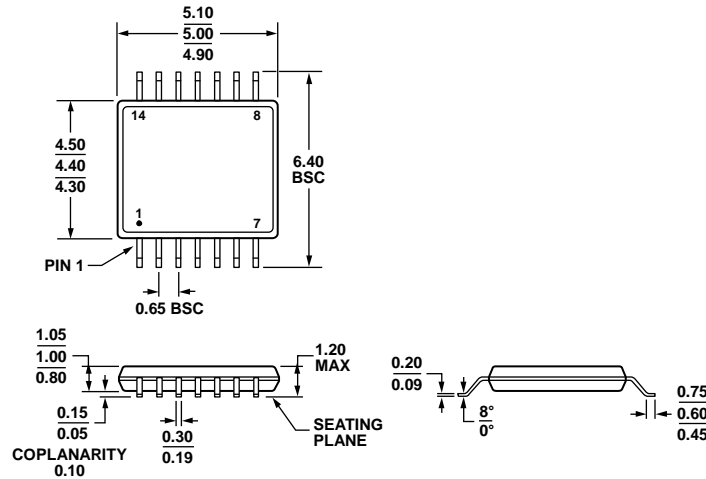
012807-A



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 61. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
4 mm x 4 mm Body, Very Very Thin Quad  
(CP-16-17)  
Dimensions shown in millimeters

06-16-2010-C



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 62. 14-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-14)  
Dimensions shown in millimeters

061908-A

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
AD8622ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARMZ-R7	-40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8622ARZ-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8622ARZ-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8624ACPZ-R2	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-17	
AD8624ACPZ-R7	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-17	
AD8624ACPZ-RL	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-17	
AD8624ARUZ	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8624ARUZ-RL	-40°C to +125°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**