# ISL32740E

Isolated 40Mbps RS-485 PROFIBUS Transceiver

FN8857
Rev.4.00
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The ISL32740E is a galvanically isolated high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses Giant Magnetoresistance (GMR) as its isolation technology.

The part is available in a 16 Ld QSOP package offering unprecedented miniaturization, and in a 16 Ld SOICW package providing a true 8mm creepage distance.

The ISL32740E is PROFIBUS compliant, including the rigorous PROFIBUS differential output voltage specifications.

A unique ceramic/polymer composite barrier provides excellent isolation and 44,000 years of barrier life.

The device is compatible with 3V as well as 5V input supplies, allowing an interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs are a full fail-safe design, ensuring a logic high R-output if A/B are floating or shorted.

## Applications

- PROFIBUS-DP and RS-485 networks
- Factory automation
- Building environmental control systems
- Industrial/process control networks
- Equipment covered under IEC 61010-1 Edition 3

## Features

- 40Mbps data rate
- 2.5kV$_{RMS}$ isolation/600V$_{RMS}$ working voltage
- 3V to 5V power supplies
- 20ns propagation delay
- 5ns pulse skew
- 50kV/µs (typical), 30kV/µs (minimum) common-mode transient immunity
- 15kV ESD protection
- Low EMC footprint
- Thermal shutdown protection
- Temperature ranges available
  - -40°C to +85°C (EIBZ)
  - -40°C to +125°C (EFBZ)
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- PROFIBUS compliant
- 16 Ld QSOP or 0.3” true 8mm 16 Ld SOICW packages
- UL 1577 recognized
- VDE V 0884-10 certified

## Related Literature

- For a full list of related documents, visit our website
  - ISL32740E product page

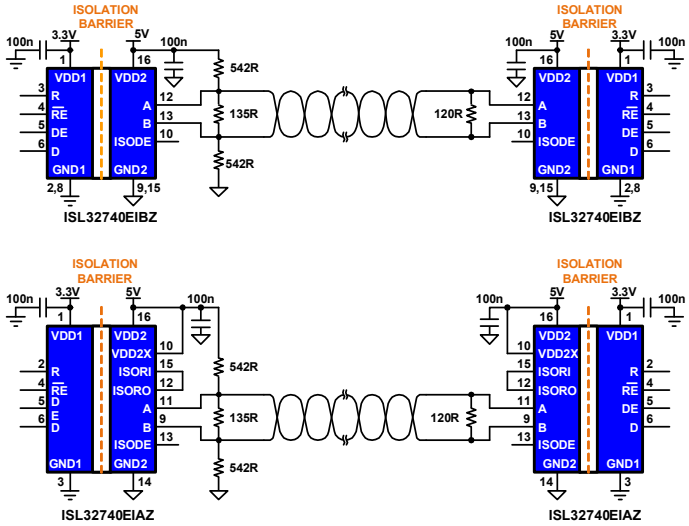



**Figure 1. Typical PROFIBUS Application**

# 1. Overview

## 1.1 Typical Operating Circuits

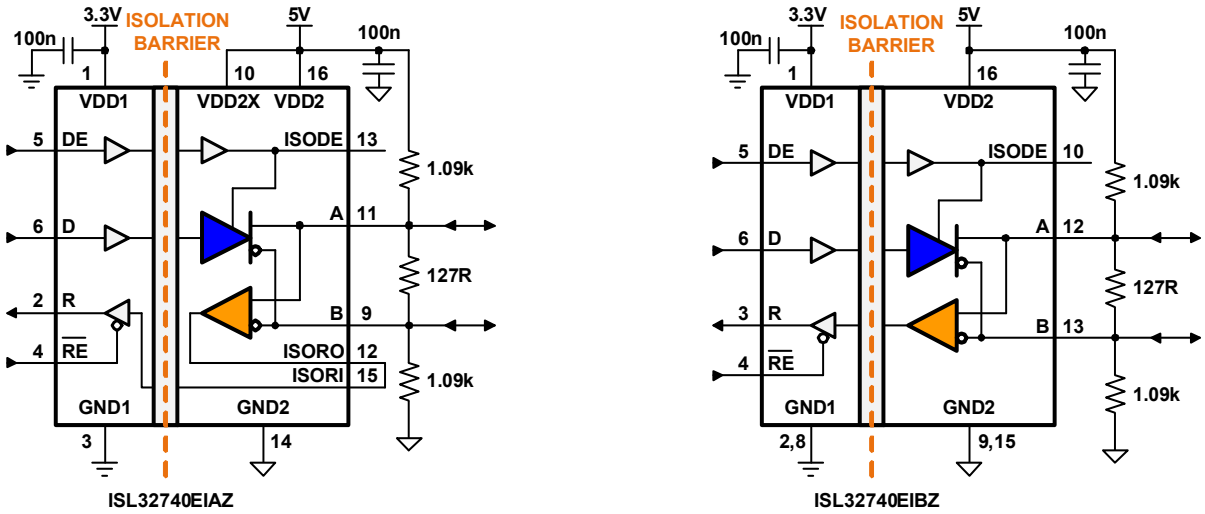



**Figure 2. Typical Operating Circuits**

## 1.2 Ordering Information

| Part Number (Notes 3, 4) | Part Marking | Temp. Range (°C) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|
| ISL32740EIBZ (Note 1) | 32740EIBZ | -40 to +85 | 16 Ld SOICW | M16.3A |
| ISL32740EFBZ (Note 1) | 32740EFBZ | -40 to +125 | 16 Ld SOICW | M16.3A |
| ISL32740EIAZ (Note 2) | 32740EIAZ | -40 to +85 | 16 Ld QSOP | M16.15B |
| ISL32740EVAL1Z | Evaluation board for ISL32740EIBZ | | | |
| ISL32740EVAL2Z | Evaluation board for ISL32740EIAZ | | | |

Notes:

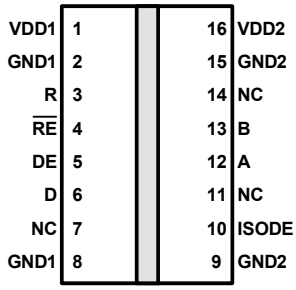
1. Add “-T” suffix for 1k unit or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. Add “-T” suffix for 2.5k unit or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the product information page for the ISL32740E. For more information on MSL, see TB363.

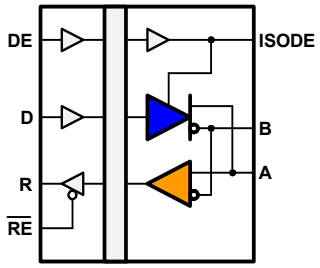
**Table 1. Key Differences Between Family of Parts**

| Part Number | Full/Half Duplex | $V_{DD1}$ (V) | $V_{DD2}$ (V) | Data Rate (Mbps) | Isolation Voltage ($kV_{RMS}$) |
|---|---|---|---|---|---|
| ISL32704E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 4 | 2.5 |
| ISL32705E | Full | 3.0 – 5.5 | 4.5 – 5.5 | 4 | 2.5 |
| ISL32740E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 40 | 2.5 |
| ISL32741E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 40 | 6 |

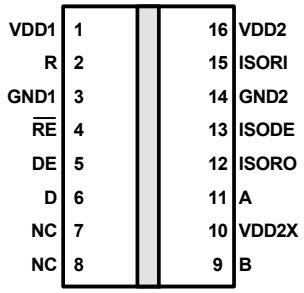
## 1.3 Pin Configurations

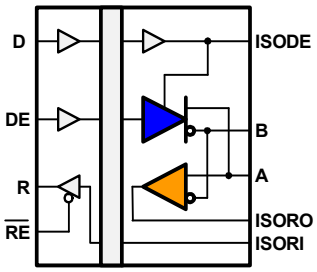
ISL32740E
(16 Ld SOICW)
Top View




ISL32740E
(16 Ld QSOP)
Top View




## 1.4 Truth Tables

| Transmitting | | | | | |
|---|---|---|---|---|---|
| **Inputs** | | | **Outputs** | | |
| $\overline{RE}$ | DE | D | ISODE | B | A |
| X | 1 | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | X | 0 | High-Z | High-Z |
| 1 | 0 | X | 0 | High-Z* | High-Z* |

| Receiving | | | |
|---|---|---|---|
| **Inputs** | | | **Output** |
| $\overline{RE}$ | DE | A-B | RO |
| 0 | 0 | $V_{AB} \geq -0.05V$ | 1 |
| 0 | 0 | $-0.05 > V_{AB} > -0.2V$ | Undetermined |
| 0 | 0 | $V_{AB} \leq -0.2V$ | 0 |
| 0 | 0 | Inputs Open/Shorted | 1 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | High-Z* |

Note: *Transceiver shutdown mode

## 1.5 Pin Descriptions

| Pin Number | | Pin Name | Function |
|---|---|---|---|
| 16 Ld SOICW | 16 Ld QSOP | | |
| 1 | 1 | VDD1 | Input power supply. |
| 3 | 2 | R | Receiver output: If A-B ≥-50mV, R is high; If A-B ≤-200mV, R is low; R = High if A and B are unconnected (floating) or shorted, or connected to a terminated bus that is not driven. |
| 2, 8 | 3 | GND1 | Input power supply ground return. Pin 2 is internally connected to Pin 8 (for SOIC package). |
| 4 | 4 | $\overline{RE}$ | Receiver output enable. R is enabled when $\overline{RE}$ is low; R is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND1. |
| 5 | 5 | DE | Driver output enable. The driver outputs, A and B, are enabled by bringing DE high. They are high impedance when DE is low. If the Tx enable function is not required, connect DE to VDD1 through a 1kΩ or greater resistor. |
| 6 | 6 | D | Driver input. A low on D forces output A low and output B high. Similarly, a high on D forces output A high and output B low. |
| 7, 11, 14 | 7, 8 | NC | No internal connection. |
| 12 | 11 | A | ±15kV IEC61000 ESD protected RS-485/RS422 level, noninverting receiver input if DE = 0 and noninverting driver output if DE = 1. |
| 13 | 9 | B | ±15kV IEC61000 ESD protected RS-485/RS422 level, inverting receiver input if DE = 0 and inverting driver output if DE = 1. |
| - | 10 | VDD2X | Transceiver power supply. Connect to VDD2 (Pin 16). |
| - | 12 | ISORO | Isolated receiver output. This pin must be connected to Pin 15. |
| - | 15 | ISORI | Isolated receiver input. This pin must be connected to Pin 12. |
| 9, 15 | 14 | GND2 | Output power supply ground return. Dual ground pins are connected internally. |
| 10 | 13 | ISODE | Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored. |
| 16 | 16 | VDD2 | Output power supply. |

# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter (Note 5) | Minimum | Maximum | Unit |
|---|---|---|---|
| **Supply Voltages (Note 8)** | | | |
| VDD1 to GND1 | -0.5 | +7 | V |
| VDD2 to GND2 | | 7 | V |
| Input Voltages D, DE, $\overline{RE}$ | -0.5 | VDD1 + 0.5 | V |
| **Input/Output Voltages** | | | |
| A, B | -9 | +13 | V |
| R | -0.5 | VDD1 + 1 | V |
| Short-Circuit Duration A, B | Continuous | | V |
| ESD Rating | See “Electrical Specifications” table on page 7 | | |

Note:
5. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 16 Ld SOICW Package (Notes 6, 7) | 43 | 20 |
| 16 Ld QSOP Package (Notes 6, 7) | 77 | 41 |

Notes:
6. $\theta_{JA}$ is measured in free air with the component soldered to a double-sided board.
7. For $\theta_{JC}$, the “case temp” location is the center of the package top side.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Maximum Junction Temperature (Plastic Package) | -55 | +150 | °C |
| Maximum Storage Temperature Range | -55 | +150 | °C |
| Maximum Power Dissipation | | 800 | mW |
| Pb-Free Reflow Profile | see TB493 | | |

## 2.3 Recommended Operation Conditions

| Parameter | | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Supply Voltages** | | | | |
| $V_{DD1}$ | | 3.0 | 5.5 | V |
| $V_{DD2}$ | | 4.5 | 5.5 | V |
| **High-Level Digital Input Voltage, $V_{IH}$** | | | | |
| $V_{DD1}$ = 3.3V | | 2.4 | $V_{DD1}$ | V |
| $V_{DD1}$ = 5.0V | | 3.0 | $V_{DD1}$ | V |
| Low-Level Digital Input Voltage, $V_{IL}$ | | 0 | 0.8 | V |

| Parameter | | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Differential Input Voltage (Note 9), $V_{ID}$ | | -7 | 12 | V |
| High-Level Output Current (Driver), $I_{OH}$ | | | 60 | mA |
| High-Level Digital Output Current (Receiver), $I_{OH}$ | | | 8 | mA |
| Low-Level Output Current (Driver), $I_{OL}$ | | | -60 | mA |
| Low-Level Digital Output Current (Receiver), $I_{OL}$ | | | -8 | mA |
| Junction Temperature, $T_J$ | | -40 | +110 | °C |
| Ambient Operating Temperature, $T_A$ | ISL32740EIBZ, ISL32740EIAZ | -40 | +85 | °C |
| | ISL32740EFBZ | -40 | +125 | |
| Digital Input Signal Rise and Fall Times, $t_{IR}$, $t_{IF}$ | | | DC Stable | |

## 2.4 Electrical Specifications

Test conditions: $T_{min}$ to $T_{max}$, $V_{DD1}$ = $V_{DD2}$ = 4.5V to 5.5V; unless otherwise stated. (Note 8)

| Parameter | Symbol | Test Conditions | | Min | Typ (Note 12) | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | | |
| Driver Line Output Voltage ($V_A$, $V_B$) (Note 8) | $V_O$ | No load | | - | - | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Note 9) | $V_{OD1}$ | No load | | - | - | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Note 9) | $V_{OD2}$ | $R_L$ = 54Ω | | 2.1 | 2.8 | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Notes 9, 13) | $V_{OD3}$ | $R_L$ = 60Ω | | 1.9 | 2.7 | - | V |
| Change in Magnitude of Differential Output Voltage (Note 14) | $\Delta V_{OD}$ | $R_L$ = 54Ω or 100Ω | | - | 0.01 | 0.20 | V |
| Driver Common-Mode Output Voltage | $V_{OC}$ | $R_L$ = 54Ω or 100Ω | | - | - | 3 | V |
| Change in Magnitude of Driver Common-Mode Output Voltage (Note 14) | $\Delta V_{OC}$ | $R_L$ = 54Ω or 100Ω | | - | 0.01 | 0.20 | V |
| Bus Input Current (A, B) (Notes 11, 15) | $I_{IN2}$ | DE = 0V | $V_{IN}$ = 12V | | - | 220 | µA |
| | | | $V_{IN}$ = -7V | -160 | | | µA |
| High-Level Input Current (DI, DE, $\overline{RE}$) | $I_{IH}$ | $V_I$ = 3.5V | | - | - | 10 | µA |
| Low-Level Input Current (DI, DE, $\overline{RE}$) | $I_{IL}$ | $V_I$ = 0.4V | | -10 | - | - | µA |
| Absolute Short-Circuit Output Current | $I_{OS}$ | DE = $V_{DD1}$, -7V ≤ $V_A$ or $V_B$ ≤ 12V | | - | - | ±250 | mA |
| Supply Current | $I_{DD1}$ | $V_{DD1}$ = 5V | | - | 4 | 6 | mA |
| | | $V_{DD1}$ = 3.3V | | - | 3 | 4 | mA |
| Positive-Going Input Threshold Voltage | $V_{TH+}$ | -7V ≤ $V_{CM}$ ≤ 12V | | - | - | -50 | mV |
| Negative-Going Input Threshold Voltage | $V_{TH-}$ | -7V ≤ $V_{CM}$ ≤ 12V | | -200 | - | - | mV |
| Receiver Input Hysteresis | $V_{HYS}$ | $V_{CM}$ = 0V | | - | 28 | - | mV |
| Differential Bus Input Capacitance | $C_D$ | | | - | 9 | 12 | pF |
| Receiver Output High Voltage | $V_{OH}$ | $I_O$ = -20µA, $V_{ID}$ = -50mV | | $V_{CC}$ - 0.2 | - | - | V |
| Receiver Output Low Voltage | $V_{OL}$ | $I_O$ = +20µA, $V_{ID}$ = -200mV | | - | - | 0.2 | V |
| High impedance Output Current | $I_{OZ}$ | 0.4V ≤ $V_O$ ≤ ($V_{DD2}$ - 0.5) | | -1 | - | 1 | µA |
| Receiver Input Resistance | $R_{IN}$ | -7V ≤ $V_{CM}$ ≤ 12V | | 54 | 80 | - | kΩ |
| Supply Current | $I_{DD2}$ | DE = $V_{DD1}$, no load | | - | 5 | 16 | mA |

Test conditions: $T_{min}$ to $T_{max}$, $V_{DD1}$ = $V_{DD2}$ = 4.5V to 5.5V; unless otherwise stated. (Note 8) **(Continued)**

| Parameter | Symbol | Test Conditions | Min | Typ (Note 12) | Max | Unit |
|---|---|---|---|---|---|---|
| **ESD Performance** | | | | | | |
| RS-485 Bus Pins (A, B) | | IEC61000-4-2, air-gap discharge to GND2 | - | ±15 | - | kV |
| | | IEC61000-4-2, contact discharge to GND2 | - | ±8 | - | kV |
| | | Human Body Model discharge (HBM) to GND2 | - | ±16.5 | - | kV |
| All Pins (R, $\overline{RE}$, D, DE) | | Human Body Model discharge (HBM) to GND1 | - | ±2 | - | kV |
| **Switching Characteristics** | | | | | | |
| **$V_{DD1}$ = 5V, $V_{DD2}$ = 5V** | | | | | | |
| Data Rate | DR | $R_L$ = 54Ω, $C_L$ = 50pF | 40 | - | - | Mbps |
| Propagation Delay (Notes 9, 16) | $t_{PD}$ | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 20 | 30 | ns |
| Pulse Skew (Notes 9, 17) | $t_{SK}$ (P) | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 1 | 5 | ns |
| Skew Limit (Note 10) | $t_{SK}$ (LIM) | $R_L$ = 54Ω, $C_L$ = 50pF | - | 2 | 10 | ns |
| Output Enable Time to High Level | $t_{PZH}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Enable Time to Low Level | $t_{PZL}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Disable Time from High Level | $t_{PHZ}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Disable Time from Low Level | $t_{PLZ}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Common-Mode Transient Immunity | CMTI | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25ns | 30 | 50 | - | kV/µs |
| **$V_{DD1}$ = 3.3V, $V_{DD2}$ = 5V** | | | | | | |
| Data Rate | DR | $R_L$ = 54Ω, $C_L$ = 50pF | 40 | - | - | Mbps |
| Propagation Delay (Notes 9, 3) | $t_{PD}$ | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 25 | 35 | ns |
| Pulse Skew (Notes 9, 4) | $t_{SK}$ (P) | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 2 | 5 | ns |
| Skew Limit (Note 10) | $t_{SK}$ (LIM) | $R_L$ = 54Ω, $C_L$ = 50pF | - | 4 | 10 | ns |
| Output Enable Time to High Level | $t_{PZH}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Enable Time to Low Level | $t_{PZL}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Disable Time from High Level | $t_{PHZ}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Disable Time from Low Level | $t_{PLZ}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Common-Mode Transient Immunity | CMTI | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25ns | 30 | 50 | - | kV/µs |

Notes: (apply to both driver and receiver sections)

8. All voltages on the isolator primary side are with respect to GND1. All line voltages and common-mode voltages on the isolator secondary or bus side are with respect to GND2.
9. Differential I/O voltage is measured at the noninverting bus Terminal A with respect to the inverting Terminal B.
10. Skew limit is the maximum propagation delay difference between any two devices at +25°C.
11. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
12. All typical values are at $V_{DD1}$, $V_{DD2}$ = 5V or $V_{DD1}$ = 3.3V and $T_A$ = +25°C.
13. -7V < $V_{CM}$ < 12V; 4.5 < $V_{DD}$ < 5.5V.
14. $\Delta V_{OD}$ and $\Delta V_{OC}$ are the changes in magnitude of $\Delta V_{OD}$ and $\Delta V_{OD}$ respectively, that occur when the input is changed from one logic state to the other.
15. This applies for both power-on and power-off; refer to ANSI standard RS-485 for the exact condition. The EIA/TIA-422 -B limit does not apply for a combined driver and receiver terminal.
16. Includes 10ns read enable time. Maximum propagation delay is 25ns after read assertion.
17. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.

## 2.5 Insulation Specifications

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Creepage Distance (external) | | Per IEC 60601 | SOICW | 8.03 | 8.3 | - | mm |
| | | | QSOP | 3.2 | - | - | mm |
| Total Barrier Thickness (internal) | | | | - | 13 | - | µm |
| Barrier Resistance | $R_{IO}$ | 500V | | - | $>10^{14}$ | - | Ω |
| Barrier Capacitance | $C_{IO}$ | f = 1MHz | | - | 7 | - | pF |
| Leakage Current | | $240V_{RMS}$, 60Hz | | - | 0.2 | - | $\mu A_{RMS}$ |
| Comparative Tracking Index | CTI | Per IEC 60112 | | ≥600 | - | - | $V_{RMS}$ |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | $V_{IO}$ | At maximum operating temperature | | 1000 | - | - | $V_{RMS}$ |
| | | | | 1500 | - | - | $V_{DC}$ |
| Barrier Life | | 100°C, $1000V_{RMS}$, 60% CL activation energy | | - | 44000 | - | Years |

## 2.6 Magnetic Field Immunity

| Parameter (Note 18) | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{DD1}$ = 5V, $V_{DD2}$ = 5V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | - | 3500 | - | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_P$ = 8µs | - | 4500 | - | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz to 1MHz | - | 4500 | - | A/m |
| Cross-Axis Immunity Multiplier (Note 19) | $K_X$ | | - | 2.5 | - | A/m |
| **$V_{DD1}$ = 3.3V, $V_{DD2}$ = 5V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | - | 1500 | - | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_P$ = 8µs | - | 2000 | - | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz to1MHz | - | 2000 | - | A/m |
| Cross-Axis Immunity Multiplier (Note 19) | $K_X$ | | - | 2.5 | - | A/m |

Notes:

18. The relevant test and measurement methods are given in the "Electromagnetic Compatibility" on page 10.
19. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than "pin-to-pin" see ("Electromagnetic Compatibility" on page 10).

# 3. Safety and Approvals

## 3.1 VDE V 0884-10

Basic Isolation; VDE File Number 5016933-4880-0001/229067

- Working voltage ($V_{IORM}$) $600V_{RMS}$ ($848V_{PK}$); Basic insulation, Pollution degree 2
- Transient overvoltage ($V_{IOTM}$) $4000V_{PK}$
- Each part tested at $1590V_{PK}$ for 1s, 5pC partial discharge limit
- Samples tested at $4000V_{PK}$ for 60s, then $1358V_{PK}$ for 10s with 5pC partial discharge limit

| Symbol | Safety-limiting Values | Value | Unit |
|---|---|---|---|
| $T_S$ | Safety Rating Ambient Temperature | 180 | °C |
| $P_S$ | Safety Rating Power (+180°C) | 270 | mW |
| $I_S$ | Supply Current Safety Rating (total of supplies) | 54 | mA |

## 3.2 UL 1577

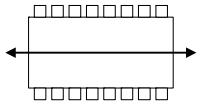
Component Recognition Program File Number: E483309

- Working voltage ($V_{IORM}$) $600V_{RMS}$ ($848V_{PK}$); basic insulation, pollution degree 2
- Transient overvoltage ($V_{IOTM}$) $4000V_{PK}$
- Each part tested at $3000V_{RMS}$ ($4243V_{PK}$) for 1s
- Each lot of samples tested at $2500V_{RMS}$ ($3536V_{PK}$) for 60s

# 4. Electromagnetic Compatibility

The ISL32740E is fully compliant with generic EMC standards EN50081, EN50082-1, and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. Compliance tests have been conducted in the following categories:

**Table 2. Compliance Test Categories**

| EN50081-1 | EN50082-2 | EN50204 |
|---|---|---|
| Residential, Commercial, and Light Industrial:<br>Methods EN55022, EN55014 | Industrial Environment<br>EN61000-4-2 (ESD)<br>EN61000-4-3 (Electromagnetic Field Immunity)<br>EN61000-4-4 (EFT)<br>EN61000-4-6 (RFI Immunity)<br>EN61000-4-8 (Power Frequency Magnetic Field immunity)<br>EN61000-4-9 (Pulsed Magnetic Field)<br>EN61000-4-10 (Damped Oscillatory Magnetic Field) | Radiated field from digital telephones |
| Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than "pin-to-pin" as shown on the right. |  | |

# 5. Application Information

The ISL32740E is an isolated PROFIBUS transceiver specifically designed for PROFIBUS-DP applications.

## 5.1 PROFIBUS

This transceiver uses a differential input receiver for maximum noise immunity and common-mode rejection. PROFIBUS (Process Field Bus) is specified in IEC61158 as a standard for field bus communication in automation technology. Two versions of PROFIBUS exist: PROFIBUS - PA for Process Automation and PROFIBUS-DP for Decentralized Peripherals. The most commonly used version, PROFIBUS-DP, is a protocol for deterministic communication between PROFIBUS masters and their remote I/O slaves.

While the physical layer of PROFIBUS-DP is based on RS-485 with its differential signaling scheme, significant differences between the two physical layers exist with regard to cable type, bus termination, and minimum bus voltage, to name just a few parameters.

**Table 3. Main Differences Between RS-485 and PROFIBUS-DP**

| Parameter | RS-485 | PROFIBUS-DP |
|---|---|---|
| Cable Type | Unshielded twisted pair | Shielded twisted pair |
| Characteristic Impedance | 120Ω | 150Ω |
| Minimum Driver Output Voltage | 1.5V | 2.1V |
| Transceiver Input Capacitance | 10 to 15pF | 10pF |
| External Fail-safe Biasing | Customer configurable (none, at single or both cable ends) | Always at both cable ends |
| Resistor Values | Customer configurable | Fixed |

## 5.2 Galvanic Isolation

To enable PROFIBUS transceivers operating over a wider common-mode voltage range than specified in RS-485 (7V to +12V), modern transceiver designs incorporate galvanic digital isolators with the transceiver circuitry. Here the ISL32740E uses a Giant Magnetoresistance (GMR) isolation. Figure 3 shows the principle operation of a single channel GMR isolator.

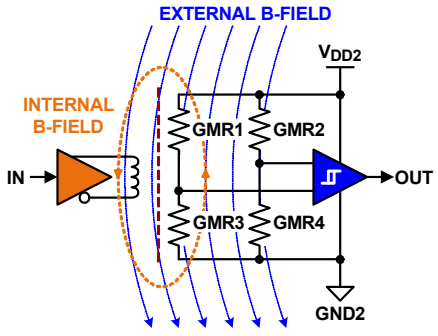



**Figure 3. Single Channel GMR Isolator**

The input signal is buffered and drives a primary coil, which creates a magnetic field that changes the resistance of the GMR resistors 1 to 4. GMR1 to GMR4 form a Wheatstone bridge in order to create a bridge output voltage that reacts only to magnetic field changes from the primary coil. Large external magnetic fields however, are treated as common-mode fields, and are therefore suppressed by the bridge configuration. The bridge output is fed into a comparator with an output signal identical in phase and shape to the input signal.

## 5.3 GMR Resistor in Detail

Figure 4 shows a GMR resistor consisting of ferromagnetic alloy layers B1 and B2 sandwiched around an ultra thin, nonmagnetic conducting middle layer A, typically copper. The GMR structure is designed so that in the absence of a magnetic field, the magnetic moments in B1 and B2 face opposite directions, thus causing heavy electron scattering across layer A, which drastically increases its resistance for current C. When a magnetic field D is applied, the magnetic moments in B1 and B2 are aligned and electron scattering is reduced. This lowers the resistance of layer A and current C increases.

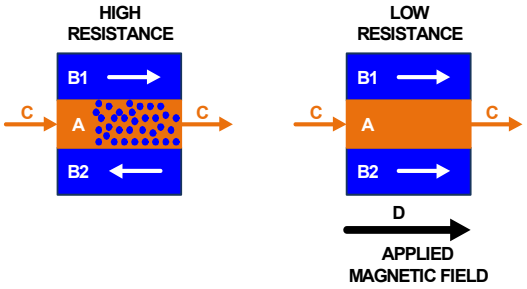



**Figure 4. Multilayer GMR Resistor**

## 5.4 Low Emissions

Because GMR isolators do not use complex encoding schemes, such as RF carriers or high-frequency clocks, and do not include power transfer coils or transformers, their radiated emission spectrum is practically undetectable.

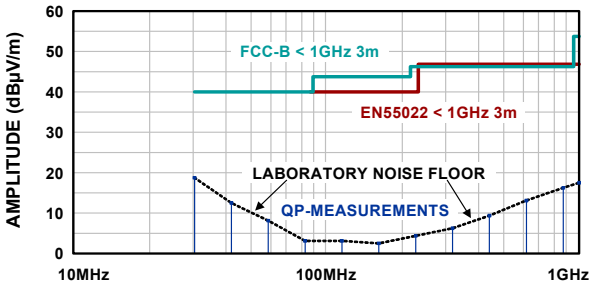



**Figure 5. Undetectable Emissions of GMR Isolators**

## 5.5 Low EMI Susceptibility

Because GMR isolators have no pulse trains or carriers to interfere with, they also have very low EMI susceptibility.

For the list of compliance tests conducted on GMR isolators refer to "Electromagnetic Compatibility" on page 10.

## 5.6 Receiver (Rx) Features

This transceiver uses a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications. Receiver inputs function with common-mode voltages as great as 7V outside the power supplies (for example, +12V and -7V), making them ideal for long networks, or industrial environments, where induced voltages are a realistic concern.

The receiver input resistance of 54kΩ surpasses the RS-422 specification of 4kΩ and is about five times the RS-485 "Unit Load" (UL) requirement of 12kΩ minimum. Thus, the ISL32740E is known as a "one-fifth UL" transceiver, and there can be up to 160 devices on the RS-485 bus while still complying with the RS-485 loading specification.

The receiver is a “full fail-safe” version that ensures a high-level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (terminated/undriven).

Rx outputs deliver large low state currents (typically >30mA) at $V_{OL}$ = 1V.

Receivers easily meet the 40Mbps data rate supported by the driver, and the receiver output is tri-statable using the active low $\overline{RE}$ input.

## 5.7 Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 2.1V across a 54Ω load (RS-485/PROFIBUS), and at least 2.6V across a 100Ω load (RS-422) even with $V_{CC}$ = 4.5V. The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

Outputs of the drivers are not slew rate limited, so faster output transition times allow data rates of at least 40Mbps. Driver outputs are tri-statable through the active high DE input.

### 5.7.1 High $V_{OD}$ Improves Noise Immunity and Flexibility

The ISL32740E driver design delivers larger differential output voltages ($V_{OD}$) than the RS-485 standard requires, or than most RS-485 transmitters can deliver. The minimum ±2.1V $V_{OD}$ ensures at least ±600mV more noise immunity than networks built using standard 1.5V $V_{OD}$ transmitters.

Another advantage of the large $V_{OD}$ is the ability to drive more than two bus terminations, which allows for using the ISL32740E in “star” and other multi-terminated, “nonstandard” network topologies.

## 5.8 Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These transmitters meet this requirement through driver output short-circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. In the event of a major short-circuit condition, the device includes a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

## 5.9 Dynamic Power Consumption

The isolator within the ISL32740E achieves its low power consumption from the way it transmits data across the barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input signal. Because the current pulses are narrow, about 2.5ns, the power consumption is independent of the mark-to-space ratio and solely depends on frequency.

**Table 4. Supply Current Increase with Data Rate**

| Data Rate (Mbps) | $I_{DD1}$ (mA) | $I_{DD2}$ (mA) |
|---|---|---|
| 1 | 0.15 | 0.15 |
| 10 | 1.5 | 1.5 |
| 20 | 3 | 3 |
| 40 | 6 | 6 |

## 5.10 Power Supply Decoupling

Both supplies, $V_{DD1}$ and $V_{DD2}$, must be bypassed with 100nF ceramic capacitors. The capacitors should be placed as close as possible to the supply pins for proper operation.

## 5.11 DC Correctness

The ISL32740E incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power-up, the bus outputs follow the truth tables on page 3. The DE input should be held low during power-up to prevent false drive data pulses on the bus.

## 5.12 Data Rate, Cables, and Terminations

Twisted pair is the cable of choice for RS-485, RS-422, and PROFIBUS networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

According to guidelines in the RS-422 and PROFIBUS specifications, networks operating at data rates in excess of 3Mbps should be limited to cable lengths of 100m (328 ft) or less and the PROFIBUS specification recommends that the more expensive “Type A” (22AWG) cable be used. The ISL32740E’s large differential output swing, fast transition times, and high drive-current output stages allow operation even at 40Mbps over standard Cat 5 cables in excess of 100m (328 ft).

The ISL324740E can also be used at slower data rates over longer cables, but there are some limitations. The Rx is optimized for high-speed operation, so its output may glitch if the Rx input differential transition times are too slow. Keeping the transition times below 500ns, (which equates to the Tx driving a 1000ft (305m) Cat 5 cable) yields excellent performance across the full operating temperature range.

To minimize reflections, proper termination is imperative when using this high data rate transceiver. In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 100Ω for Cat 5, 120Ω for RS-485, and 150Ω for Type A) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting transceivers to the main cable should be kept as short as possible.

PROFIBUS specifies line termination with fail-safe biasing networks of fixed resistor values at both cable ends.

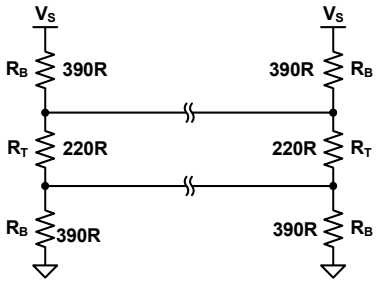



**Figure 6. Line Termination for PROFIBUS-DP**

For isolated data links meeting the requirements of EIA-485, the resistor values for the fail-safe biasing network can be calculated using (EQ. 1) through (EQ. 4).

For data links longer than 100m (330ft) apply fail-safe biasing at both cable ends to compensate for the attenuation of the bus fail-safe voltage caused by the voltage divider action of the cable’s DC resistance and the remote fail-safe biasing network. Use (EQ. 1) to calculate the bias resistors, $R_B$, and (EQ. 2) to determine the termination resistors, $R_T$.

(EQ. 1) $$R_B \geq \frac{V_S}{V_{AB}} \times \frac{Z_0}{2}$$

$$R_T = \frac{2R_B \times Z_0}{2R_B - Z_0} \quad \text{(EQ. 2)}$$

where:

- $R_B$ is the value of the biasing resistors
- $R_T$ is the value of the termination resistors
- $V_S$ is the minimum transceiver supply voltage
- $V_{AB}$ is the minimum bus voltage during bus idling
- $Z_0$ is the characteristic cable impedance of 120Ω

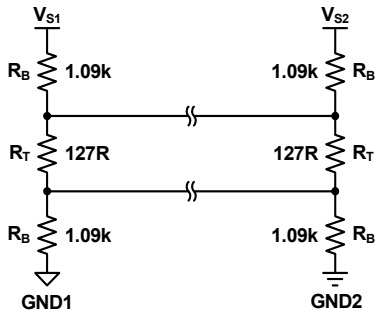



**Figure 7. Dual Fail-Safe Biasing for Long Data Links**

For data links shorter than 100m, use a single fail-safe biasing network. Match the termination resistor value at the cable end without fail-safe biasing with the characteristic cable impedance: $R_{T1} = Z_0$. Then calculate $R_B$ using (EQ. 3) and $R_{T2}$ using (EQ. 4).

$$R_B \geq \frac{V_S}{V_{AB}} \times \frac{Z_0}{4} \quad \text{(EQ. 3)}$$

$$R_{T2} = \frac{2R_B \times Z_0}{2R_B - Z_0} \quad \text{(EQ. 4)}$$

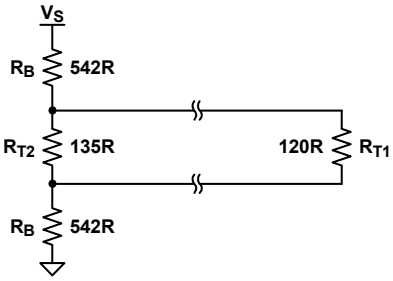



**Figure 8. Single Fail-Safe Biasing for Short Data Links**

Note that the resistor values in Figures 7 and 8 have been calculated for $V_S = 4.5V$, $V_{AB} = 0.25V$, and $Z_0 = 120\Omega$.

## 5.13 Transient Protection

Protecting the ISL32740E against transients exceeding the device's transient immunity requires the addition of an external TVS. For this purpose, Semtech's RClamp0512TQ was chosen due to its high transient protection levels, low junction capacitance, and small form factor.

**Table 5. RCLAMP0512 TVS Features**

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| ESD (IEC61000-4-2) | Air | $V_{ESD}$ | ±30 | kV |
| | Contact | $V_{ESD}$ | ±30 | kV |
| EFT (IEC61000-4-4) | | $V_{EFT}$ | ±4 | kV |
| Surge (IEC61000-4-5) | | $V_{SURGE}$ | ±1.3 | kV |
| Junction Capacitance | | $C_J$ | 3 | pF |
| Form Factor | | - | 1 x 0.6 | mm |

The TVS is implemented between the bus lines and isolated ground (GND2).

Because transient voltages on the bus lines are referenced to Earth potential, also known as Protective Earth (PE), a high-voltage capacitor ($C_{HV}$) is inserted between GND2 and PE, providing a low-impedance path for high-frequency transients.

Note that the connection from the PE point on the isolated side to the PE point on the non-isolated side (Earth) is usually made using the metal chassis of the equipment, or through a short, thick wire of low-inductance.

A high-voltage resistor ($R_{HV}$) is added in parallel to $C_{HV}$ to prevent the build-up of static charges on floating grounds (GND2) and cable shields (typically used in PROFIBUS). The bill of materials for the circuit in Figure 9 is listed in Table 6 on page 16.

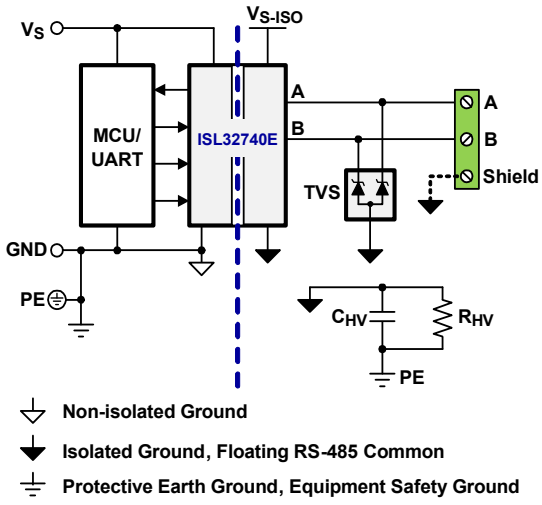



**Figure 9. Transient Protection for ISL32740E**

**Table 6. BOM for Circuit in Figure 9**

| Name | Function | Order No. | Vendor |
|---|---|---|---|
| TVS | 170W (8, 20µs) 2-LINE PROTECTOR | RCLAMP0512TQ | SEMTECH |
| $C_{HV}$ | 4.7nF, 2kV, 10% CAPACITOR | 1812B472K202NT | NOVACAP |
| $R_{HV}$ | 1MΩ, 2kV, 5% RESISTOR | HVC12061M0JT3 | TT-ELECTRONICS |

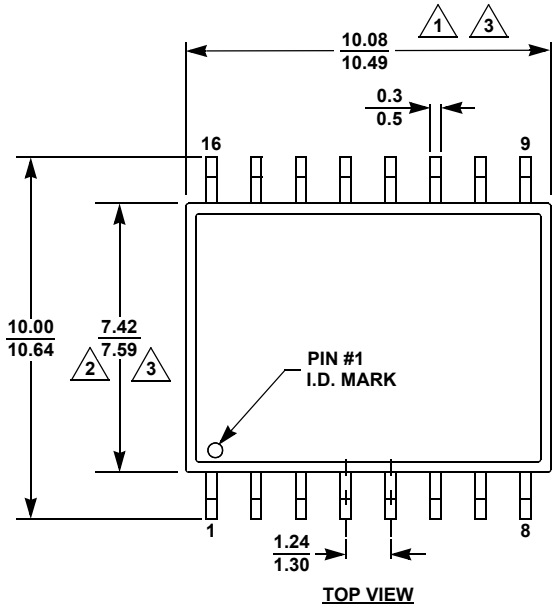
# 6. Revision History

| Rev. | Date | Description |
|---|---|---|
| 4.00 | Nov 30, 2017 | Updated certification file number for VDE. |
| 3.00 | Oct 2, 2017 | Updated thermal resistance values for the QSOP package. Changed $\theta_{JA}$ from “92” to “77” and $\theta_{JC}$ from “37” to “41”. |
| 2.00 | Aug 24, 2017 | Updated Table 1 on page 2.<br>Updated receiving truth table. |
| 1.00 | Jul 6, 2017 | Applied new formatting standards.<br>Updated Title.<br>Added ISL32740EIAZ and ISL32740EFBZ information throughout document.<br>Updated Note 1.<br>Updated Pin descriptions for Pins A, B, GND2, ISODE, and VDD2.<br>Updated thermal resistance for the SOICW package. Changed $\theta_{JA}$ from “60” to “43” and $\theta_{JC}$ from “12” to “20”.<br>Updated Total Barrier Thickness (internal) spec removed minimum and changed typical from “16” to “13”.<br>Updated “Magnetic Field Immunity” on page 8, removed all MIN values.<br>Updated POD M16.3A to the latest revision. Changes are as follows:<br>-Revised the land pattern. |
| 0.00 | Feb 28, 2017 | Initial release |

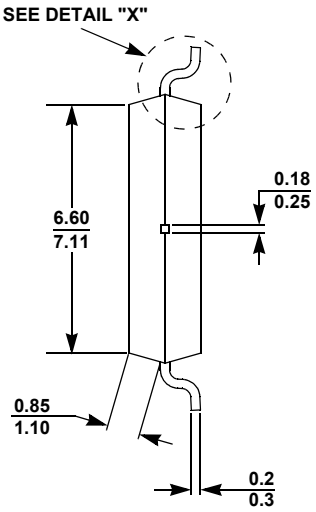
# 7. Package Outline Drawings

For the most recent package outline drawing, see M16.3A.

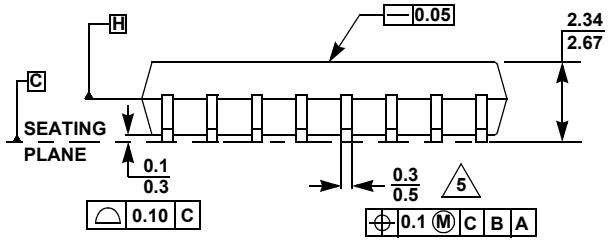
M16.3A
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOICW)
Rev 1, 6/17



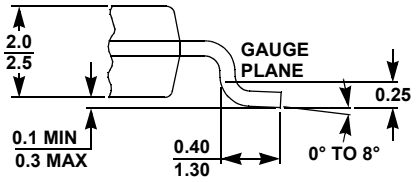

TOP VIEW



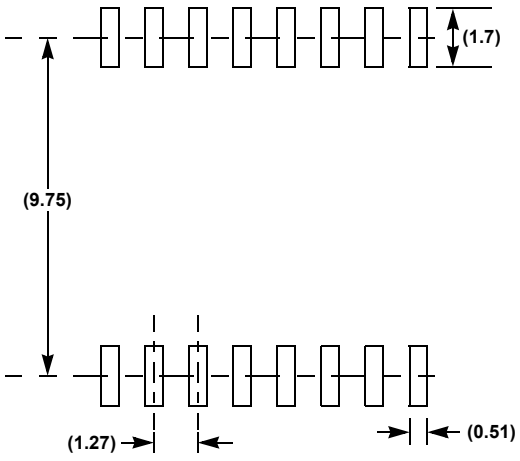

END VIEW




SIDE VIEW




DETAIL X



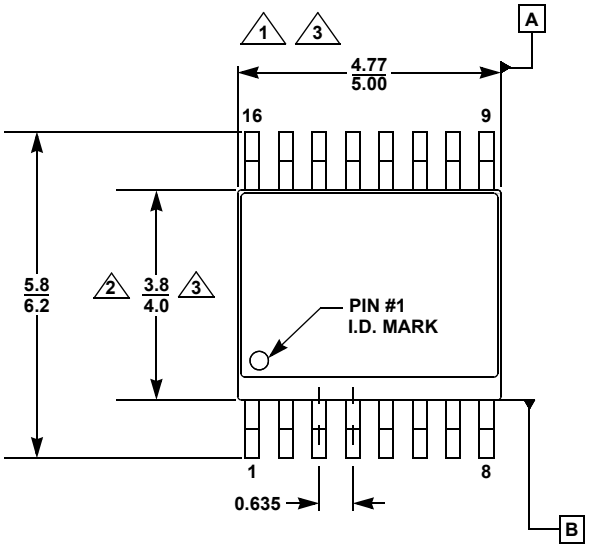

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

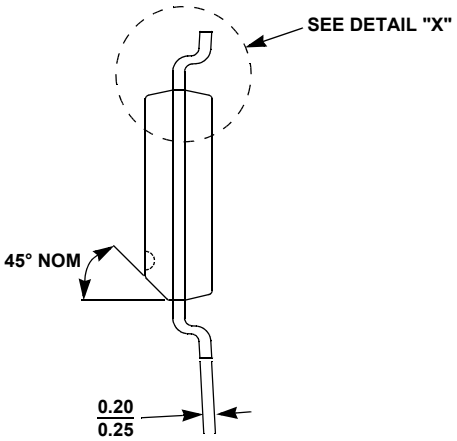
20. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
21. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
22. Dimensions are measured at datum plane H.
23. Dimensioning and tolerancing per ASME Y14.5M-1994.
24. Dimension does not include dambar protrusion.
25. Dimension in ( ) are for reference only.
26. Pin spacing is a BASIC dimension; tolerances do not accumulate.
27. Dimensions are in mm.

For the most recent package outline drawing, see M16.15B.

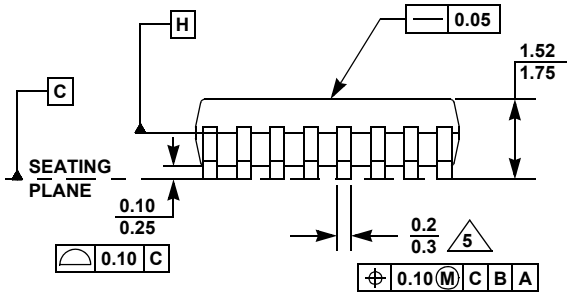
M16.15B
16 LEAD QUARTER-SIZE SMALL OUTLINE PLASTIC PACKAGE (QSOP)
Rev 0, 9/16



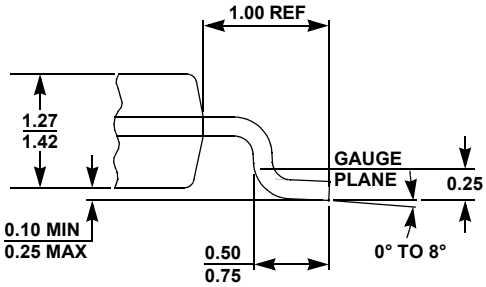

TOP VIEW



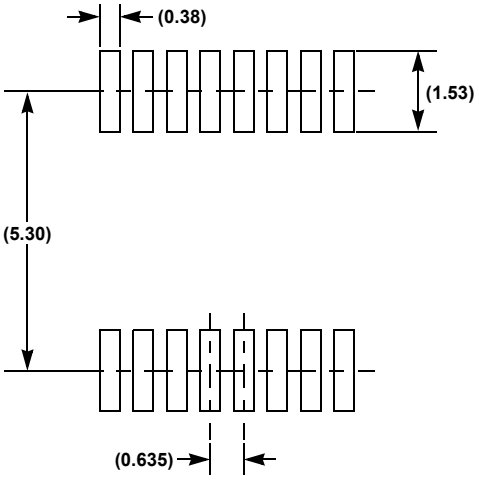

END VIEW




SIDE VIEW




DETAIL X




TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion.
6. Dimension in ( ) are for reference only.
7. Pin spacing is a BASIC dimension; tolerances do not accumulate.
8. Dimensions are in mm.

# 8. About Intersil

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